

### General Description

- Bottom Source Technology
- Very Low  $R_{DS(ON)}$
- Low Gate Charge
- High Current Capability
- RoHS and Halogen-Free Compliant

### Applications

- DC/DC Converters in Computing, Servers, and POL
- Non-Isolated DC/DC Converters in Telecom and Industrial

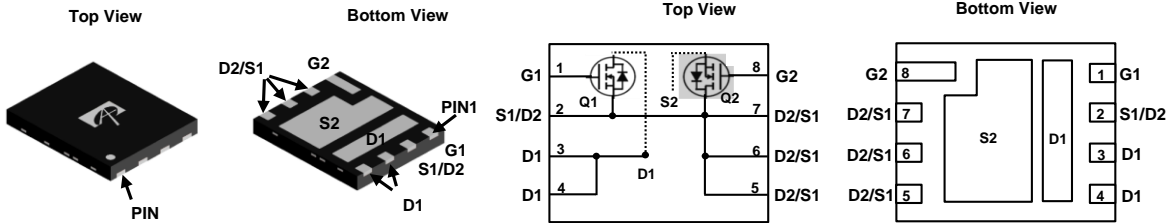
### Product Summary

	Q1	Q2
$V_{DS}$	30V	30V
$I_D$ (at $V_{GS}=10V$ )	55A	85A
$R_{DS(ON)}$ (at $V_{GS}=10V$ )	< 4.95m $\Omega$	< 1.35m $\Omega$
$R_{DS(ON)}$ (at $V_{GS}=4.5V$ )	< 7.95m $\Omega$	< 1.75m $\Omega$

100% UIS Tested  
 100% Rg Tested



DFN 5X6E



Orderable Part Number	Package Type	Form	Minimum Order Quantity
AONX36322	DFN 5x6E	Tape & Reel	3000

### Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Max Q1	Max Q2	Units	
Drain-Source Voltage	$V_{DS}$	30	30	V	
Gate-Source Voltage	$V_{GS}$	$\pm 20$	$\pm 12$	V	
Continuous Drain Current <sup>G</sup>	$I_D$	$T_C=25^\circ\text{C}$	55	85	A
		$T_C=100^\circ\text{C}$	35	85	
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	120	340	A	
Continuous Drain Current	$I_{DSM}$	$T_A=25^\circ\text{C}$	21	38	A
		$T_A=70^\circ\text{C}$	16	30	
Avalanche Current <sup>C</sup>	$I_{AS}$	60	80	A	
Avalanche energy	$E_{AS}$	18	32	mJ	
$V_{DS}$ Spike	$V_{SPIKE}$	36	36	V	
Power Dissipation <sup>B</sup>	$P_D$	$T_C=25^\circ\text{C}$	24	52	W
		$T_C=100^\circ\text{C}$	9.6	20	
Power Dissipation <sup>A</sup>	$P_{DSM}$	$T_A=25^\circ\text{C}$	3.5	3.5	W
		$T_A=70^\circ\text{C}$	2.2	2.2	
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 150		$^\circ\text{C}$	

### Thermal Characteristics

Parameter	Symbol	Typ Q1	Typ Q2	Max Q1	Max Q2	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	$t \leq 10s$	25	25	35	$^\circ\text{C/W}$
Maximum Junction-to-Ambient <sup>A,D</sup>		Steady-State	50	50	65	$^\circ\text{C/W}$
Maximum Junction-to-Case (Note)	$R_{\theta JC}$	4	1.8	5.2	2.4	$^\circ\text{C/W}$

Note: Bottom S2, D1.

**Q1 Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V	30			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			1 5	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V			±100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.3	1.7	2.2	V
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =20A T <sub>J</sub> =125°C		3.5	4.95	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =20A		5	7	
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =20A		57		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =1A, V <sub>GS</sub> =0V		0.7	1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current				30	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =15V, f=1MHz		1145		pF
C <sub>oss</sub>	Output Capacitance			375		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			55		pF
R <sub>g</sub>	Gate resistance	f=1MHz	0.6	1.2	1.9	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g(10V)</sub>	Total Gate Charge	V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, I <sub>D</sub> =20A		16	25	nC
Q <sub>g(4.5V)</sub>	Total Gate Charge			7.5	15	
Q <sub>gs</sub>	Gate Source Charge			2.5		
Q <sub>gd</sub>	Gate Drain Charge			3.0		
Q <sub>gs</sub>	Gate Source Charge	V <sub>GS</sub> =4.5V, V <sub>DS</sub> =15V, I <sub>D</sub> =20A		2.5		nC
Q <sub>gd</sub>	Gate Drain Charge			3.0		
t <sub>D(on)</sub>	Turn-On DelayTime	V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, R <sub>L</sub> =0.75Ω, R <sub>GEN</sub> =3Ω		6.5		ns
t <sub>r</sub>	Turn-On Rise Time			4.5		
t <sub>D(off)</sub>	Turn-Off DelayTime			19		
t <sub>f</sub>	Turn-Off Fall Time			3		
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =20A, dI/dt=500A/μs		11.5		ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =20A, dI/dt=500A/μs		20		nC

A. The value of R<sub>θJA</sub> is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25° C. The Power dissipation P<sub>DSM</sub> is based on R<sub>θJA</sub> ≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Single pulse width limited by junction temperature T<sub>J(MAX)</sub>=150° C.

D. The R<sub>θJA</sub> is the sum of the thermal impedance from junction to case R<sub>θJC</sub> and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=150° C. The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

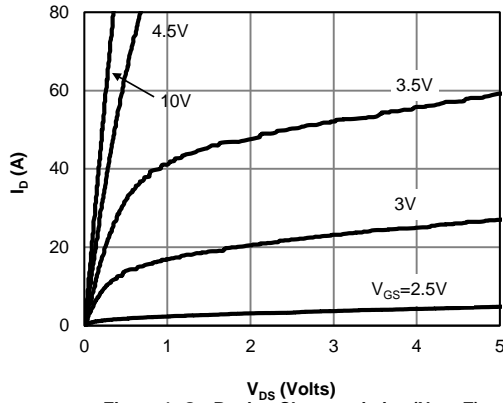
H. These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25° C.

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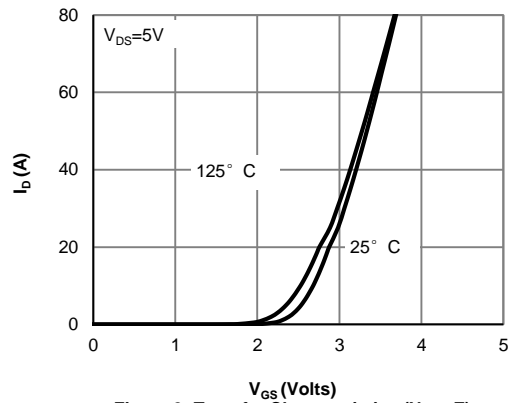
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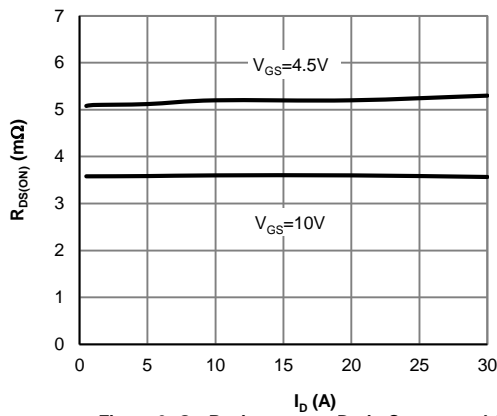
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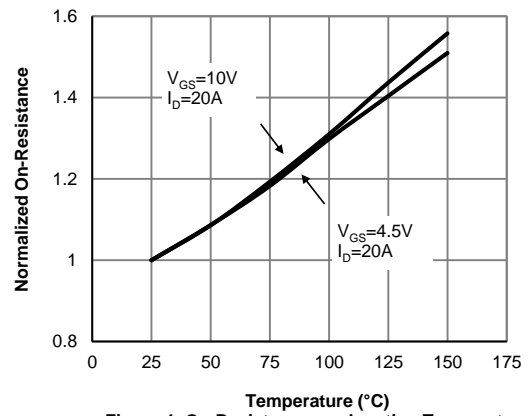
**Figure 1: On-Region Characteristics (Note E)**



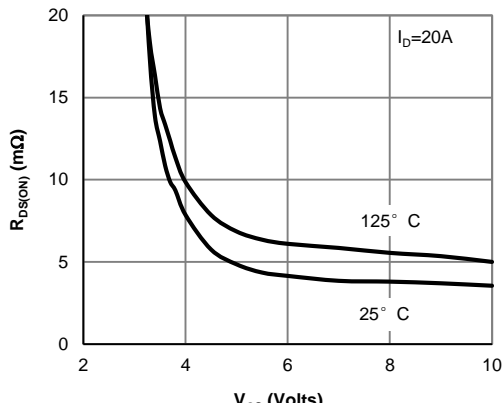
**Figure 2: Transfer Characteristics (Note E)**



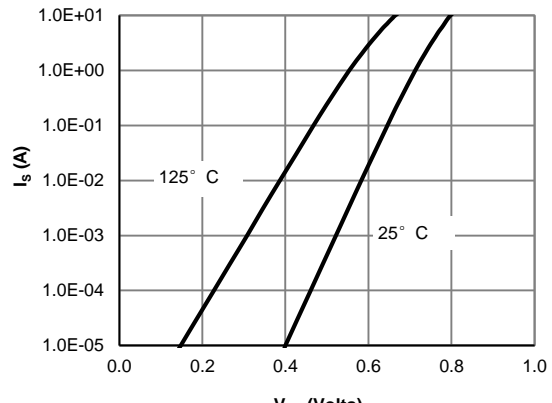
**Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)**



**Figure 4: On-Resistance vs. Junction Temperature (Note E)**

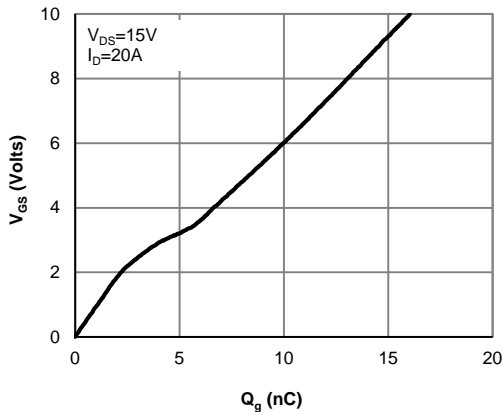


**Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)**

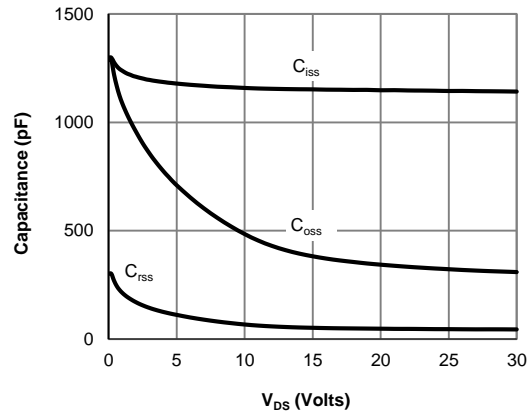


**Figure 6: Body-Diode Characteristics (Note E)**

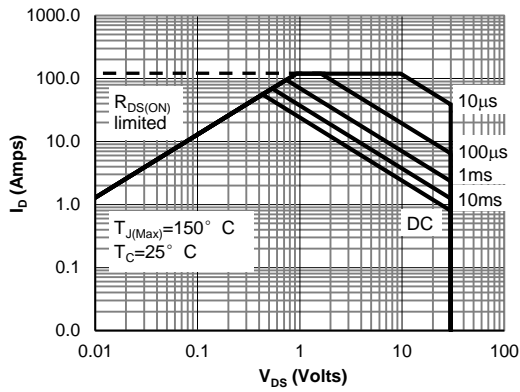
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



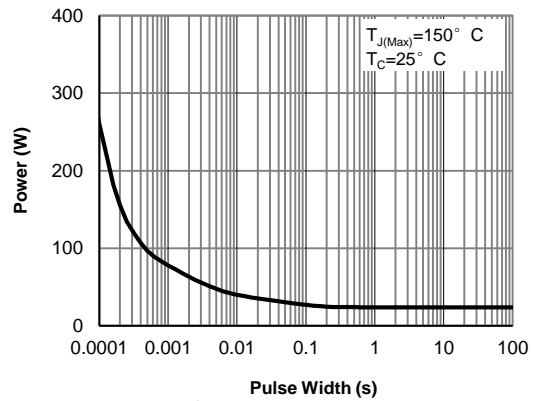
**Figure 7: Gate-Charge Characteristics**



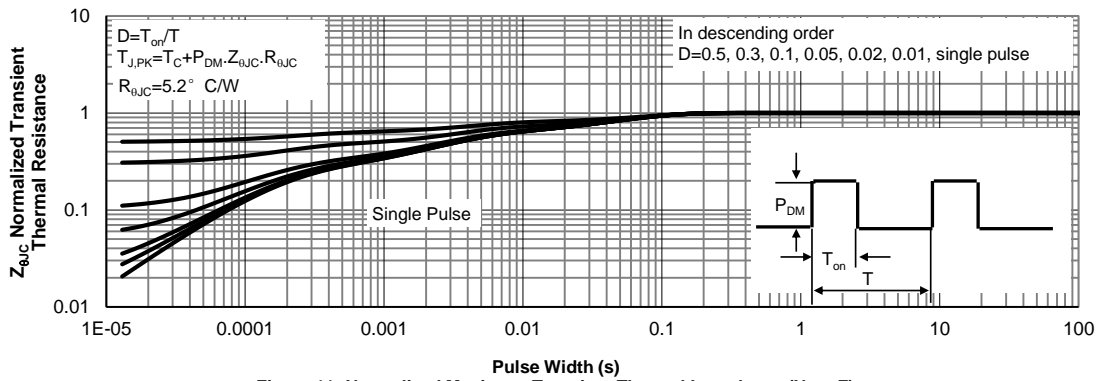
**Figure 8: Capacitance Characteristics**



**Figure 9: Maximum Forward Biased Safe Operating Area (Note F)**



**Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)**



**Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)**

**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

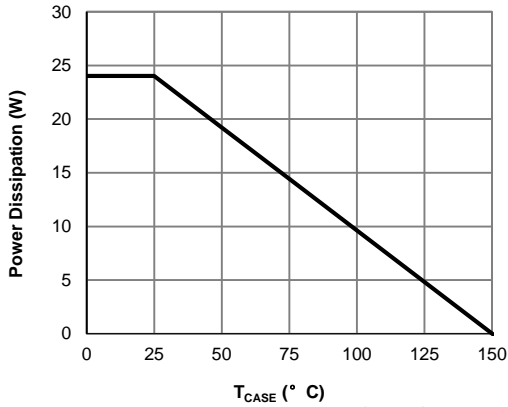


Figure 12: Power De-rating (Note F)

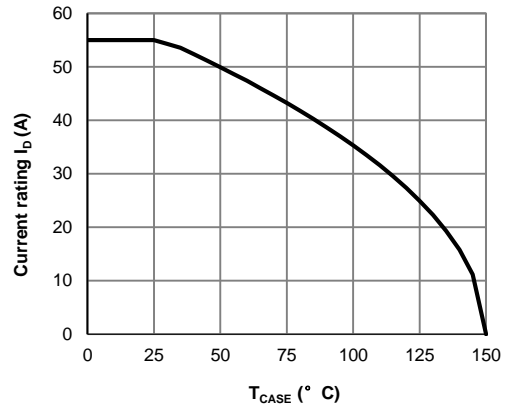


Figure 13: Current De-rating (Note F)

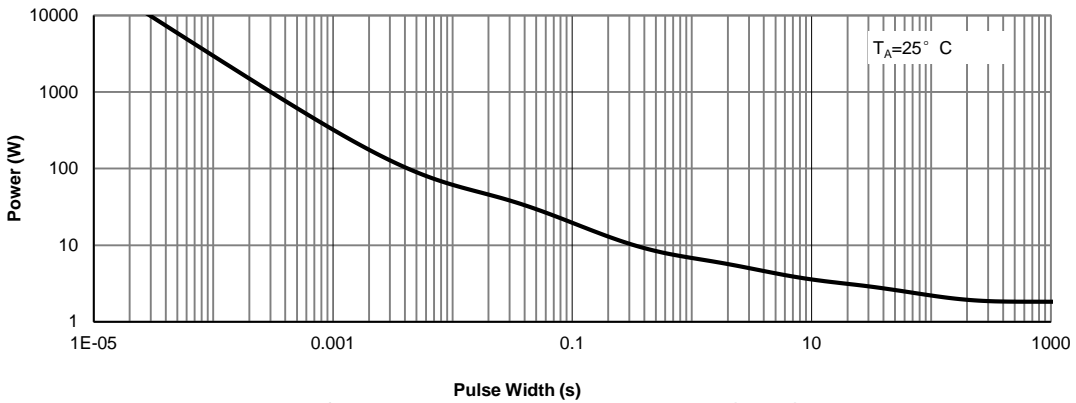


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

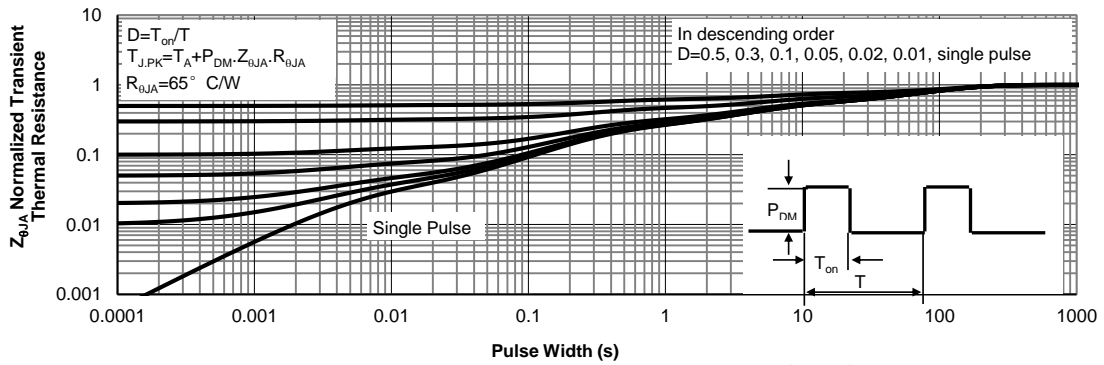


Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

**Q2 Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

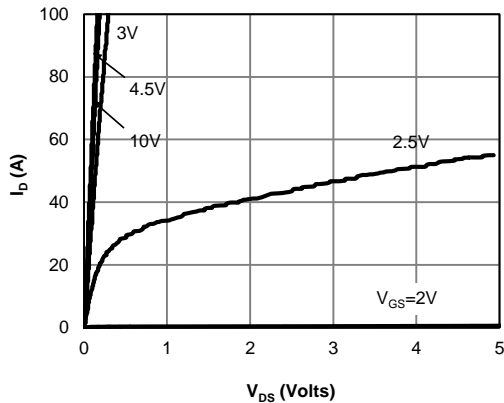
Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V	30			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			1 5	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±12V			±100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.2	1.5	1.9	V
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =20A T <sub>J</sub> =125°C		0.9	1.35	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =20A		1.45	2.2	
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =20A		200		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =1A, V <sub>GS</sub> =0V		0.7	1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current				60	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =15V, f=1MHz		4175		pF
C <sub>oss</sub>	Output Capacitance			875		pF
C <sub>riss</sub>	Reverse Transfer Capacitance			125		pF
R <sub>g</sub>	Gate resistance	f=1MHz	0.6	1.3	2.1	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g(10V)</sub>	Total Gate Charge	V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, I <sub>D</sub> =20A		65	100	nC
Q <sub>g(4.5V)</sub>	Total Gate Charge			30	50	
Q <sub>gs</sub>	Gate Source Charge			9.5		
Q <sub>gd</sub>	Gate Drain Charge			7		
Q <sub>gs</sub>	Gate Source Charge	V <sub>GS</sub> =4.5V, V <sub>DS</sub> =15V, I <sub>D</sub> =20A		9.5		nC
Q <sub>gd</sub>	Gate Drain Charge			7		
t <sub>D(on)</sub>	Turn-On DelayTime	V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, R <sub>L</sub> =0.75Ω, R <sub>GEN</sub> =3Ω		9		ns
t <sub>r</sub>	Turn-On Rise Time			8		
t <sub>D(off)</sub>	Turn-Off DelayTime			50.5		
t <sub>f</sub>	Turn-Off Fall Time			8.5		
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =20A, dI/dt=500A/μs		17		ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =20A, dI/dt=500A/μs		42		nC

- A. The value of R<sub>θJA</sub> is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25° C. The Power dissipation P<sub>DSM</sub> is based on R<sub>θJA</sub> t<sub>≤</sub> 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.
- B. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
- C. Single pulse width limited by junction temperature T<sub>J(MAX)</sub>=150° C.
- D. The R<sub>θJA</sub> is the sum of the thermal impedance from junction to case R<sub>θJC</sub> and case to ambient.
- E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.
- F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=150° C. The SOA curve provides a single pulse rating.
- G. The maximum current rating is package limited.
- H. These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25° C.

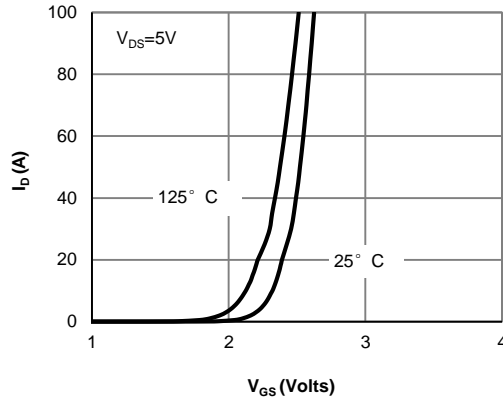
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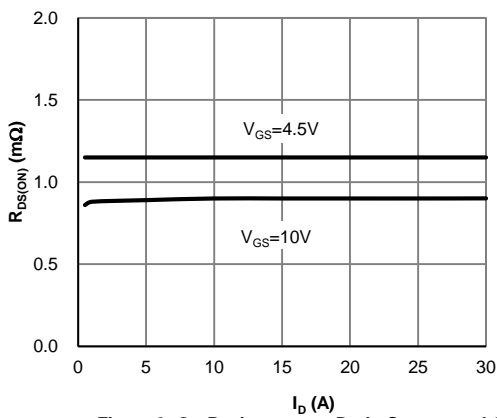
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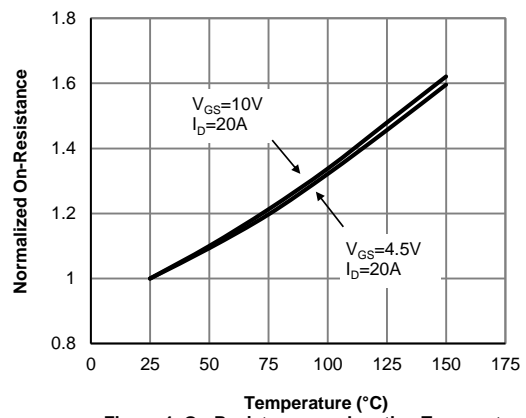
**Figure 1: On-Region Characteristics (Note E)**



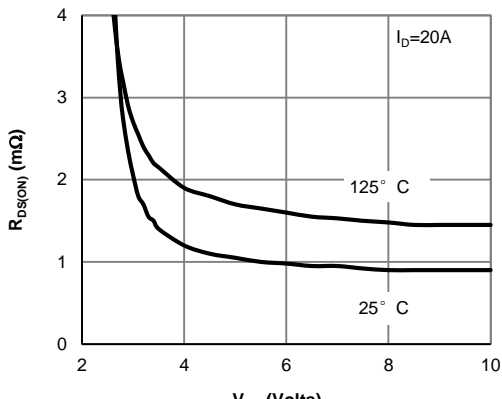
**Figure 2: Transfer Characteristics (Note E)**



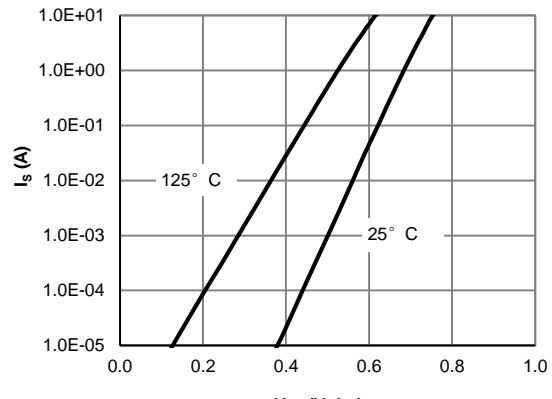
**Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)**



**Figure 4: On-Resistance vs. Junction Temperature (Note E)**

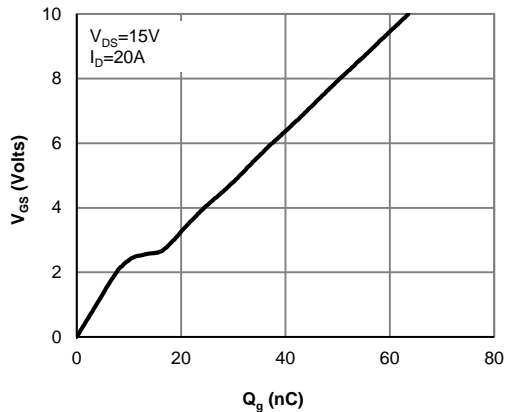


**Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)**

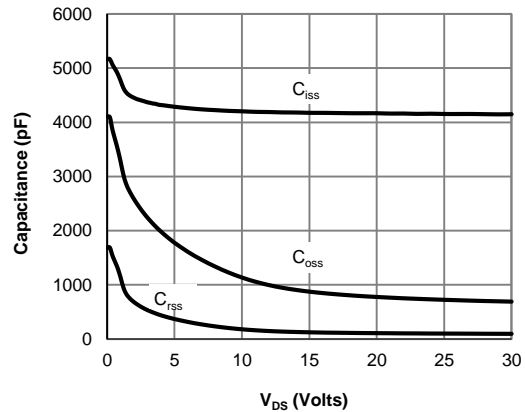


**Figure 6: Body-Diode Characteristics (Note E)**

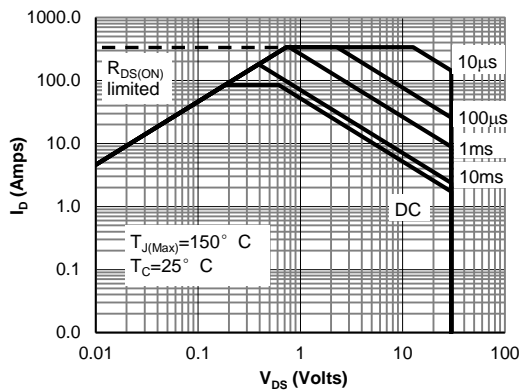
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



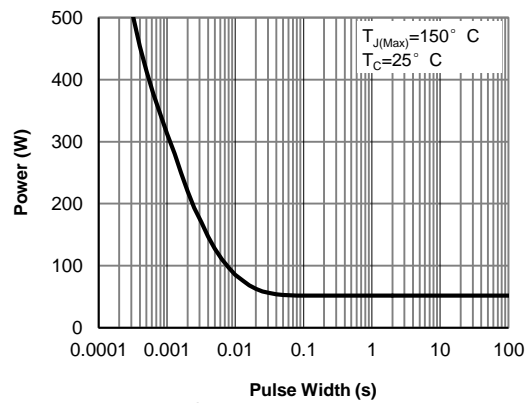
**Figure 7: Gate-Charge Characteristics**



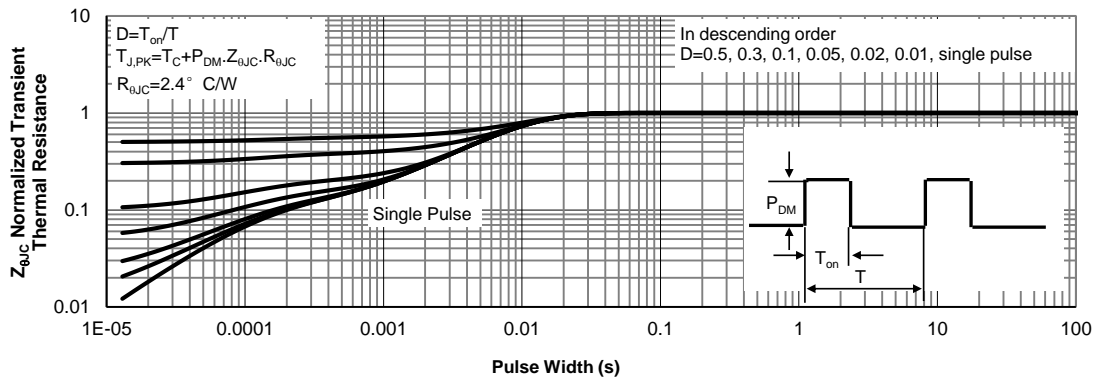
**Figure 8: Capacitance Characteristics**



**Figure 9: Maximum Forward Biased Safe Operating Area (Note F)**



**Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)**



**Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)**



**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

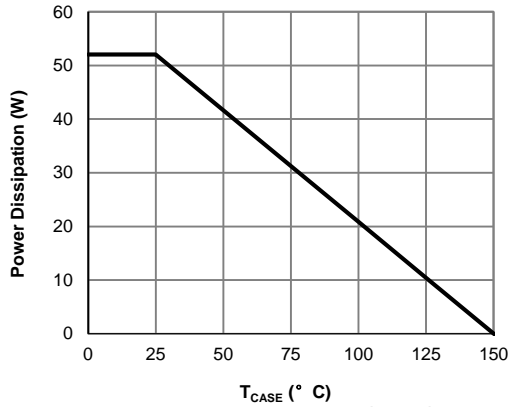


Figure 12: Power De-rating (Note F)

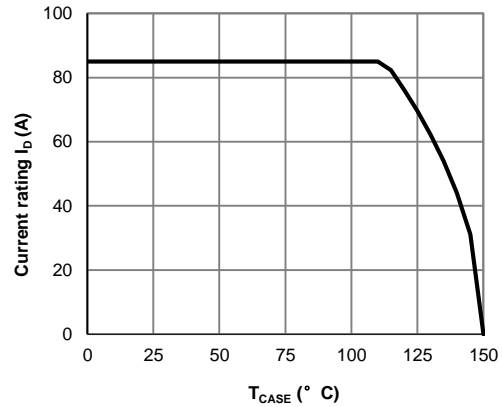


Figure 13: Current De-rating (Note F)

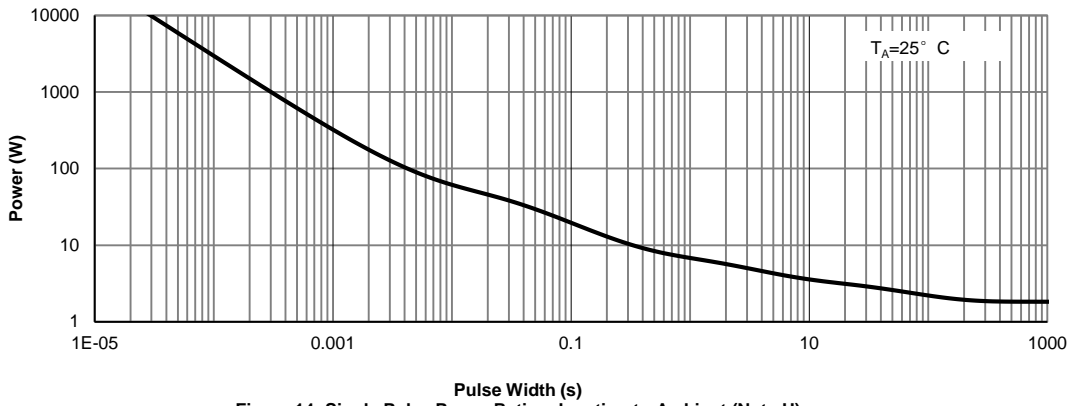


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

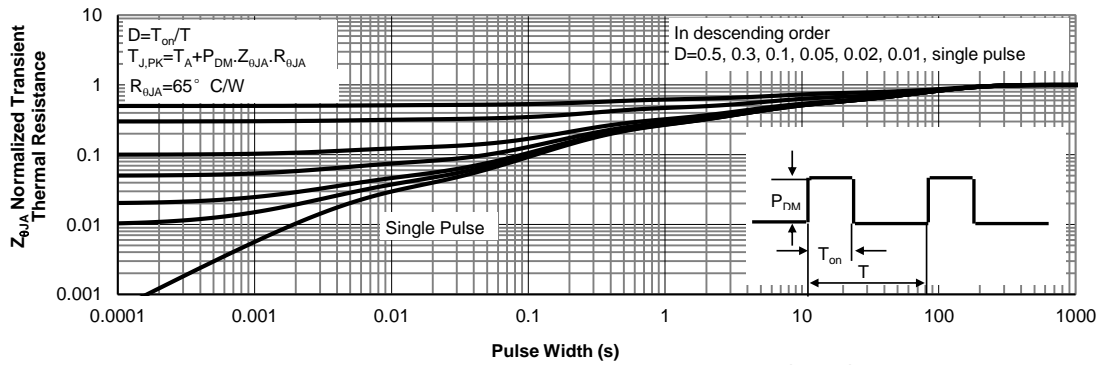


Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

Figure A: Gate Charge Test Circuit & Waveforms

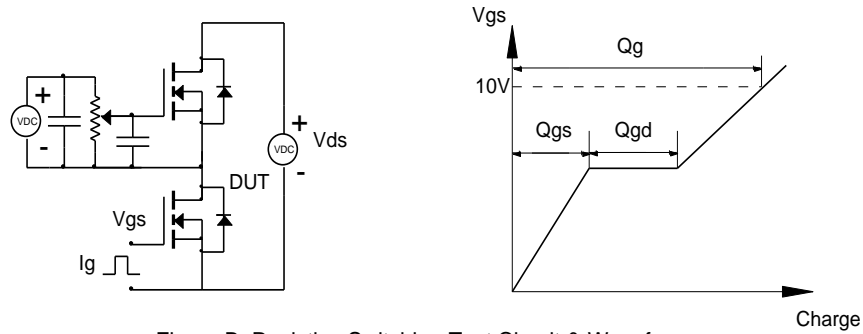


Figure B: Resistive Switching Test Circuit & Waveforms

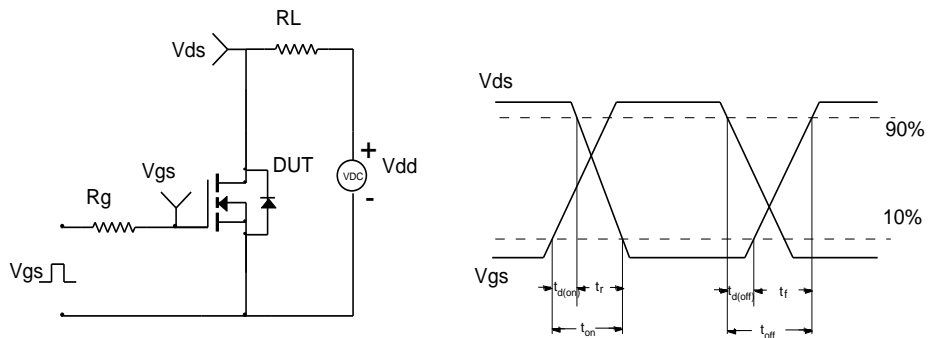


Figure C: Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

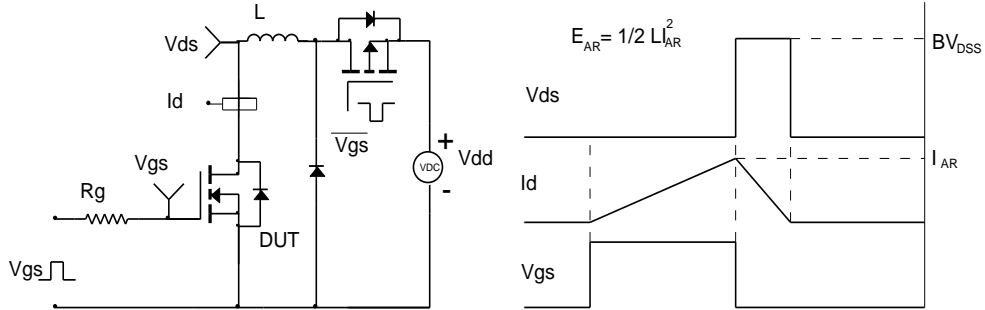
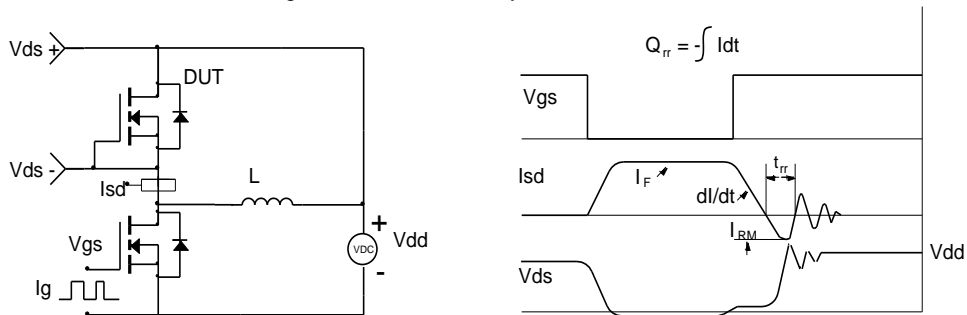


Figure D: Diode Recovery Test Circuit & Waveforms



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