

General Description

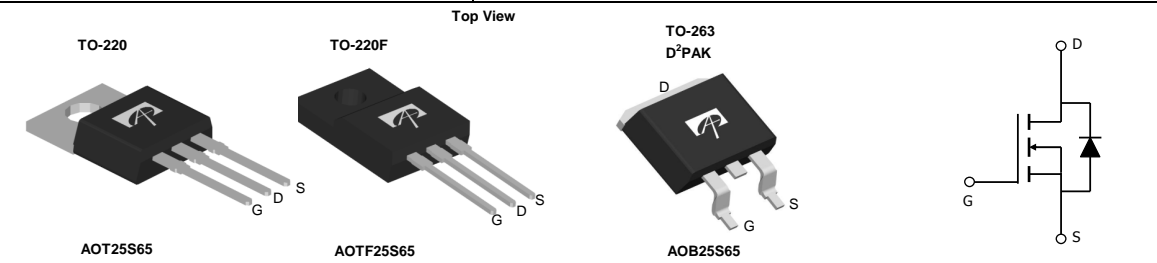
The AOT25S65 & AOB25S65 & AOTF25S65 have been fabricated using the advanced α MOS™ high voltage process that is designed to deliver high levels of performance and robustness in switching applications. By providing low $R_{DS(on)}$, Q_g and E_{OSS} along with guaranteed avalanche capability these parts can be adopted quickly into new and existing offline power supply designs.

For Halogen Free add "L" suffix to part number:
 AOT25S65L & AOB25S65L & AOTF25S65L

Product Summary

| | |
|----------------------|---------------|
| $V_{DS} @ T_{j,max}$ | 750V |
| I_{DM} | 104A |
| $R_{DS(ON),max}$ | 0.19 Ω |
| $Q_{g,typ}$ | 26.4nC |
| $E_{oss} @ 400V$ | 5.8 μ C |

100% UIS Tested
 100% R_g Tested


Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

| Parameter | Symbol | AOT25S65/AOB25S65 | AOTF25S65 | AOTF25S65L | Units | |
|---|----------------|---------------------------------|-----------|------------|------------------|---------------------|
| Drain-Source Voltage | V_{DS} | 650 | | | V | |
| Gate-Source Voltage | V_{GS} | ± 30 | | | V | |
| Continuous Drain Current | I_b | $T_C=25^\circ\text{C}$ | 25 | 25* | A | |
| | | $T_C=100^\circ\text{C}$ | 16 | 16* | | |
| Pulsed Drain Current ^C | I_{DM} | 104 | | | | |
| Avalanche Current ^C | I_{AR} | 7 | | | A | |
| Repetitive avalanche energy ^C | E_{AR} | 96 | | | mJ | |
| Single pulsed avalanche energy ^G | E_{AS} | 750 | | | mJ | |
| Power Dissipation ^B | P_D | $T_C=25^\circ\text{C}$ | 357 | 50 | 40 | W |
| | | Derate above 25°C | 2.9 | 0.4 | 0.3 | W/ $^\circ\text{C}$ |
| MOSFET dv/dt ruggedness | dv/dt | 100 | | | V/ns | |
| Peak diode recovery dv/dt ^H | | 20 | | | | |
| Junction and Storage Temperature Range | T_J, T_{STG} | -55 to 150 | | | $^\circ\text{C}$ | |
| Maximum lead temperature for soldering purpose, 1/8" from case for 5 seconds ^J | T_L | 300 | | | $^\circ\text{C}$ | |

Thermal Characteristics

| Parameter | Symbol | AOT25S65/AOB25S65 | AOTF25S65 | AOTF25S65L | Units |
|--|-----------------|-------------------|-----------|------------|---------------------------|
| Maximum Junction-to-Ambient ^{A,D} | $R_{\theta JA}$ | 65 | 65 | 65 | $^\circ\text{C}/\text{W}$ |
| Maximum Case-to-sink ^A | $R_{\theta CS}$ | 0.5 | -- | -- | $^\circ\text{C}/\text{W}$ |
| Maximum Junction-to-Case | $R_{\theta JC}$ | 0.35 | 2.5 | 3.1 | $^\circ\text{C}/\text{W}$ |

* Drain current limited by maximum junction temperature.

Electrical Characteristics (T_J=25°C unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|-----------------------------|---|---|-----|-------|------|-------|
| STATIC PARAMETERS | | | | | | |
| BV _{DSS} | Drain-Source Breakdown Voltage | I _D =250μA, V _{GS} =0V, T _J =25°C | 650 | - | - | V |
| | | I _D =250μA, V _{GS} =0V, T _J =150°C | 700 | 750 | - | |
| I _{DSS} | Zero Gate Voltage Drain Current | V _{DS} =650V, V _{GS} =0V | - | - | 1 | μA |
| | | V _{DS} =520V, T _J =150°C | - | 10 | - | |
| I _{GSS} | Gate-Body leakage current | V _{DS} =0V, V _{GS} =±30V | - | - | ±100 | nA |
| V _{GS(th)} | Gate Threshold Voltage | V _{DS} =5V, I _D =250μA | 2.6 | 3.3 | 4 | V |
| R _{DS(ON)} | Static Drain-Source On-Resistance | V _{GS} =10V, I _D =12.5A, T _J =25°C | - | 0.165 | 0.19 | Ω |
| | | V _{GS} =10V, I _D =12.5A, T _J =150°C | - | 0.47 | 0.53 | Ω |
| V _{SD} | Diode Forward Voltage | I _S =12.5A, V _{GS} =0V, T _J =25°C | - | 0.84 | - | V |
| I _S | Maximum Body-Diode Continuous Current | | - | - | 25 | A |
| I _{SM} | Maximum Body-Diode Pulsed Current | | - | - | 104 | A |
| DYNAMIC PARAMETERS | | | | | | |
| C _{ISS} | Input Capacitance | V _{GS} =0V, V _{DS} =100V, f=1MHz | - | 1278 | - | pF |
| C _{OSS} | Output Capacitance | | - | 87 | - | pF |
| C _{o(er)} | Effective output capacitance, energy related ^H | V _{GS} =0V, V _{DS} =0 to 480V, f=1MHz | - | 64.5 | - | pF |
| C _{o(tr)} | Effective output capacitance, time related ^I | | - | 236.7 | - | pF |
| C _{rss} | Reverse Transfer Capacitance | V _{GS} =0V, V _{DS} =100V, f=1MHz | - | 1.4 | - | pF |
| R _g | Gate resistance | V _{GS} =0V, V _{DS} =0V, f=1MHz | - | 4.9 | - | Ω |
| SWITCHING PARAMETERS | | | | | | |
| Q _g | Total Gate Charge | V _{GS} =10V, V _{DS} =480V, I _D =12.5A | - | 26.4 | - | nC |
| Q _{gs} | Gate Source Charge | | - | 6.2 | - | nC |
| Q _{gd} | Gate Drain Charge | | - | 9.5 | - | nC |
| t _{D(on)} | Turn-On Delay Time | V _{GS} =10V, V _{DS} =400V, I _D =12.5A, R _G =25Ω | - | 29 | - | ns |
| t _r | Turn-On Rise Time | | - | 30 | - | ns |
| t _{D(off)} | Turn-Off Delay Time | | - | 112 | - | ns |
| t _f | Turn-Off Fall Time | | - | 34 | - | ns |
| t _{rr} | Body Diode Reverse Recovery Time | I _F =12.5A, dI/dt=100A/μs, V _{DS} =400V | - | 408 | - | ns |
| I _{rm} | Peak Reverse Recovery Current | I _F =12.5A, dI/dt=100A/μs, V _{DS} =400V | - | 33 | - | A |
| Q _{rr} | Body Diode Reverse Recovery Charge | I _F =12.5A, dI/dt=100A/μs, V _{DS} =400V | - | 8.27 | - | μC |

A. The value of R_{θJA} is measured with the device in a still air environment with T_A=25°C.

B. The power dissipation P_D is based on T_{J(MAX)}=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150°C. Ratings are based on low frequency and duty cycles to keep initial T_J=25°C.

D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=150°C. The SOA curve provides a single pulse rating.

G. L=60mH, I_{AS}=5A, V_{DD}=150V, Starting T_J=25°C

H. C_{o(er)} is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 80% V_{(BR)DSS}.

I. C_{o(tr)} is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 80% V_{(BR)DSS}.

J. Wavesoldering only allowed at leads.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

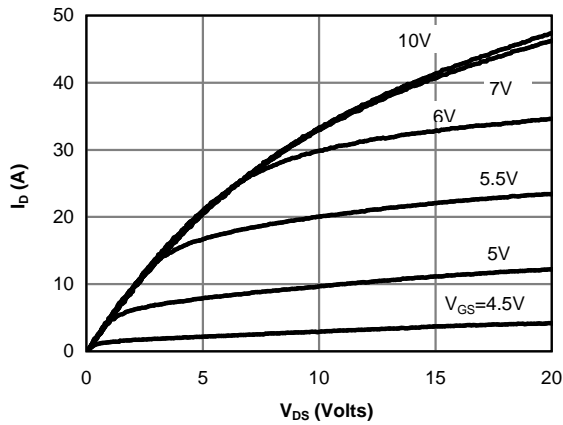


Figure 1: On-Region Characteristics @ 25°C

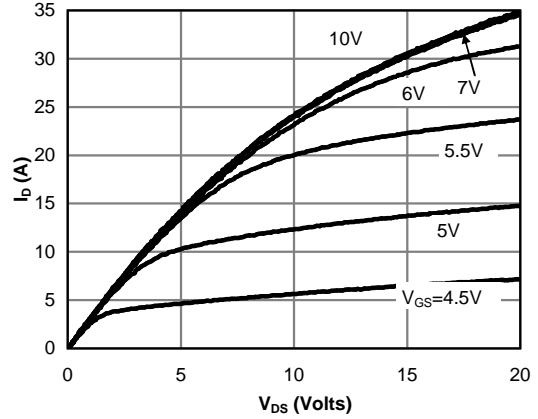


Figure 2: On-Region Characteristics @ 125°C

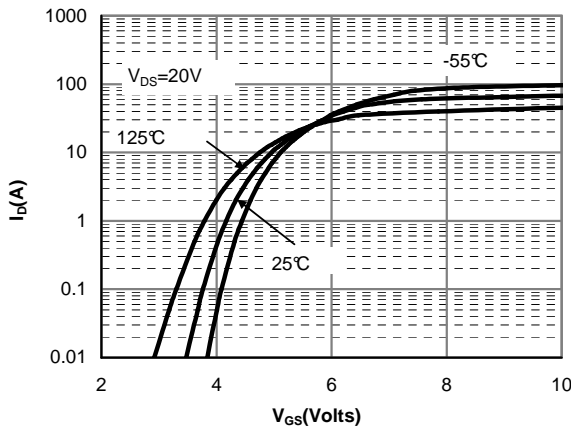


Figure 3: Transfer Characteristics

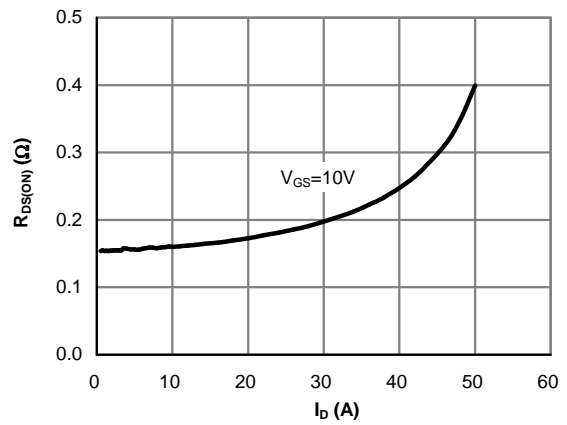


Figure 4: On-Resistance vs. Drain Current and Gate Voltage

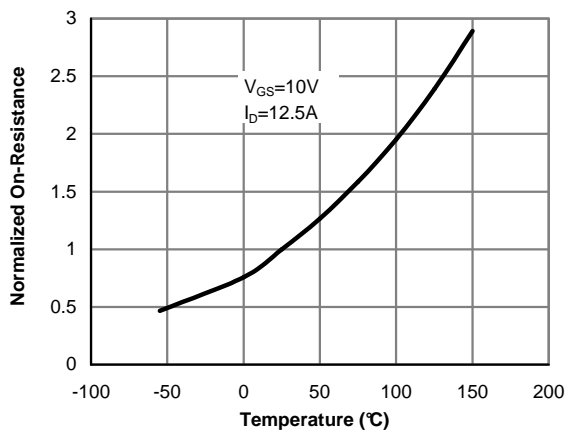


Figure 5: On-Resistance vs. Junction Temperature

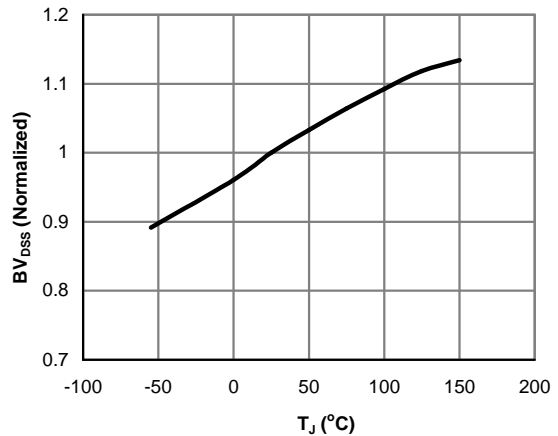


Figure 6: Break Down vs. Junction Temperature

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

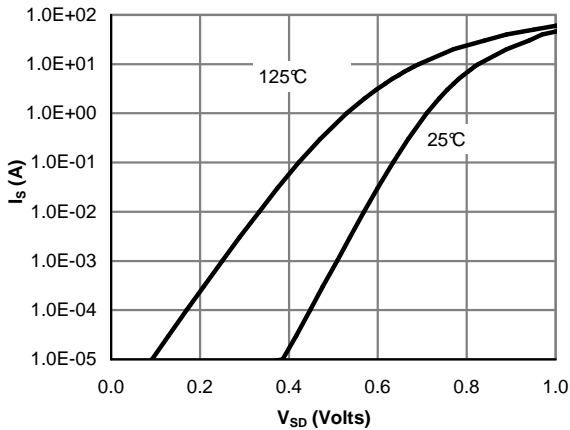


Figure 7: Body-Diode Characteristics (Note E)

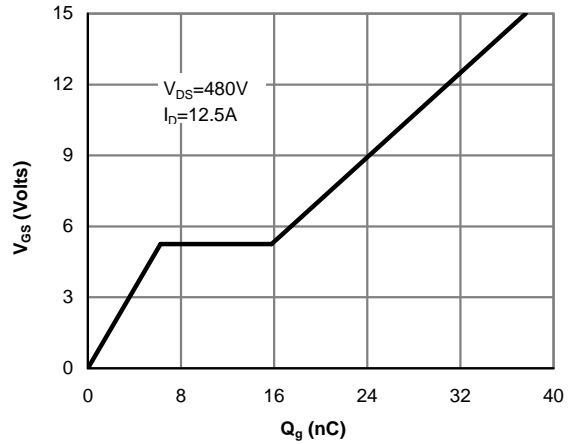


Figure 8: Gate-Charge Characteristics

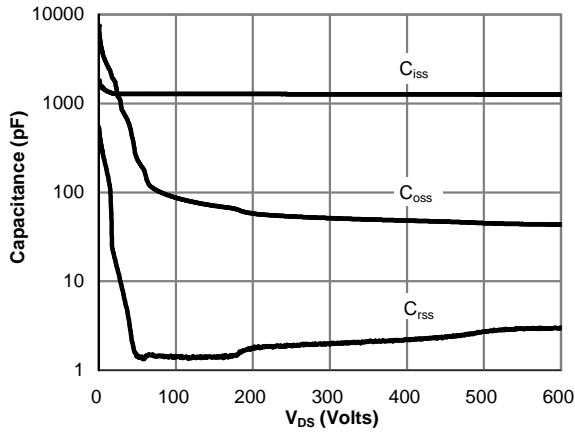


Figure 9: Capacitance Characteristics

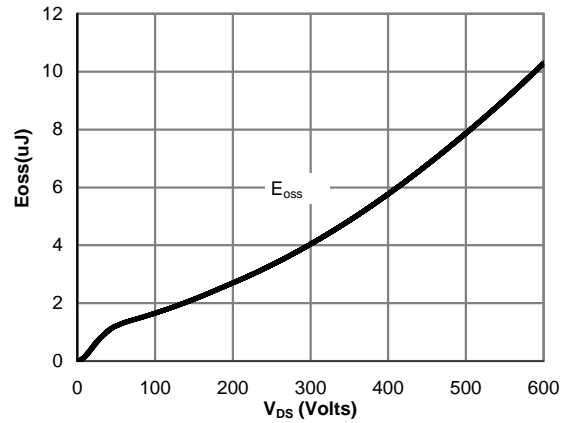


Figure 10: Coss stored Energy

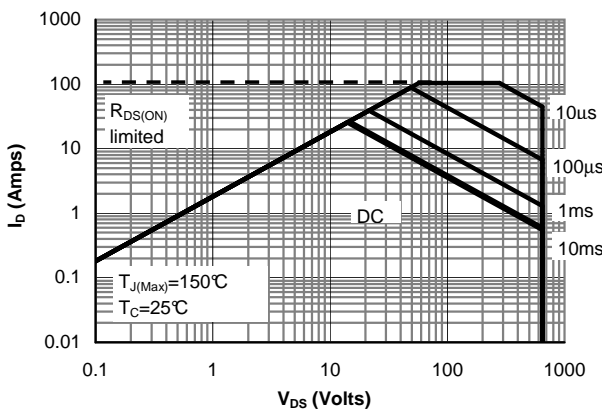


Figure 11: Maximum Forward Biased Safe Operating Area for AOT(B)25S65 (Note F)

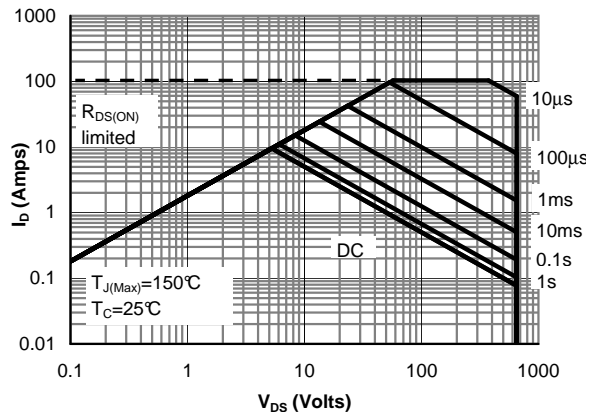


Figure 12: Maximum Forward Biased Safe Operating Area for AOTF25S65 (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

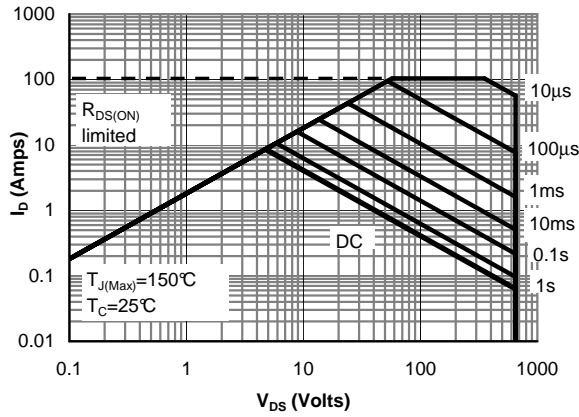


Figure 13: Maximum Forward Biased Safe Operating Area for AOTF25S65L(Note F)

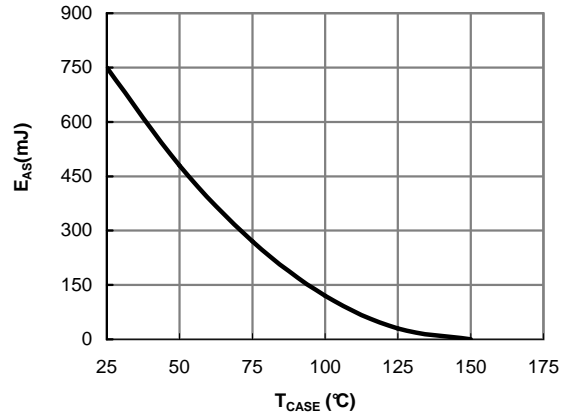


Figure 14: Avalanche energy

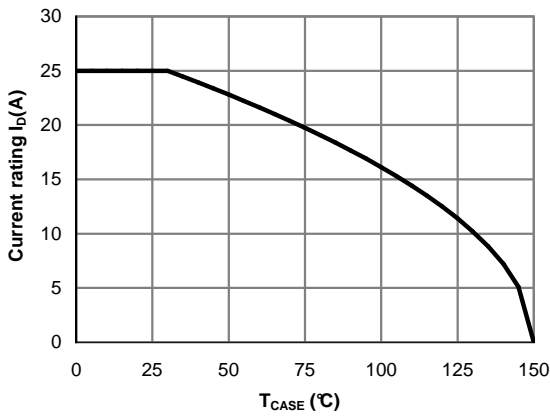


Figure 15: Current De-rating (Note B)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

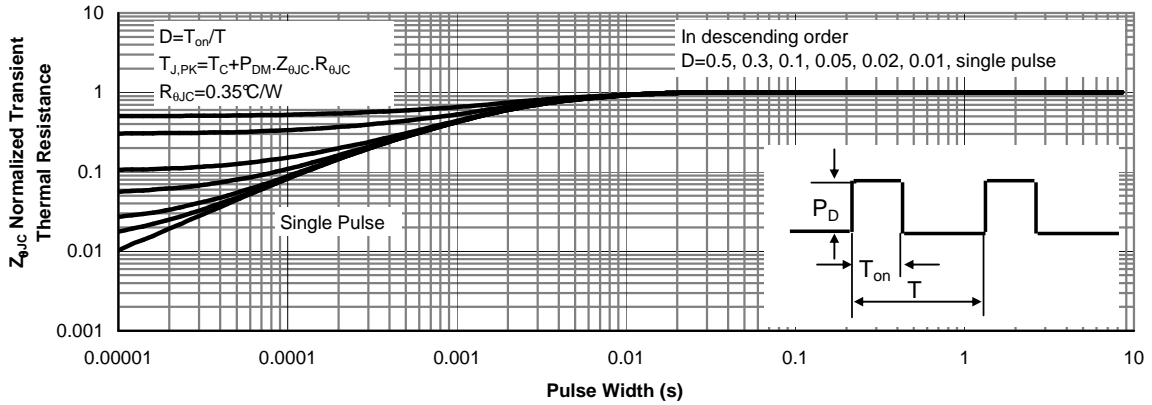


Figure 16: Normalized Maximum Transient Thermal Impedance for AOT(B)25S65 (Note F)

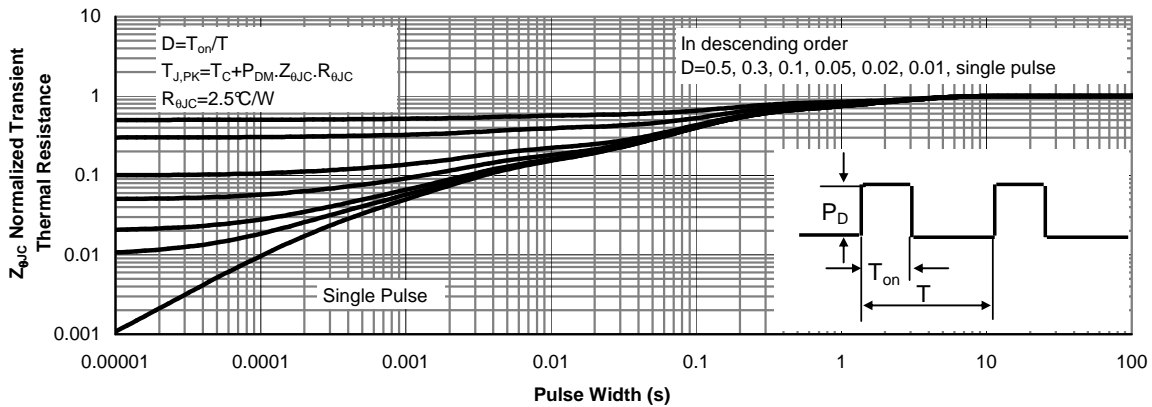


Figure 17: Normalized Maximum Transient Thermal Impedance for AOTF25S65 (Note F)

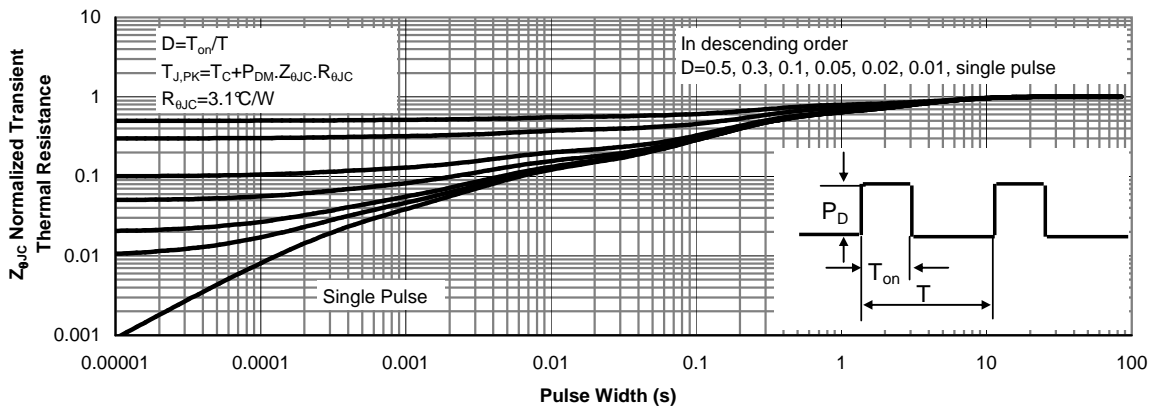
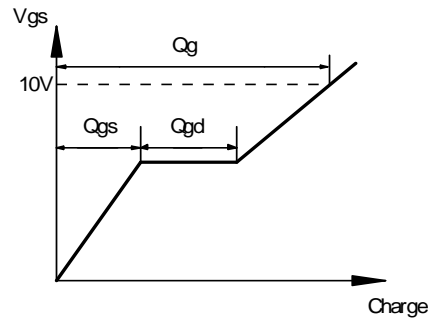
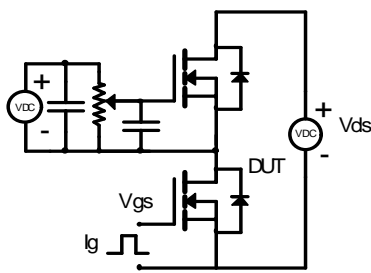
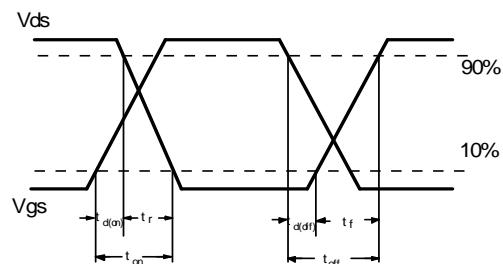
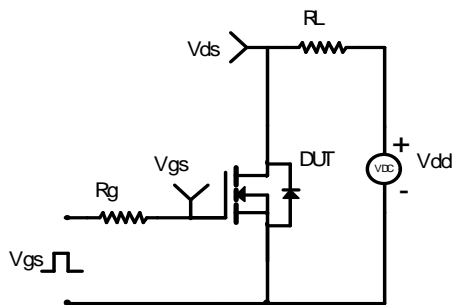


Figure 18: Normalized Maximum Transient Thermal Impedance for AOTF25S65L (Note F)

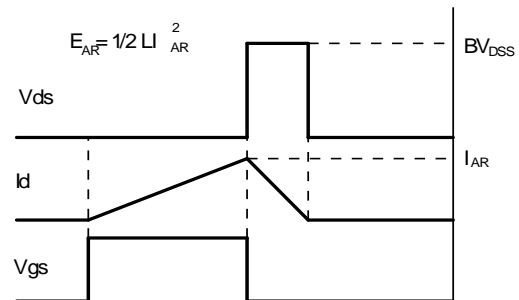
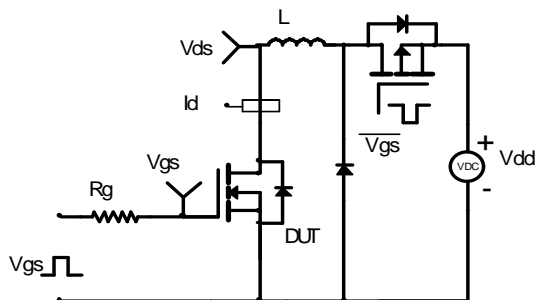
Gate Charge Test Circuit & Waveform



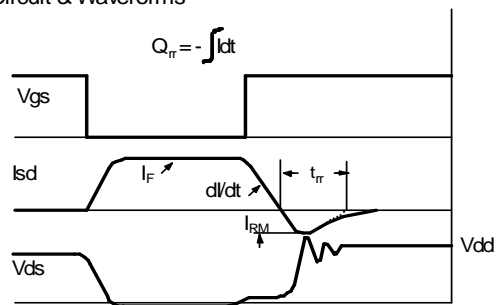
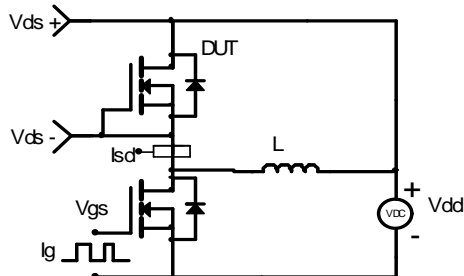
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



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