

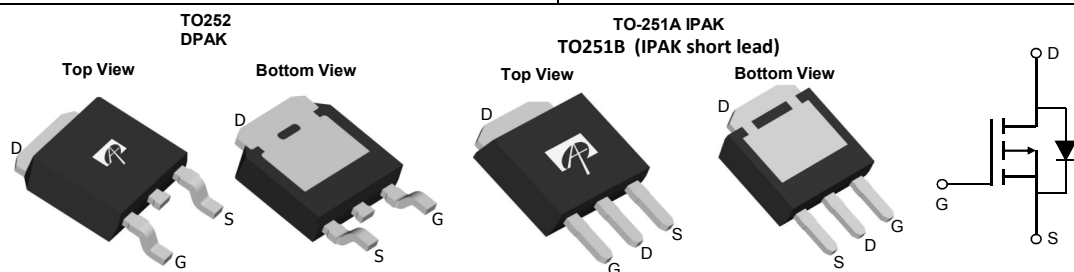
### General Description

The AOD423/AOI423/AOY423 uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and low gate resistance. With the excellent thermal resistance of the DPAK/IPAK package, this device is well suited for high current load applications.

### Product Summary

$V_{DS}$	-30V
$I_D$ (at $V_{GS} = -20V$ )	-70A
$R_{DS(ON)}$ (at $V_{GS} = -20V$ )	< 6.2m $\Omega$ (< 6.7m $\Omega^*$ )
$R_{DS(ON)}$ (at $V_{GS} = -10V$ )	< 8m $\Omega$ (< 8.5m $\Omega^*$ )

100% UIS Tested  
 100%  $R_g$  Tested



Orderable Part Number	Package Type	Form	Minimum Order Quantity
AOD423	TO-252	Tape & Reel	2500
AOI423	TO-251A	Tube	4000
AOY423	TO-251B	Tube	4000

### Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	-30	V
Gate-Source Voltage	$V_{GS}$	$\pm 25$	V
Continuous Drain Current <sup>G</sup>	$I_D$	$T_C=25^\circ C$	-70
		$T_C=100^\circ C$	-67
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	-200	A
Continuous Drain Current	$I_{DSM}$	$T_A=25^\circ C$	-15
		$T_A=70^\circ C$	-12
Avalanche Current <sup>C</sup>	$I_{AS}, I_{AR}$	-50	A
Avalanche energy $L=0.1mH$ <sup>C</sup>	$E_{AS}, E_{AR}$	125	mJ
Power Dissipation <sup>B</sup>	$P_D$	$T_C=25^\circ C$	90
		$T_C=100^\circ C$	45
Power Dissipation <sup>A</sup>	$P_{DSM}$	$T_A=25^\circ C$	2.5
		$T_A=70^\circ C$	1.6
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 175	$^\circ C$

### Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	16	20	$^\circ C/W$
Maximum Junction-to-Ambient <sup>A,D</sup>		Steady-State	41	50
Maximum Junction-to-Case	$R_{\theta JC}$	0.9	1.6	$^\circ C/W$

\* package TO251A, TO251B

**Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =-250μA, V <sub>GS</sub> =0V	-30			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =-30V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			-1 -5	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> = ±25V			±100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> I <sub>D</sub> =-250μA	-1.5	-2.5	-3.5	V
I <sub>D(ON)</sub>	On state drain current	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-5V	-200			A
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =-20V, I <sub>D</sub> =-20A TO252 T <sub>J</sub> =125°C		5.1 7.6	6.2 9.2	mΩ
		V <sub>GS</sub> =-10V, I <sub>D</sub> =-20A TO252		6.2	8	mΩ
		V <sub>GS</sub> =-20V, I <sub>D</sub> =-20A TO251A, TO251B		5.6	6.7	mΩ
		V <sub>GS</sub> =-10V, I <sub>D</sub> =-20A TO251A, TO251B		6.7	8.5	mΩ
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =-5V, I <sub>D</sub> =-20A		42		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =-1A, V <sub>GS</sub> =0V		-0.7	-1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current <sup>G</sup>				-70	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =-15V, f=1MHz		2760		pF
C <sub>oss</sub>	Output Capacitance			550		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			375		pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz	1.5	3	6.0	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g</sub>	Total Gate Charge	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-15V, I <sub>D</sub> =-20A		45	65	nC
Q <sub>gs</sub>	Gate Source Charge			10		nC
Q <sub>gd</sub>	Gate Drain Charge			12		nC
t <sub>D(on)</sub>	Turn-On DelayTime	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-15V, R <sub>L</sub> =0.75Ω, R <sub>GEN</sub> =3Ω		13		ns
t <sub>r</sub>	Turn-On Rise Time			23		ns
t <sub>D(off)</sub>	Turn-Off DelayTime			35		ns
t <sub>f</sub>	Turn-Off Fall Time			26		ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =-20A, dI/dt=500A/μs		15		ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =-20A, dI/dt=500A/μs		30		nC

A. The value of R<sub>θJA</sub> is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25° C. The Power dissipation P<sub>DSM</sub> is based on R<sub>θJA</sub> and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175° C may be used if the PCB allows it.

B. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=175° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=175° C. Ratings are based on low frequency and duty cycles to keep initial T<sub>J</sub>=25° C.

D. The R<sub>θJA</sub> is the sum of the thermal impedance from junction to case R<sub>θJC</sub> and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=175° C. The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25° C.

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**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

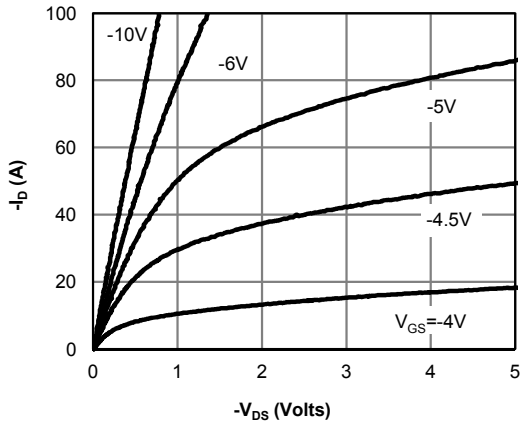


Fig 1: On-Region Characteristics (Note E)

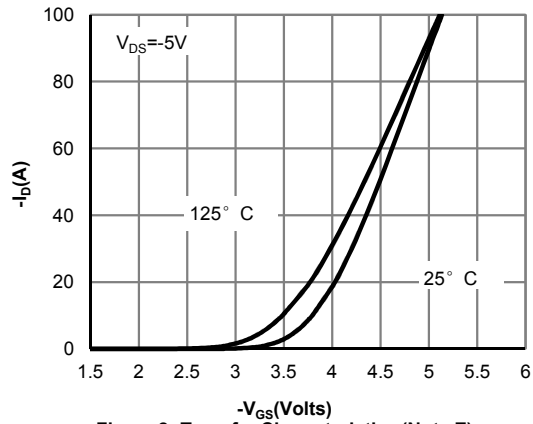


Figure 2: Transfer Characteristics (Note E)

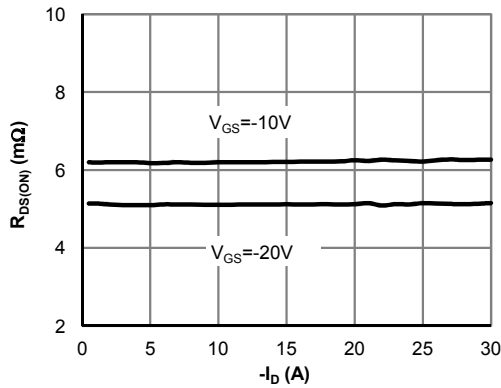


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

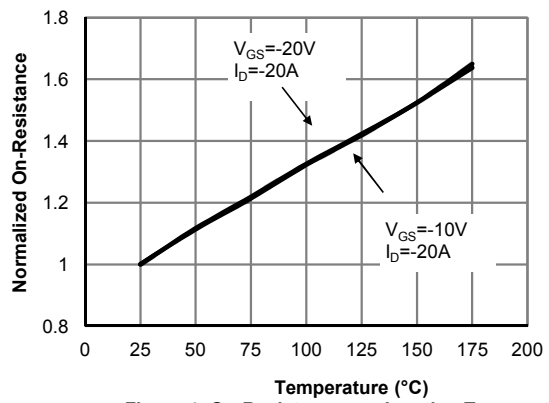


Figure 4: On-Resistance vs. Junction Temperature (Note E)

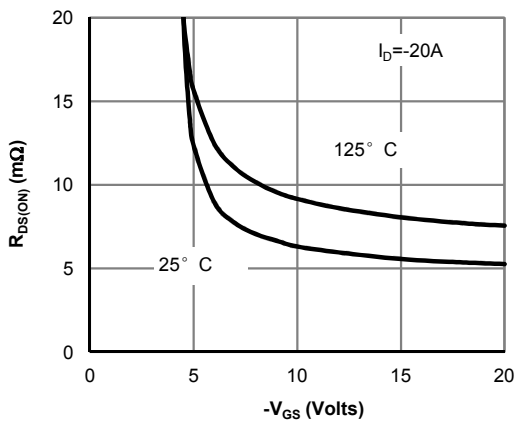


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

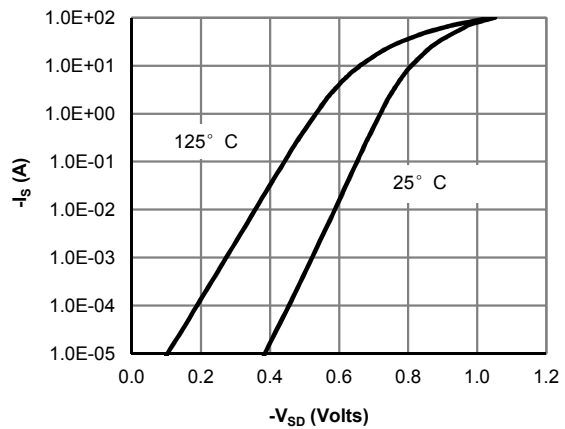


Figure 6: Body-Diode Characteristics (Note E)

**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

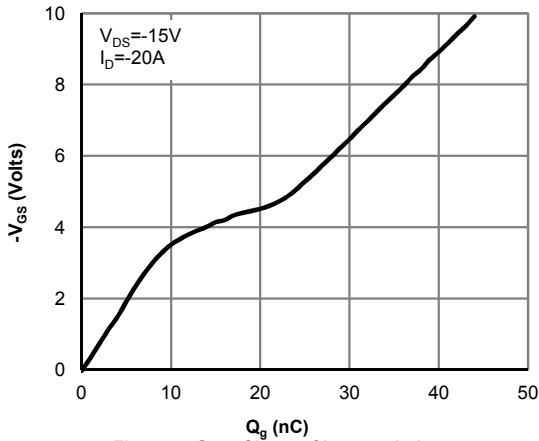


Figure 7: Gate-Charge Characteristics

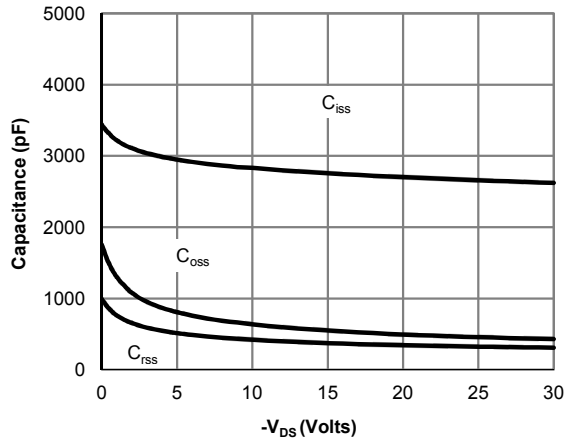


Figure 8: Capacitance Characteristics

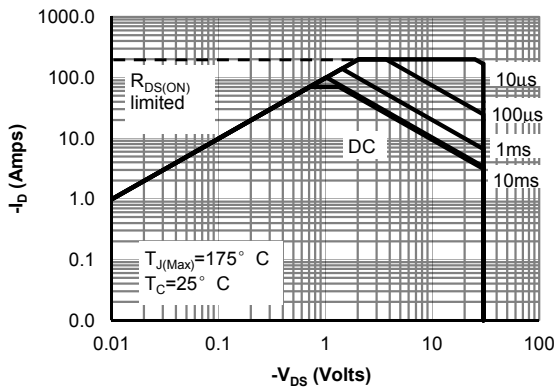


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

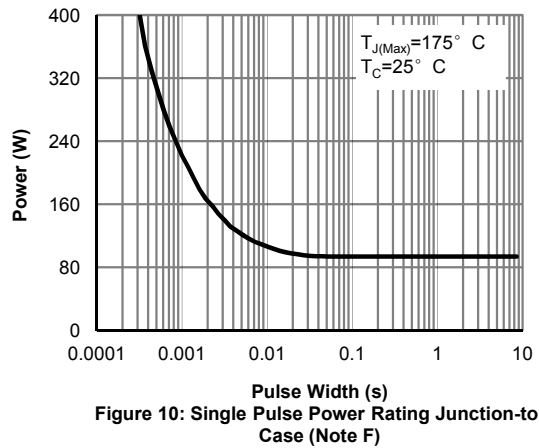


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

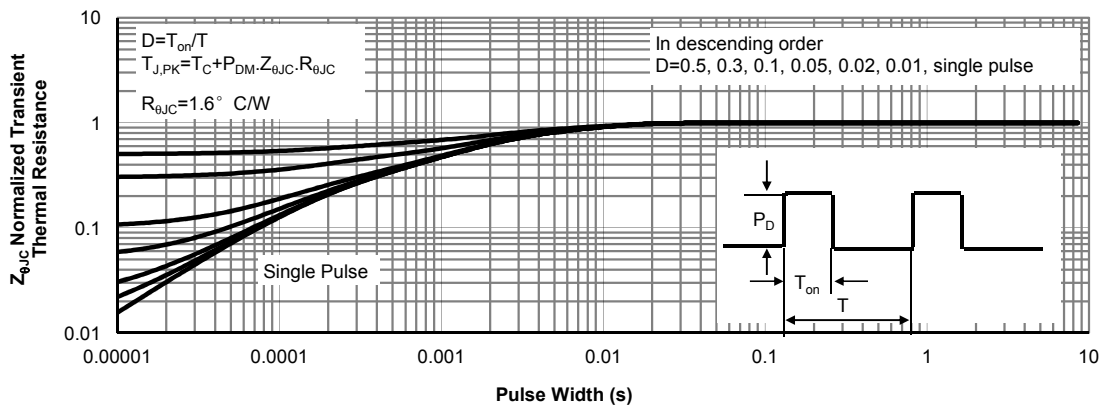


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

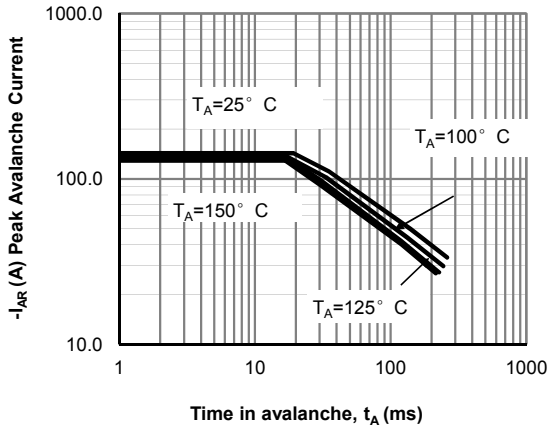


Figure 12: Single Pulse Avalanche capability (Note C)

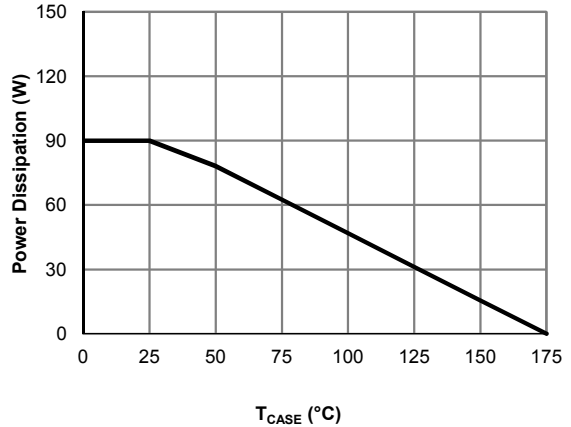


Figure 13: Power De-rating (Note F)

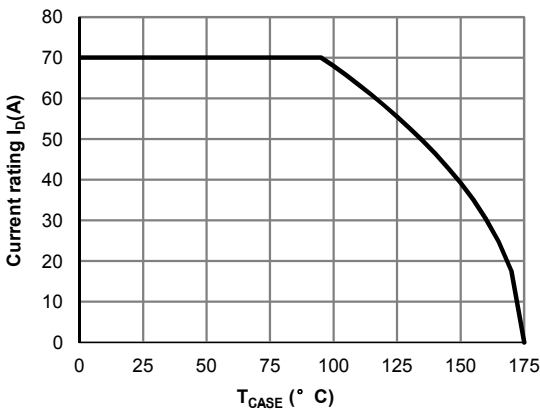


Figure 14: Current De-rating (Note F)

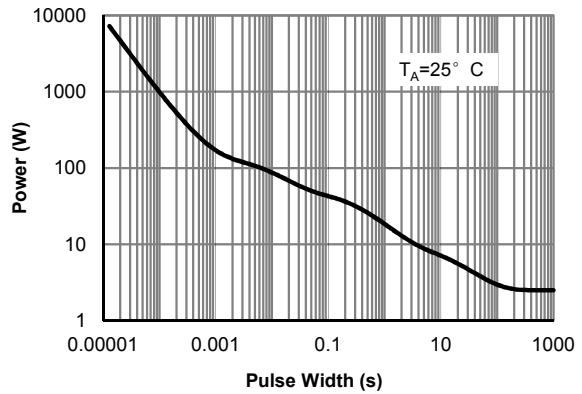


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

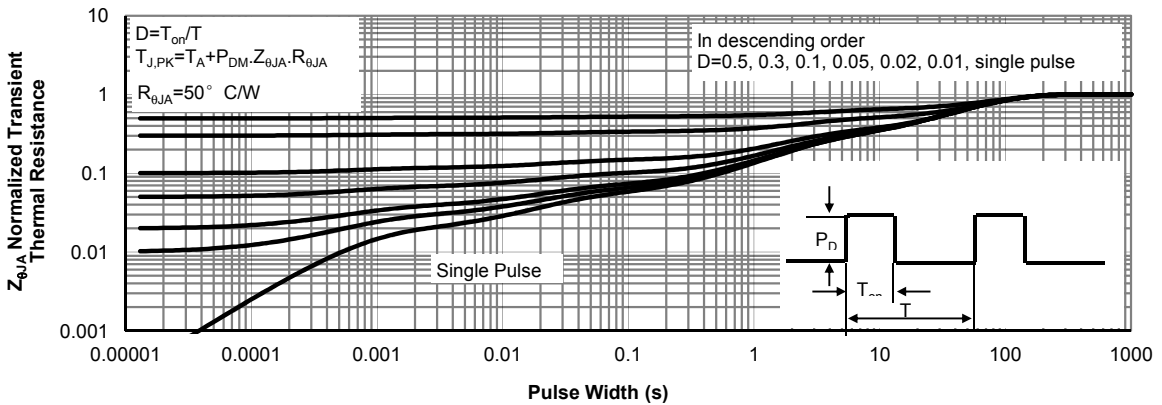
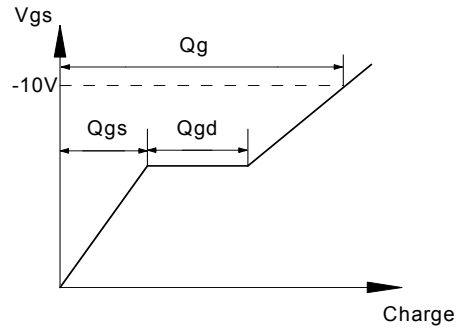
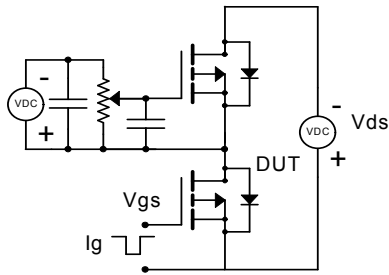
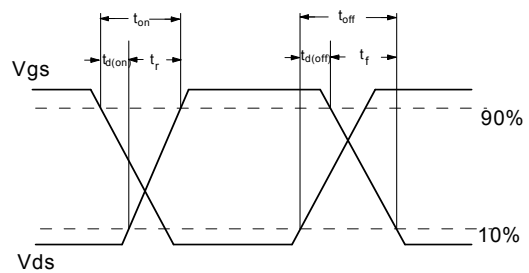
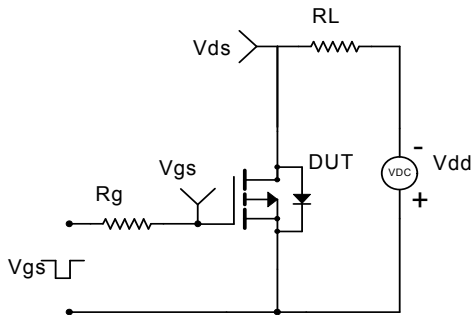


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

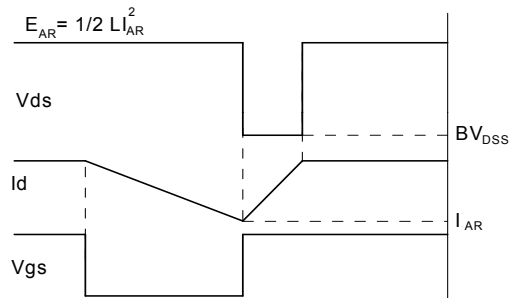
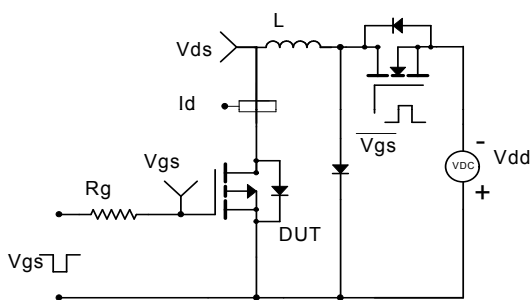
**Gate Charge Test Circuit & Waveform**



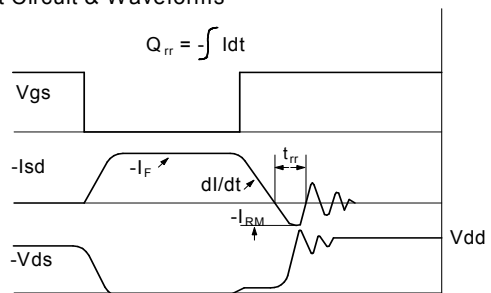
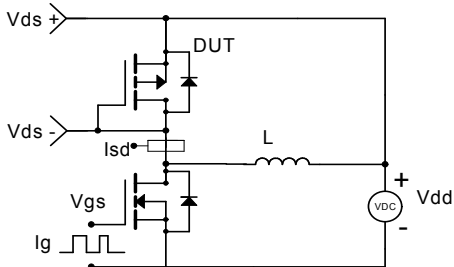
**Resistive Switching Test Circuit & Waveforms**



**Unclamped Inductive Switching (UIS) Test Circuit & Waveforms**



**Diode Recovery Test Circuit & Waveforms**



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