

## General Description

The AOZ1231-01 is high-efficiency, easy-to-use DC/DC synchronous buck regulator that operates up to 28V. The device is capable of supplying 4A of continuous output current with an output voltage adjustable down to 0.8V ( $\pm 1.0\%$ ).

The AOZ1231-01 integrates an internal linear regulator to generate 5.3V  $V_{CC}$  from the input source. If the input voltage is lower than 5.3V, the linear regulator operates in low drop-output mode and the  $V_{CC}$  voltage is equal to input voltage minus the drop-output voltage of the internal linear regulator.

A proprietary constant on-time PWM control with input feed-forward results in ultra-fast transient response while maintaining relatively constant switching frequency over the entire input voltage range. The switching frequency can be externally set up to 1MHz.

The devices feature multiple protection functions such as  $V_{CC}$  under-voltage lockout, cycle-by-current limit, output over-voltage protection, short-circuit protection, and thermal shutdown.

The AOZ1231-01 is available in a 5mm  $\times$  5mm QFN-30L package and is rated over a  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  ambient temperature range.

## Features

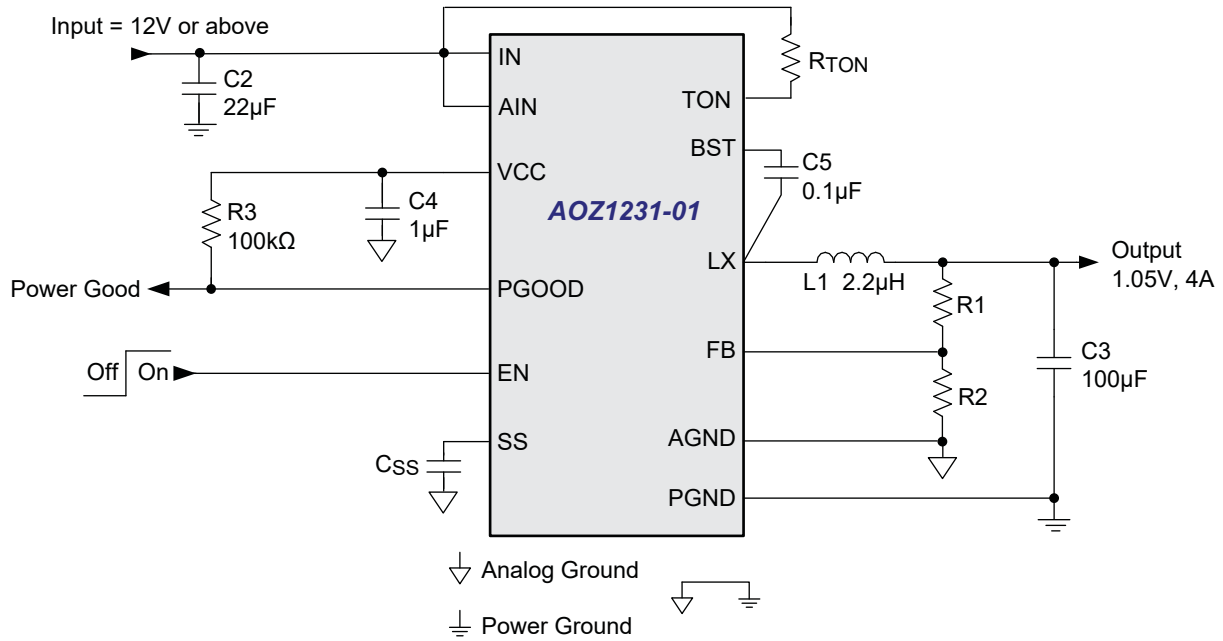
- Wide input voltage range:
  - 4.5V to 28V (internal  $V_{CC}$ )
  - 2.7V to 28V (external  $V_{CC}$ )
- 4A continuous output current
- Output voltage adjustable to 0.8V ( $\pm 1.0\%$ )
- Low  $R_{DS(ON)}$  internal NFETs
  - 40m $\Omega$  high-side
  - 25m $\Omega$  low-side
- Constant On-time with input feed-forward
- Programmable frequency up to 1MHz
- Internal 5.3V, 20mA linear regulator
- Ceramic capacitor stable
- Adjustable soft start
- Power Good output
- Over voltage protection
- Integrated bootstrap diode
- Cycle-by-cycle current limit
- Short-circuit protection
- Thermal shutdown
- Thermally enhanced 5mm  $\times$  5mm QFN-30L package

## Applications

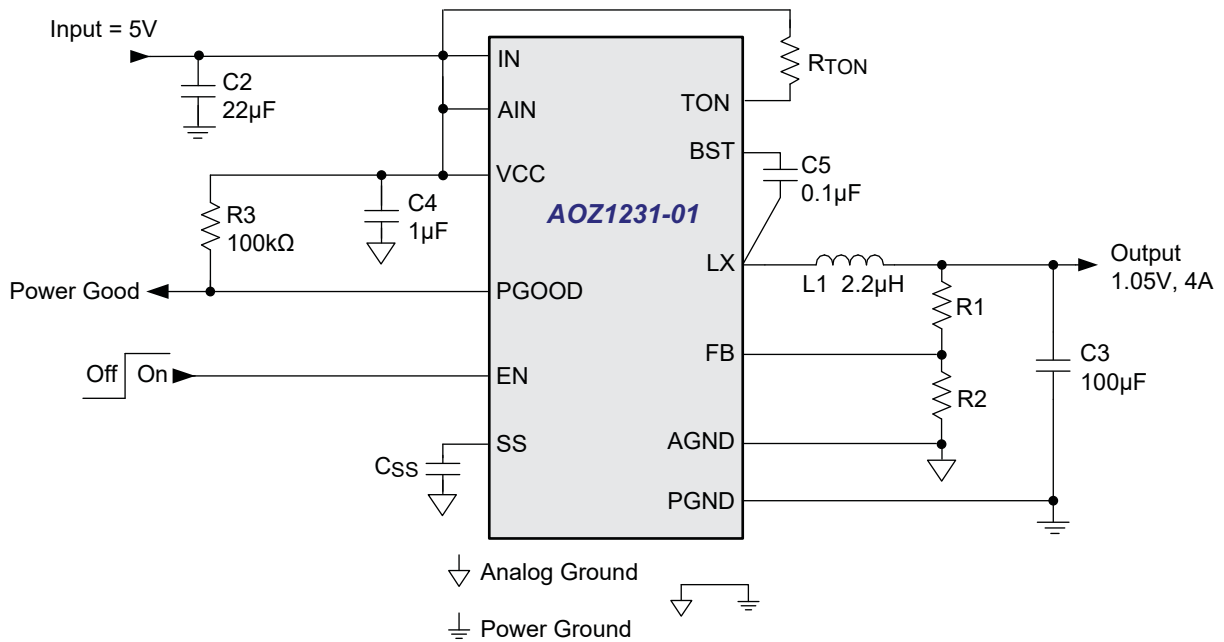
- Portable computers
- Compact desktop PCs
- Servers
- Graphics cards
- Set top boxes
- LCD TVs
- Cable modems
- Point of load DC/DC converters
- Telecom/Networking/Datacom equipment



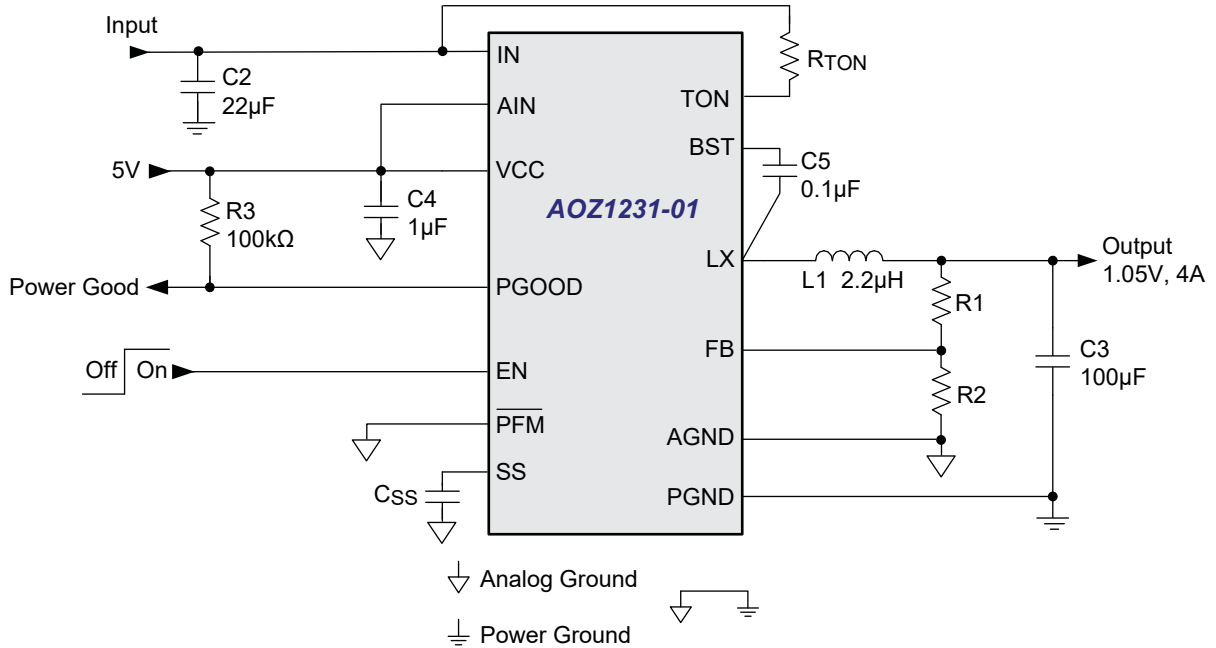
Typical Application for  $V_{IN} = 12V$  or above



Typical Application for  $V_{IN} = 5V$



Typical Application for High Light Load Efficiency Requirement or  $V_{IN} = 3.3V$



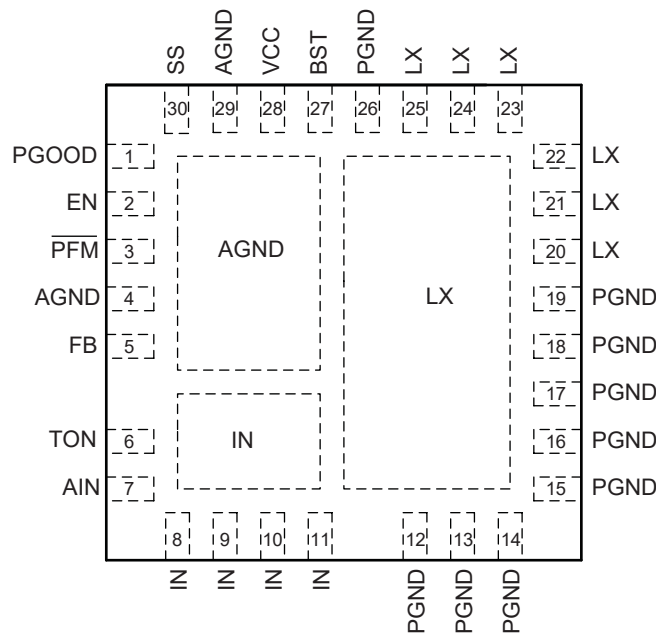
Ordering Information

Part Number	Ambient Temperature Range	Package	Environmental
AOZ1231QI-01	-40°C to +85°C	30-Pin 5mm x 5mm QFN	Green Product



AOS Green Products use reduced levels of Halogens, and are also RoHS compliant. Please visit [www.aosmd.com/media/AOSGreenPolicy.pdf](http://www.aosmd.com/media/AOSGreenPolicy.pdf) for additional information.

## Pin Configuration



30-pin 5mm x 5mm QFN  
(Top View)

## Pin Description

Pin Number	Pin Name	Pin Function
1	PGOOD	Power Good Signal Output. PGOOD is an open-drain output used to indicate the status of the output voltage. It is internally pulled low when the output voltage is 10% lower than the nominal regulation voltage for 50 $\mu$ s (typical time) or 15% higher than the nominal regulation voltage. PGOOD is pulled low during soft-start and shut down.
2	EN	Enable Input. The AOZ1231-01 is enabled when EN is pulled high. The device shuts down when EN is pulled low.
3	$\overline{\text{PFM}}$	PFM Selection Input. Connect $\overline{\text{PFM}}$ pin to VCC/VIN for forced PWM operation. Connect $\overline{\text{PFM}}$ pin to ground for PFM operation to improve light load efficiency.
4, 29	AGND	Analog Ground.
5	FB	Feedback Input. Adjust the output voltage with a resistive voltage-divider between the regulator's output and AGND.
6	TON	On-Time Setting Input. Connect a resistor between VIN and TON to set the on time.
7	AIN	Supply Input for analog functions.
8, 9, 10, 11	IN	Supply Input. IN is the regulator input. All IN pins must be connected together.
12, 13, 14, 15, 16, 17, 18, 19, 26	PGND	Power Ground.
20, 21, 22, 23, 24, 25	LX	Switching Node.
27	BST	Bootstrap Capacitor Connection. The AOZ1231-01 includes an internal bootstrap diode. Connect an external capacitor between BST and LX as shown in the Typical Application diagrams.
28	VCC	Output for internal linear regulator. Bypass VCC to AGND with a 1 $\mu$ F ceramic capacitor. Place the capacitor close to VCC pin.
30	SS	Soft-Start Time Setting Pin. Connect a capacitor between SS and AGND to set the soft-start time.

## Absolute Maximum Ratings

Exceeding the Absolute Maximum Ratings may damage the device.

Parameter	Rating
IN, AIN, TON, PFM to AGND	-0.3V to 30V
LX to AGND	-2V to 30V
BST to AGND	-0.3V to 36V
SS, PGOOD, FB, EN to AGND	-0.3V to 6V
PGND to AGND	-0.3V to +0.3V
Junction Temperature ( $T_J$ )	+150°C
Storage Temperature ( $T_S$ )	-65°C to +150°C
ESD Rating <sup>(1)</sup>	2kV

### Note:

1. Devices are inherently ESD sensitive, handling precautions are required. Human body model rating: 1.5k $\Omega$  in series with 100pF.
2. LX to PGND Transient ( $t < 20$ ns) ----- -7V to  $V_{IN} + 7$ V.

## Maximum Operating Ratings

The device is not guaranteed to operate beyond the Maximum Operating ratings.

Parameter	Rating
Supply Voltage ( $V_{IN}$ )	4.5V to 28V
Output Voltage Range	0.8V to 0.85 $\cdot V_{IN}$
Ambient Temperature ( $T_A$ )	-40°C to +85°C
Package Thermal Resistance	
HS MOSFET	25°C/W
LS MOSFET	20°C/W
PWM Controller	50°C/W

## Electrical Characteristics

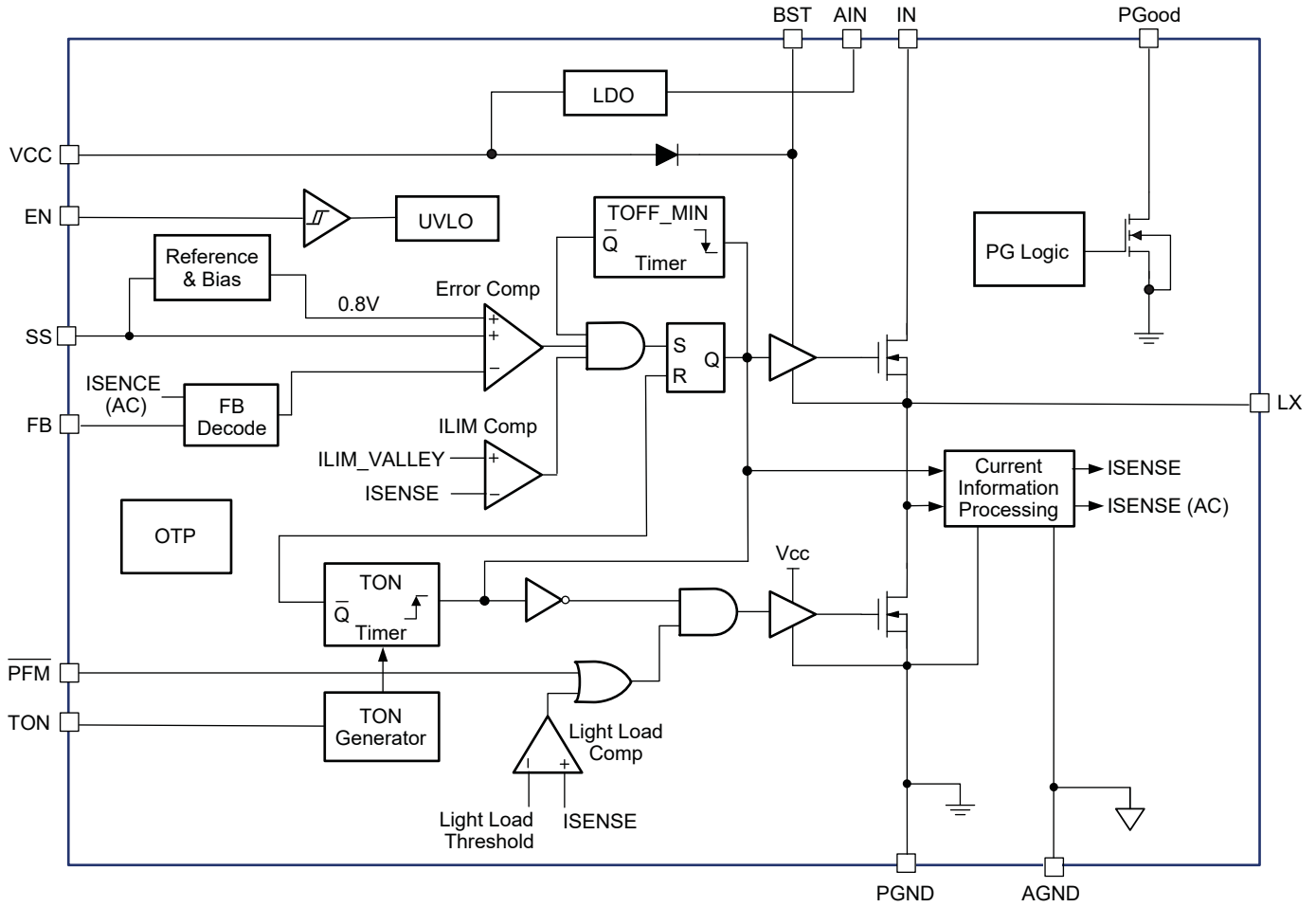
$T_A = 25^\circ\text{C}$ ,  $V_{IN} = 12\text{V}$ ,  $EN = 5\text{V}$ , unless otherwise specified. Specifications in **BOLD** indicate a temperature range of  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
$V_{IN}$	IN Supply Voltage		<b>4.5</b>		<b>28</b>	V
$V_{UVLO}$	Under-Voltage Lockout Threshold of $V_{CC}$	$V_{CC}$ rising $V_{CC}$ falling	<b>3.2</b>	<b>4.0</b> <b>3.7</b>	<b>4.4</b>	V
$I_q$	Quiescent Supply Current of $V_{CC}$	$I_{OUT} = 0$ , $V_{FB} = 1.0\text{V}$ , $V_{EN} > 2\text{V}$		<b>2</b>	<b>3</b>	mA
$I_{OFF}$	Shutdown Supply Current	$V_{EN} = 0\text{V}$		<b>1</b>	<b>20</b>	$\mu\text{A}$
$V_{FB}$	Feedback Voltage	$T_A = 25^\circ\text{C}$ $T_A = 0^\circ\text{C}$ to $85^\circ\text{C}$	0.792 0.788	0.800 0.800	0.808 0.812	V
	Load Regulation			0.5		%
	Line Regulation			1		%
$I_{FB}$	FB Input Bias Current				200	nA
<b>Enable</b>						
$V_{EN}$	EN Input Threshold	Off threshold On threshold	2.5		0.5	V
$V_{EN\_HYS}$	EN Input Hysteresis			100		mV
<b>PFM Control</b>						
	Input Threshold	PFM Mode threshold Force PWM threshold	2.5		0.5	V
	Input Hysteresis			100		mV
<b>Modulator</b>						
$T_{ON}$	On Time	$R_{TON} = 100\text{k}\Omega$ , $V_{IN} = 12\text{V}$ $R_{TON} = 100\text{k}\Omega$ , $V_{IN} = 24\text{V}$	200	250 150	300	ns
$T_{ON\_MIN}$	Minimum On Time			100		ns
$T_{OFF\_MIN}$	Minimum Off Time			250		ns

**Electrical Characteristics (Continued)**
 $T_A = 25^\circ\text{C}$ ,  $V_{IN} = 12\text{V}$ ,  $V_{EN} = 5\text{V}$ , unless otherwise specified. Specifications in **BOLD** indicate a temperature range of  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

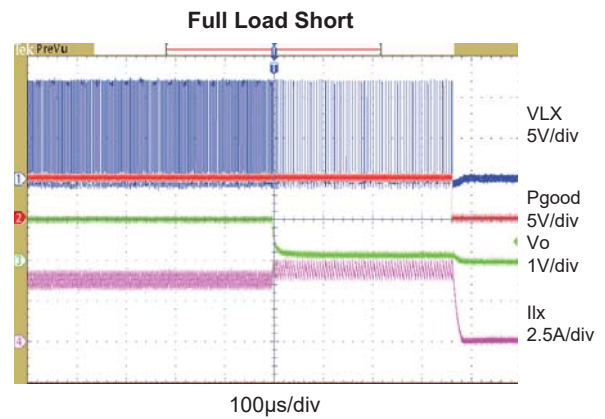
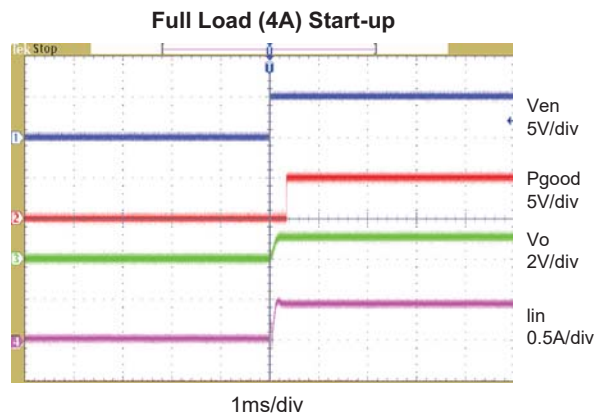
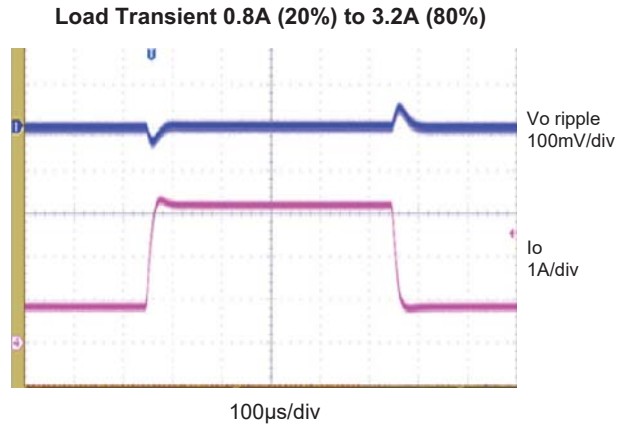
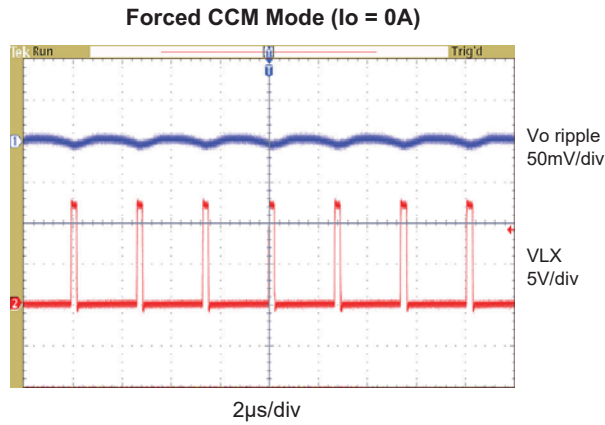
Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
<b>Soft-Start</b>						
$I_{SS\_OUT}$	SS Source Current	$V_{SS} = 0$ , $C_{SS} = 0.001\mu\text{F}$ to $0.1\mu\text{F}$	7	10	15	$\mu\text{A}$
<b>Power Good Signal</b>						
$V_{PG\_LOW}$	PGOOD Low Voltage	$I_{OL} = 1\text{mA}$			<b>0.5</b>	V
	PGOOD Leakage Current				<b><math>\pm 1</math></b>	$\mu\text{A}$
$V_{PGH}$ $V_{PGL}$	PGOOD Threshold	FB rising FB falling	12 -12	15 -10	18 -8	%
	PGOOD Threshold Hysteresis			3		%
$T_{PG\_L}$	PGOOD Fault Delay Time (FB falling)			50		$\mu\text{s}$
<b>Under Voltage and Over Voltage Protection</b>						
$V_{PL}$	Under Voltage threshold	FB falling	-30	-25	-20	%
$T_{PL}$	Under Voltage Delay Time			128		$\mu\text{s}$
$V_{PH}$	Over Voltage Threshold	FB rising	12	15	18	%
$T_{UV\_LX}$	Under Voltage Shutdown Blanking Time	$V_{IN} = 12\text{V}$ , $V_{EN} = 0\text{V}$ , $V_{CC} = 5\text{V}$		20		mS
<b>Power Stage Output</b>						
$R_{DS(ON)}$	High-Side NFET On-Resistance	$V_{IN} = 12\text{V}$		40	60	m $\Omega$
	High-Side NFET Leakage	$V_{EN} = 0\text{V}$ , $V_{LX} = 0\text{V}$			10	$\mu\text{A}$
$R_{DS(ON)}$	Low-Side NFET On-Resistance	$V_{LX} = 12\text{V}$		25	30	m $\Omega$
	Low-Side NFET Leakage	$V_{EN} = 0\text{V}$			10	$\mu\text{A}$
<b>Over-current and Thermal Protection</b>						
$I_{LIM}$	Valley Current Limit	$V_{IN} = 4.5\text{V}$ $V_{IN} = 28\text{V}$	3 4			A
	Thermal Shutdown Threshold	$T_J$ rising $T_J$ falling		145 100		$^\circ\text{C}$

Functional Block Diagram



## Typical Performance Characteristics

Circuit of Typical Application.  $T_A = 25^\circ\text{C}$ ,  $V_{IN} = 12\text{V}$ ,  $V_{OUT} = 1.05\text{V}$ ,  $f_s = 600\text{kHz}$  unless otherwise specified.





## Detailed Description

The AOZ1231-01 is a high-efficiency, easy-to-use, synchronous buck regulators optimized for notebook computers. The regulator is capable of supplying 4A of continuous output current with an output voltage adjustable down to 0.8V. The programmable operating frequency range of 100kHz to 1MHz enables optimizing the configuration for PCB area and efficiency.

The input voltage range for the AOZ1231-01 is 4.5V to 28V. The constant on-time PWM with input feed-forward control scheme results in ultra-fast transient response while maintaining relatively constant switching frequency over the entire input range. The true AC current mode control scheme guarantees the regulator is stable with ceramic output capacitors. The switching frequency can be externally programmed up to 1MHz. Protection features include  $V_{CC}$  under-voltage lockout, valley current limit, output over voltage protection, under voltage protection, short-circuit protection, and thermal shutdown.

The AOZ1231-01 is available in a 30-pin 5mm × 5mm QFN package.

### Input Power Architecture

The AOZ1231-01 integrates an internal linear regulator to generate 5.3V  $V_{CC}$  from input. If the input voltage is lower than 5.3V, the linear regulator operates in low drop-output mode where the  $V_{CC}$  voltage is equal to the input voltage minus the drop-output voltage of the internal linear regulator.

### Enable and Soft Start

The AOZ1231-01 has an external soft start feature to limit in-rush current and ensure the output voltage smoothly ramps up to regulation voltage. The soft start process begins when  $V_{CC}$  rises to 4.1V and voltage on the EN pin is HIGH. An internal current source charges the external soft-start capacitor and the FB voltage follows the voltage of the soft-start pin ( $V_{SS}$ ) when it is lower than 0.8V. When  $V_{SS}$  is higher than 0.8V, the FB voltage is regulated by the internal precise band-gap voltage (0.8V). The soft-start time can be calculated by with the following formula:

$$T_{SS}(\mu s) = 330 \times C_{SS}(nF)$$

If  $C_{SS}$  is 1nF, the soft-start time will be 330 $\mu$ s.  
If  $C_{SS}$  is 10nF, the soft-start time will be 3.3ms.

### Constant-On-Time PWM Control with Input Feed-Forward

The control algorithm of the AOZ1231-01 is constant-on-time PWM Control with input feed-forward.

The simplified control schematic is shown in Figure 1.

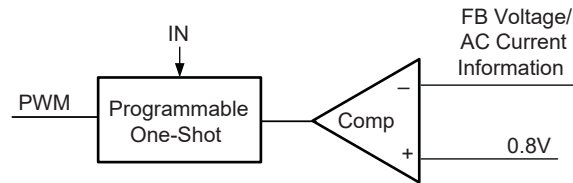


Figure 1. Simplified Control Schematic of AOZ1231-01

The high-side switch on-time is determined solely by a one-shot with a pulse width that can be programmed by one external resistor and is inversely proportional to the input voltage ( $V_{IN}$ ). The one-shot is triggered when the internal 0.8V is lower than the combined information of FB voltage and the AC current information of inductor, which is processed and obtained through the sensed lower-side MOSFET current once it turns-on. The added AC current information can help the stability of constant-on time control even with pure ceramic output capacitors, which have a very low ESR. The AC current information has no DC offset, which does not cause offset with output load change, which is fundamentally different from other  $V^2$  constant-on time control schemes.

The constant-on-time PWM control architecture is a pseudo-fixed frequency with input voltage feed-forward. The internal circuit of the AOZ1231-01 sets the on-time of high-side switch inversely proportional to the  $V_{IN}$  voltage:

$$T_{ON} = \frac{26.3 \times 10^{-12} \times R_{TON}(\Omega)}{V_{IN}(V)} \quad (1)$$

To achieve the flux balance of inductor, the buck converter has the equation:

$$F_{SW} = \frac{V_{OUT}}{V_{IN} \times T_{ON}} \quad (2)$$

Once the product of  $V_{IN} \times T_{ON}$  is constant, the switching frequency keeps constant and is independent with input voltage.

An external resistor between the IN and TON pin sets the switching frequency according to the following equation:

$$F_{SW} = \frac{V_{OUT} \times 10^{12}}{26.3 \times R_{TON}} \quad (3)$$

A further simplified equation will be:

$$F_{SW}(kHz) = \frac{38000 \times V_{OUT}(V)}{R_{TON}(k\Omega)} \quad (4)$$

If  $V_{OUT}$  is 1.8V,  $R_{TON}$  is 137k $\Omega$ , the switching frequency will be 500kHz.

This algorithm results in a nearly constant switching frequency despite the lack of a fixed-frequency clock generator.

### True Current Mode Control

The constant-on-time control scheme is intrinsically unstable if the output capacitor's ESR is not large enough to use as an effective current-sense resistor. Ceramic capacitors usually can not be used as an output capacitor.

The AOZ1231-01 senses the low-side MOSFET current and processes it into DC current and AC current information using an Alpha & Omega proprietary technique. The AC current information is decoded and added on the FB pin on phase. With AC current information, the stability of the constant-on-time control is significantly improved even without the help of the output capacitor's ESR. Thus a pure ceramic capacitor solution can be used. The pure ceramic capacitor solution can significantly reduce the output ripple (no ESR caused overshoot and undershoot) and uses less PCB board area.

### Valley Current-Limit Protection

The AOZ1231-01 provides valley current-limit protection by using the  $R_{DS(ON)}$  of the lower MOSFET current sensing. To detect real current information, a minimum constant off (250ns typical) is implemented after a constant-on time. If the current exceeds the valley current-limit threshold, the PWM controller is not allowed to initiate a new cycle. The actual peak current is greater than the valley current-limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are a function of the inductor value and input and output

voltages. The current limit will keep the low-side MOSFET on and will not allow another high-side on-time, until the current in the low-side MOSFET reduces below the current limit. During the current limit, the inductor current is shown in Figure 2.

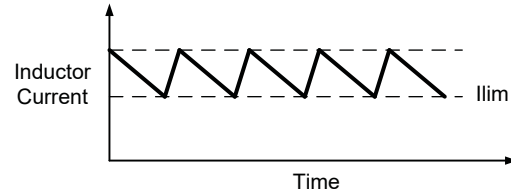


Figure 2. Inductor Current

After 128 $\mu$ s (typical), the AOZ1231-01 considers this as a true fail condition, turns off both high-side and low-side MOSFETs and latches off. Only triggering the enable can restart the AOZ1231-01.

### Output Voltage Under-voltage Protection

If the output voltage is reduced 10% by over-current or short circuit, AOZ1231-01 will wait for 128 $\mu$ s (typical), turns off both high-side and low-side MOSFETs and latches off. Only triggering the enable can restart the AOZ1231-01.

### Output Voltage Over-voltage Protection

The threshold of OVP is set to 15% higher than 800mV. When the Vfb voltage exceeds the OVP threshold, the high-side MOSFET is turned off and the low-side MOSFETs is turned on until Vfb voltage is less than 800mV.

### Power Good Output

The power good (PGOOD) output, which is an open drain output, requires the pull-up resistor. When the output voltage is 10% below the nominal regulation voltage for 50 $\mu$ s (typical), PGOOD is pulled low. When the output voltage is 15% higher than the nominal regulation voltage, PGOOD is also pulled low.

When combined with the under-voltage-protection circuit, this current-limit method is effective in almost every circumstance. In forced-PWM mode, the AOZ1231-01 also implements a negative current limit to prevent excessive reverse inductor currents when VOUT is sinking current.

## Application Information

The basic AOZ1231-01 application circuits is shown in pages 2 and 3. Component selection is explained below.

### Input Capacitor

The input capacitor must be connected to the IN pins and PGND pins of the AOZ1231-01 to maintain steady input voltage and filter out the pulsing input current. A small decoupling capacitor, usually 1 $\mu$ F, should be connected to the VCC pin and AGND pins for stable operation of the AOZ1231-01. The voltage rating of the input capacitor must be greater than the maximum input voltage plus ripple voltage.

The input ripple voltage can be approximated by equation below:

$$\Delta V_{IN} = \frac{I_O}{f \times C_{IN}} \times \left(1 - \frac{V_O}{V_{IN}}\right) \times \frac{V_O}{V_{IN}}$$

Since the input current is discontinuous in a buck converter, the current stress on the input capacitor is another concern when selecting the capacitor. For a buck circuit, the RMS value of the input capacitor current can be calculated by:

$$I_{CIN\_RMS} = I_O \times \sqrt{\frac{V_O}{V_{IN}} \left(1 - \frac{V_O}{V_{IN}}\right)}$$

if let  $m$  equal the conversion ratio:

$$\frac{V_O}{V_{IN}} = m$$

The relationship between the input capacitor RMS current and voltage conversion ratio is calculated and shown in Figure 3. It can be seen that when  $V_O$  is half of  $V_{IN}$ ,  $C_{IN}$  is under the worst current stress. The worst current stress on  $C_{IN}$  is  $0.5 \times I_O$ .

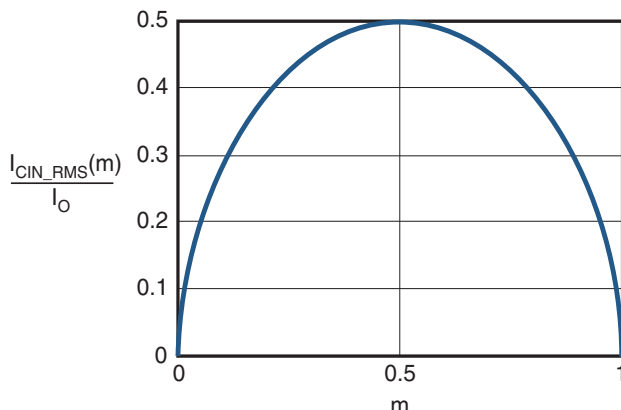


Figure 3.  $I_{CIN}$  vs. Voltage Conversion Ratio

For reliable operation and best performance, the input capacitors must have a current rating higher than  $I_{CIN\_RMS}$  at the worst operating conditions. Ceramic capacitors are preferred as input capacitors because of their low ESR and high ripple current rating. Depending on the application circuits, other low ESR tantalum capacitors or aluminum electrolytic capacitors may be used. When selecting ceramic capacitors, X5R or X7R type dielectric ceramic capacitors are preferred for their better temperature and voltage characteristics. Note that the ripple current rating from capacitor manufacturers is based on a certain life time. Further de-rating may be necessary for practical design requirements.

### Inductor

The inductor is used to supply constant current to output when it is driven by a switching voltage. For a given input and output voltage, inductance and switching frequency together decide the inductor ripple current, which is:

$$\Delta I_L = \frac{V_O}{f \times L} \times \left(1 - \frac{V_O}{V_{IN}}\right)$$

The peak inductor current is:

$$I_{Lpeak} = I_O + \frac{\Delta I_L}{2}$$

High inductance provides low inductor ripple current but requires a larger size inductor to avoid saturation. Low ripple current reduces inductor core losses. It also reduces RMS current through the inductor and switches, which results in less conduction loss. Usually, peak to peak ripple current on inductor is designed to be 30% to 50% of output current.

When selecting the inductor, make sure it is able to handle the peak current without saturation even at the highest operating temperature.

The inductor takes the highest current in a buck circuit. The conduction loss on inductor needs to be checked for thermal and efficiency requirements.

Surface mount inductors in different shape and styles are available from Coilcraft, Elytone and Murata. Shielded inductors are small and radiate less EMI noise. They also cost more than unshielded inductors. The choice depends on EMI requirement, price and size.

## Output Capacitor

The output capacitor is selected based on the DC output voltage rating, output ripple voltage specification and ripple current rating.

The selected output capacitor must have a higher rated voltage specification than the maximum desired output voltage including ripple. De-rating needs to be considered for long term reliability.

Output ripple voltage specification is another important factor for selecting the output capacitor. In a buck converter circuit, output ripple voltage is determined by inductor value, switching frequency, output capacitor value and ESR. It is calculated by the equation below:

$$\Delta V_O = \Delta I_L \times \left( ESR_{CO} + \frac{1}{8 \times f \times C_O} \right)$$

where,

$C_O$  is output capacitor value and

$ESR_{CO}$  is the Equivalent Series Resistor of the output capacitor.

When a low ESR ceramic capacitor is used as the output capacitor, the impedance of the capacitor at the switching frequency dominates. Output ripple is mainly caused by capacitor value and inductor ripple current. The output ripple voltage calculation can be simplified to:

$$\Delta V_O = \Delta I_L \times \frac{1}{8 \times f \times C_O}$$

If the impedance of the ESR at switching frequency dominates, the output ripple voltage is mainly decided by capacitor ESR and inductor ripple current. The output ripple voltage calculation can be further simplified to:

$$\Delta V_O = \Delta I_L \times ESR_{CO}$$

For lower output ripple voltage across the entire operating temperature range, X5R or X7R dielectric type ceramic capacitors, or other low ESR tantalum are recommended to be used as output capacitors.

In a buck converter, output capacitor current is continuous. The RMS current of output capacitor is decided by the peak-to-peak inductor ripple current. It can be calculated by:

$$I_{CO\_RMS} = \frac{\Delta I_L}{\sqrt{12}}$$

Usually, the ripple current rating of the output capacitor is a smaller issue because of the low current stress. When the buck inductor is selected to be very small and inductor ripple current is high, output capacitor could be overstressed.

## Thermal Management and Layout Consideration

In the AOZ1231-01 buck regulator circuit, high pulsing current flows through two circuit loops. The first loop starts from the input capacitors, to the IN pins, to the LX pins, to the filter inductor, to the output capacitor and load, and then returns to the input capacitor through ground. Current flows in the first loop when the high side switch is on. The second loop starts from the inductor, to the output capacitors and load, to the low side switch. Current flows in the second loop when the low side low side switch is on.

In PCB layout, minimizing the board area of the two loops reduces the noise of the circuit and improves efficiency. A ground plane is strongly recommended to connect input capacitor, output capacitor, and PGND pins of the AOZ1231-01.

In the AOZ1231-01 buck regulator circuit, the major power dissipating components are the AOZ1231-01 and the output inductor. The total power dissipation of the converter circuit can be measured by input power minus output power:

$$P_{total\_loss} = V_{IN} \times I_{IN} - V_O \times I_O$$

The power dissipation of the inductor can be approximately calculated by output current and DCR of inductor:

$$P_{inductor\_loss} = I_O^2 \times R_{inductor} \times 1.1$$

The actual junction temperature can be calculated with power dissipation in the AOZ1231-01 and thermal impedance from junction to ambient:

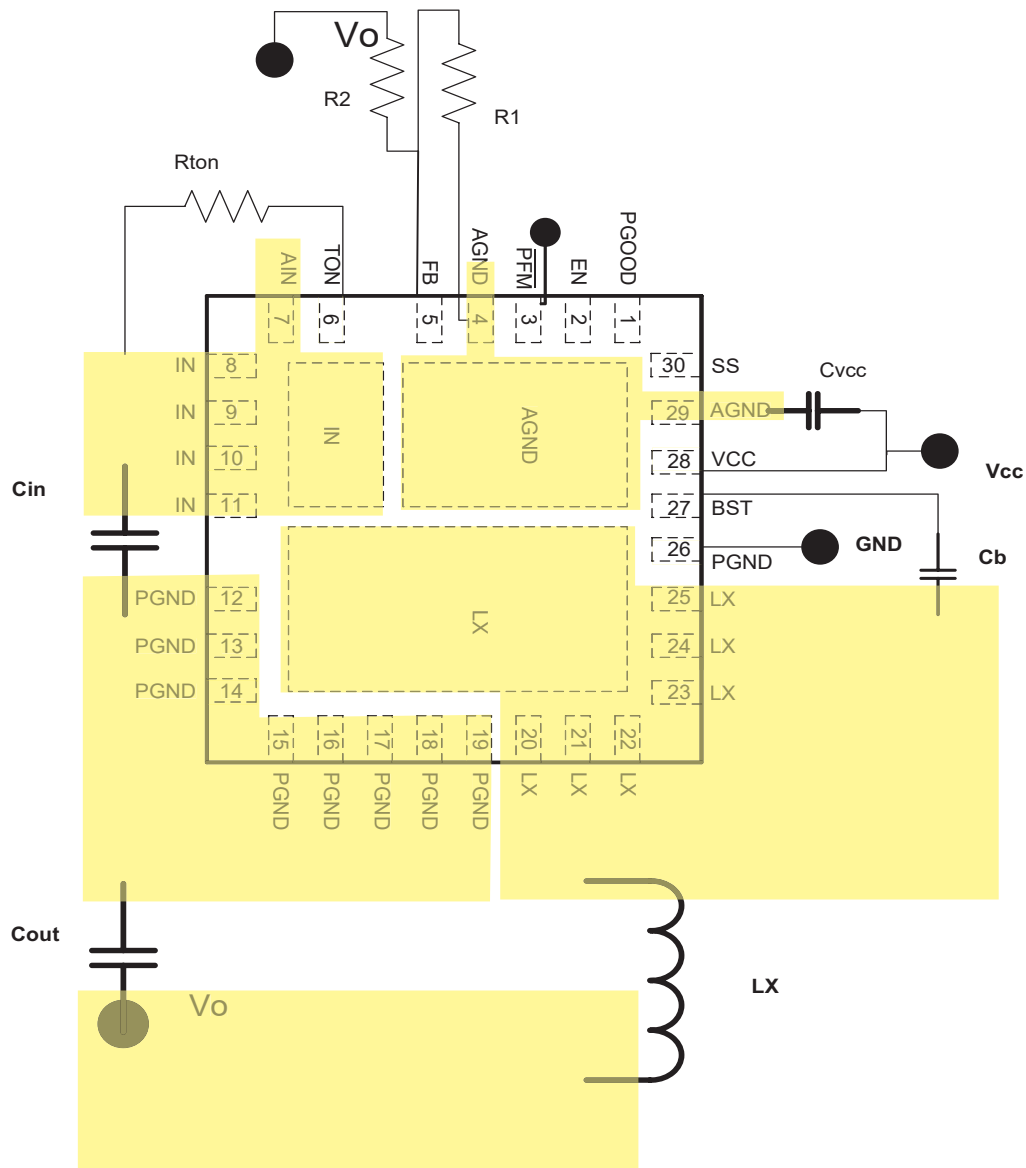
$$T_{junction} = (P_{total\_loss} - P_{inductor\_loss}) \times \Theta_{JA}$$

The maximum junction temperature of the AOZ1231-01 is 150°C, which limits the maximum load current capability.

The thermal performance of the AOZ1231-01 is strongly affected by the PCB layout. Extra care should be taken by users during design process to ensure that the IC will operate under the recommended environmental conditions.

Several layout tips are listed below for the best electric and thermal performance.

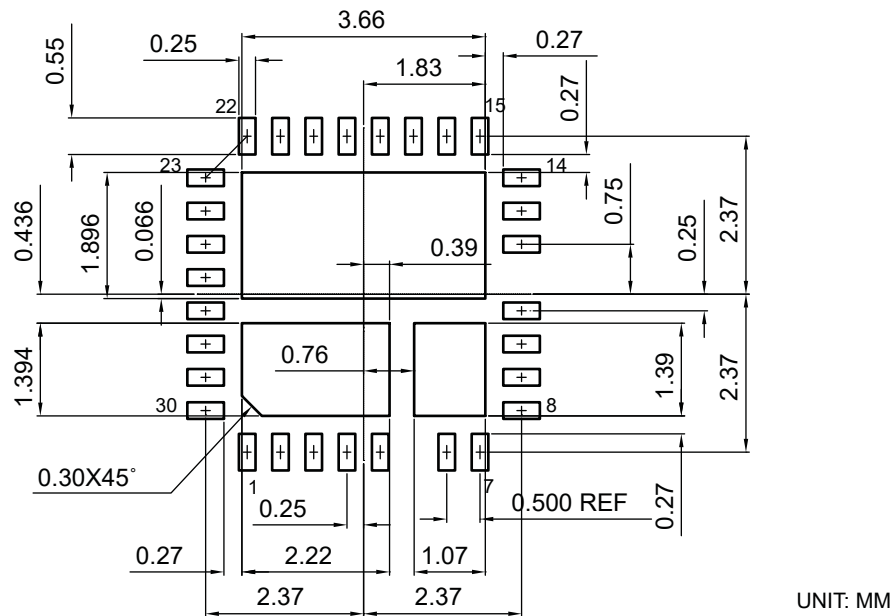
1. The LX pins and pad are connected to internal low side switch drain. They are low resistance thermal conduction path and the most noisy switching node. Connect a large copper plane to the LX pins to help thermal dissipation.
2. The IN pins and pad are connected to the internal high side switch drain. They are also low resistance thermal conduction path. Connect a large copper plane to the IN pins to help thermal dissipation.
3. Do not use thermal relief connection to the PGND pins. Pour a maximized copper area to the PGND pins to help thermal dissipation.
4. Input capacitors should be connected as close as possible to the IN pins and the PGND pins to reduce the switching spikes.
5. Decoupling capacitor  $C_{VCC}$  should be connected as close as possible to VCC and AGND.
6. Voltage divider R1 and R2 should be placed as close as possible to FB and AGND.
7.  $R_{ton}$  should be connected as close as possible to Pin 6 (TON pin).
8. Pin 26 (PGND) is connected to the ground plane through via. A ground plane is preferred.
9. Keep sensitive signal traces such as the feedback trace away from the LX pins.
10. Pour copper plane on all unused board area and connect it to stable DC nodes, like VIN, GND or VOUT.





Package Dimensions, QFN 5x5, 30 Lead EP3\_S (Continued)

RECOMMENDED LAND PATTERN



UNIT: MM

Dimensions in millimeters

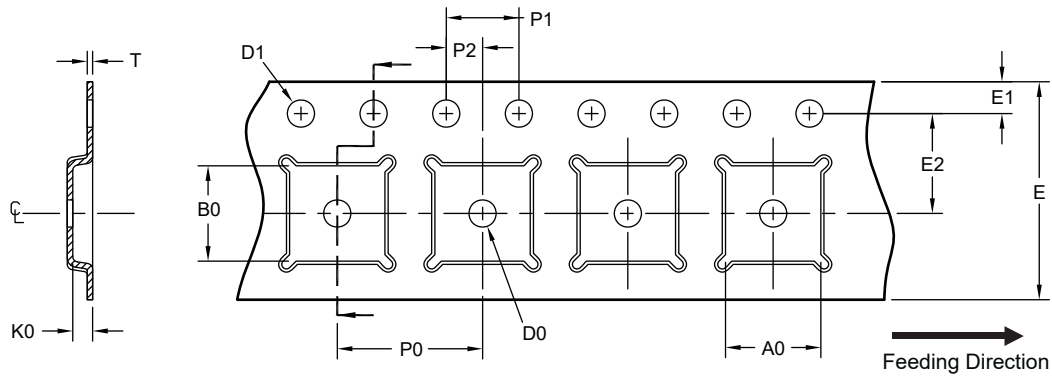
Symbols	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3	0.20 REF		
b	0.20	0.25	0.35
D	5.00 BSC		
D1	2.12	2.22	2.32
D2	0.97	1.07	1.17
D3	3.56	3.66	3.76
E	5.00 BSC		
E1	1.294	1.394	1.494
E2	1.796	1.896	1.996
e	0.50 BSC		
L	0.30	0.40	0.50
L1	0.336	0.436	0.536
L2	—	0.066	0.166
L3	0.29	0.39	0.49
L4	0.66	0.76	0.86
L5	0.17	0.27	0.37
aaa	0.15		
bbb	0.10		
ccc	0.10		
ddd	0.08		

Dimensions in inches

Symbols	Min.	Typ.	Max.
A	0.031	0.035	0.039
A1	0.000	0.001	0.002
A3	0.008 REF		
b	0.008	0.010	0.014
D	0.197 BSC		
D1	0.083	0.087	0.091
D2	0.038	0.042	0.046
D3	0.140	0.144	0.148
E	0.197 BSC		
E1	0.051	0.055	0.059
E2	0.110	0.114	0.118
e	0.020 BSC		
L	0.012	0.016	0.020
L1	0.013	0.017	0.021
L2	—	0.003	0.007
L3	0.011	0.015	0.019
L4	0.026	0.030	0.034
L5	0.007	0.011	0.015
aaa	0.006		
bbb	0.004		
ccc	0.004		
ddd	0.003		

### Tape and Reel Dimensions, QFN 5x5, 30 Lead EP3\_S

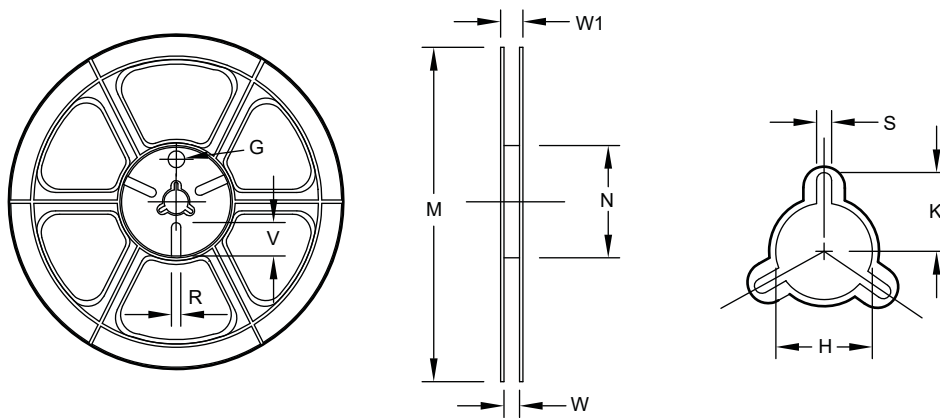
#### Carrier Tape



UNIT: mm

Package	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
QFN 5x5 (12mm)	5.25 ±0.10	5.25 ±0.10	1.10 ±0.10	1.50 Min.	1.50 +0.10/-0	12.00 ±0.3	1.75 ±0.10	5.50 ±0.05	8.00 ±0.10	4.00 ±0.10	2.00 ±0.05	0.30 ±0.05

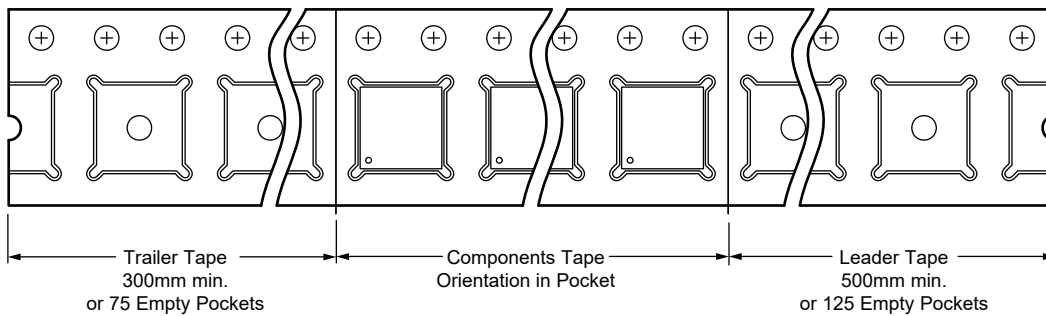
#### Reel



UNIT: mm

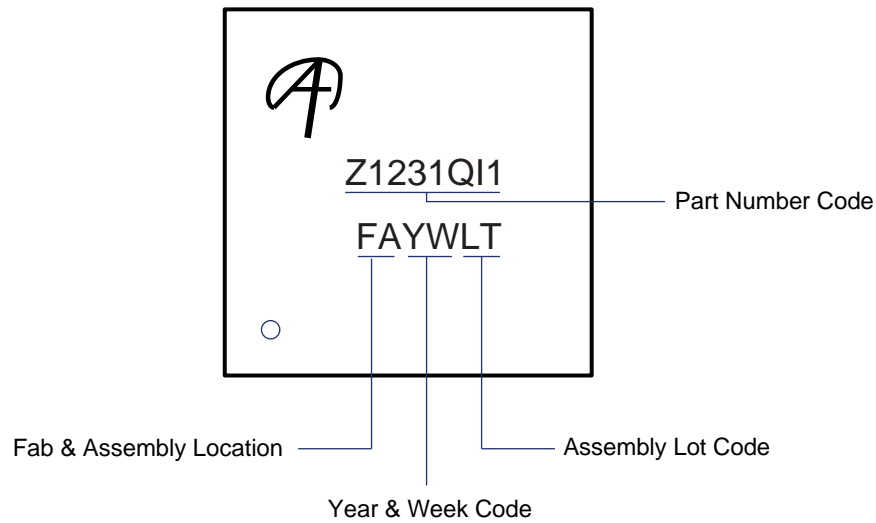
Tape Size	Reel Size	M	N	W	W1	H	K	S	G	R	V
12mm	ø330	ø330.0 ±2.0	ø79.0 ±1.0	12.4 +2.0/-0.0	17.0 +2.6/-1.2	ø13.0 ±0.5	10.5 ±0.2	2.0 ±0.5	-	-	-

#### Leader/Trailer and Orientation





**Part Marking**



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- |   |   |
|---|---|
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|---|---|

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