ALPHA & OMEGA
SEMICONDUCTOR

AOZ5311NQI

High-Current, High-Performance DrMOS Power Module

General Description

The AOZ5311NQI is a high efficiency synchronous buck power stage module consisting of two asymmetrical MOSFETs and an integrated driver. The MOSFETs are individually optimized for operation in the synchronous buck configuration. The High-Side MOSFET is optimized to achieve low capacitance and gate charge for fast switching with low duty cycle operation. The Low-Side MOSFET has ultra low ON resistance to minimize conduction loss.

The AOZ5311NQI uses a PWM input for accurate control of the power MOSFETs switching activities, is compatible with 3V and 5V (CMOS) logic and supports Tri-State PWM.

A number of features are provided making the AOZ5311NQI a highly versatile power module. The boot-strap switch is integrated in the driver. The Low-Side MOSFET can be driven into diode emulation mode to provide asynchronous operation and improve light-load performance. The pin-out is also optimized for low parasitics, keeping their effects to a minimum.

Features

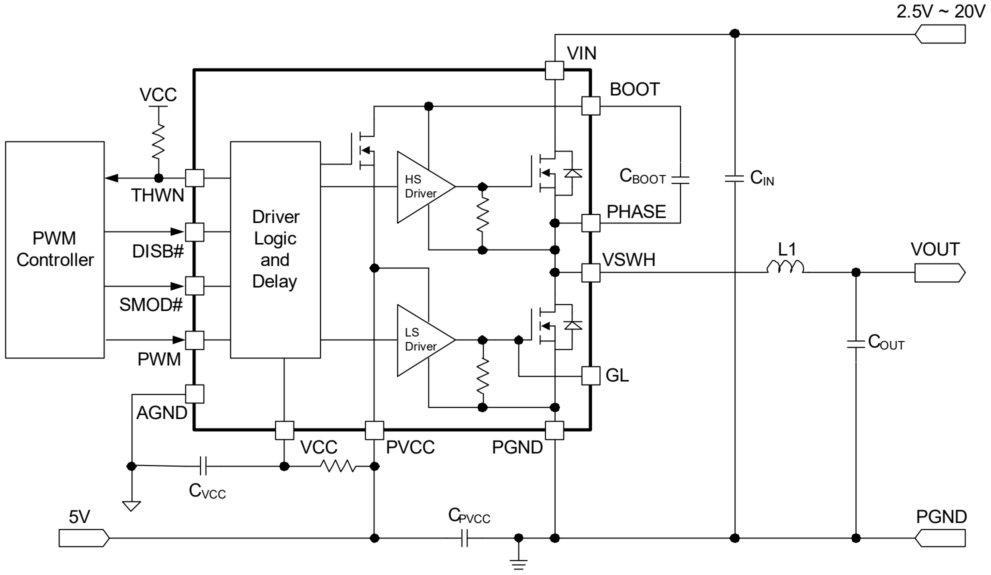
- 2.5V to 20V power supply range
- 4.5V to 5.5V driver supply range
- 55A continuous output current
    - Up to 80A for 10ms on pulse
    - Up to 120A for 10us on pulse
- Up to 2MHz switching operation
- 3V / 5V PWM / Tri-State input compatible
- Under-Voltage lockout protection
- SMOD# control for Diode Emulation / CCM operation
- < 1mV detection threshold for efficient ZCD control
- Low profile 5x5 QFN-31L package

Applications

- Memory and graphic cards
- VRMs for motherboards
- Point of load DC/DC converters
- Video gaming console

Green
Product

Typical Application Circuit

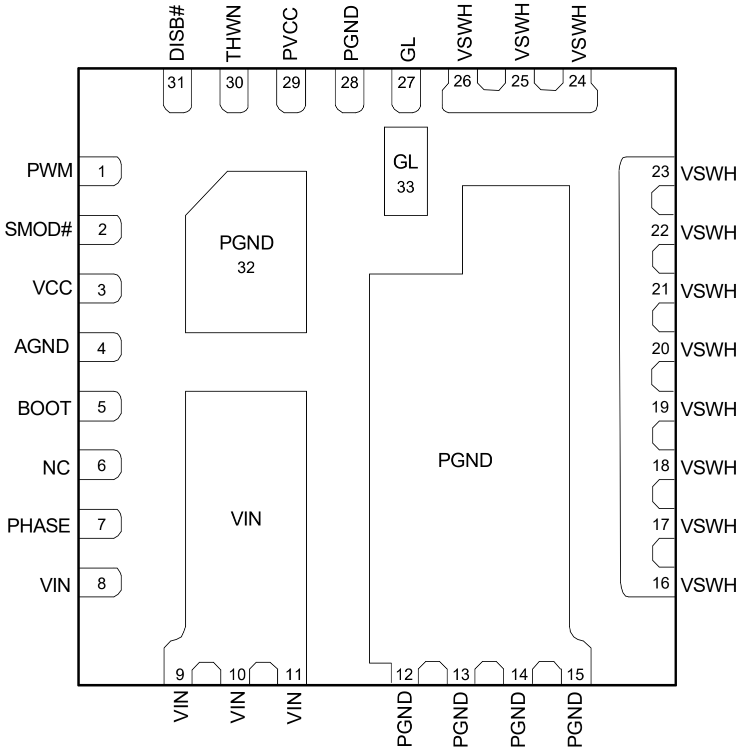


Ordering Information

Part Number	Ambient Temperature Range	Package	Environmental
AOZ5311NQI	-40°C to 125°C	QFN5x5-31L	RoHS

AOS Green Products use reduced levels of Halogens, and are also RoHS compliant.
Please visit www.aosmd.com/media/AOSGreenPolicy.pdf for additional information.

Pin Configuration

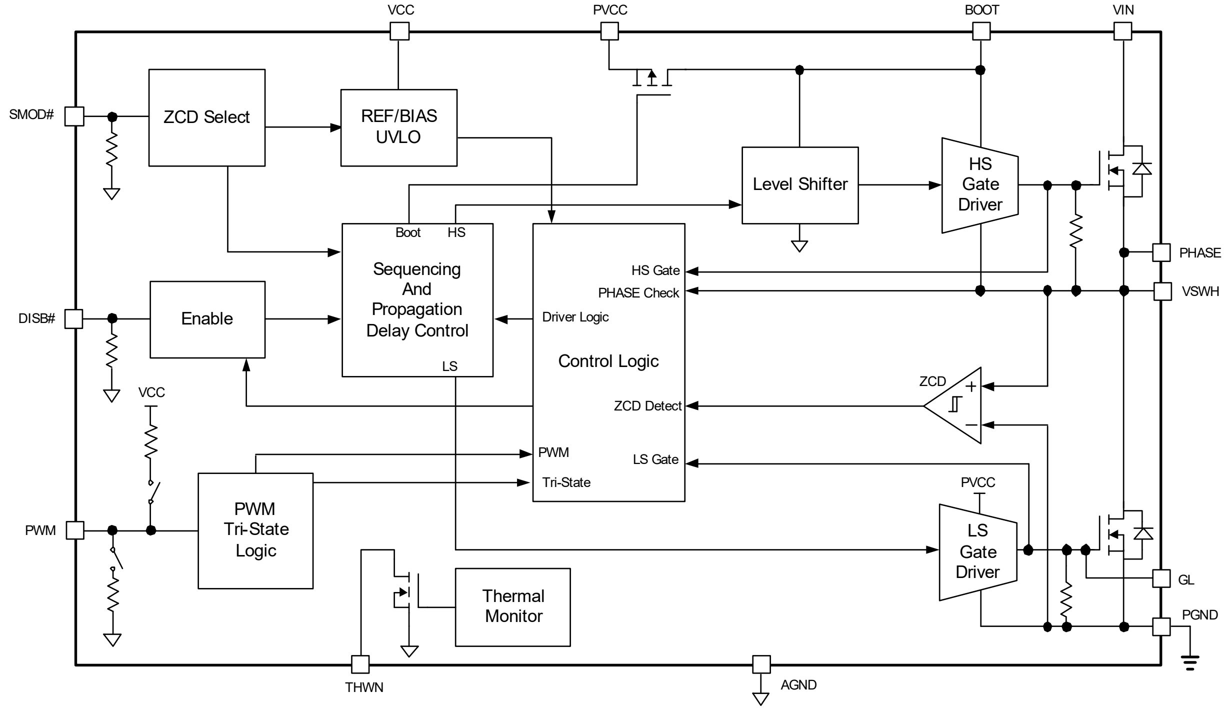


QFN5x5-31L
(Top View)

Pin Description

Pin Number	Pin Name	Pin Function
1	PWM	PWM input signal from the controller IC. When DISB#=0V, the internal resistor divider will be disconnected and this pin will be at high impedance.
2	SMOD#	Pull low to enable Discontinuous Mode of Operation (DCM), Diode Emulation or Skip Mode. There is an internal pull-down resistor to AGND.
3	VCC	5V Bias for Internal Logic Blocks. Ensure to position a 1µF MLCC directly between VCC and AGND (Pin 4).
4	AGND	Signal Ground.
5	BOOT	High-Side MOSFET Gate Driver supply rail. Connect a 100nF ceramic capacitor between BOOT and the PHASE (Pin 7).
6	NC	Internally connected to VIN paddle. It can be left floating (no connect) or tied to VIN.
7	PHASE	This pin is dedicated for bootstrap capacitor AC return path connection from BOOT (Pin 5).
8, 9, 10, 11	VIN	Power stage High Voltage Input (Drain connection of High-Side MOSFET).
12, 13, 14, 15	PGND	Power Ground pin for power stage (Source connection of Low-Side MOSFET).
16,17,18,19, 20,21,22, 23, 24, 25, 26	VSWH	Switching node connected to the Source of High-Side MOSFET and the Drain of Low-Side MOSFET. These pins are used for Zero Cross Detection and Anti-Overlap Control as well as main inductor terminal.
27, 33	GL	Low-Side MOSFET Gate connection. This is for test purposes only.
28, 32	PGND	Power Ground pin for High-Side and Low-Side MOSFET Gate Drivers. Ensure to connect 1µF directly between PGND and PVCC (Pin 29).
29	PVCC	5V power rail for High-Side and Low-Side MOSFET gate drivers. Ensure to position a 1µF MLCC directly between PVCC to PGND (Pin 28).
30	THWN	Thermal warning indicator. This is an open−drain output. When the temperature at the driver IC die reaches the Over Temperature Threshold, this pin is pulled low.
31	DISB#	Output disable pin. When this pin is pulled to a logic low level, the IC is disabled. There is an internal pull−down resistor to AGND.

Functional Block Diagram



Absolute Maximum Ratings

Exceeding the Absolute Maximum ratings may damage the device.

Parameter	Rating
Low Voltage Supply (VCC, PVCC)	-0.3V to 7V
High Voltage Supply (VIN)	-0.3V to 25V
Control Inputs (PWM, SMOD#, DISB#)	-0.3V to (VCC+0.3V)
Output (THWN)	-0.3V to (VCC+0.3V)
Bootstrap Voltage DC (BOOT-PGND)	-0.3V to 28V
Bootstrap Voltage Transient(1) (BOOT-PGND)	-8V to 30V
Bootstrap Voltage DC (BOOT-PHASE/VSWH)	-0.3V to 7V
BOOT Voltage Transient(1) (BOOT-PHASE/VSWH)	-0.3V to 9V
Switch Node Voltage DC (PHASE/VSWH)	-0.3V to 25V
Switch Node Voltage Transient(1) (PHASE/VSWH)	-8V to 33V
Low-Side Gate Voltage DC (GL)	(PGND-0.3V) to (PVCC+0.3V)
Low-Side Gate Voltage Transient(2) (GL)	(PGND-2.5V) to (PVCC+0.3V)
VSWH Current DC	55A
VSWH Current 10ms Pulse	80A
VSWH Current 10us Pulse	120A
Storage Temperature (T_S)	-65°C to +150°C
Max Junction Temperature (T_J)	150°C
ESD Rating(3)	2kV

Notes:

1. Peak voltages can be applied for 10ns per switching cycle.
2. Peak voltages can be applied for 20ns per switching cycle.
3. Devices are inherently ESD sensitive, handling precautions are required. Human body model rating: 1.5kΩ in series with 100pF.

Recommended Operating Conditions

The device is not guaranteed to operate beyond the Maximum Recommended Operating Conditions.

Parameter	Rating
High Voltage Supply (VIN)	2.5V to 20V
Low Voltage/ MOSFET Driver Supply (VCC, PVCC)	4.5V to 5.5V
Control Inputs (PWM, SMOD#, DISB#)	0V to VCC
Output (THWN)	0V to VCC
Operating Frequency	200kHz to 2MHz

Electrical Characteristics(4)

T_J = 0°C to 150°C. Typical values reflect 25°C ambient temperature; VIN = 12V, VOUT = 1V, PVCC = VCC = DISB# = 5V, unless otherwise specified. Min/Max values are guaranteed by test, design, or statistical correlation.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
GENERAL						
V_{IN}	Power Stage Power Supply		2.5		20	V
V_{CC}	Low Voltage Bias Supply	PVCC = VCC	4.5		5.5	V
$R_{\theta JC}$(5)	Thermal Resistance	Reference to High-Side MOSFET temperature rise		2.5		°C/W
$R_{\theta JA}$(5)		Freq = 300kHz. AOS Demo Board		12.5		°C/W
INPUT SUPPLY AND UVLO						
V_{CC_UVLO}	Under-Voltage Lockout	VCC Rising		3.5	3.9	V
V_{CC_HYST}		VCC Hysteresis		400		mV
I_{VCC}	Control Circuit Bias Current	DISB# = 0V		1		μA
		SMOD# = 5V, PWM = 0V		550		μA
		SMOD# = 0V, PWM = 0V		535		μA
		SMOD# = 0V, PWM =1.65V		430		μA
I_{PVCC}	Drive Circuit Operating Current	PWM = 400kHz, 20% Duty Cycle		13		mA
		PWM = 1MHz, 20% Duty Cycle		33		mA
PWM INPUT						
V_{PWM_H}	Logic High Input Voltage		2.7			V
V_{PWM_L}	Logic Low Input Voltage				0.72	V
I_{PWM_SRC}	PWM Pin Input Current	PWM = 0V		-150		μA
I_{PWM_SNK}		PWM = 3.3V		150		μA
V_{TRI}	PWM Input Tri-State Window		1.35		2.1	V
V_{PMW_FLOAT}	PWM Tri-State Voltage Clamp	PWM = Floating		1.65		V
DISB# INPUT						
$V_{DISB\#\_ON}$	Enable Input Voltage		2.0			V
$V_{DISB\#\_OFF}$	Disable Input Voltage				0.8	V
$R_{DISB\#}$	DISB# Input Resistance	Pull-Down Resistor		850		kΩ
SMOD# INPUT						
$V_{SMOD\#\_H}$	Logic High Input Voltage		2.0			V
$V_{SMOD\#\_L}$	Logic Low Input Voltage				0.8	V
$R_{SMOD\#}$	SMOD# Input Resistance	Pull-Down Resistor		850		kΩ
GATE DRIVER TIMING						
t_{PDLU}	PWM to High-Side Gate	PWM: H → L, VSWH: H → L		24		ns
t_{PDLL}	PWM to Low-Side Gate	PWM: L → H, GL: H → L		25		ns
t_{PDHU}	Low-side to High-Side Gate Deadtime	GL: H → L, VSWH: L → H		15		ns
t_{PDHL}	High-Side to Low-side Gate Deadtime	VSWH: H → 1V, GL: L → H		13		ns
t_{TSSHD}	Tri-State Shutdown Delay	PWM: L → V_{TRI}, GL: H → L and PWM: H → V_{TRI}, VSWH: H → L		25		ns
t_{TSEXIT}	Tri-State Propagation Delay	PWM: V_{TRI} → H, VSWH: L → H PWM: V_{TRI} → L, GL: L → H		35		ns

Electrical Characteristics(4)

T_J = 0°C to 150°C. Typical values reflect 25°C ambient temperature; VIN = 12V, VOUT = 1V, PVCC = VCC = DISB# = 5V, unless otherwise specified. Min/Max values are guaranteed by test, design, or statistical correlation.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
ZERO CROSS DETECTION						
V_{ZCD}	Zero Cross Detect Threshold	SMOD# = L		0.5		mV
t_{ZCD}	Zero Cross Detect Blanking Time	SMOD# = L		350		ns
THERMAL NOTIFICATION(5)						
T_{JTHWN}	Junction Thermal Threshold	Temperature Rising		150		°C
T_{JHYST}	Junction Thermal Hysteresis			30		°C
V_{THWN}	THWN Pin Output Low	I_{THWN} = 0.5mA		60		mV
R_{THWN}	THWN Pull-Down Resistance			120		Ω

Notes:

4. All voltages are specified with respect to the corresponding AGND pin.
5. Characterization value. Not tested in production.

Timing Diagram

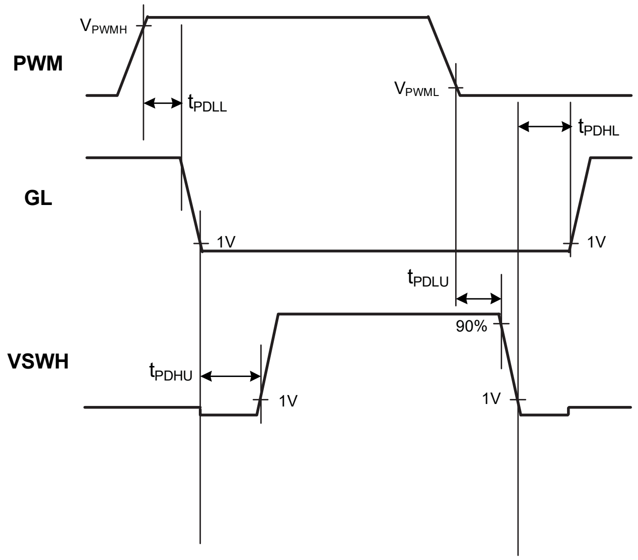


Figure 1. PWM Logic Input Timing Diagram

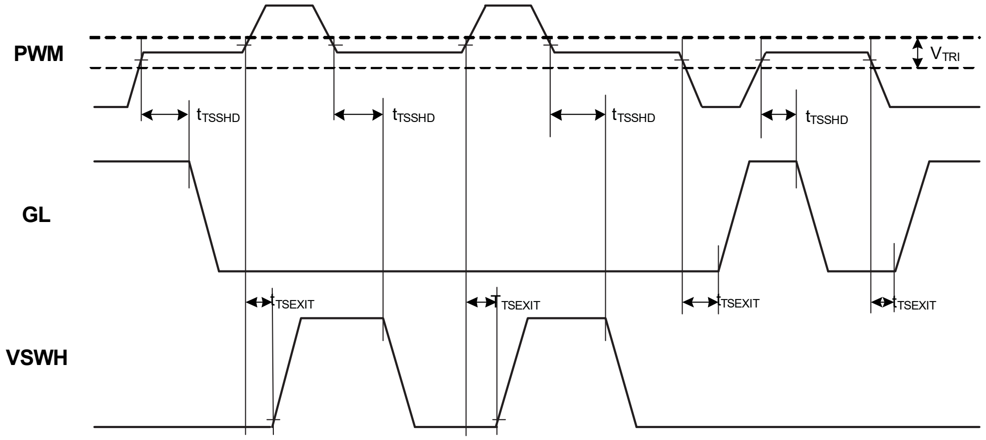


Figure 2. PWM Tri-State Hold Off and Exit Timing Diagram

Table 1. Input Control Truth Table

DISB#	SMOD#	PWM(6)	GH (Not a Pin)	GL
L	X	X	L	L
H	L	H	H	L
H	L	H to Tri-State	L	H, Forward IL L, Reverse IL
H	L	L to Tri-State	L	L
H	L	L	L	H
H	H	H	H	L
H	H	L	L	H
H	H	Tri-state	L	L

Note:

6. Diode emulation mode is activated when SMOD# is LOW and PWM transition from HIGH to Tri-State.Zero Cross Detection (ZCD) at I_L*$Rdson_{(LS)}$ = 0.5mV to turn off GL.

Typical Performance Characteristics

T_A = 25°C, VIN = 12V, PVCC = VCC = 5V, unless otherwise specified.

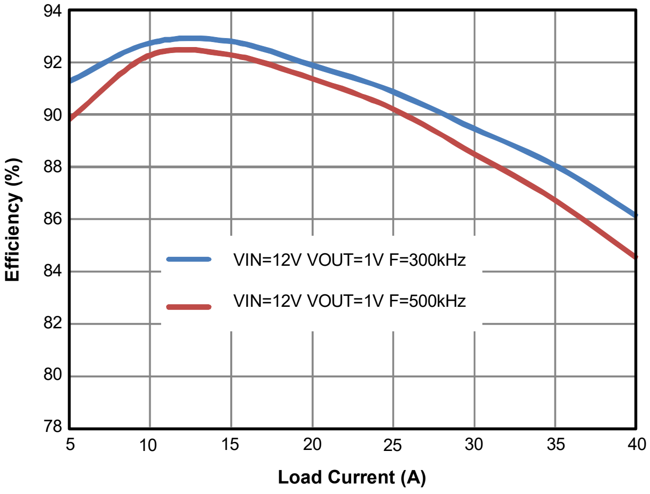


Figure 3. Efficiency vs. Load Current

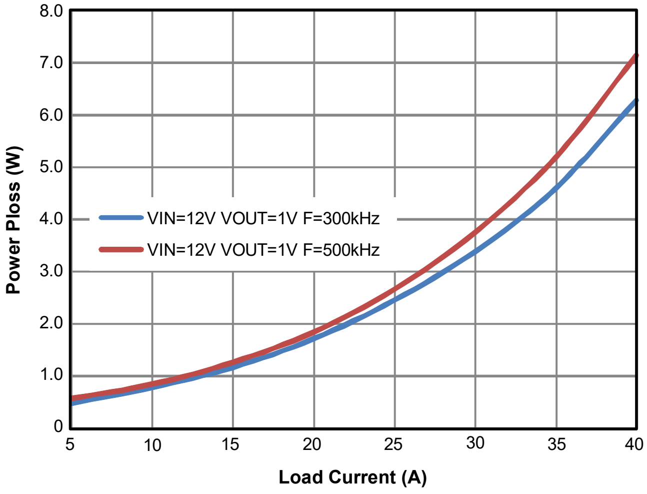


Figure 4. Power Loss vs. Load Current

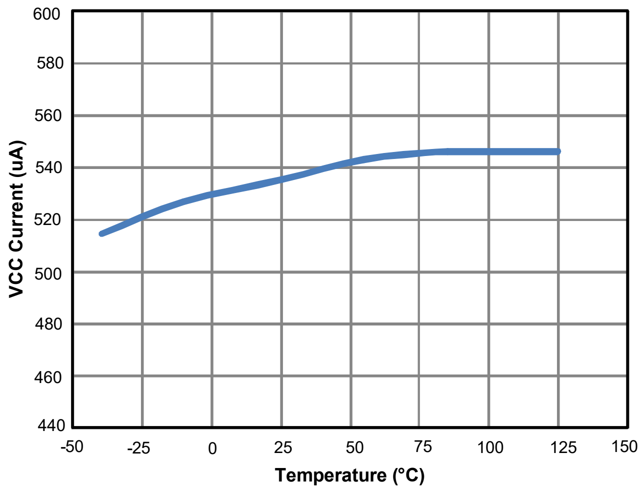


Figure 5. Supply Current (I_{VCC}) vs. Temperature

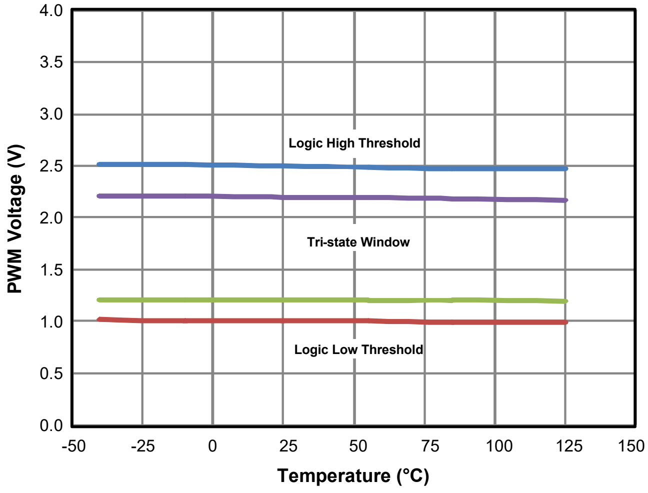


Figure 6. PWM Threshold vs. Temperature

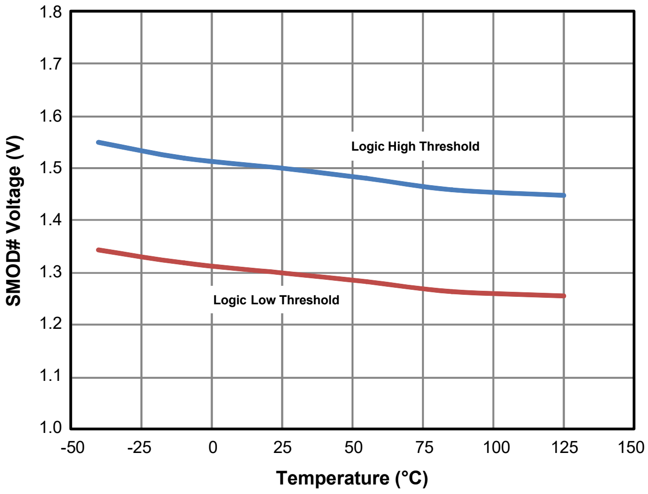


Figure 7. SMOD# Threshold vs. Temperature

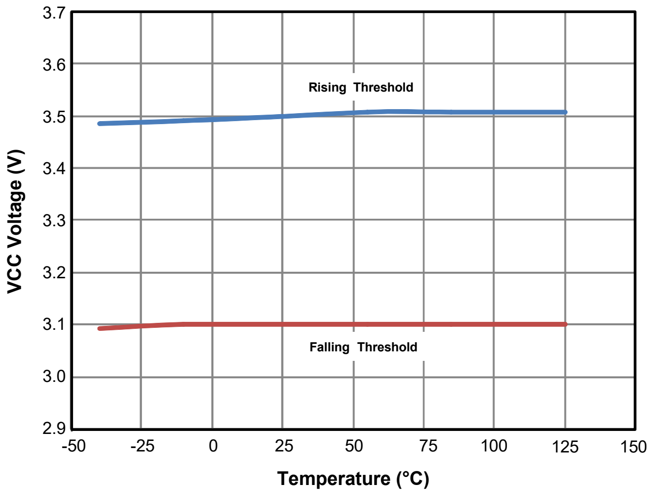


Figure 8. UVLO (VCC) Threshold vs. Temperature

Typical Performance Characteristics

T_A = 25°C, VIN = 12V, PVCC = VCC = 5V, unless otherwise specified.

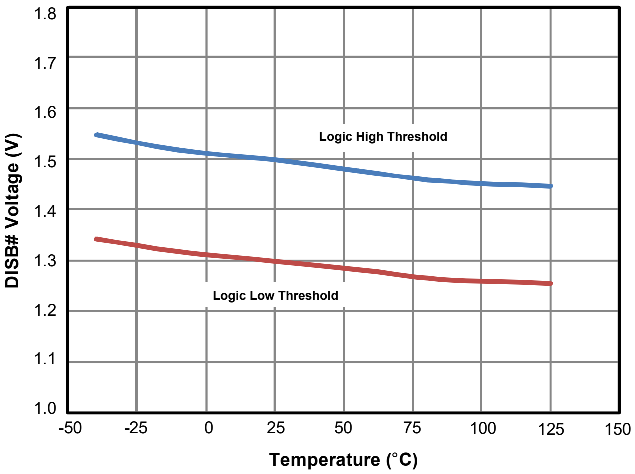


Figure 9. DISB# Threshold vs. Temperature

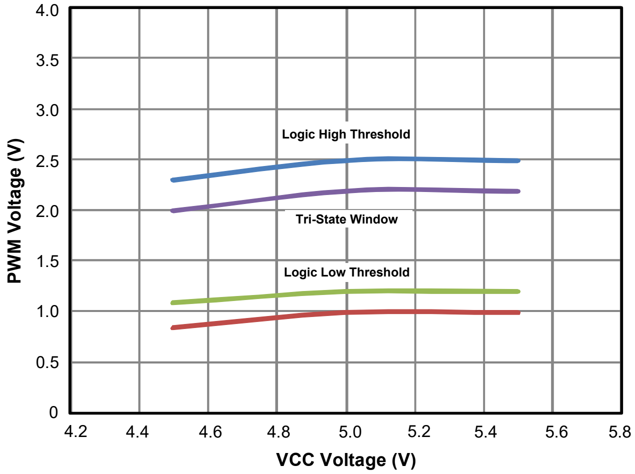


Figure 10. PWM Threshold vs. VCC Voltage

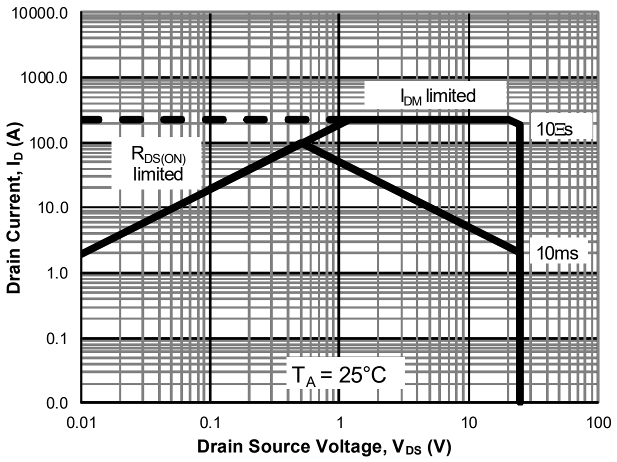


Figure 11. High-Side MOSFET SOA

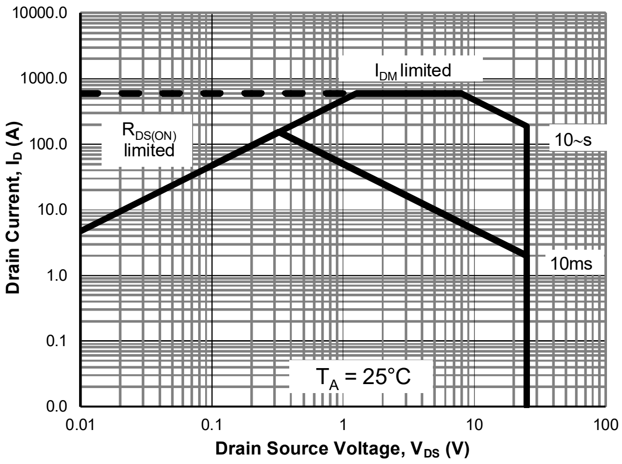


Figure 12. Low-Side MOSFET SOA

Application Information

AOZ5311NQI is a fully integrated power module designed to work over an input voltage range of 2.5V to 20V with a separate 5V supply for gate drive and internal control circuitry. The MOSFETs are individually optimized for efficient operation on both High-Side and Low-Side for a low duty cycle synchronous buck converter. High current MOSFET Gate Drivers are integrated in the package to minimize parasitic loop inductance for optimum switching efficiency.

Powering the Module and the Gate Drives

An external supply PVCC = 5V is required for driving the MOSFETs. The MOSFETs are designed with optimally customized gate thresholds voltages to achieve the most advantageous compromise between fast switching speed and minimal power loss. The integrated gate driver is capable of supplying large peak current into the Low-Side MOSFET to achieve fast switching. A ceramic bypass capacitor of 1µF or higher is recommended from PVCC (Pin 29) to PGND (Pin 28). The control logic supply VCC (Pin 3) can be derived from the gate drive supply PVCC (Pin 29) through an RC filter to bypass the switching noise (See Typical Application Circuit).

The boost supply for driving the High-Side MOSFET is generated by connecting a small capacitor (100nF) between the BOOT (Pin 5) and the switching node PHASE (Pin 7). It is recommended that this capacitor C_{BOOT} should be connected to the device across Pin 5 and Pin 7 as close as possible. A bootstrap switch is integrated into the device to reduce external component count. An optional resistor R_{BOOT} in series with C_{BOOT} between 1Ω to 5Ω can be used to slow down the turn on speed of the High-Side MOSFET to achieve both short switching time and low VSWH switching node spikes at the same time.

Under-Voltage Lockout

AOZ5311NQI starts up to normal operation when VCC rises above the Under-Voltage Lock-Out (UVLO) threshold voltage. The UVLO release is set at 3.5V typically. Since the PWM control signal is provided from an external controller or a digital processor, extra caution must be taken during start up. AOZ5311NQI must be powered up before PWM input is applied.

Normal system operation begins with a soft start sequence by the controller to minimize in-rush current during start up. Powering the module with a full duty cycle PWM signal may lead to many undesirable consequences due to excessive power. AOZ5311NQI provides some protections such as UVLO and thermal monitor. For system level protection, the PWM controller should monitor the current output and protect the load under all possible operating and transient conditions.

Disable (DISB#) Function

The AOZ5311NQI can be enabled and disabled through DISB# (Pin 31). The driver output is disabled when DISB# input is connected to AGND. The module would be in standby mode with low quiescent current of less than 1µA. The module will be active when DISB# is connected to VCC Supply. The driver output will follow PWM input signal. A weak pull-down resistor is connected between DISB# and AGND.

Power up sequence design must be implemented to ensure proper coordination between the module and external PWM controller for soft start and system enable/disable. It is recommended that the AOZ5311NQI should be disabled before the PWM controller is disabled. This would make sure AOZ5311NQI will be operating under the recommended conditions.

Input Voltage VIN

AOZ5311NQI is rated to operate over a wide input range from 2.5V to 20V. For high current synchronous buck converter applications, large pulse current at high frequency and high current slew rates (di/dt) will be drawn by the module during normal operation. It is strongly recommended to place a bypass capacitor very close to the package leads at the input supply (VIN). Both X7R or X5R quality surface mount ceramic capacitors are suitable.

The High-Side MOSFET is optimized for fast switching by using low gate charges (Q_G) device. When the module is operated at high duty cycle ratio, conduction loss from the High-Side MOSFET will be higher. The total power loss for the module is still relatively low but the High-Side MOSFET higher conduction loss may have higher temperature. The two MOSFETs have their own exposed pads and PCB copper areas for heat dissipation. It is recommended that worst case junction temperature be measured for both High-Side MOSFET and Low-Side MOSFET to ensure that they are operating within Safe Operating Area (SOA).

PWM Input

AOZ5311NQI is compatible with 3V and 5V (CMOS) PWM logic. Refer to Figure 1 for PWM logic timing and propagation delays diagram between PWM input and the MOSFET gate drives. AOZ5311NQI is compatible with 3V and 5V (CMOS) PWM logic. Refer to Figure 1 for PWM logic timing and propagation delays diagram between PWM input and the MOSFET gate drives.

The PWM is also compatible with Tri-State input. When the PWM output from the external PWM controller is in high impedance or not connected both High-Side and Low-Side MOSFETs are turned off and VSWH is in high impedance state. Table 2 shows the thresholds level for high-to-low and low-to-high transitions as well as Tri-State window.

There is a Hold-off Delay between the corresponding PWM Tri-State signal and the MOSFET gate drivers to prevent spurious triggering of Tri-State mode which may be caused by noise or PWM signal glitches. The Hold-off Delay is typically 25ns.

Table 2. PWM Input and Tri-State Thresholds

Thresholds →	V_{PWMH}	V_{PWML}	V_{TRIH}	V_{TRIL}
AOZ5311NQI	2.7 V	0.72 V	1.35 V	2.1 V

Note: See Figure 2 for propagation delays and tri-state window.

Diode Mode Emulation of Low Side MOSFET (SMOD#)

AOZ5311NQI can be operated in the diode emulation or pulse skipping mode using SMOD# (Pin 2). This enables the converter to operate in asynchronous mode during start up, light load or under pre-bias conditions.

When SMOD# is high, the module will operate in Continuous Conduction Mode (CCM). The Driver logic will use the PWM signal and generate both the High-Side and Low-Side complementary gate drive outputs with minimal anti-overlap delays to avoid cross conduction.

When SMOD# is low, the module can operate in Discontinuous Conduction Mode (DCM). The High-Side MOSFET gate drive output is not affected but Low-Side MOSFET will enter diode emulation mode. See Table 2 for all truth table for DISB#, SMOD# and PWM inputs.

Gate Drives

AOZ5311NQI has an internal high current high speed driver that generates the floating gate driver for the High-Side MOSFET and a complementary driver for the Low-Side MOSFET. An internal shoot through protection scheme is implemented to ensure that both MOSFETs cannot be turned on at the same time. The operation of PWM signal transition is illustrated as below.

1. PWM from logic Low to logic High

When the falling edge of Low-Side Gate Driver output GL goes below 1V, the blanking period is activated. After a pre-determined value (t_{PDHU}), the complementary High-Side Gate Driver output GH is turned on.

2. PWM from logic High to logic Low

When the falling edge of switching node VSWH goes below 1V, the blanking period is activated. After a pre-determined value (t_{PDHL}), the complementary Low-Side Gate Driver output GL is turned on

This mechanism prevents cross conduction across the input bus line VIN and PGND. The anti-overlap circuit monitors the switching node VSWH to ensure a smooth transition between the two MOSFETs under any load transient conditions.

Thermal Warning (THWN)

The driver IC temperature is internally monitored and an thermal warning flag at THWN (Pin 30) is asserted if it exceeds 150°C. This warning flag is reset when the temperature drop back to 120°C. THWN is an open drain output that is pulled to AGND to indicate an over-temperature condition. It should be connected to VCC through a resistor for monitoring purpose. The device will not power down during the over temperature condition.

PCB Layout Guidelines

AOZ5311NQI is a high current module rated for operation up to 2MHz. This requires fast switching speed to keep the switching losses and device temperatures within limits. An integrated gate driver within the package eliminates driver-to-MOSFET gate pad parasitic of the package or on PCB.

To achieve high switching speeds, high levels of slew rate (dv/dt and di/dt) will be present throughout the power train which requires careful attention to PCB layout to minimize voltage spikes and other transients. As with any synchronous buck converter layout, the critical requirement is to minimize the path of the primary switching current loop formed by the High-Side MOSFET, Low-Side MOSFET, and the input bypass capacitor C_{IN}. The PCB design is greatly simplified by the optimization of the AOZ5311NQI pin out. The power inputs of VIN and PGND are located adjacent to each other and the input bypass capacitors C_{IN} should be placed as close as possible to these pins. The area of the secondary switching loop is formed by Low-Side MOSFET, output inductor L1, and output capacitor C_{OUT} is the next critical requirement. This requires second layer or "Inner 1" to be the PGND plane. VIAs should then be placed near PGND pads.

While AOZ5311NQI is a highly efficient module, it is still dissipating significant amount of heat under high power conditions. Special attention is required for thermal design. MOSFETs in the package are directly attached to individual exposed pads (VIN and PGND) to simplify thermal management. Both VIN and VSWH pads should be attached to large areas of PCB copper. Thermal relief pads should be placed to ensure proper heat dissipation to the board. An inner power plane layer dedicated to VIN, typically the high voltage system input, is desirable and VIAs should be provided near the device to connect the VIN pads to the power plane. Significant amount of heat can also be dissipated through multiple PGND pins. A large copper area connected to the PGND pins in addition to the system ground plane through VIAs will further improve thermal dissipation.

As shown on Figure. 13, the top most layer of the PCB should comprise of wide and exposed copper area for the primary AC current loop which runs along VIN pad originating from the input capacitors C10, C11 and C12 that are mounted to a large PGND pad. They serve as thermal relief as heat flows down to the VIN exposed pad that fan out to a wider area. Adding VIAs will only help transfer heat to cooler regions of the PCB board through the other layers beneath but serve no purpose to AC activity as all the AC current sees the lowest impedance on the top layer only.

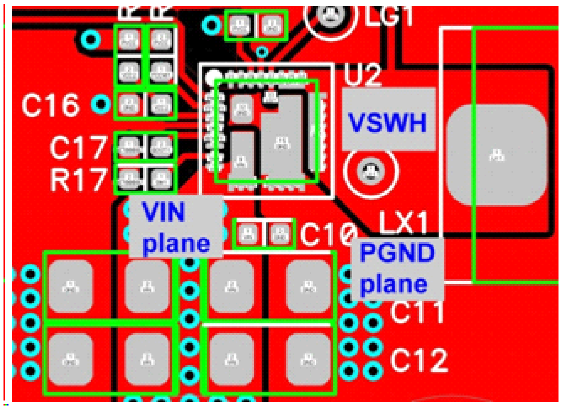


Figure 13. Top Layer of Demo Board, VIN, VSWH and PGND Copper Planes

As the primary and secondary (complimentary) AC current loops move through VIN to VSWH and through PGND to VSWH, large positive and negative voltage spike appear at the VSWH terminal which are caused by the large internal di/dt produced by the package parasitic. To minimize the effects of this interference at the VSWH terminal, at which the main inductor L1 is mounted, size just enough for the inductor to physically fit. The goal is to employ the least amount of copper area for this VSWH terminal, only enough so the inductor can be securely mounted.

To minimize the effects of switching noise coupling to the rest of the sensitive areas of the PCB, the area directly underneath the designated VSWH pad or inductor terminal is voided and the shape of this void is replicated descending down through the rest of the layers. Refer to Figure 14.

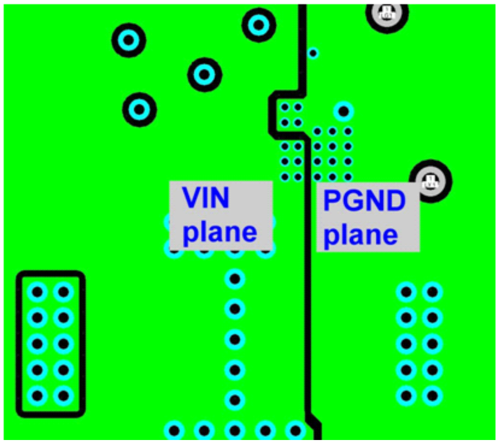
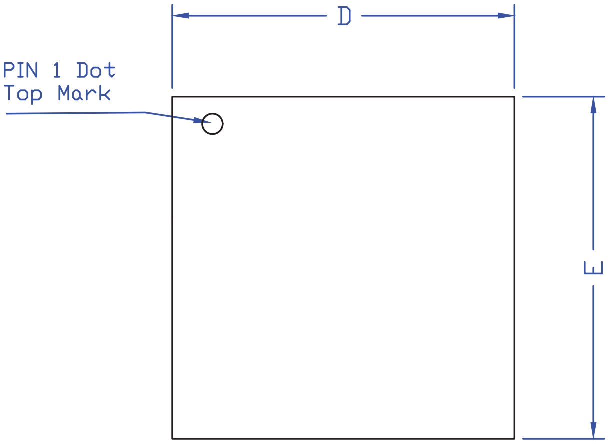


Figure 14. Bottom Layer PCB layout, VSWH Copper Plane Voided on Descending Layers

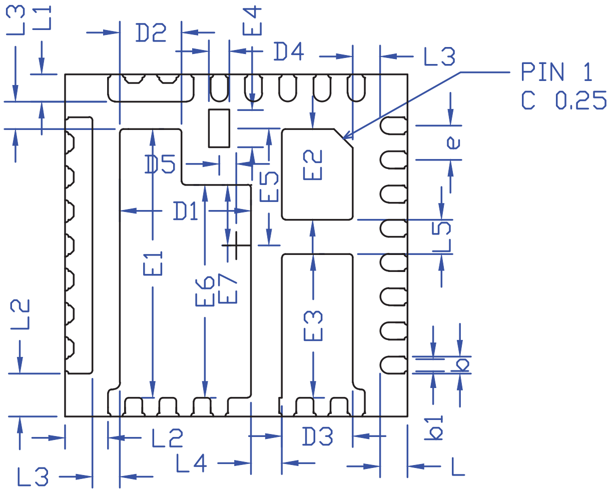
Positioning via through the landing pattern of the VIN and PGND thermal pads will help quickly facilitate the thermal build up and spread the heat much more quickly towards the surrounding copper layers descending from the top layer. (See RECOMMENDED LANDING PATTERN AND VIA PLACEMENT section).

The exposed pads dimensional footprint of the 5x5 QFN package is shown on the package dimensions page. For optimal thermal relief, it is recommended to fill the PGND and VIN exposed landing pattern with 10mil diameter VIAs. 10mil diameter is a commonly used via diameter as it is optimally cost effective based on the tooling bit used in manufacturing. Each via is associated with a 20mil diameter keep out. Maintain a 5mil clearance (127um) around the inside edge of each exposed pad in an event of solder overflow, potentially shorting with the adjacent expose thermal pad.

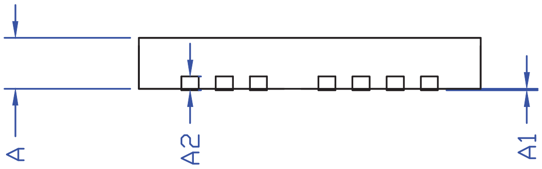
Package Dimensions, QFN5x5-31L



TOP VIEW



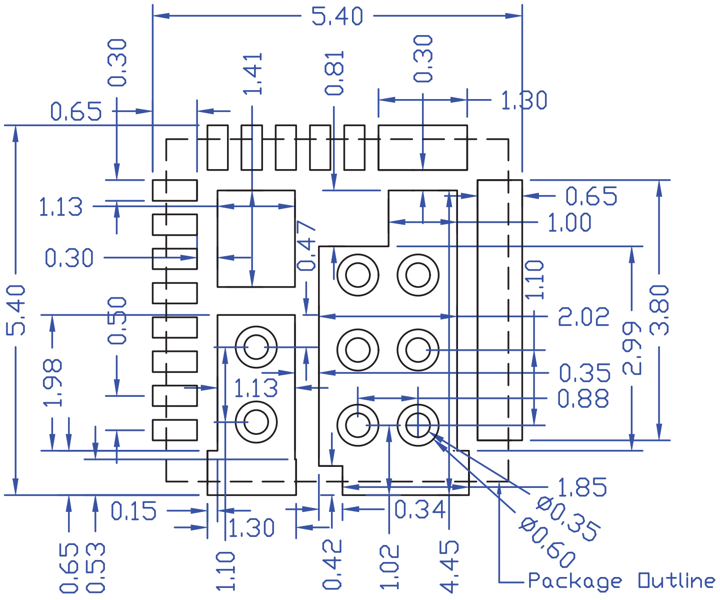
BOTTOM VIEW



SIDE VIEW

SYMBOLS	DIMENSION IN MM			DIMENSION IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	-	0.05	0.000	-	0.002
A2	0.20REF			0.008REF		
D	4.90	5.00	5.10	0.193	0.197	0.201
E	4.90	5.00	5.10	0.193	0.197	0.201
D1	1.87	1.92	1.97	0.074	0.076	0.078
D2	0.85	0.90	0.95	0.033	0.035	0.037
D3	0.99	1.04	1.09	0.039	0.041	0.043
D4	0.25	0.30	0.35	0.010	0.012	0.014
D5	0.20	0.25	0.30	0.008	0.010	0.012
E1	3.88	3.93	3.98	0.153	0.155	0.156
E2	1.27	1.32	1.37	0.050	0.052	0.054
E3	2.05	2.10	2.15	0.081	0.083	0.085
E4	0.50	0.55	0.60	0.020	0.022	0.024
E5	1.66	1.71	1.76	0.065	0.067	0.069
E6	3.06	3.11	3.16	0.121	0.122	0.124
E7	0.84	0.89	0.94	0.033	0.035	0.037
L	0.35	0.40	0.45	0.014	0.016	0.018
L1	0.35	0.40	0.45	0.014	0.016	0.018
L2	0.58	0.63	0.68	0.023	0.025	0.027
L3	0.35	0.40	0.45	0.014	0.016	0.018
L4	0.40	0.45	0.50	0.016	0.018	0.020
L5	0.45	0.50	0.55	0.018	0.020	0.022
b	0.20	0.25	0.30	0.008	0.010	0.012
b1	0.13	0.18	0.23	0.005	0.007	0.009
e	0.50BSC			0.020BSC		

RECOMMENDED LAND PATTERN

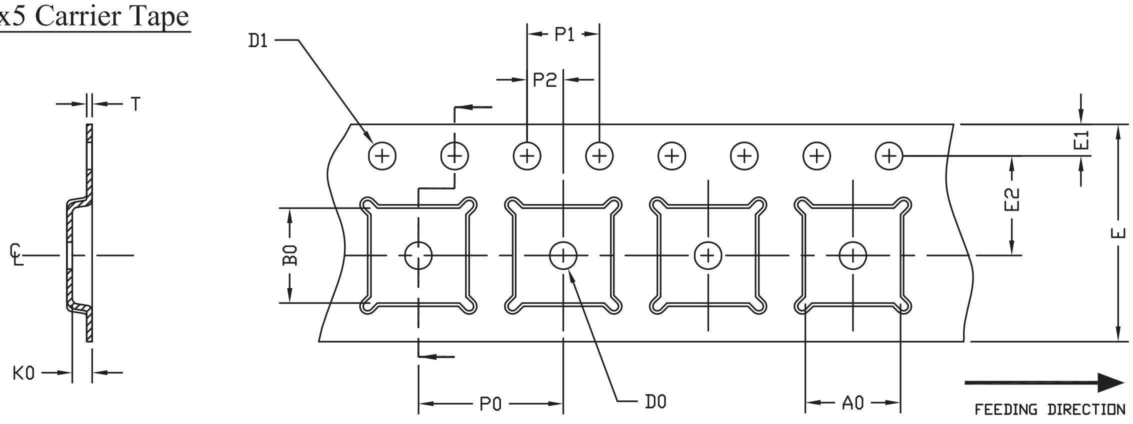


UNIT: mm

NOTE
CONTROLLING DIMENSION IS MILLIMETER.
CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

Tape and Reel Dimensions, QFN5x5-31L

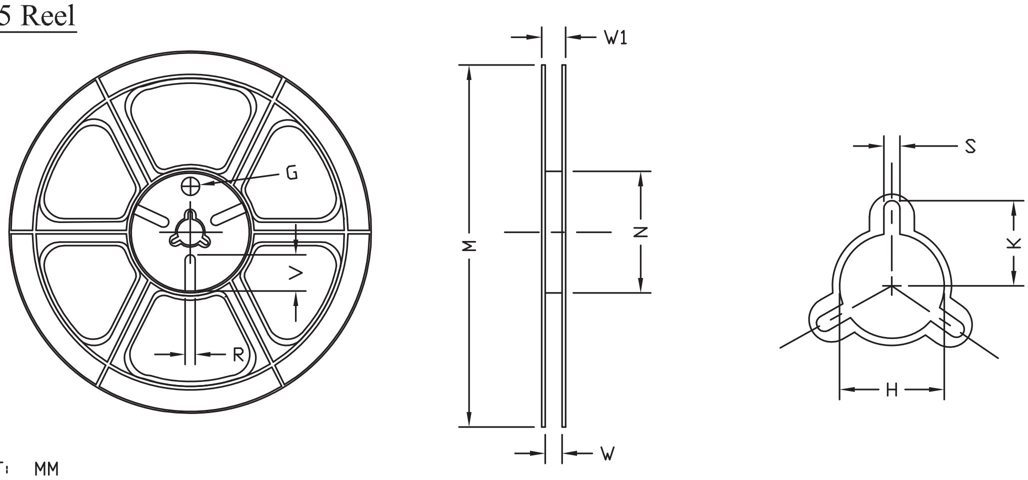
QFN5x5 Carrier Tape



UNIT: MM

PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
QFN5x5 (12 mm)	5.25 ±0.10	5.25 ±0.10	1.10 ±0.10	1.50 MIN.	1.50 $^{+0.1}_{-0.0}$	12.0 ±0.3	1.75 ±0.10	5.50 ±0.05	8.00 ±0.10	4.00 ±0.10	2.00 ±0.05	0.30 ±0.05

QFN5x5 Reel



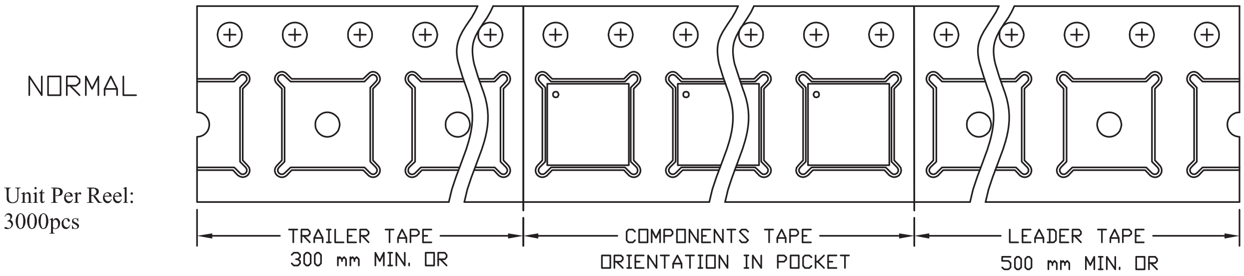
UNIT: MM

TAPE SIZE	REEL SIZE	M	N	W	W1	H	K	S	G	R	V
12 mm	ø330	ø330.0 ±2.0	ø100.0 ±1.0	12.4 $^{+2.0}_{-0.0}$	17.0 $^{+2.6}_{-1.2}$	ø13.0 ±0.5	10.5 ±0.2	2.0 ±0.5	---	---	---

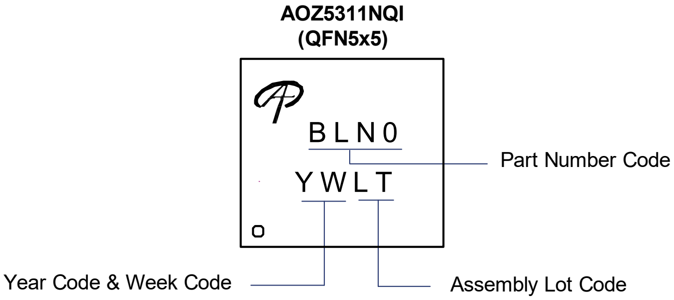
Tape and Reel Dimensions, QFN5x5-31L

QFN5x5 Tape

Leader / Trailer
& Orientation



Part Marking



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