AOZ5332QI

High-Current, High-Performance DrMos Power Module

General Description

The AOZ5332QI is a high efficiency synchronous buck power stage module consisting of two asymmetrical MOSFETs and an integrated driver. The MOSFETs are individually optimized for operation in the synchronous buck configuration. The High-Side MOSFET is optimized to achieve low capacitance and gate charge for fast switching with low duty cycle operation. The Low-Side MOSFET has ultra low ON resistance to minimize conduction loss.

The AOZ5332QI uses a PWM input for accurate control of the power MOSFETs switching activities, is compatible with 3V and 5V (CMOS) logic and supports Tri-State PWM.

A number of features are provided making the AOZ5332QI a highly versatile power module. The boot-strap diode is integrated in the driver. The Low-Side MOSFET can be driven into diode emulation mode to provide asynchronous operation and improve light-load performance. The pin-out is also optimized for low para-sitics, keeping their effects to a minimum.

Features

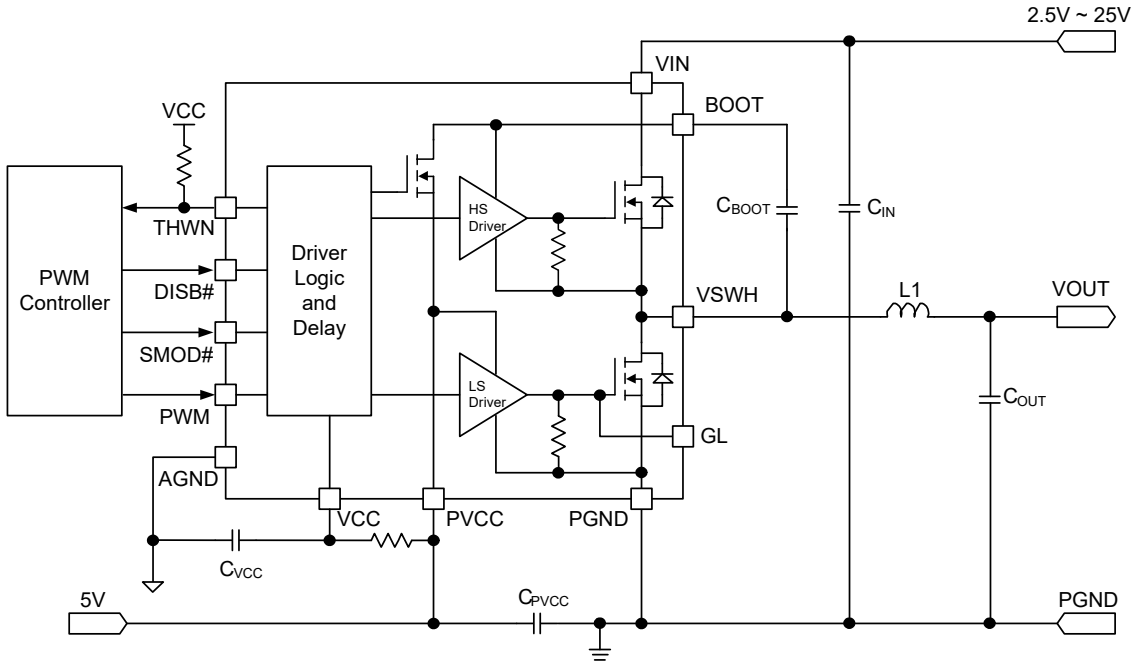
- 2.5V to 25V power supply range
- 4.5V to 5.5V driver supply range
- 50A continuous output current
  - Up to 80A with 10ms ON pulse
  - Up to 120A with 10us ON pulse
- Up to 2MHz switching operation
- 3V / 5V PWM / Tri-State input compatible
- Under-Voltage Lockout protection
- SMOD# control for Diode Emulation / CCM operation
- Low Profile 5x5 QFN-31L package

Applications

- Memory and graphic cards
- VRMs for motherboards
- Point of load DC/DC converters
- Video gaming console

Green Product

Typical Application

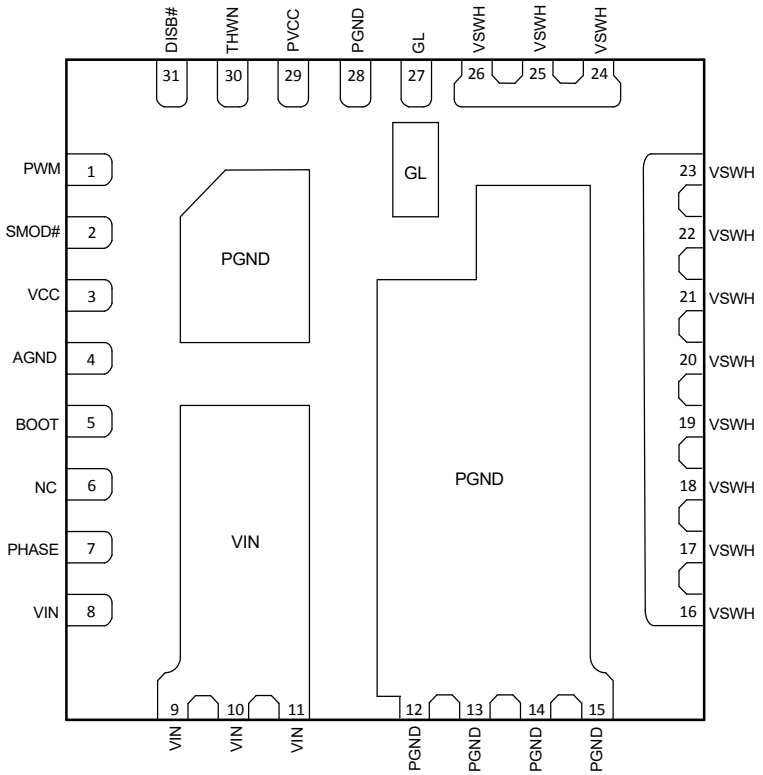


Ordering Information

Part Number	Ambient Temperature Range	Package	Environmental
AOZ5332QI	-40°C to +125°C	QFN5x5-31L	RoHS

All AOS products are offered in packages with Pb-free plating and compliant to RoHS standards. Please visit www.aosmd.com/media/AOSGreenPolicy.pdf for additional information.

Pin Configuration

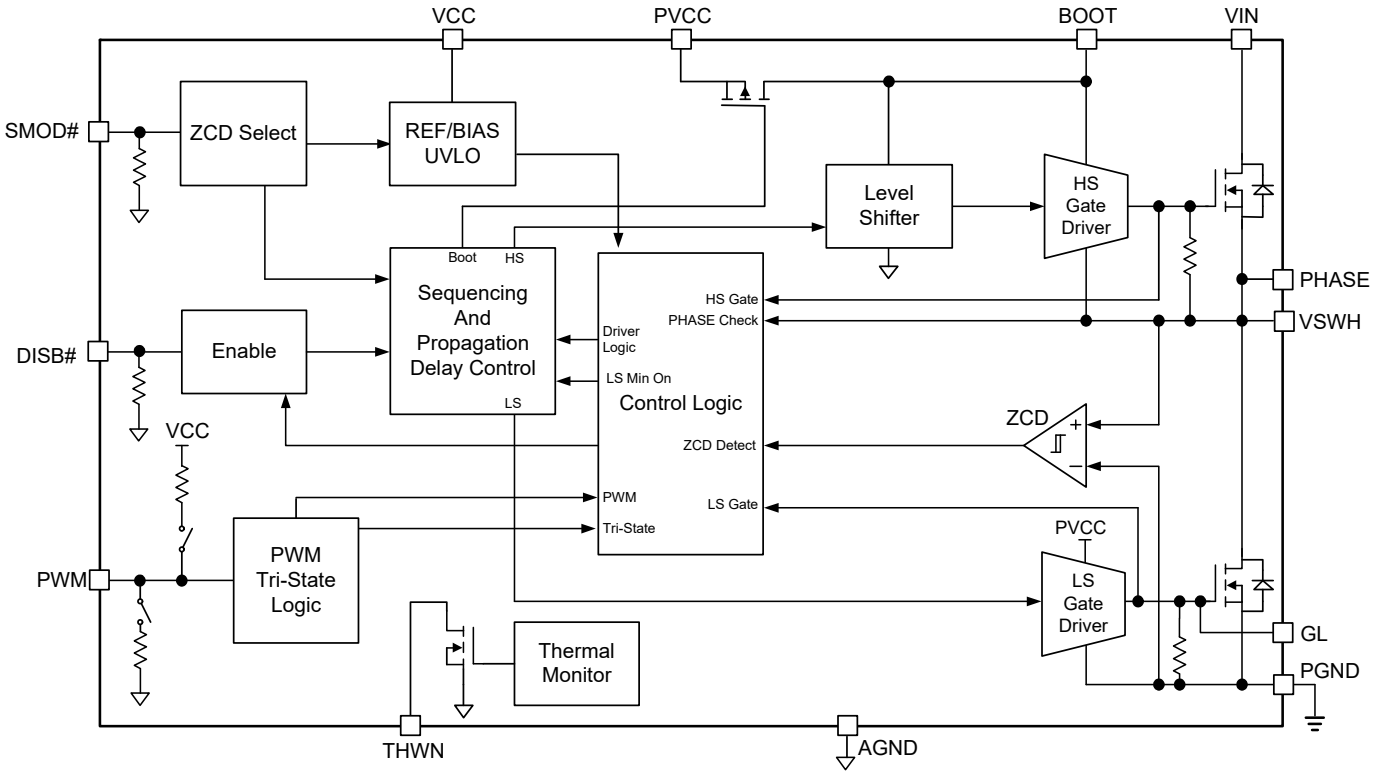


QFN5x5-31L
(Top View)

Pin Description

Pin Number	Pin Name	Pin Function
1	PWM	PWM input signal from the controller IC. When DISB#=0V, the internal resistor divider will be disconnected and this pin will be at high impedance.
2	SMOD#	Pull low to enable Discontinuous Mode of Operation (DCM), Diode Emulation or Skip Mode. There is an internal pull-down resistor to AGND.
3	VCC	5V Bias for Internal Logic Blocks. Ensure to position a 1µF MLCC directly between VCC and AGND (Pin 4).
4	AGND	Signal Ground.
5	BOOT	High-Side MOSFET Gate Driver supply rail. Connect a 100nF ceramic capacitor between BOOT and the PHASE (Pin 7).
6	NC	Internally connected to VIN paddle. It can be left floating (no connect) or tied to VIN.
7	PHASE	This pin is dedicated for bootstrap capacitor AC return path connection from BOOT (Pin 5).
8, 9, 10, 11	VIN	Power stage High Voltage Input (Drain connection of High-Side MOSFET).
12, 13, 14, 15	PGND	Power Ground pin for power stage (Source connection of Low-Side MOSFET).
16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26	VSWH	Switching node connected to the Source of High-Side MOSFET and the Drain of Low-Side MOSFET. These pins are used for Zero Cross Detection and Anti-Overlap Control as well as main inductor terminal.
27, 33	GL	Low-Side MOSFET Gate connection. This is for test purposes only.
28	PGND	Power Ground pin for High-Side and Low-Side MOSFET Gate Drivers. Ensure to connect 1µF directly between PGND and PVCC (Pin 29).
29	PVCC	5V Power Rail for High-Side and Low-Side MOSFET Drivers. Ensure to position a 1µF MLCC directly between PVCC and PGND (Pin 28).
30	THWN	Thermal warning indicator. This is an open−drain output. When the temperature at the driver IC die reaches the Over Temperature Threshold, this pin is pulled low.
31	DISB#	Output disable pin. When this pin is pulled to a logic low level, the IC is disabled. There is an internal pull−down resistor to AGND.

Functional Block Diagram



Absolute Maximum Ratings

Exceeding the Absolute Maximum Ratings may damage the device.

Parameter	Rating
Low Voltage Supply (VCC, PVCC)	-0.3V to 7V
High Voltage Supply (VIN)	-0.3V to 30V
Control Inputs (PWM, SMOD#, DISB#)	-0.3V to (VCC+0.3V)
Output (THWN)	-0.3V to (VCC+0.3V)
Bootstrap Voltage DC (BOOT-PGND)	-0.3V to 33V
Bootstrap Voltage Transient(1) (BOOT-PGND)	-8V to 40V
Bootstrap Voltage DC (BOOT-PHASE/VSWH)	-0.3V to 7V
BOOT Voltage Transient(1) (BOOT-PHASE/VSWH)	-0.3V to 9V
Switch Node Voltage DC (PHASE/VSWH)	-0.3V to 30V
Switch Node Voltage Transient(1) (PHASE/VSWH)	-8V to 38V
Low-Side Gate Voltage DC (GL)	(PGND-0.3V) to (PVCC+0.3V)
Low-Side Gate Voltage Transient(1) (GL)	(PGND-2.5V) to (PVCC+0.3V)
VSWH Current DC	50A
VSWH Current 10ms Pulse	80A
VSWH Current 10us Pulse	120A
Storage Temperature (T_S)	-65°C to +150°C
Max Junction Temperature (T_J)	150°C
ESD Rating(3)	2kV

Notes:

1. Peak voltages can be applied for 10ns per switching cycle.
2. Peak voltages can be applied for 20ns per switching cycle.
3. Devices are inherently ESD sensitive, handling precaution are required. Human body model rating: 1.5Ω in series with 100pF.

Recommended Operating Ratings

The device is not guaranteed to operate beyond the Maximum Operating Ratings.

Parameter	Rating
High Voltage Supply (VIN)	2.5V to 25V
Low Voltage / MOSFET Driver Supply VCC, PVCC	4.5V to 5.5V
Control Inputs (PWM, SMOD#, DISB#)	0V to VCC
Output (THWN)	0V to VCC
Operating Frequency	200kHz to 2MHz

Electrical Characteristics(4)

T_A = 25°C to 125°C. Typical values reflect 25°C ambient temperature; V_{IN} = 12V, VCC= PVCC= DISB# = 5.0V, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
General						
V_{IN}	Power Stage Power Supply		2.5		25	V
V_{CC}	Low Voltage Bias Supply	PVCC = VCC	4.5		5.5	V
$R_{\theta JC}$(4)	Thermal Resistance	PCB Temp = 100°C		2.5		°C/W
$R_{\theta JA}$(4)				13.8		°C/W
Input Supply and UVLO						
V_{CC_UVLO}	Under-Voltage Lockout	VCC Rising		3.5	3.9	V
V_{CC_HYST}		VCC Hysteresis		400		mV

Electrical Characteristics[4]

T_A = 25°C to 125°C. Typical values reflect 25°C ambient temperature; V_{IN} = 12V, VCC= PVCC= DISB# = 5.0V, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{VCC}	Control Circuit Bias Current	DISB# = 0V		1		μA
		SMOD# = 5V, PWM = 0V		550		
		SMOD# = 0V, PWM = 0V		535		
		SMOD# = 0V, PWM =1.65V		430		
I_{PVCC}	Drive Circuit Operating Current	PWM = 400kHz, 20% Duty Cycle		20		mA
		PWM = 1MHz, 20% Duty Cycle		50		mA
PWM Input						
V_{PWMH}	Logic High Input Voltage		2.7			V
V_{PWML}	Logic Low Input Voltage				0.72	V
I_{PWM_SRC}	PWM Pin Input Current	PWM = 0V		-150		μA
I_{PWM_SNK}		PWM = 3.3V		150		μA
V_{TRI}	PWM Tri-State Window		1.35		1.95	V
V_{PMW_FLOAT}	PWM Tri-State Voltage Clamp	PWM = Floating		1.65		V
DISB# Input						
$V_{DISB\#\_ON}$	Enable Input Voltage		2.0			V
$V_{DISB\#\_OFF}$	Disable Input Voltage				0.8	V
$R_{DISB\#}$	DISB# Input Resistance	Pull-Down Resistor		850		kΩ
SMOD# Input						
$V_{SMOD\#\_H}$	Logic High Input Voltage		2.0			V
$V_{SMOD\#\_L}$	Logic Low Input Voltage				0.8	V
$R_{SMOD\#}$	SMOD# Input Resistance	Pull-Down Resistor		850		kΩ
Gate Driver Timing						
t_{PDLU}	PWM to High-Side Gate	PWM: H → L, VSWH: H → L		30		ns
t_{PDLL}	PWM to Low-Side Gate	PWM: L → H, GL: H → L		25		ns
t_{PDHU}	Low-Side to High-Side Gate Deadtime	GL: H → L, GH[6]: L → H		15		ns
t_{PDHL}	High-Side Low-Side to Low-Side Gate Tri-State Deadtime	VSWH: H → 1V, GL: L → H		13		ns
t_{TSSHD}	Tri-State Shutdown Delay	PWM: L → V_{TRI}, GL: H → L and PWM: H → V_{TRI}, VSWH: H → L		25		ns
t_{TSEXIT}	Tri-State Propagation Delay	PWM: V_{TRI} → H, VSWH: L → H PWM: V_{TRI} → L, GL: L → H		35		ns
t_{LGMIN}	LS Minimum On Time	SMOD# = L		350		ns
Thermal Notification[5]						
t_{JTHWN}	Junction Thermal Threshold	Temperature Rising		150		°C
t_{JHYST}	Junction Thermal Hysteresis			30		°C
V_{THWN}	THWN Pin Output Low	I_{THWN} = 0.5mA		60		mV
R_{THWN}	THWN Pull-Down Resistance			120		Ω

Note:

4. All voltages are specified with respect to the corresponding AGND pin.
5. Characterization value. Not tested in production.
6. GH is an internal pin.

Table 1. Input Control Truth Table

DISB#	SMOD#	PWM	GH (Not a Pin)	GL
L	X	X	L	L
H	L	H	H	L
H	L	L	L	H, Forward I_L L, Reverse I_L
H	X	Tri-State	L	L
H	H	H	H	L
H	H	L	L	H

Timing Diagrams

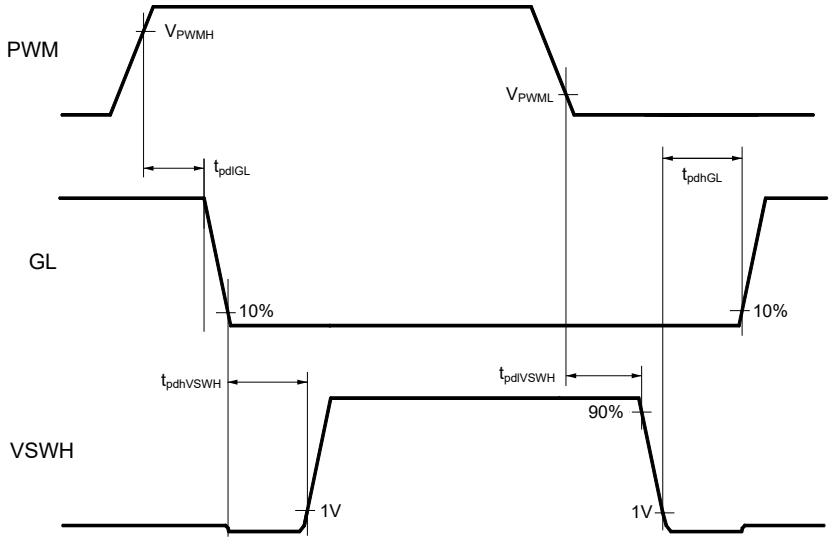


Figure 1. PWM Logic Input Timing Diagram

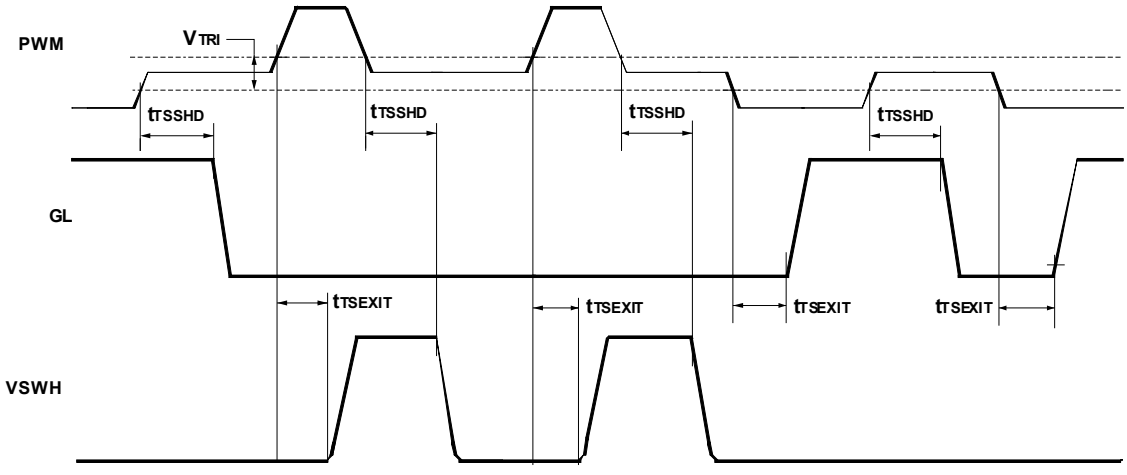


Figure 2. PWM Tri-State Hold Off and Exit Timing Diagram

Typical Characteristics

T_A = 25°C, V_{IN} = 12V, PVCC = VCC = 5V, unless otherwise specified.

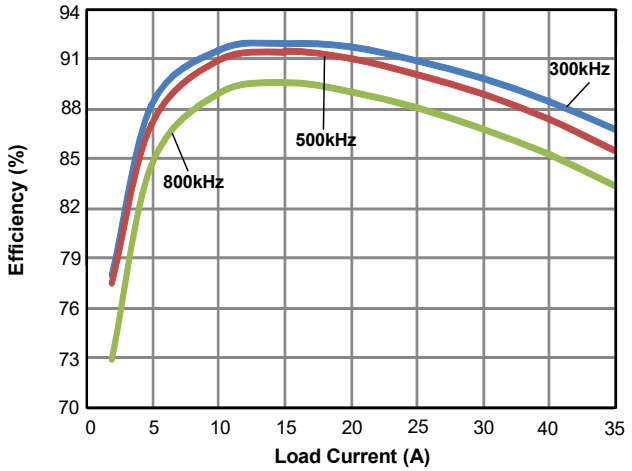


Figure 3. Efficiency vs Load Current

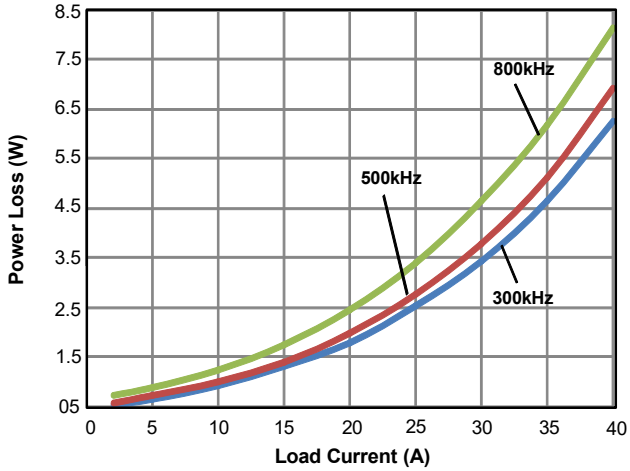


Figure 4. Power Loss vs Load Current

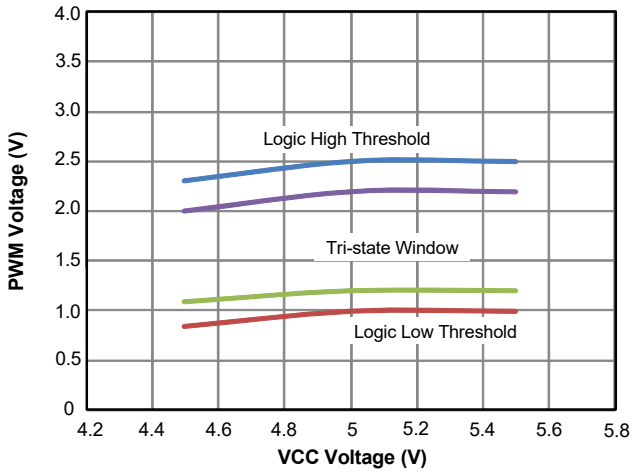


Figure 5. PWM Threshold Voltage vs VCC Voltage

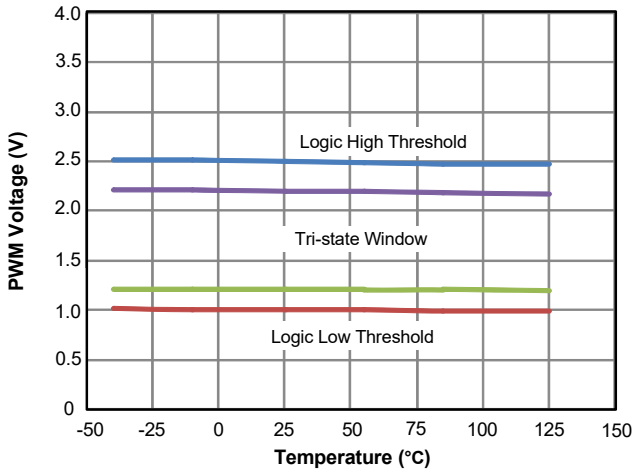


Figure 6. PWM Threshold Voltage vs Temperature

Typical Characteristics (continued)

T_A = 25°C, V_{IN} = 12V, PVCC = VCC = 5V, unless otherwise specified.

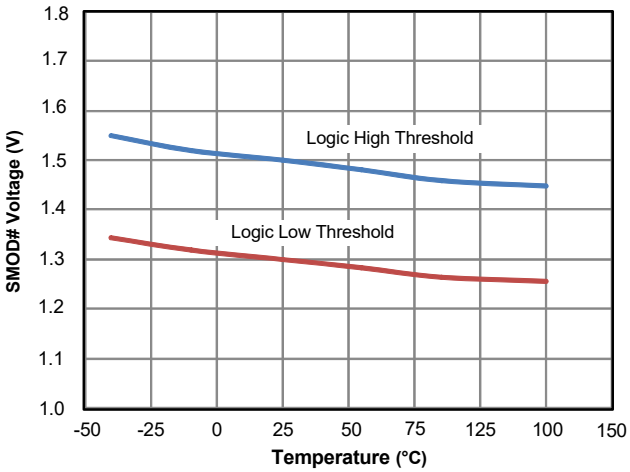


Figure 7. SMOD# Threshold Voltage vs Temperature

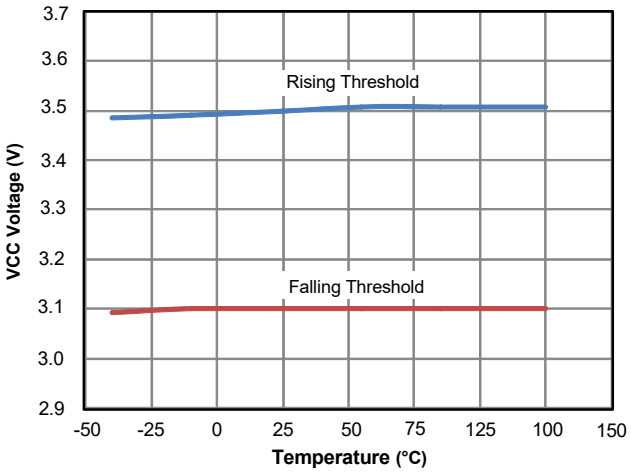


Figure 8. VCC UVLO Threshold Voltage vs Temperature

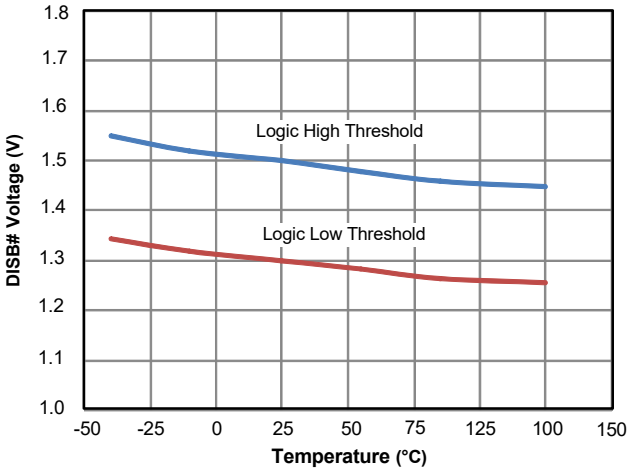


Figure 9. DISB# Threshold Voltage vs Temperature

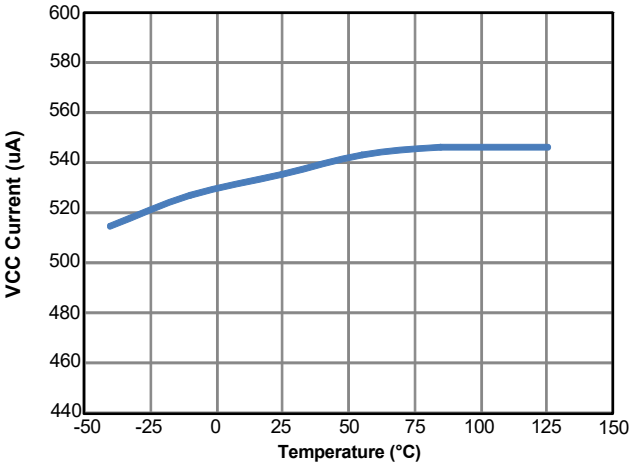


Figure 10. VCC Quiescent Current vs Temperature (SMOD# = 5V, PWM = 0V)

Application Information

AOZ5332QI is a fully integrated power module designed to work over an input voltage range of 2.5V to 25V with a separate 5V supply for gate drive and internal control circuitry. The MOSFETs are individually optimized for efficient operation on either High-Side or Low-Side switches in a low duty cycle synchronous buck converter. High current MOSFET Gate Drivers are also integrated, minimizing parasitic loop inductance resulting to optimum switching.

Powering the Module and the Gate Drives

An external supply PVCC = 5V is required for driving the MOSFETs. The MOSFETs are designed with optimally customized gate thresholds voltages, achieving the most advantageous compromise between fast switching speed and minimal power loss. The control logic supply VCC can be derived from the gate drive supply PVCC through an RC filter to bypass the switching noise. The gate driver is capable of supplying several amperes of peak current into the Low-Side MOSFET to achieve extremely fast switching. A ceramic bypass capacitor of 1μF or higher is recommended from PVCC to AGND.

The boost supply for driving the High-Side MOSFET is generated by connecting a small capacitor (100nF) between the BOOT pin and the PHASE node. It is recommended that this capacitor Cboot be connected as close as possible to the device across pins 5 and 7. The Bootstrap Diode is integrated into the package. Rboot is an optional resistor used by designers to slow down the turn on speed of the High-Side MOSFET. Typical values between 1Ω to 5Ω is a compromise between the need to keep both the switching time and VSWH node spikes as low as possible.

Under-voltage Lockout

The AOZ5332QI carries out normal operation when VCC rises above the UVLO exit threshold voltage. The under-voltage lockout is set at 3.5V nominally and exits the lockout when the VCC rises above this voltage threshold. Since the PWM control signals are provided typically from an external controller, extra care must be taken during start up.

Typical system operation begins with a soft start sequence to minimize in-rush current through the converter during start up. Powering the module with a full duty cycle PWM signal may lead to a number of undesirable consequences as explained below. AOZ5332QI provides UVLO and thermal monitor protection. The PWM controller should provides current monitoring and protection under all possible operating and transient conditions.

Disable (DISB#) Function

The AOZ5332QI provides enable and disable function through DISB# pin. In the low state, the DISB# pin shuts down the driver IC and disables both High-Side and Low-Side MOSFETs. In this state, standby current is minimized. A weak internal pull-down resistor is connected to AGND.

In the high state, the DISB# pin enables the driver IC, and the driver signal follows the external PWM signal.

Input Voltage VIN

AOZ5332QI is rated to operate over a wide input range of 2.5V to 25V. As with any other synchronous buck converter, large pulse currents at high frequency and extremely high di/dt rates will be drawn by the module during normal operation. It is strongly recommended to bypass the input supply (VIN) very close to the package leads with X7R or X5R quality surface mount ceramic capacitors.

The High-Side MOSFET is optimized for fast switching with low duty ratios made possible due to low gate charges (Q_G). When the module is operated at low VIN the duty cycle ratio will be higher and conduction losses in the High-Side MOSFET will also be correspondingly higher. The total power loss for the module may still be low but the High-Side MOSFET higher conduction losses may generate higher temperature. The two MOSFETs have their own exposed pads and PCB copper areas for heat dissipation. Hence, it is recommended that worst case junction temperature be measured for both High-Side MOSFET and Low-Side MOSFET to ensure they are operating within safe limits at high duty cycle ratio.

PWM Input

AOZ5332QI is compatible with 3V and 5V (CMOS) PWM logic. Refer to Figure 1 for PWM logic timing and propagation delays diagram between PWM input and the MOSFET gate drives.

The PWM input is also a Tri-State compatible input. When the PWM output of the Master Controller is in high impedance or not connected, both the gate driver outputs will turn off the MOSFETs. The PWM Input and Tri-State Thresholds table in Table 2 lists the thresholds levels for high and low level transitions as well as Tri-State window. As shown in Figure 2, there is a HOLDOFF delay between the corresponding PWM Tri-State signal and the output gate drivers being pulled low. This delay is typically 25ns and intended to prevent spurious triggering caused by Tri-State mode entrance.

Table 2. PWM Input and Tri-State Threshold

Threshold	V_{PWMH}	V_{PWML}	V_{TRIH}	V_{TRIL}
AOZ5332QI	2.7V	0.72V	1.35V	1.95V

Note: See Figure 2 for propagation delays and Tri-State window.

Diode Mode Emulation of Low-Side MOSFET (SMOD#)

AOZ5332QI can be operated in the diode emulation or pulse skipping mode using the SMOD# pin. This enables the converter to operate in asynchronous mode during start up, light load or under pre-bias conditions. If SMOD# is taken high, the controller will use the PWM signal and generate both the High and Low-Side complementary gate drive outputs with minimal anti-overlap delays necessary to avoid cross conduction. When the SMOD# pin is pulled low, the High-Side MOSFET drive is not affected but the module's diode emulation mode is activated for the Low-Side MOSFET. See Table 1 for all possible logic inputs and corresponding output drive conditions.

Gate Drives

AOZ5332QI has an internal high current high speed driver for both High-Side MOSFET and Low-Side MOSFET. Propagation delays between transitions of the PWM waveform and corresponding gate drives are kept to the minimum. AOZ5332QI has an internal adaptive logic to avoid shoot through and optimize dead time. The shoot through protection ensures that both High-Side and Low-Side MOSFETs are not turned ON at the same time.

1) PWM from logic Low to logic High

When the falling edge of GL goes below 1V, the blanking period is activated. After a pre-determined value (t_{PDHU}), the High-Side MOSFET is turned on. High-Side

2) PWM from logic High to logic Low

When the falling edge of VSWH voltage goes below 1V, the blanking period is activated. After a pre-determined value (t_{PDHL}), the low-side MOSFET is turned on.

Thermal Warning (THWN)

The module temperature is internally sensed and an alarm is asserted if it exceeds 150°C. The alarm is reset when the temperature cools down to 120°C. The THWN is an open drain pin that is pulled to AGND to indicate an over-temperature condition. It may be pulled up to VCC through a resistor for monitoring purposes. The AOZ5332QI device will not power down during the over temperature condition.

PCB Layout Guidelines

AOZ5332QI is a high current module rated for operation up to 2MHz. This requires fast switching speeds to keep the switching losses and device temperatures within limits. Having a robust gate driver integrated in the package eliminates driver-to-MOSFET gate pad parasitics of the package or PCB.

While excellent switching speeds can be achieved, correspondingly high levels of dv/dt and di/dt will be observed throughout the power train which requires careful attention to PCB layout to minimize voltage spikes and other transients. As with any synchronous buck converter layout, the critical requirement is to minimize the area of the primary switching current loop, formed by the VIN, VSWH and the input bypass capacitor C_{VIN}. The PCB design is somewhat simplified because of the optimized pin out in AOZ5332QI. The bulk of VIN and PGND pins are located adjacent to each other and the input capacitors should be placed as close as possible to these pins. The area of the secondary switching loop, formed by Low-Side MOSFET, output inductor and output capacitor Cout is the next critical parameter. This requires the second layer or “Inner 1” be the PGND plane. Via should be placed near input capacitors’ PGND pads.

While AOZ5332QI is optimally efficient, it can still dissipate high power which requires attention to thermal design. MOSFETs in the package are directly attached to individual exposed pads to simplify thermal management. Both VIN and VSWH pads should be attached to large areas of PCB copper. Thermal relief pads should be placed correspondingly to ensure proper heat dissipation to the board. An inner power plane layer dedicated to VIN, typically the High Voltage system input, is desirable and vias should be provided near the device to connect the VIN pads to the power plane. Significant amount of heat is dissipated through multiple PGND pins. A large copper area connected to the PGND pins in addition to the system ground plane through vias will further improve thermal dissipation.

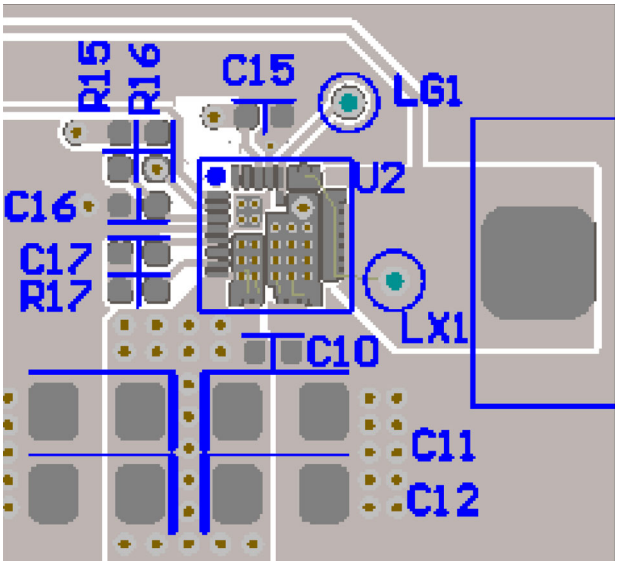


Figure 11. Top Layer of Demo Board, VIN, VSWH and PGND Copper Pads

As shown on Figure 11, the top most layer of the PCB should comprise of wide and exposed copper area for the primary AC current loop that runs along VIN pad originating from the input capacitors that are mounted to a large PGND pad. They serve as thermal relief as heat flows down to the VIN exposed pad that fan out to a wider area. Adding vias will only help transfer heat to cooler regions of the PCB board through the other layers beneath but serve no purpose to AC activity as all the AC current sees the lowest impedance on the top layer only.

As the primary and secondary (complimentary) AC current loops move through VIN to VSWH and through PGND to VSWH, large positive and negative voltage spike appear at the VSWH terminal which are caused by the large internal dI/dts produced by the in- package parastics. To minimize the effects of this interference, the VSWH terminal at which the main inductor L is mounted so the inductor can physically fit. The goal is to employ the least amount of copper area for this VSWH terminal just enough so the inductor can be securely mounted.

To minimize the effects of switching noise coupling to the rest of the sensitive areas of the PCB, the area directly underneath the designated VSWH pad or Inductor terminal is voided and the shape of this void is replicated descending down through the rest of the layers. Refer to Figure 12.

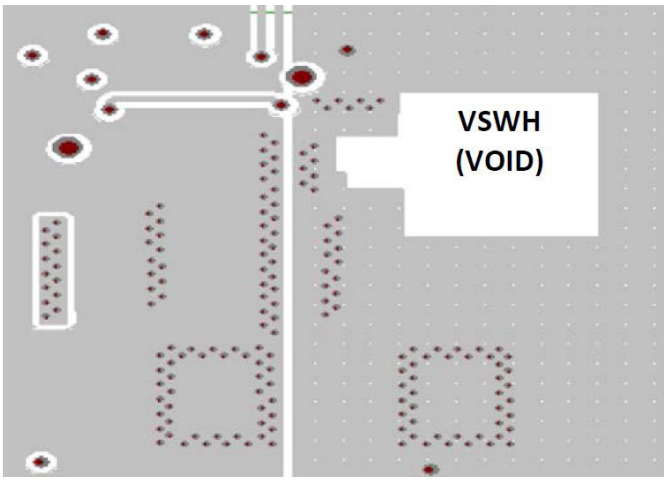


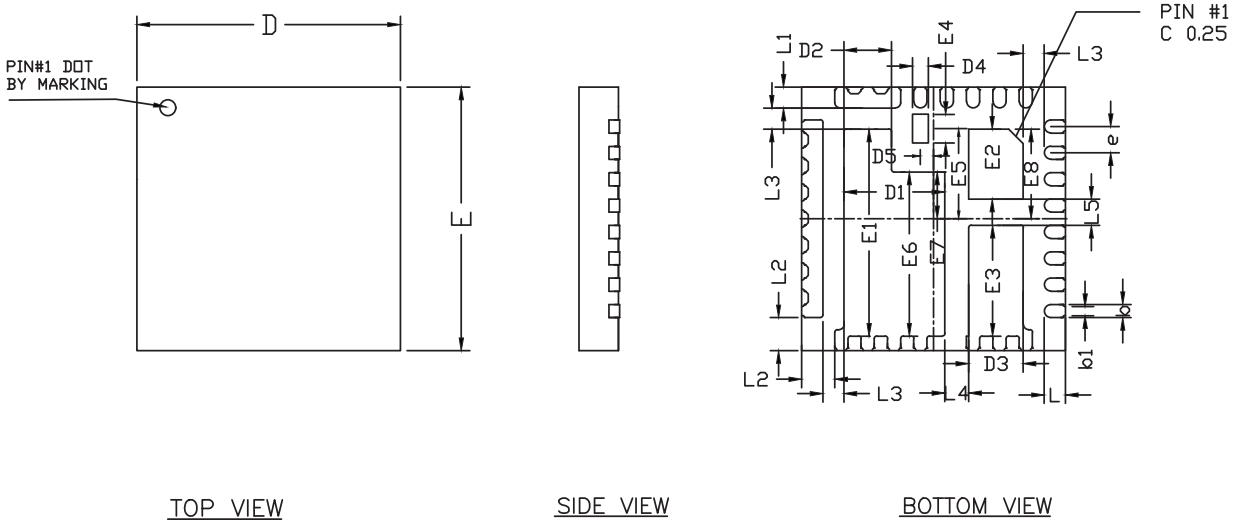
Figure 12. Bottom Layer of PCB

Positioning via through the landing pattern of the VIN and PGND thermal pads will help quickly facilitate the thermal build up and spread the heat much more quickly towards the surrounding copper layers descending from the top layer. (See RECOMMENDED LANDING PATTERN AND VIA PLACEMENT section).

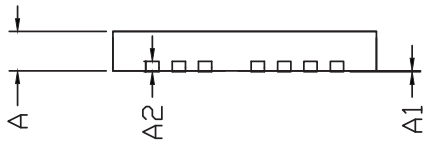
The exposed pads dimensional footprint of the 5x5 QFN package is shown on the package dimensions page. For optimal thermal relief, it is recommended to fill the PGND and VIN exposed landing pattern with 10mil diameter vias. 10mil diameter is a commonly used via diameter as it is optimally cost effective based on the tooling bit used in manufacturing. Each via is associated with a 20mil diameter keep out. Maintain a 5mil clearance (127um) around the inside edge of each exposed pad in an event of solder overflow, potentially shorting with the adjacent expose thermal pad.

The exposed pads dimensional footprint of the 5x5 QFN package is shown on the package dimensions page. For optimal thermal relief, it is recommended to fill the PGND and VIN exposed landing pattern with 10mil diameter vias. 10mil diameter is a commonly used via diameter as it is optimally cost effective based on the tooling bit used in manufacturing. Each via is associated with a 20mil diameter keep out. Maintain a 5mil clearance (127um) around the inside edge of each exposed pad in an event of solder overflow, potentially shorting with the adjacent expose thermal pad.

Package Dimensions, QFN5x5A-31L, EP3_S

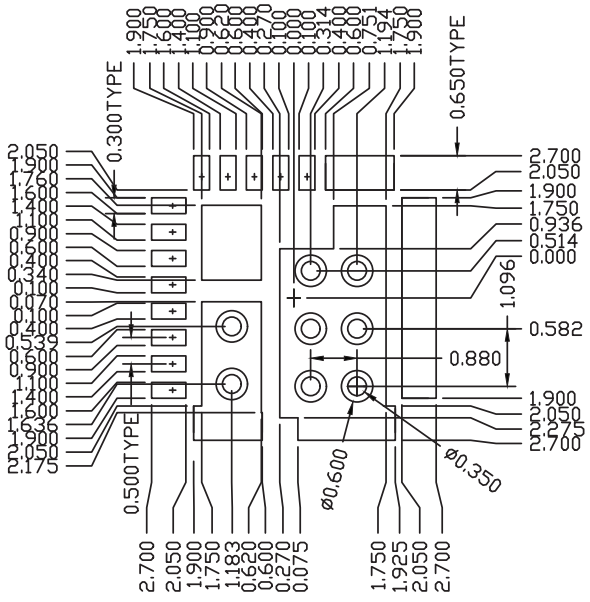


TOP VIEW SIDE VIEW BOTTOM VIEW



SIDE VIEW

RECOMMENDED LAND PATTERN

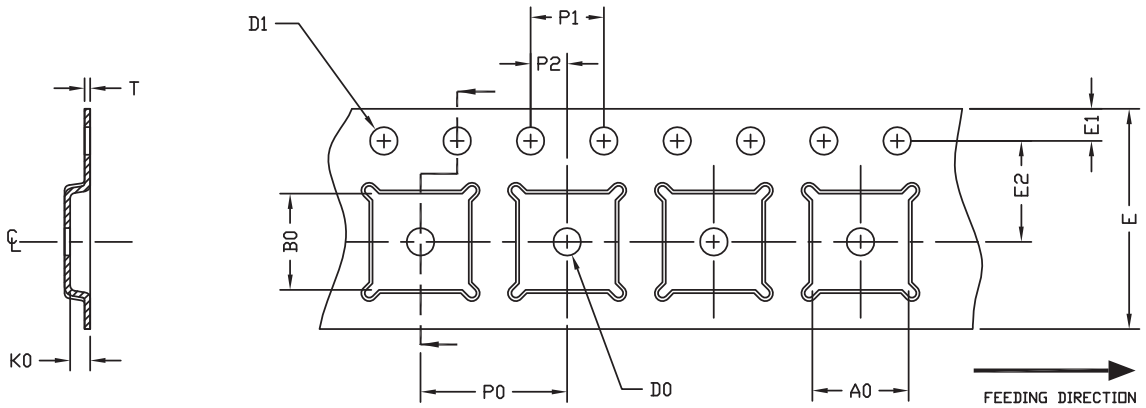


SYMBOLS	DIMENSION IN MM			DIMENSION IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.700	0.750	0.800	0.028	0.030	0.031
A1	0.000	-	0.050	0.000	-	0.002
A2		0.2REF			0.008REF	
D	4.900	5.000	5.100	0.193	0.197	0.201
E	4.900	5.000	5.100	0.193	0.197	0.201
D1	1.870	1.920	1.970	0.074	0.076	0.078
D2	0.850	0.900	0.950	0.033	0.035	0.037
D3	0.990	1.040	1.090	0.039	0.041	0.043
D4	0.250	0.300	0.350	0.010	0.012	0.014
D5	0.200	0.250	0.300	0.008	0.010	0.012
E1	3.875	3.925	3.975	0.153	0.155	0.156
E2	1.270	1.320	1.370	0.050	0.052	0.054
E3	2.050	2.100	2.150	0.081	0.083	0.085
E4	0.500	0.550	0.600	0.020	0.022	0.024
E5	1.661	1.711	1.761	0.065	0.067	0.069
E6	3.061	3.111	3.161	0.121	0.122	0.124
E7	0.836	0.886	0.936	0.033	0.035	0.037
E8	1.650	1.700	1.750	0.065	0.067	0.069
L	0.350	0.400	0.450	0.014	0.016	0.018
L1	0.350	0.400	0.450	0.014	0.016	0.018
L2	0.575	0.625	0.675	0.023	0.025	0.027
L3	0.350	0.400	0.450	0.014	0.016	0.018
L4	0.400	0.450	0.500	0.016	0.018	0.020
L5	0.450	0.500	0.550	0.018	0.020	0.022
b	0.200	0.250	0.300	0.008	0.010	0.012
b1	0.130	0.180	0.230	0.005	0.007	0.009
e		0.50BSC			0.02BSC	

UNIT: mm

Tape and Reel Drawing, QFN5x5A-31L, EP3_S

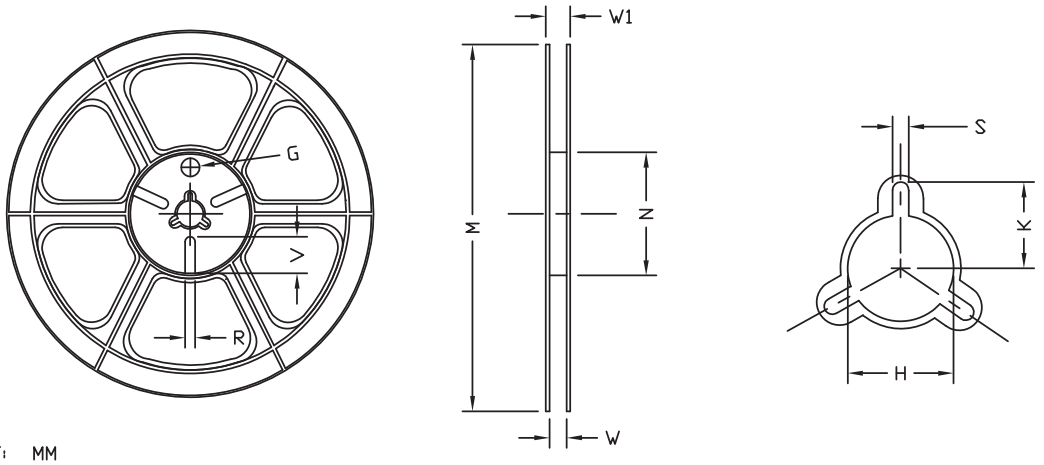
Carrier Tape



UNIT: MM

PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
QFN5x5 (12 mm)	5.25 ±0.10	5.25 ±0.10	1.10 ±0.10	1.50 MIN.	1.50 +0.1 −0.0	12.0 ±0.3	1.75 ±0.10	5.50 ±0.05	8.00 ±0.10	4.00 ±0.10	2.00 ±0.05	0.30 ±0.05

Reel

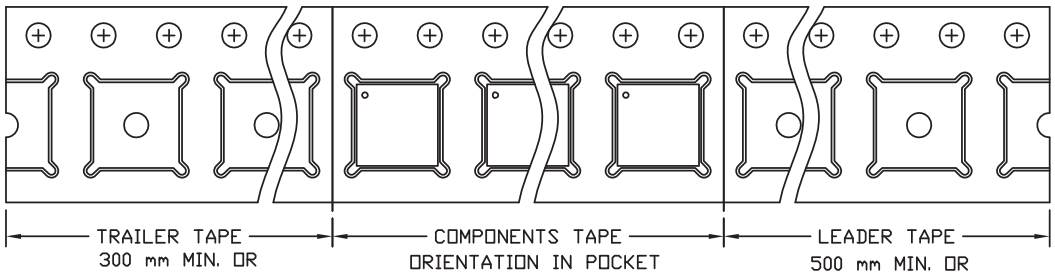


UNIT: MM

TAPE SIZE	REEL SIZE	M	N	W	W1	H	K	S	G	R	V
12 mm	Ø330	Ø330.0 ±2.0	Ø79.0 ±1.0	12.4 +2.0 −0.0	17.0 +2.6 −1.2	Ø13.0 ±0.5	10.5 ±0.2	2.0 ±0.5	---	---	---

Leader/Trailer & Orientation

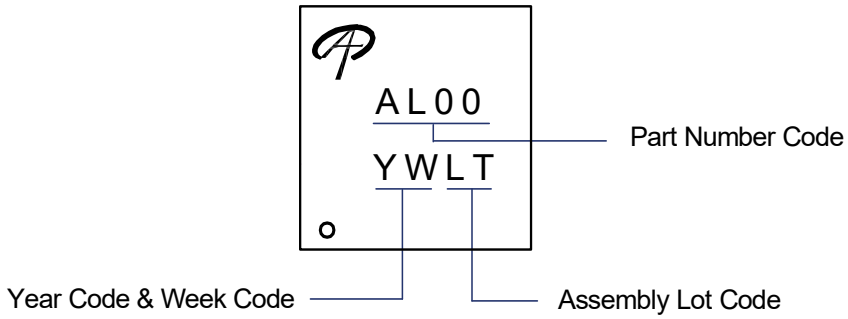
NORMAL



Unit Per Reel:
3000pcs

Part Marking

AOZ5332QI
(5mm x 5mm QFN)



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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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