AOZ5507QI

High-Current, High-Performance DrMOS Power Module

General Description

AOZ5507QI is a high efficiency synchronous buck power stage module consisting of two asymmetrical MOSFETs and an integrated driver. The MOSFETs are individually optimized for operation in the synchronous buck configuration. The High-Side MOSFET is optimized to achieve low capacitance and gate charge for fast switching with low duty cycle operation. The Low-Side MOSFET has ultra-low ON resistance to minimize conduction loss.

AOZ5507QI uses a PWM input for accurate control of the power MOSFETs switching activities, is compatible with 5V (CMOS) logic and supports Tri-State PWM.

A number of features are provided making the AOZ5507QI a highly versatile power module. The bootstrap switch is integrated in the driver. The Low-Side MOSFET can be driven into diode emulation mode to provide asynchronous operation and improve light-load performance. The pin-out is also optimized for low parasitics, keeping their effects to a minimum.

Features

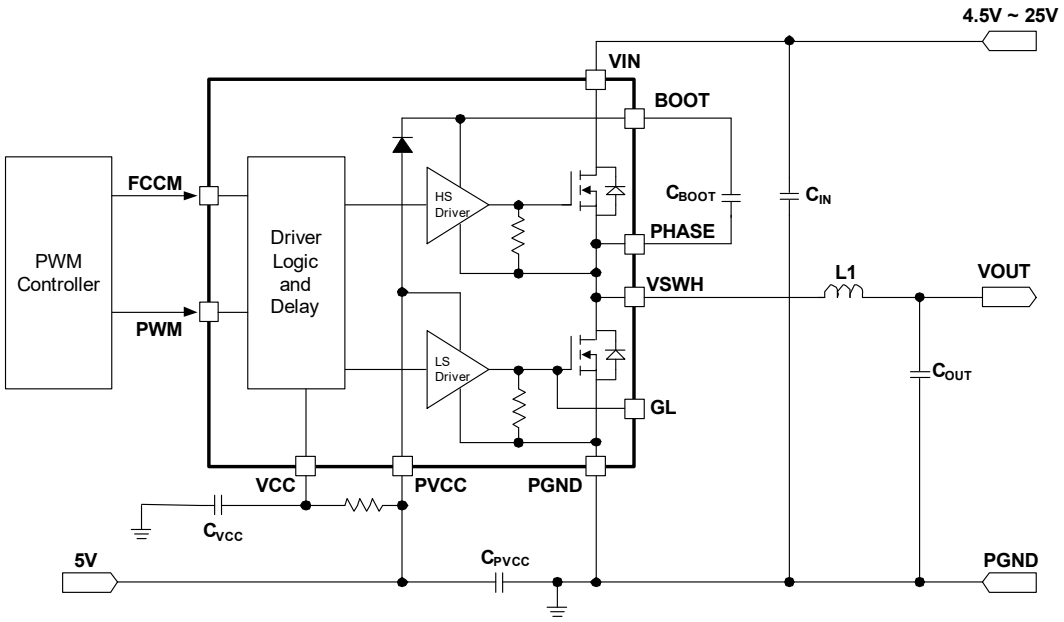
- 4.5V to 25V power supply range
- 4.5V to 5.5V driver supply range
- 30A continuous output current
  - Up to 50A with 10ms on pulse
  - Up to 80A with 10us on pulse
- Up to 2MHz switching operation
- 5V PWM / Tri-State input compatible
- Under-voltage Lockout protection
- FCCM control for Diode Emulation / CCM operation
- Low profile 3.5mm x 4.5mm QFN-22L package

Applications

- Memory and graphics cards
- VRMs for motherboards
- Point of load DC/DC converters
- Video gaming consoles

Green Product

Typical Application Circuit

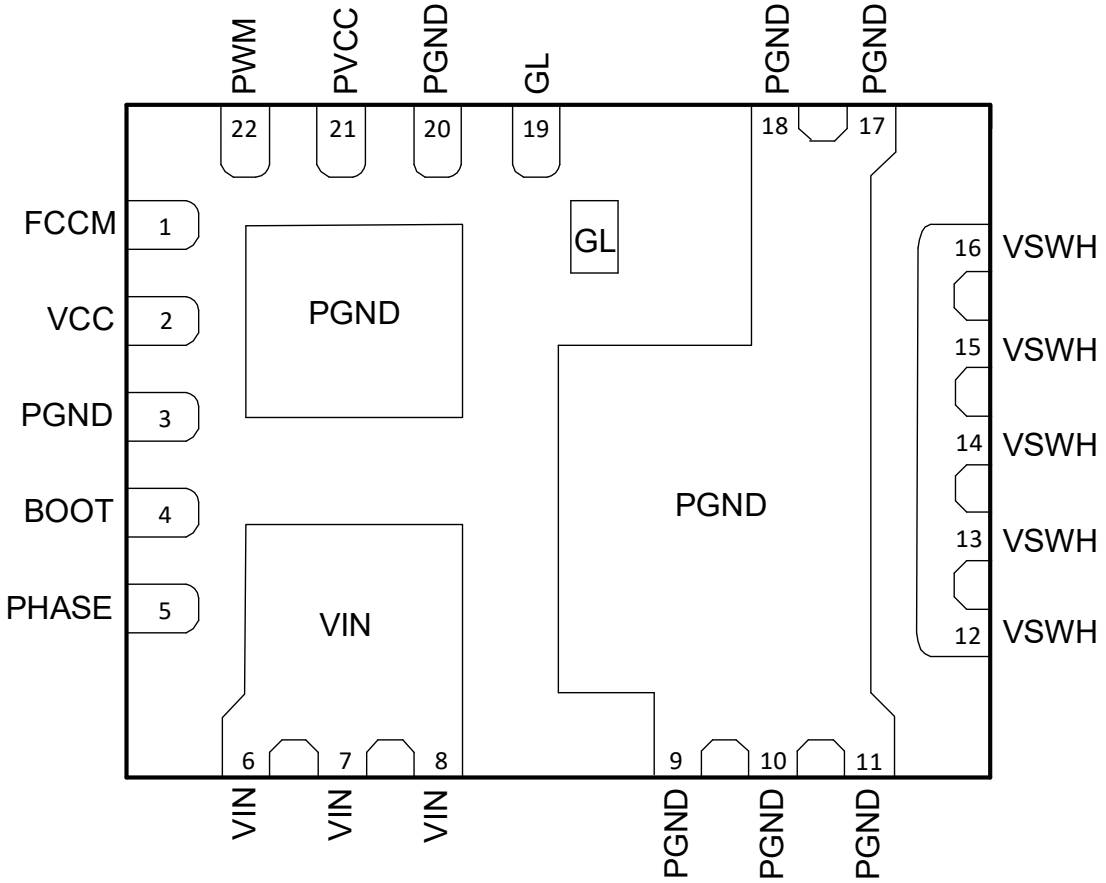


Ordering Information

Part Number	Junction Temperature Range	Package	Environmental
AOZ5507QI	-40°C to +150°C	QFN3.5x4.5-22L	RoHS

AOS Green Products use reduced levels of Halogens, and are also RoHS compliant.

Pin Configuration

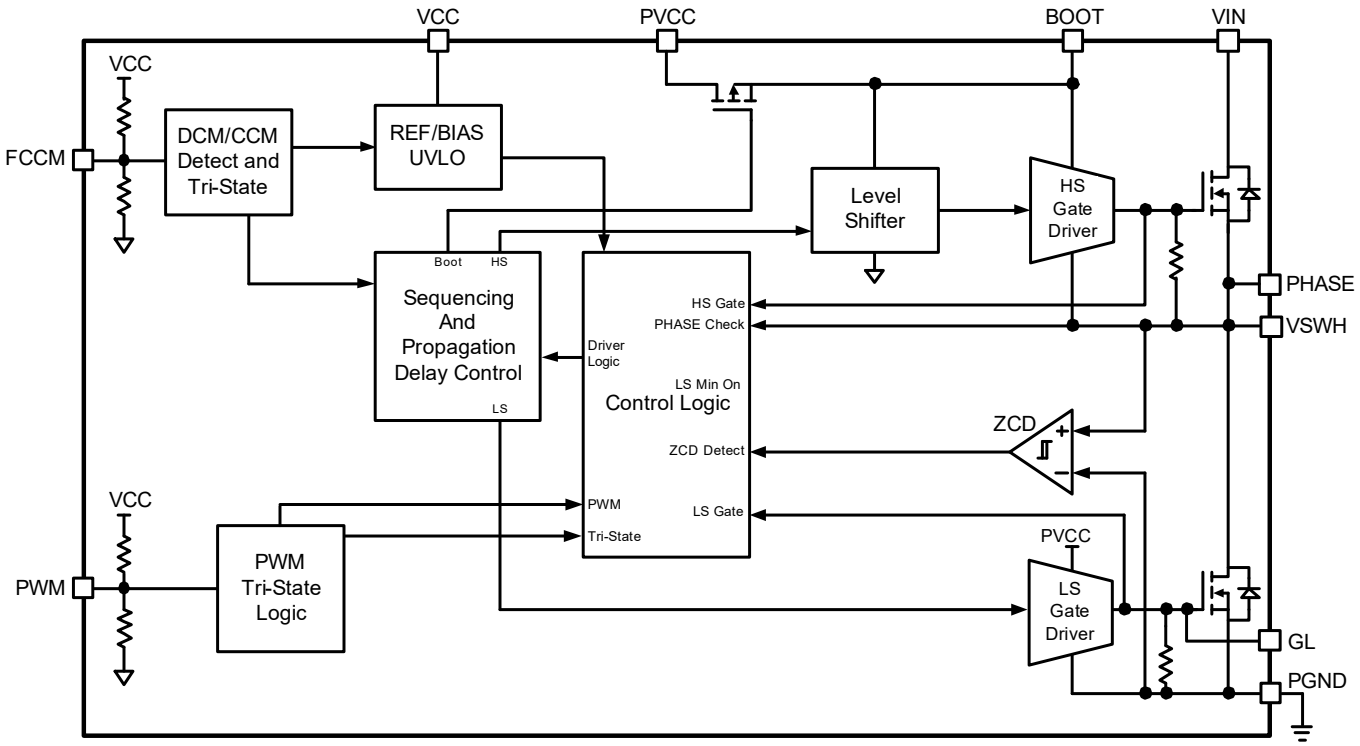


QFN3.5x4.5-22L
(Top View)

Pin Description

Pin Number	Pin Name	Pin Function
1	FCCM	Continuous conduction mode of operation is allowed when FCCM = High. Discontinuous mode is allowed and diode emulation mode is active when FCCM = Low. High impedance on the input of FCCM will shut down both High-Side and Low-Side MOSFETs.
2	VCC	5V Bias for Internal Logic Blocks. Ensure to position a 1µF MLCC directly between VCC and PGND (Pin 20).
3	PGND	Internally connected to PGND paddle. It can be left floating (no connect) or tied to PGND.
4	BOOT	High-Side MOSFET Gate Driver supply rail. Connect a 100nF ceramic capacitor between BOOT and the PHASE (Pin 5).
5	PHASE	This pin is dedicated for bootstrap capacitor AC return path connection from BOOT (Pin 4).
6,7,8	VIN	Power stage High Voltage Input (Drain connection of High-Side MOSFET).
9, 10, 11, 17, 18	PGND	Power Ground pin for power stage (Source connection of Low-Side MOSFET).
12, 13, 14, 15, 16	VSWH	Switching node connected to the Source of High-Side MOSFET and the Drain of Low-Side MOSFET. These pins are used for Zero Cross Detection and Anti-Overlap Control as well as main inductor terminal.
19	GL	Low-Side MOSFET Gate connection. This is for test purposes only.
20	PGND	Power Ground pin for High-Side and Low-Side MOSFET Gate Drivers. Ensure to connect 1µF directly between PGND and PVCC (Pin 21).
21	PVCC	5V Power Rail for High-Side and Low-Side MOSFET Drivers. Ensure to position a 1µF MLCC directly between PVCC and PGND (Pin 20).
22	PWM	PWM input signal from the controller IC. This input is compatible with 5V and Tri-State logic levels.

Functional Block Diagram



Absolute Maximum Ratings

Exceeding the Absolute Maximum ratings may damage the device.

Parameter	Rating
Low Voltage Supply (VCC, PVCC)	-0.3V to 7V
High Voltage Supply (VIN)	-0.3V to 30V
Control Inputs (PWM, FCCM)	-0.3V to (VCC+0.3V)
Bootstrap Voltage DC (BOOT-PGND)	-0.3V to 35V
Bootstrap Voltage Transient(1) (BOOT-PGND)	-8V to 40V
Bootstrap Voltage DC (BOOT-PHASE/VSWH)	-0.3V to 7V
BOOT Voltage Transient(1) (BOOT-PHASE/VSWH)	-0.3V to 9V
Switch Node Voltage DC (PHASE/VSWH)	-0.3V to 30V
Switch Node Voltage Transient(1) (PHASE/VSWH)	-8V to 38V
Low-Side Gate Voltage DC (GL)	(PGND-0.3V) to (PVCC+0.3V)
Low-Side Gate Voltage Transient(2) (GL)	(PGND-2.5V) to (PVCC+0.3V)
VSWH Current DC	30A
VSWH Current 10ms Pulse	50A
VSWH Current 10us Pulse	80A
Storage Temperature (T_S)	-65°C to +150°C
Max Junction Temperature (T_J)	150°C
ESD Rating(3)	2kV

Notes:

1. Peak voltages can be applied for 10ns per switching cycle.
2. Peak voltages can be applied for 20ns per switching cycle.
3. Devices are inherently ESD sensitive, handling precautions are required. Human body model rating: 1.5Ω in series with 100pF.

Recommended Operating Conditions

The device is not guaranteed to operate beyond the Maximum Recommended Operating Conditions.

Parameter	Rating
High Voltage Supply (VIN)	4.5V to 25V
Low Voltage / MOSFET Driver Supply (VCC, PVCC)	4.5V to 5.5V
Control Inputs (PWM, FCCM)	0V to VCC
Operating Frequency	200kHz to 2MHz

Electrical Characteristics[4]

T_J = 0°C to 150°C, VIN = 12V, VOUT = 1V, PVCC = VCC = 5V, unless otherwise specified. Min/Max values are guaranteed by test, design or statistical correlation.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
GENERAL						
V_{IN}	Power Stage Power Supply		4.5		25	V
V_{CC}	Low Voltage Bias Supply	PVCC = VCC	4.5		5.5	V
$R_{\theta JC}$[5]	Thermal Resistance	PCB Temp = 100°C		2.5		°C / W
$R_{\theta JA}$[5]				18.5		°C / W
INPUT SUPPLY AND UVLO						
V_{CC_UVLO}	Under-voltage LockOut	VCC Rising		3.5	3.9	V
V_{CC_HYST}		VCC Hysteresis		400		mV
I_{VCC}	Control Circuit Bias Current	FCCM = Floating, PWM = Floating		3	5	µA
		FCCM = 5V, PWM = Floating		170		
		FCCM = 0V, PWM = Floating		180		
PWM INPUT						
V_{PWMH}	Logic High Input Voltage		4.2			V
V_{PWML}	Logic Low Input Voltage				0.72	V
I_{PWM_SRC}	PWM Pin Input Current	PWM = 0V		-200		µA
I_{PWM_SNK}		PWM = 5V		200		µA
V_{TRI}	PWM Tri-State Window		1.6		3.4	V
FCCM INPUT						
V_{FCCM_H}	Logic High Input Voltage		3.9			V
V_{FCCM_L}	Logic Low Input Voltage				1.1	V
I_{FCCM}	FCCM Pin Input Current	FCCM = 0V		50		µA
		FCCM = 5V		-50		µA
V_{TRI}	FCCM Tri-State Window		2.0		3.0	V
t_{PS4_EXIT}	PS4 Exit Latency			5	15	µs
GATE DRIVER TIMINGS						
t_{PDLU}	PWM to HS Gate	PWM: H → L, VSWH: H → L		30		ns
t_{PDLL}	PWM to LS Gate	PWM: L → H, GL: H → L		25		ns
t_{PDHU}	LS to HS Gate Deadtime	GL: H → L, VSWH: L → H		15		ns
t_{PDHL}	HS to LS Gate Deadtime	VSWH: H → 1V, GL: L → H		13		ns
t_{TSSHD}	Tri-State Shutdown Delay	PWM: L → V_{TRI}, GL: H → L and PWM: H → V_{TRI}, VSWH: H → L		150		ns
t_{TSEXIT}	Tri-State Propagation Delay	PWM: V_{TRI} → H, VSWH: L → H PWM: V_{TRI} → L, GL: L → H		45		ns
t_{LGMIN}	LS Minimum On Time	FCCM = 0V (DCM Mode)		350		ns

Notes:

4. All voltages are specified with respect to the corresponding AGND pin.
5. Characterization value. Not tested in production.

Timing Diagrams

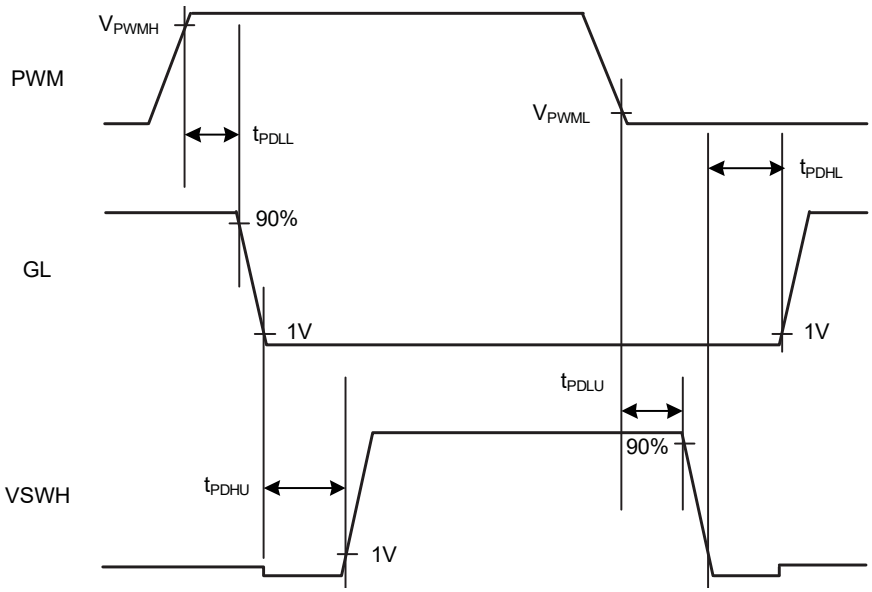


Figure 1. PWM Logic Input Timing Diagram

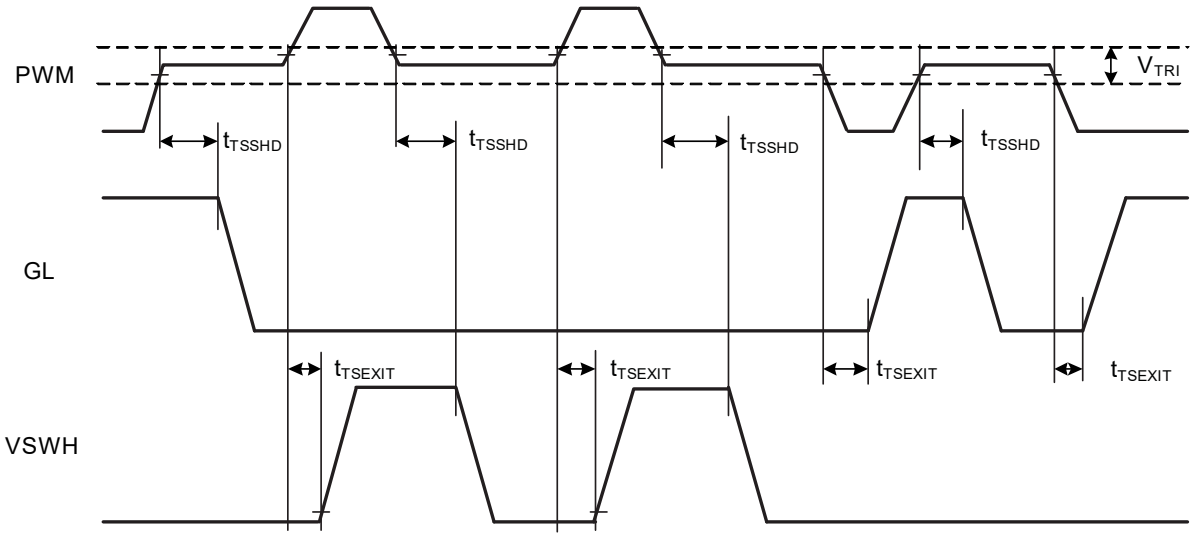


Figure 2. PWM Tri-State Holdoff and Exit Timing Diagram

Typical Performance Characteristics

T_A = 25°C, VIN = 12V, VOUT = 1V, PVCC = VCC = 5V, unless otherwise specified.

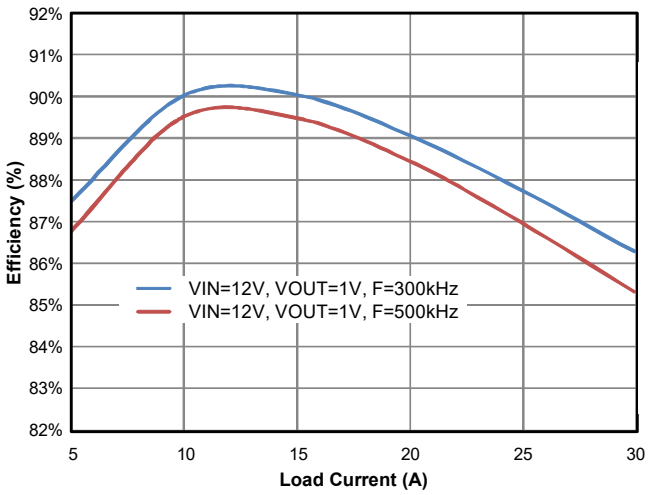


Figure 3. Efficiency vs. Load Current

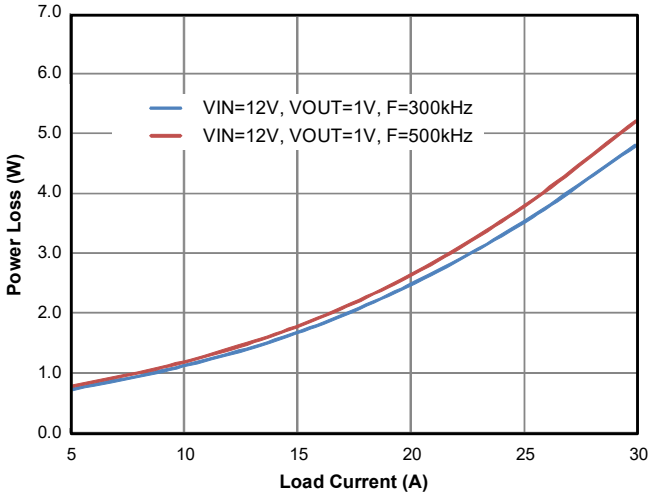


Figure 4. Power Loss vs. Load Current

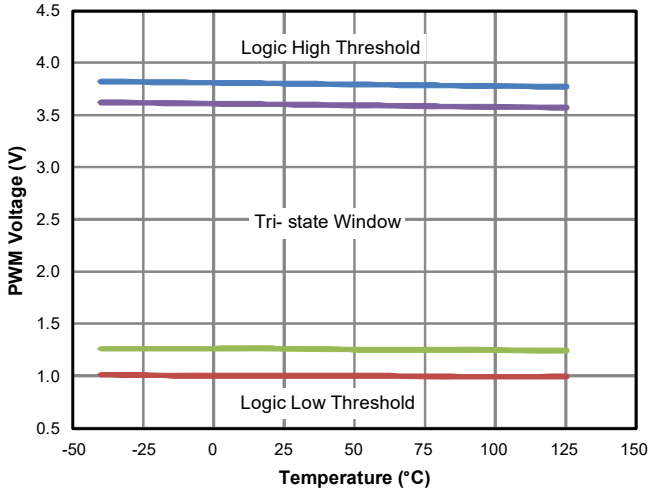


Figure 5. PWM Threshold vs. Temperature

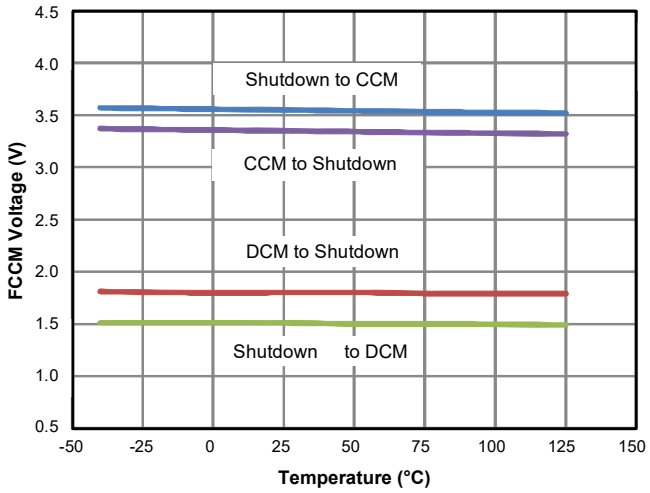


Figure 6. FCCM Threshold vs. Temperature

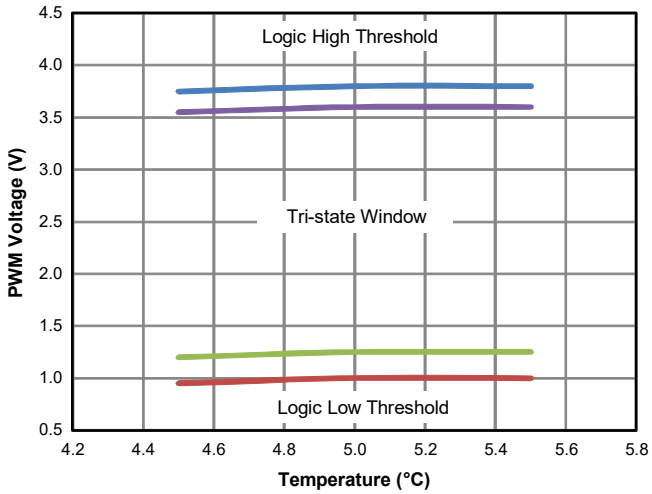


Figure 7. PWM Threshold vs. VCC Voltage

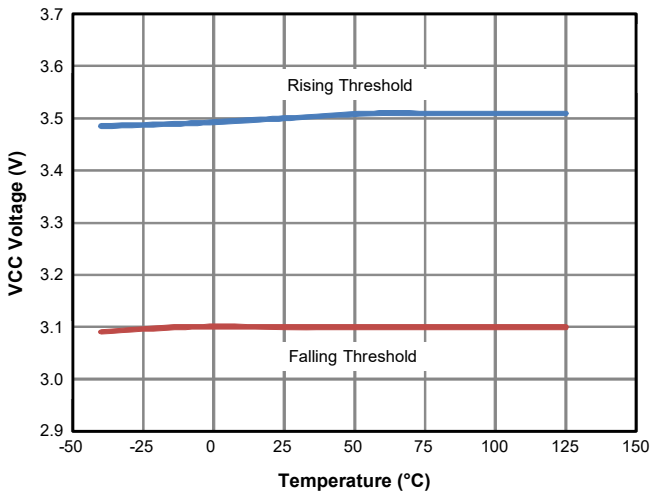


Figure 8. UVLO (VCC) Threshold vs. Temperature

Typical Performance Characteristics

T_A = 25°C, VIN = 12V, VOUT = 1V, PVCC = VCC = 5V, unless otherwise specified.

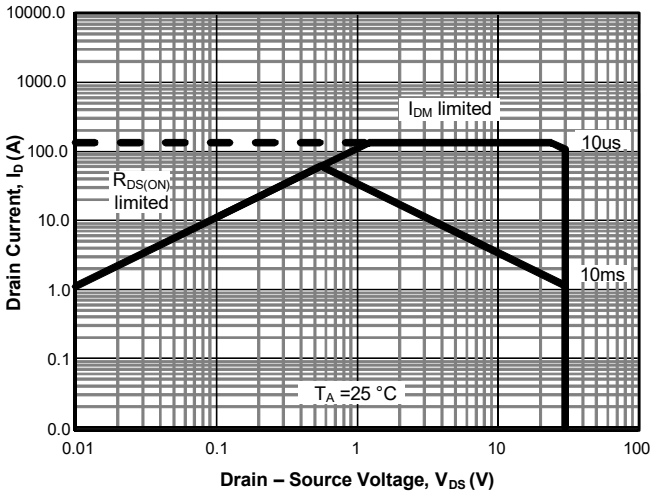


Figure 9. High-Side MOSFET SOA

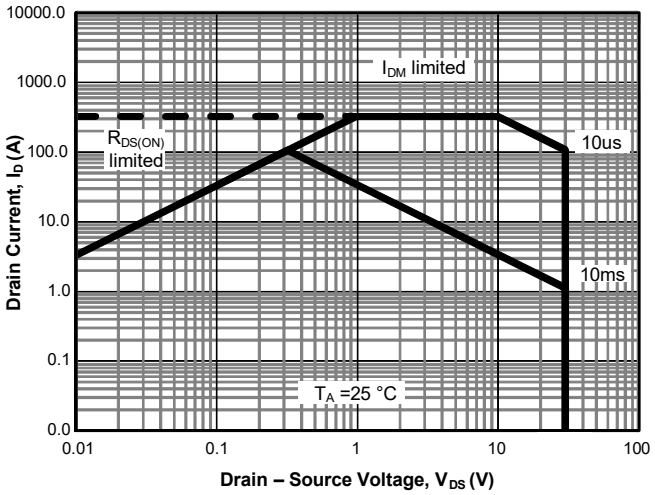


Figure 10. Low-Side MOSFET SOA

Application Information

AOZ5507QI is a fully integrated power module designed to work over an input voltage range of 4.5V to 25V with a separate 5V supply for gate drive and internal control circuitry. The MOSFETs are individually optimized for efficient operation on both High-Side and Low-Side for a low duty cycle synchronous buck converter. High current MOSFET Gate Drivers are integrated in the package to minimize parasitic loop inductance for optimum switching efficiency.

Powering the Module and the Gate Drives

An external supply PVCC = 5V is required for driving the MOSFETs. The MOSFETs are designed with optimally customized gate thresholds voltages to achieve the most advantageous compromise between fast switching speed and minimal power loss. The integrated gate driver is capable of supplying large peak current into the Low-Side MOSFET to achieve fast switching. A ceramic bypass capacitor of 1μF or higher is recommended from PVCC (Pin 21) to PGND (Pin 20). The control logic supply VCC (Pin 2) can be derived from the gate drive supply PVCC (Pin 21) through an RC filter to bypass the switching noise (See Typical Application Circuit).

The boost supply for driving the High-Side MOSFET is generated by connecting a small capacitor (100nF) between the BOOT (Pin 4) and the switching node PHASE (Pin 5). It is recommended that this capacitor C_{BOOT} should be connected to the device across Pin 4 and Pin 5 as close as possible. A bootstrap diode is integrated into the device to reduce external component count. An optional resistor R_{BOOT} in series with C_{BOOT} between 1Ω to 5Ω can be used to slow down the turn on speed of the High-Side MOSFET to achieve both short switching time and low VSWH switching node spikes at the same time.

Under-voltage LockOut

AOZ5507QI starts up to normal operation when VCC rises above the Under-Voltage LockOut (UVLO) threshold voltage. The UVLO release is set at 3.5V typically. Since the PWM control signal is provided from an external controller or a digital processor, extra caution must be taken during start up. AOZ5507QI must be powered up before PWM input is applied.

Normal system operation begins with a soft start sequence by the controller to minimize in-rush current during start up. Powering the module with a full duty cycle PWM signal may lead to many undesirable consequences due to excessive power. AOZ5507QI provides some protections such as UVLO and thermal monitor. For system level protection, the PWM controller should monitor the current output and protect the load under all possible operating and transient conditions.

Input Voltage VIN

AOZ5507QI is rated to operate over a wide input range from 4.5V to 25V. For high current synchronous buck converter applications, large pulse current at high frequency and high current slew rates (di/dt) will be drawn by the module during normal operation. It is strongly recommended to place a bypass capacitor very close to the package leads at the input supply (VIN). Both X7R or X5R quality surface mount ceramic capacitors are suitable.

The High-Side MOSFET is optimized for fast switching by using a low gate charge (Q_G) device. When the module is operated at high duty cycle ratio, conduction loss from the High-Side MOSFET will be higher. The total power loss for the module is still relatively low but the High-Side MOSFET higher conduction loss may have higher temperature. The two MOSFETs have their own exposed pads and PCB copper areas for heat dissipation. It is recommended that worst case junction temperature be measured for both High-Side MOSFET and Low-Side MOSFET to ensure that they are operating within Safe Operating Area (SOA).

PWM Input

AOZ5507QI is compatible with 5V (CMOS) PWM logic. Refer to Figure 1 for PWM logic timing and propagation delays diagram between PWM input and the MOSFET gate drives. AOZ5507QI is compatible with 5V (CMOS) PWM logic. Refer to Figure 1 for PWM logic timing and propagation delays diagram between PWM input and the MOSFET gate drives.

The PWM is also compatible with Tri-State input. When the PWM output from the external PWM controller is in high impedance or not connected both High-Side and Low-Side MOSFETs are turned off and VSWH is in high impedance state. Table 1 shows the thresholds level for high-to-low and low-to-high transitions as well as Tri-State window.

There is a Holdoff Delay between the corresponding PWM Tri-State signal and the MOSFET gate drivers to prevent spurious triggering of Tri-State mode which may be caused by noise or PWM signal glitches. The Holdoff Delay is typically 175ns.

Table 1. PWM Input and Tri-State Thresholds

Thresholds →	V_{PWMH}	V_{PWML}	V_{TRIH}	V_{TRIL}
AOZ5507QI	4.20V	0.72V	1.60V	3.40V

Note: See Figure 2 for propagation delays and Tri-State window.

Diode Mode Emulation of Low-Side MOSFET (FCCM)

AOZ5507QI can be operated in the diode emulation or pulse skipping mode using FCCM (Pin 1). This enables the converter to operate in asynchronous mode during start up, light load or under pre-bias conditions.

When FCCM is high, the module will operate in Continuous Conduction Mode (CCM). The Driver logic will use the PWM signal and generate both the High-Side and Low-Side complementary gate drive outputs with minimal anti-overlap delays to avoid cross conduction.

When FCCM is low, the module can operate in Discontinuous Conduction Mode (DCM). The High-Side MOSFET gate drive output is not affected but Low-Side MOSFET will enter diode emulation mode. See Table 2 for the truth table for PWM and FCCM inputs.

Table 2. Control Logic Truth Table

FCCM	PWM	GH	GL
L	L	L	H if I_L > 0A L if I_L < 0A
L	H	H	L
H	L	L	H
H	H	H	L
L	Tri-State	L	L
H	Tri-State	L	L
Tri-State	X	L	L

Note: Diode Emulation mode is activated when FCCM pin is Low.

Gate Drives

AOZ5516QI has an internal high current high speed driver that generates the floating gate driver for the High-Side MOSFET and a complementary driver for the Low-Side MOSFET. An internal shoot-through protection scheme is implemented to ensure that both MOSFETs cannot be turned on at the same time. The operation of PWM signal transition is illustrated as below.

1) PWM from logic Low to logic High

When the falling edge of Low-Side Gate Driver output GL goes below 1V, the blanking period is activated. After a pre-determined value (t_{PDHU}), the complementary High-Side Gate Driver output GH is turned on.

2) PWM from logic High to logic Low

When the falling edge of switching node VSWH goes below 1V, the blanking period is activated. After a pre-determined value (t_{PDHL}), the complementary Low-Side Gate Driver output GL is turned on.

This mechanism prevents cross conduction across the input bus line VIN and PGND. The anti-overlap circuit monitors the switching node VSWH to ensure a smooth transition between the two MOSFETs under any load transient conditions.

PCB Layout Guidelines

AOZ5507QI is a high current module rated for operation up to 2MHz. This requires high switching speed to keep the switching losses and device temperatures within limits. An integrated gate driver within the package eliminates driver-to-MOSFET gate pad parasitic of the package or on PCB.

To achieve high switching speeds, high levels of slew rate (dv/dt and di/dt) will be present throughout the power train which requires careful attention to PCB layout to minimize voltage spikes and other transients. As with any synchronous buck converter layout, the critical requirement is to minimize the path of the primary switching current loop formed by the High-Side MOSFET, Low-Side MOSFET, and the input bypass capacitor C_{IN}. The PCB design is greatly simplified by the optimization of the AOZ5507QI pin out. The power inputs of VIN and PGND are located adjacent to each other and the input bypass capacitors C_{IN} should be placed as close as possible to these pins. The area of the secondary switching loop is formed by Low-Side MOSFET, output inductor L1, and output capacitor C_{OUT} is the next critical requirement. This requires second layer or “Inner 1” to be the PGND plane. VIAs should then be placed near PGND pads.

While AOZ5507QI is a highly efficient module, it still dissipates a significant amount of heat under high power conditions. Special attention is required for thermal design. MOSFETs in the package are directly attached to individual exposed pads (VIN and PGND) to simplify thermal management. Both VIN and VSWH pads should be attached to large areas of PCB copper. Thermal relief pads should be placed to ensure proper heat dissipation to the board. An inner power plane layer dedicated to VIN, typically the high voltage system input, is desirable and VIAs should be provided near the device to connect the VIN pads to the power plane. Significant amount of heat can also be dissipated through multiple PGND pins. A large copper area connected to the PGND pins in addition to the system ground plane through VIAs will further improve thermal dissipation.

As shown on Figure. 11, the top most layer of the PCB should comprise of wide and exposed copper area for the primary AC current loop which runs along VIN pad originating from the input capacitors C10, C11, and C12 that are mounted to a large PGND pad. They serve as thermal relief as heat flows down to the VIN exposed pad that fans out to a wider area. Adding VIAs will only help transfer heat to cooler regions of the PCB board through the other layers beneath but serve no purpose to AC activity as all the AC current sees the lowest impedance on the top layer only.

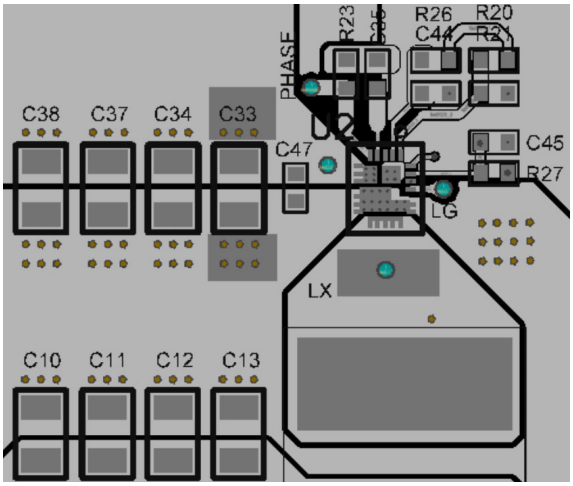


Figure 11. Top Layer of Demo Board, VIN, VSWH and PGND Copper Pads

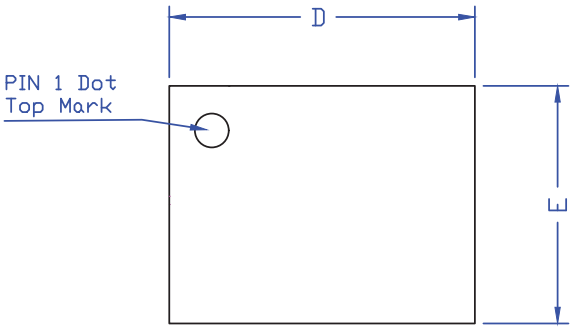
As the primary and secondary (complimentary) AC current loops move through VIN to VSWH and through PGND to VSWH, large positive and negative voltage spikes appear at the VSWH terminal which are caused by the large internal di/dt produced by the package parasitic. To minimize the effects of this interference at the VSWH terminal, at which the main inductor L1 is mounted, size just enough for the inductor to physically fit. The goal is to employ the least amount of copper area for this VSWH terminal, only enough so the inductor can be securely mounted.

To minimize the effects of switching noise coupling to the rest of the sensitive areas of the PCB, the area directly underneath the designated VSWH pad or inductor terminal is voided and the shape of this void is replicated descending down through the rest of the layers.

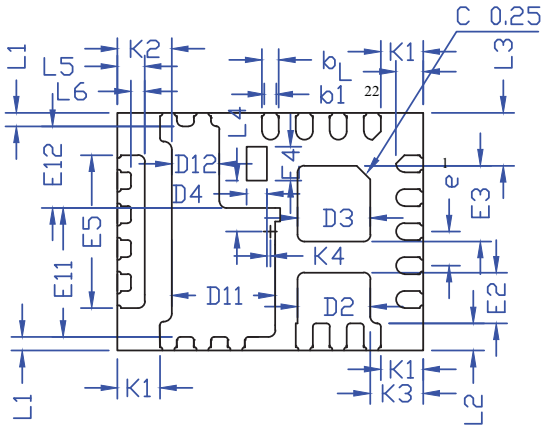
Positioning VIAs through the landing pattern of the VIN and PGND thermal pads will help quickly facilitate the thermal build up and spread the heat much more quickly towards the surrounding copper layers descending from the top layer. (See RECOMMENDED LANDING PATTERN AND VIA PLACEMENT section).

The exposed pads dimensional footprint of the 3.5x4.5 QFN package is shown on the package dimensions page. For optimal thermal relief, it is recommended to fill the PGND and VIN exposed landing pattern with 10mil diameter VIAs. 10mil diameter is a commonly used via diameter as it is optimally cost effective based on the tooling bit used in manufacturing. Each via is associated with a 20mil diameter keep out. Maintain a 5mil clearance (127um) around the inside edge of each exposed pad in the event of solder overflow potentially shorting with the adjacent exposed thermal pad.

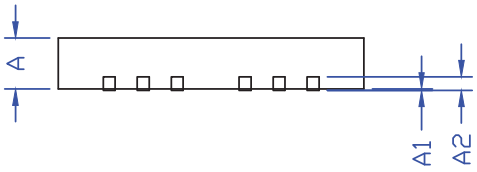
Package Dimensions, QFN3.5x4.5-22L



TOP VIEW



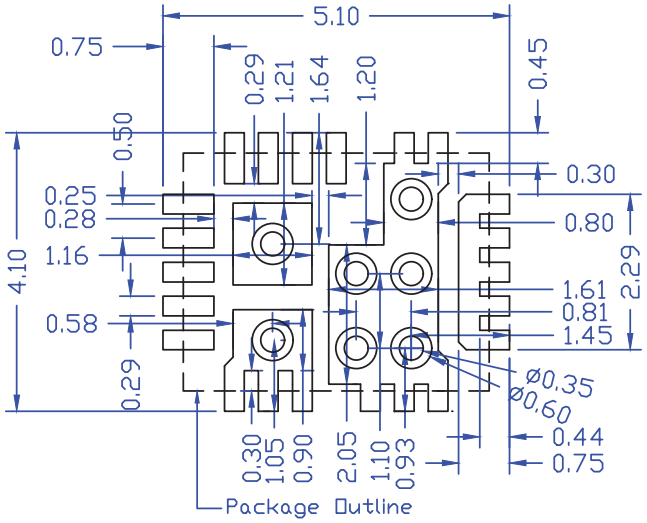
BOTTOM VIEW



SIDE VIEW

SYMBOLS	DIMENSION IN MM			DIMENSION IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	-	0.05	0.000	-	0.002
A2		0.2REF			0.008REF	
E	3.40	3.50	3.60	0.134	0.138	0.142
E11	1.85	1.90	1.95	0.073	0.075	0.077
E12	1.15	1.20	1.25	0.045	0.047	0.049
E2	0.70	0.75	0.80	0.027	0.029	0.031
E3	1.07	1.12	1.17	0.042	0.044	0.046
E4	0.45	0.50	0.55	0.018	0.020	0.022
E5	2.20	2.25	2.30	0.087	0.089	0.091
D	4.40	4.50	4.60	0.173	0.177	0.181
D11	1.47	1.52	1.57	0.058	0.060	0.062
D12	0.65	0.70	0.75	0.026	0.028	0.030
D2	1.02	1.07	1.12	0.040	0.042	0.044
D3	1.02	1.07	1.12	0.040	0.042	0.044
D4	0.25	0.30	0.35	0.010	0.012	0.014
L	0.35	0.40	0.45	0.014	0.016	0.018
L1	0.15	0.20	0.25	0.006	0.008	0.010
L2	0.35	0.40	0.45	0.014	0.016	0.018
L3	0.73	0.78	0.83	0.029	0.031	0.033
L4	0.70	0.75	0.80	0.028	0.030	0.031
L5	0.35	0.40	0.45	0.014	0.016	0.018
L6	0.15	0.20	0.25	0.006	0.008	0.010
K1	0.58	0.63	0.68	0.023	0.025	0.027
K2	0.75	0.80	0.85	0.030	0.031	0.033
K3	0.73	0.78	0.83	0.029	0.031	0.033
K4	0.00	0.05	0.10	0.000	0.002	0.004
b	0.20	0.25	0.30	0.008	0.010	0.012
b1	0.13	0.18	0.23	0.005	0.007	0.009
e		0.50BSC			0.02BSC	

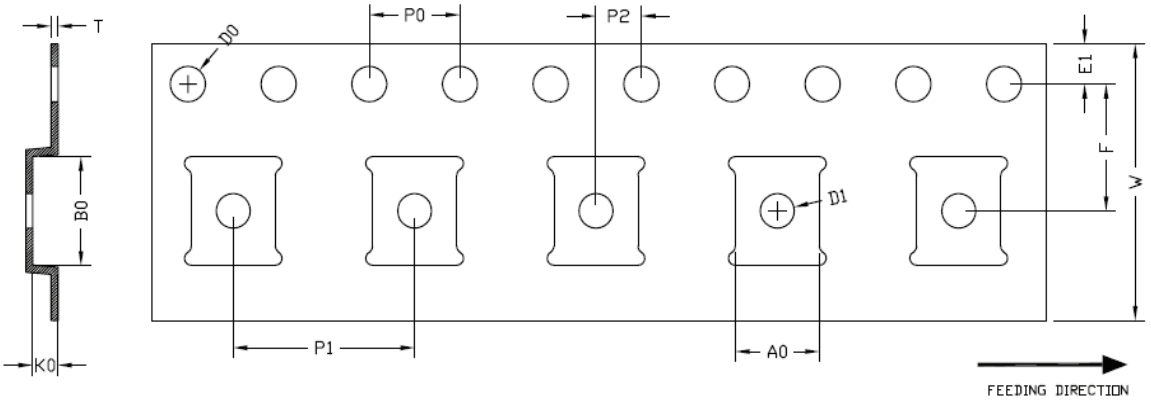
RECOMMENDED LAND PATTERN



UNIT: mm

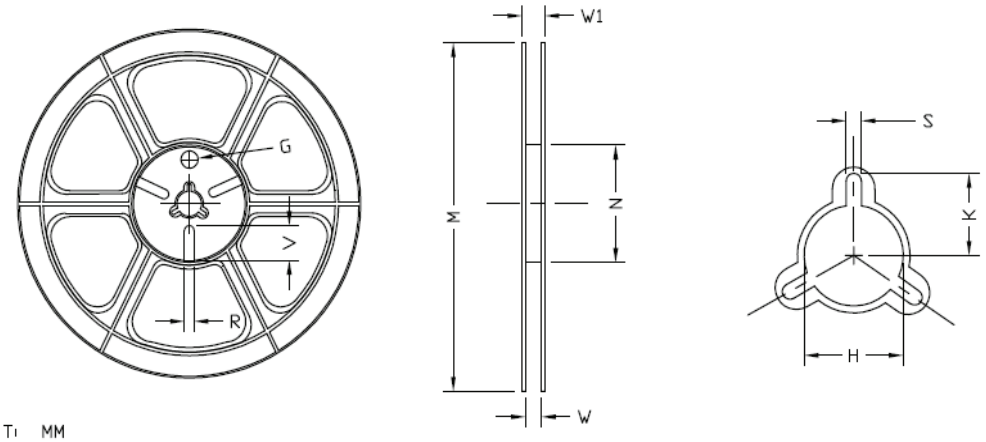
NOTE
CONTROLLING DIMENSION IS MILLIMETER.
CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

Tape and Reel Drawing, QFN3.5x4.5-22L



UNIT: MM

PACKAGE	A0	B0	K0	D0	D1	W	E1	F	P0	P1	P2	T
QFN4.5x3.5	3.71 ±0.10	4.71 ±0.10	1.11 ±0.10	1.55 ±0.05	1.50 Min.	12.00 ±0.30	1.75 ±0.10	5.50 ±0.10	4.00 ±0.10	8.00 ±0.10	2.00 ±0.10	0.30 ±0.05

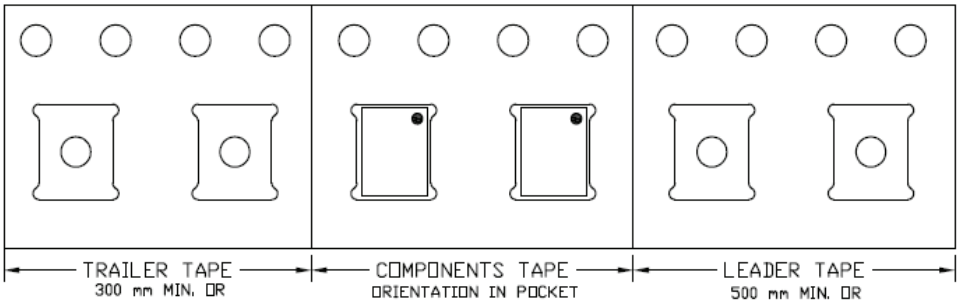


UNIT: MM

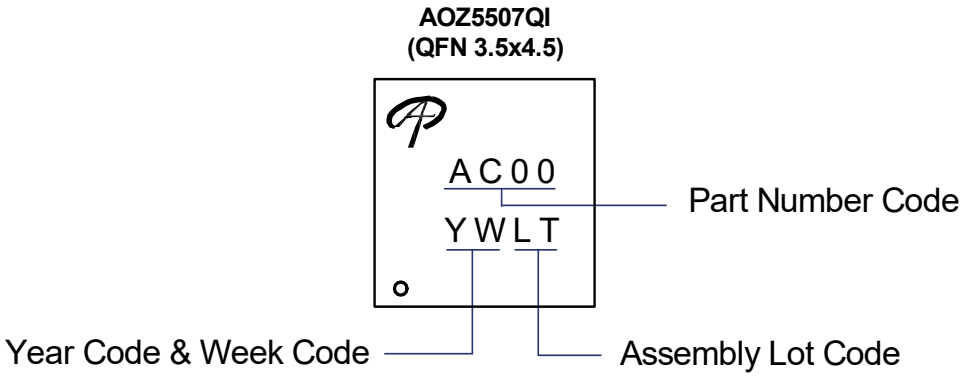
TAPE SIZE	REEL SIZE	M	N	W	W1	H	K	S	G	R	V
12 mm	ø330	ø330.00 ±0.50	ø97.00 ±0.10	13.00 ±0.30	17.40 ±1.00	ø13.00 +0.50 −0.20	10.60	2.00 ±0.50	---	---	---

Leader / Trailer & Orientation

Unit Per Reel: 5000pcs



Part Marking



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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.

2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

单击下面可查看定价，库存，交付和生命周期等信息

>>AOS(万代)