AOZ7100QI

USB Type-C and USB PD Source Controller

General Description

The AOZ7100 is a USB Type-C controller that supports to Power Delivery 2.0/3.0. It has a built-in 32-bit MCU, GPIOs, I2C interface and 10bits ADC unit for fulfilling power control and protection on charger and adapter applications. It is available in 28-pin WQFN package.

Features

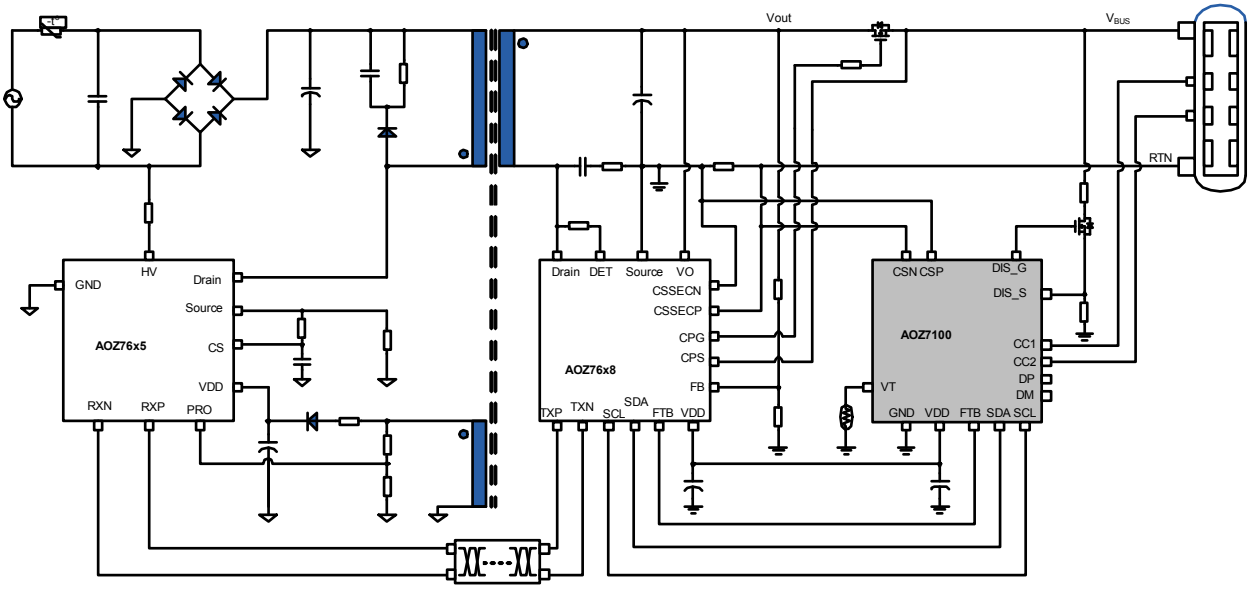
- Support USB PD 2.0/3.0 via CC1 & CC2 pins
- Support BC 1.2 via DP & DM pins
- Discharge MOS control and cold-socket detection
- CC1/CC2 with high noise immunity
- Support over voltage detection for CC1/CC2
- Support external NTC over temperature Detection
- Support under voltage protection (UVP)
- One high accuracy 10bit-SAR ADC for Voltage and low-side Current monitors
- Built-in 32-bit MCU
- Built-in 16 KB SRAM
- Built-in 32 KB EEPROM

Applications

- USB Type-C PD Charger
- Smart Charger
- Expose PAD

Green Product

Typical Application

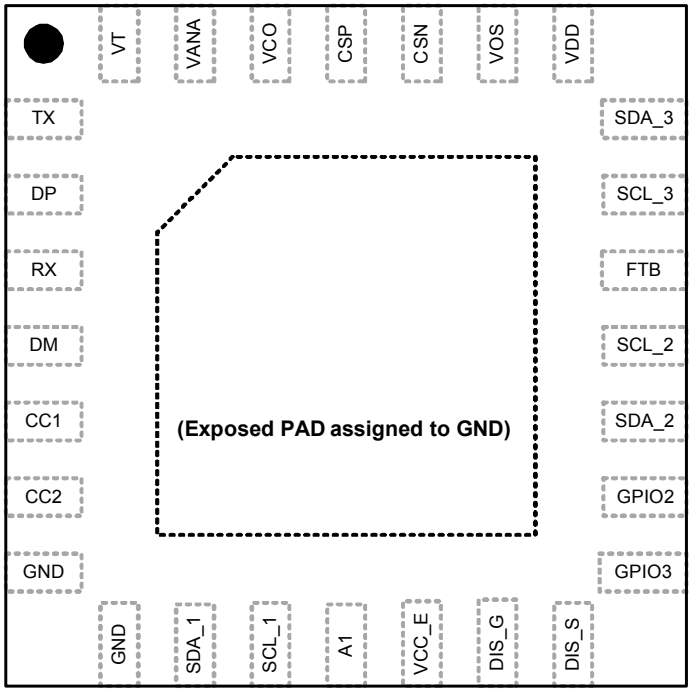


Ordering Information

Part Number	Ambient Temperature Range	Package	Environmental
AOZ7100QI	-40°C to +85°C	WQFN 4X4-28L	Green Product

AOS Green Products use reduced levels of Halogens, and are also RoHS compliant.

Pin Configuration



QFN 4mm x 4mm 28-pin
(Top View)

Pin Description

Pin Number	Pin Name	Pin Function
1	TX	GPIO/ UART_TX
2	DP	USB D+ Channel
3	RX	GPIO/ UART_RX
4	DM	USB D- Channel
5	CC1	Configuration Channel 1 of Type C
6	CC2	Configuration Channel 1 of Type C
7	GND	Ground
8	GND	Ground
9	SDA_1	I2C slave SDA of built-in EEPROM:
10	SCL_1	I2C slave SCL of built-in EEPROM:
11	A1	Slave I2C: device address pin of built-in EEPROM:
12	VCC_E	EEPROM power input
13	DIS_G	VBUS Discharge Function: to NMOS gate terminal
14	DIS_S	VBUS Discharge Function: to NMOS source terminal / VBUS monitor
15	GPIO3	General Purpose I/O
16	GPIO2	General Purpose I/O
17	SDA_2	General Purpose I/O: Specific master SDA to AOZ-76x8
18	SCL_2	General Purpose I/O: Specific master SCL to AOZ-76x8
19	FTB	Fault Interrupt Channel
20	SCL_3	I2C Master SCL to external slave device or built-in EEPROM
21	SDA_3	I2C Master SDA to external slave device or built-in EEPROM
22	VDD	Power Input
23	VOS	Output Voltage detection
24	CSN	Low-side current sense Input-negative
25	CSP	Low-side Current Sense Input-positive
26	VCO	LDO output 1.2V for MCU Core
27	VANA	LDO output 3.3V for built-in analog device
28	VT	Temperature sense pin (Need External NTC Resistor)& RESET PIN input
Expose PAD		Ground

Absolute Maximum Ratings

Exceeding the Absolute Maximum Ratings may damage the device.

Parameter	Rating
VDD	0V to 6.0V
V_{SDA}, V_{SCL}, V_{FTB}	0V to 6.0V
V_{CSP}, V_{CSN}, V_{CC1}, V_{CC2}, V_{GPIO_DM}, V_{GPIO_DN}, VT, VOS, V_{DIS_G}, V_{DIS_S}	-0.3V to +6.0V
VANA	-0.3V to +3.6V
VCO	-0.3V to +1.3V
GND	-0.3V to +0.3V
Package Power Dissipation	2.9W
Junction Temperature (T_J)	+150°C
Storage Temperature (T_S)	-65°C to +150°C
ESD HBM(1)	4kV
ESD CDM(1)	250V

Notes:

1. Devices are inherently ESD sensitive, handling precautions are required. Human body model rating: 1.5kΩ in series with 100pF.

Recommended Operating Conditions

The device is not guaranteed to operate beyond the Maximum Recommended Operating Conditions.

Parameter	Rating
Supply Voltage (VDD)	3.3V to 5.5V
Ambient Temperature (T_A)	-40°C to +105°C
Package Thermal Resistance (θ_{JA}) (θ_{JC})	 42°C/W 9 °C/W

Electrical Characteristics

V_O=5V, T_A = -25°C to 85°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VDD Supply Input						
V_{DD_ON}	Power On Threshold		2.9	3	3.1	V
I_{VDD}	Operating Average Current	V_{VDD} =5V		2.5		mA
V_{VDD_th}	Threshold Voltage of UVLO		2.7	2.8	2.9	V
P_{AVDD_PSC}	Power Saving Current	V_{VDD} =5V, Enter sleep mode	500	600		µA
VANA LDO						
V_{VANA}	LDO Voltage to Peripheral Units	$C_{\_VANA}$ =1uF	2.9	3.1	3.6	V
VCO LDO						
V_{CO}	LDO Voltage to MCU Core	$C_{\_VCO}$ =1uF	1.1	1.2	1.3	V
V_{reset_vco}	Power-On Reset Voltage	Vary by Firmware design		0.4		V
GPIOs						
V_{GPIO}	VGPIO_ABS	Maximum Voltage per GPIO	2.9	3.1	3.5	V
I_{GPIO}	IGPIO_ABS	Maximum Current per GPIO	2.0	2.5	3.0	mA
GPIO_INH	“H” Level	Threshold to Logical “1”	2.0	2.2		V
GPIO_INL	“H” Level	Threshold to Logical “0”		0.4	0.6	V

Electrical Characteristics *(Continued)*

V_O=5V, T_A = -25°C to 85°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Fault Bar (FTB Pin)						
V_{FTBL}	Low Level Threshold Voltage				0.6	V
V_{FTBH}	High Level Threshold Voltage		1.8			V
V_{FTBHYS}	Hysteresis of Schmitt Trigger Inputs		0.1			V
V_{FTBOL}	Low Level Output Voltage	Open drain, 3mA sink			0.4	V
V_{FPO}	Output Level			$V_{ANA-0.1}$		V
EXTERNAL OTP (VT)						
I_{OTP}	OTP Detect Source Current	Vary by Firmware design	18	20	22	µA
V_{OTP}	OTP Enable Level	VT pin connect with (100k NTC+ 8kΩ resistor) to GND (Vary by Firmware design)		0.8		V
V_{OTPHYS}	Hysteresis Voltage	100kΩ NTC+ 8kΩ resistor (Vary by Firmware design)		100		mV
t_{OTP}	Debounce Time	100kΩ NTC+ 8kΩ resistor (Vary by Firmware design)		60		mSec
V_{reset_VT}	Power on Reset Voltage	(Vary by Firmware design)		0.4		V
VBUS Monitor (DIS_S Pin)						
V_{BUSM_L}	Input Low Threshold	VBUS=5V, R_{DIS_1}=10kΩ, R_{DIS_2}=1.2kΩ		0.15		V
V_{BUSM_H}	Input High Threshold	VBUS=5V, R_{DIS_1}=10kΩ, R_{DIS_2}=1.2kΩ		0.3		V
t_{BUSM_de}	Denounce Timer	Programmable parameter	0.1		1	mSec
DP and DM Pins						
V_{O_DP} / V_{O_DM}	Line Output Voltage	V_{VANA}=2.9~3.6V		2.7		V
Power Delivery PHY Interface						
$I_{CC\_Default}$	Default Current	VDD =5V, Detach	64	80	96	µA
$R_{d\_1.5A}$	Pull-Down Resister		4.6	5.1	5.6	kΩ
CC_{CLP}	Clamp Voltage to CC1/2		3.0	3.3	3.5	V
I2C PHY Interface						
V_{IL}	Low Level Threshold Voltage				0.6	V
V_{IH}	High Level Threshold Voltage		1.8			V
V_{HYS}	Hysteresis of Schmitt Trigger Inputs		0.1			V
V_{OL}	Low Level Output Voltage	Open Drain, 3mA Sink Current			0.4	V
t_{SP}	Pulse Width of Spikes Suppressed by Input Filter		32			ns
f_{SCL}	SCL Clock Frequency		100		400	kHz
$t_{HD:STA}$	Hold Time (repeated) START Condition		0.6			µS

Electrical Characteristics *(Continued)*

V_O=5V, T_A = -25°C to 85°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{LOW}	Low Period of SCL Clock		1.3			µS
t_{HIGH}	High Period of SCL Clock		0.6			µS
$t_{SU:STA}$	Set-up Time for a Repeated START Condition		0.6			µS
$t_{HD:DAT}$	Data Hold Time		50		900	nS
$t_{SU:DAT}$	Data Set-up Time		100			nS
t_{R2}	Rising Time (SDA or SCL)		20+0.1 Cb*		300	nS
t_{F2}	Falling Time (SDA or SCL)		20+0.1 Cb*		300	nS
$t_{SU:STO}$	Set-up Time for STOP Condition		0.6			µS
t_{BUF}	Bus Free Time between STOP & START Condition		1.3			µS
C_b	Capacitive Load of Each Bus Line				400	pF

Notes:

2. Guaranteed by design.

3. Refer to Figure 1 for I2C Timing Definitions.

4. Cb= capacitance for bus line in pF.

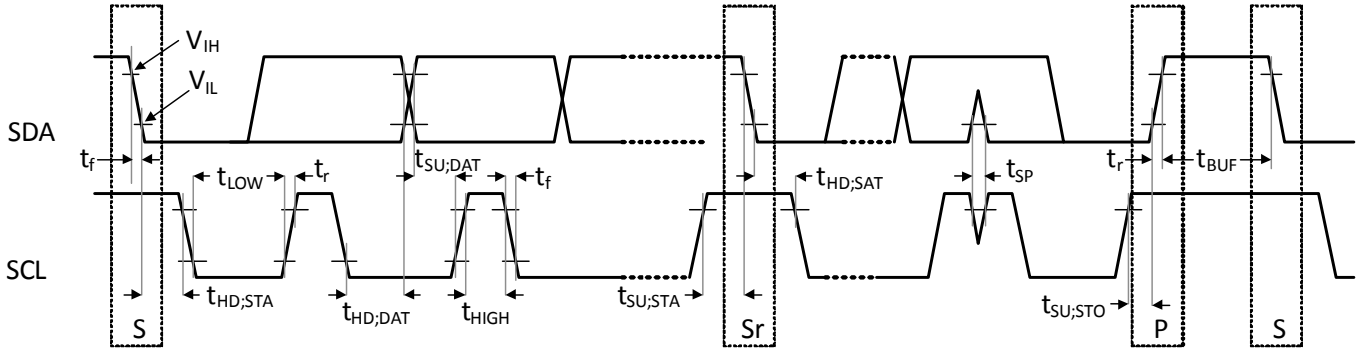
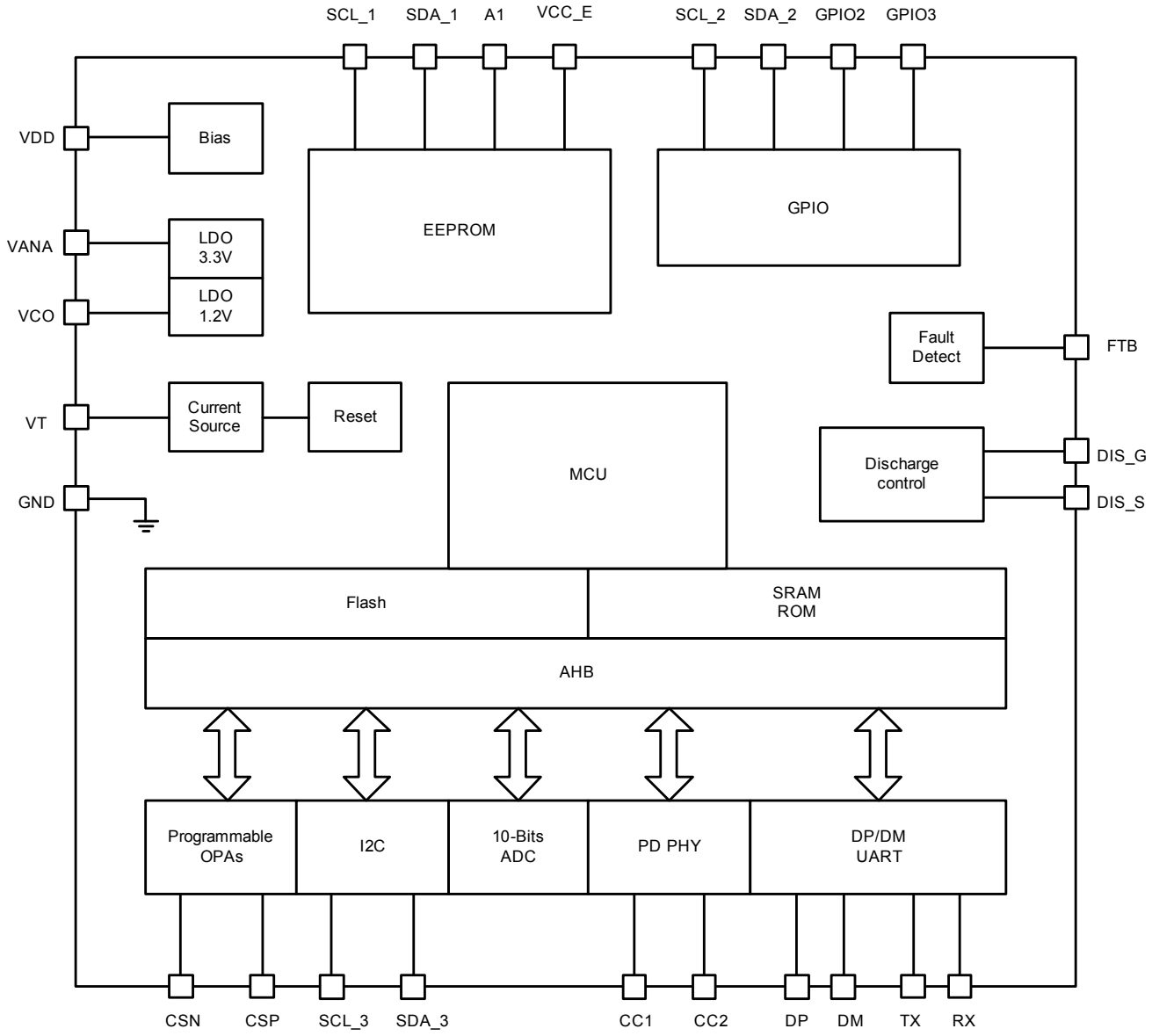


Figure 1. I²C Timing Definitions (reproduced from Phillips I²C specification version 1.1)

Functional Block Diagram



Detailed Description

USB Implementers Forum (USB-IF) released USB Power Delivery (PD) 2.0/3.0 Specifications for intelligent and flexible system level management of power. Both power provider and power consumer would need Power Delivery interface to negotiate and share the message such as VBUS and protection method. Existing PD interface of AOZ7100 could fulfill Dual Role Port application for power provider and consumer. An I2C master interface is adapted for power management and expanding peripheral control mechanism.

Start Up Via Pin VDD

Using external device's LDO or possible source, AO7100 can be powered to start up. AOZ7100 is designed to operate with low supply voltages down to 2.9V. Two internal LDOs of AOZ7100 operate to provide individual power to MCU core, comparators and built-in ADCs. It is recommended to add over 1uF ceramic capacitor to VANA and VCO output pin respectively.

I2C Master Interface

AOZ7100 has two I2C master Interface to fulfill design flexibility and expand digital control mechanism. Two pull-up resistors are built into AOZ7100 for minimizing external component.

Configuration Channel CC1/CC2

CC channels are used for connection detect, PD interface configuration and message sending/receiving.

GPIOs Device

GPIOs can be utilized to control other switch component or sense specific digital signal. Additionally, firmware hardware of MASK ROM can be selectable by status of the GPIOs.

Mask-ROM (Option)

High reliability built-in Mask-ROM can be merged into AOZ7100 to store the boot-loader or customized firmware. Additional, Multi Mask-ROM providing different firmware version is adapted in advance to ensure design selection. For the product development or validation period, it is recommended to use built-in I2C-EEPROM to store the boot-loader or firmware.

32kB EEPROM

An EEPROM device is integrated into AOZ7100 for customized development period or final product. Microcontroller of AOZ7100 could be programmed by downloading firmware of EEPROM. Pin SDA(S) and SCL(S) could be used to implement update or download firmware. Pin A1 is device address input that would be internally pulled down to GND. Therefore, EEPROM provides design flexibility to fulfill system function.

VBUS Voltage Monitor Pin VOS

VOS could monitor VBUS level via divided resistors. Firmware can set individual OVP level to corresponding Power Data Object (PDO). Once built-in OVP is triggered, AOZ7100 could turn off load switch and set VBUS back to default 5V.

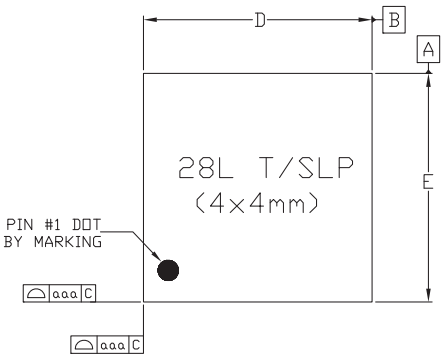
VBUS Current Monitor Pin CSP & CSN

Pin CSP and CSN are used to sense load current. Firmware can set individual OCP level to corresponding Power Data Object (PDO). Under overload conditions, AOZ7100 could take Current Fold-Back mechanism to reduce the power dissipation within safe operating area.

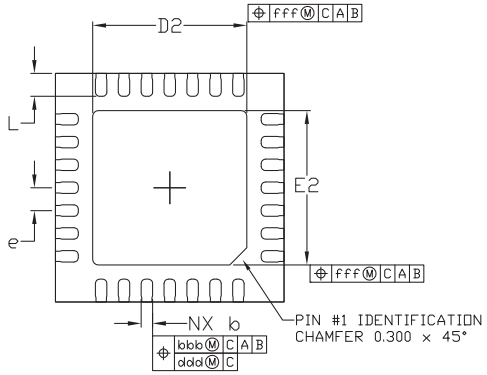
External Discharge Switch Control and Cold-Socket Detect

AOZ7100 provide gate driver pin DIS_G to control external discharge switch. Once receiving PD hard reset message or taking protection, external discharge switch would be used to discharge. In addition, AOZ7100 can check cold socket of receptacle via DIS_S with appropriate divided pull down resistor.

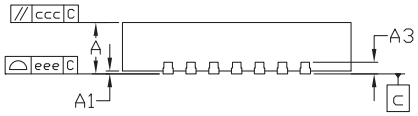
Packaging Dimensions WQFN4x4-28L



TOP VIEW



BOTTOM VIEW



SIDE VIEW

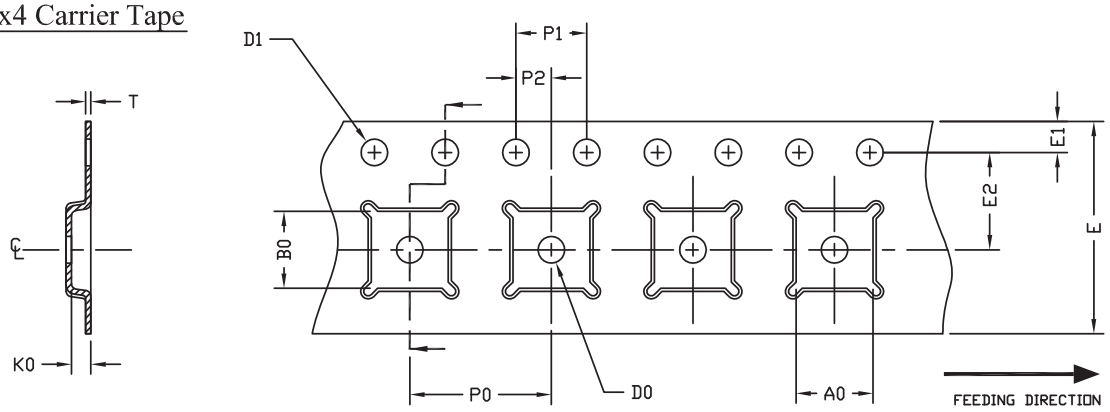
Dimensional Ref.			
REF.	Min.	Nom.	Max.
A	0.700	0.750	0.800
A1	0.000	--	0.050
A3	0.203 Ref.		
D	3.950	4.000	4.050
E	3.950	4.000	4.050
D2	2.650	2.700	2.750
E2	2.650	2.700	2.750
b	0.150	0.200	0.250
L	0.350	0.400	0.450
e	0.400 BSC		
Tol. of Form&Position			
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

Notes

1. All DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER JEDEC MO-220.

Tape and Reel, WQFN4x4-28L

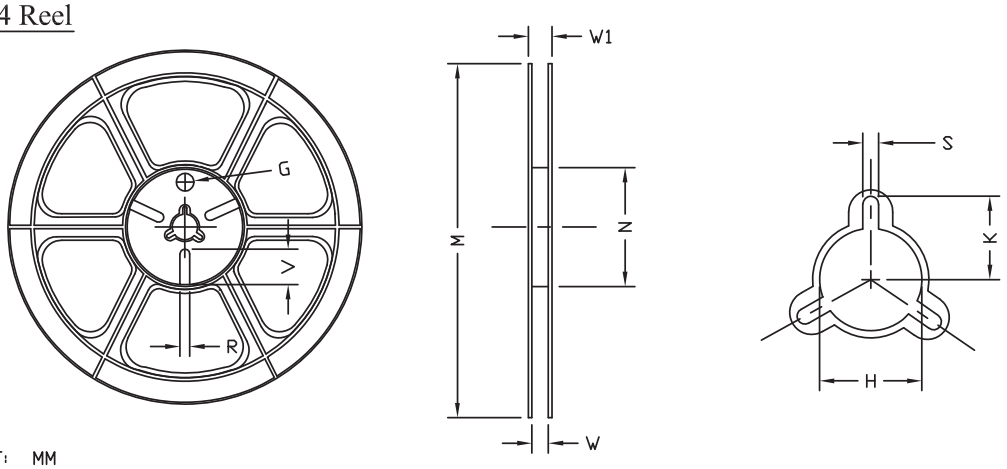
QFN4x4 Carrier Tape



UNIT: MM

PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
QFN4x4 (12 mm)	4.35 ±0.10	4.35 ±0.10	1.10 ±0.10	1.50 MIN.	1.50 +0.1 −0.0	12.0 ±0.3	1.75 ±0.10	5.50 ±0.05	8.00 ±0.10	4.00 ±0.10	2.00 ±0.05	0.30 ±0.05

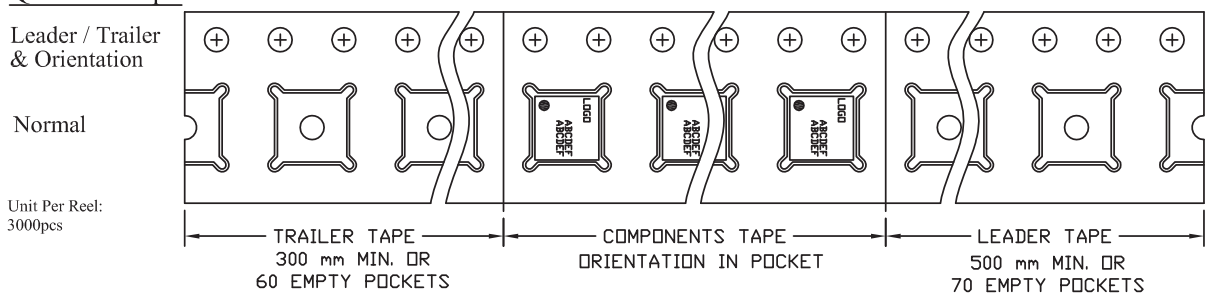
QFN4x4 Reel



UNIT: MM

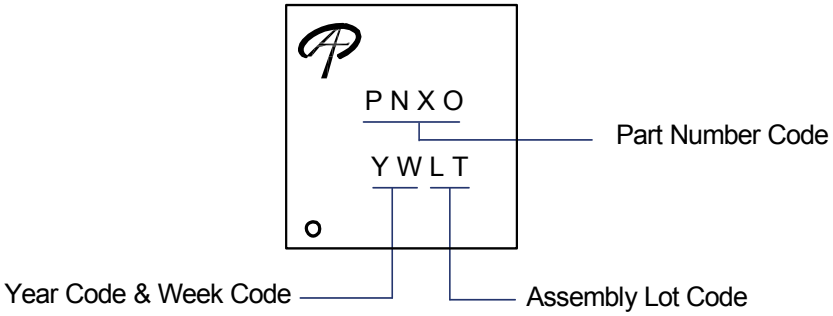
TAPE SIZE	REEL SIZE	M	N	W	W1	H	K	S	G	R	V
12 mm	ø330	ø330.0 ±2.0	ø79.0 ±1.0	12.4 +2.0 −0.0	17.0 +2.6 −1.2	ø13.0 ±0.5	10.5 ±0.2	2.0 ±0.5	---	---	---

QFN4x4 Tape



Part Marking

AOZ7100QI
(4mm x 4mm WQFN)



Part No.	Description	Code
AOZ7100QI	Green Product	BU00

LEGAL DISCLAIMER

Applications or uses as critical components in life support devices or systems are not authorized. AOS does not assume any liability arising out of such applications or uses of its products. AOS reserves the right to make changes to product specifications without notice. It is the responsibility of the customer to evaluate suitability of the product for their intended application. Customer shall comply with applicable legal requirements, including all applicable export control rules, regulations and limitations.

AOS' products are provided subject to AOS' terms and conditions of sale which are set forth at:
http://www.aosmd.com/terms_and_conditions_of_sale

LIFE SUPPORT POLICY

ALPHA AND OMEGA SEMICONDUCTOR PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.

2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

单击下面可查看定价，库存，交付和生命周期等信息

>>AOS(万代)