AOZ7111

Critical Conduction Mode PFC Controller

General Description

The AOZ7111 is an active power factor correction (PFC) controller for boost PFC applications that operate in critical conduction mode (CRM). The device uses a voltage mode PWM which does not need rectified AC line voltage information, it saves the power loss of an input sensing network necessary for traditional current-mode CRM PFC controller. The AOZ7111 minimizes the number of external components by integrating safety features that make it an excellent choice for designing robust PFC stages.

The AOZ7111 is available in a SO-8 package and it is rated over a -40°C to +125°C ambient temperature range.

Features

- No AC input voltage sensing requirement
- AC Fault Detect™ makes system more robust
- Maximum switching frequency limitation
- Additional OVP detection pin
- Output over-voltage / open-feedback protection and disable function
- Internal closed loop soft-start
- Dynamic OVP function
- Non-linear gain error amplifier enable fast line and load transient response
- No need for the auxiliary winding with minus current detection (ZCD)
- 150µs internal start-up timer
- MOSFET over-current protection and inductor saturation protection
- Under-voltage lockout with hysteresis
- Lower startup and operating current
- +300mA / -800mA peak gate drive current
- Thermal shutdown
- SO-8 package

Applications

- Adapter / ballast
- LCD TV / LED TV
- SMPS

Green Product

Typical Application

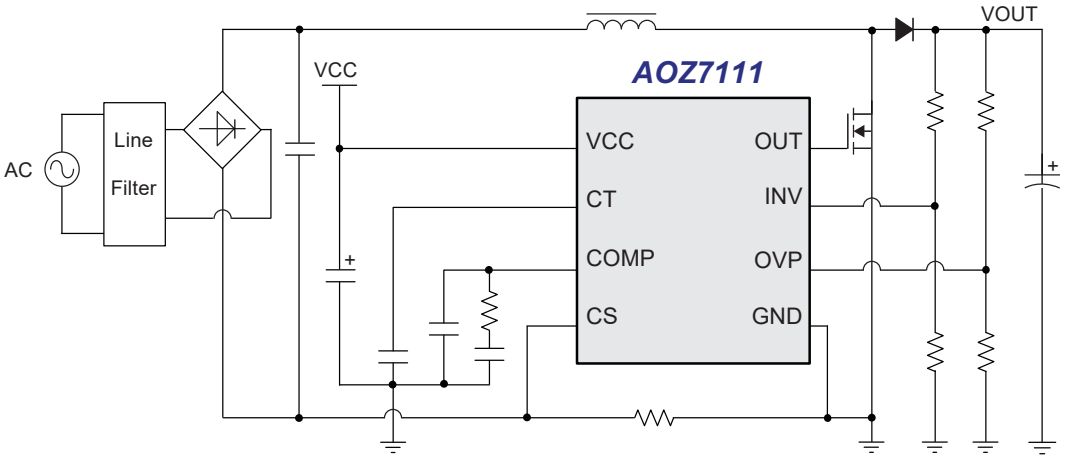


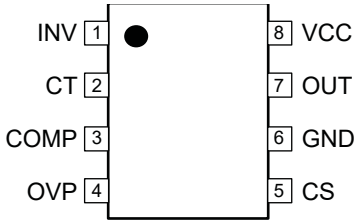
Figure 1. Typical Boost PFC Application

Ordering Information

Part Number	Ambient Temperature Range	Package	Environmental
AOZ7111AI	-40°C to +125°C	SO-8	Green Product

AOS Green Products use reduced levels of Halogens, and are also RoHS compliant.
Please visit www.aosmd.com/media/AOSGreenPolicy.pdf for additional information.

Pin Configuration



SO-8
(Top View)

Pin Description

Pin Number	Pin Name	Pin Function
1	INV	Inverting input of the error amplifier. The output voltage of the boost PFC converter should be resistively divided to 2.5V.
2	CT	The Ct pin sources a current to charge an external timing capacitor. The circuit controls the power switch on time by comparing the Ct voltage to an internal voltage derived from V_{COMP}. The Ct pin discharge the external timing capacitor at the end of the on time.
3	COMP	This pin is the output of the transconductance error amplifier. Components for the compensation should be connected between this pin and GND.
4	OVP	The OVP pin is used to detect PFC output over-voltage when the INV pin information is not correct.
5	CS	This pin is the input of the zero current detection and over-current protection comparator.
6	GND	The GND pin is analog ground.
7	OUT	This pin is the gate drive output.
8	VCC	This is the IC supply pin.

Absolute Maximum Ratings

Exceeding the Absolute Maximum Ratings may damage the device.

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	-0.3	20	V
I_{OH}, I_{OL}	Peak Drive Output Current	-800	+300	mA
I_{CLAMP}	Driver Output Clamping Diode VO>VCC or VO<-0.3V	-10	+10	mA
V_{IN}	INV, OVP Pin Input Voltage	-0.3	5	V
	CT, COMP Pin Input Voltage	-0.3	9.5	V
	CS Pin Input Voltage	-5	0.3	V
	Driver Output Voltage	-0.3	V_{CC}	V
T_J	Operating Junction Temperature		+150	°C
T_A	Operating Temperature Range	-40	+125	°C
T_S	Storage Temperature Range	-65	+150	°C
ESD	Electrostatic Discharge Capability (Human Body Model, JES22-A114)		2.5	kV
T_L	Lead Temperature (Soldering, 10s)		300	°C
Θ_{JA}	Package Thermal Resistance (Junction-to-Ambient)		150	°C/W

Electrical Characteristics

T_A = 25°C, V_{CC} = 14V, unless otherwise specified(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SUPPLY						
V_{CC}	Operating Range	After Turn On	**10.5**		**18**	V
V_{START}	Start Threshold Voltage	V_{CC} Increasing	**11**	12	**13**	V
V_{STOP}	Stop Threshold Voltage	V_{CC} Decreasing	**8.5**	9.5	**10.5**	V
V_{UVLO_HY}	Input Under-Voltage Lockout Hysteresis			2.5		V
V_Z	Zener Voltage	I_{CC} = 20mA	**18**	20	**22**	V
I_{IN_NS}	Non-Switching Supply Current	V_{COMP} < 0.9V, V_{IN} = 14V	0.5	1.0	1.5	mA
I_{STB}	Standby Current	V_{INV} < 0.2V		30	60	µA
ERROR AMPLIFIER						
V_{REF}	Voltage Reference	T_J = 25°C	2.465	2.5	2.535	V
V_{REF_LINE}	Line Regulation	V_{CC} = 14V ~ 18V			10	mV
G_m	Transconductance	V_{INV} = 2.4V to 2.6V	75	100	125	µS
I_O	Error Amplifier Current Capability	Source: V_{INV} = V_{REF} -0.1V Sink: V_{INV} = V_{REF} +0.1V		-10 +10		µA
C_{t_OFFSET}	Minimum Control Voltage to Generate Drive Pluses			1.0		V
RAMP OSCILLATOR						
F_{MAX}	Maximum Oscillating Frequency			350		KHz
T_{START}	Restart Timer Delay		50	150	300	µs
$V_{CT(MAX)}$	CT Peak Voltage	V_{COMP} = Open		8		V
I_{CHARGE}	On Time Capacitor Charge Current		**150**	200	**250**	µA

Electrical Characteristics (Continued)

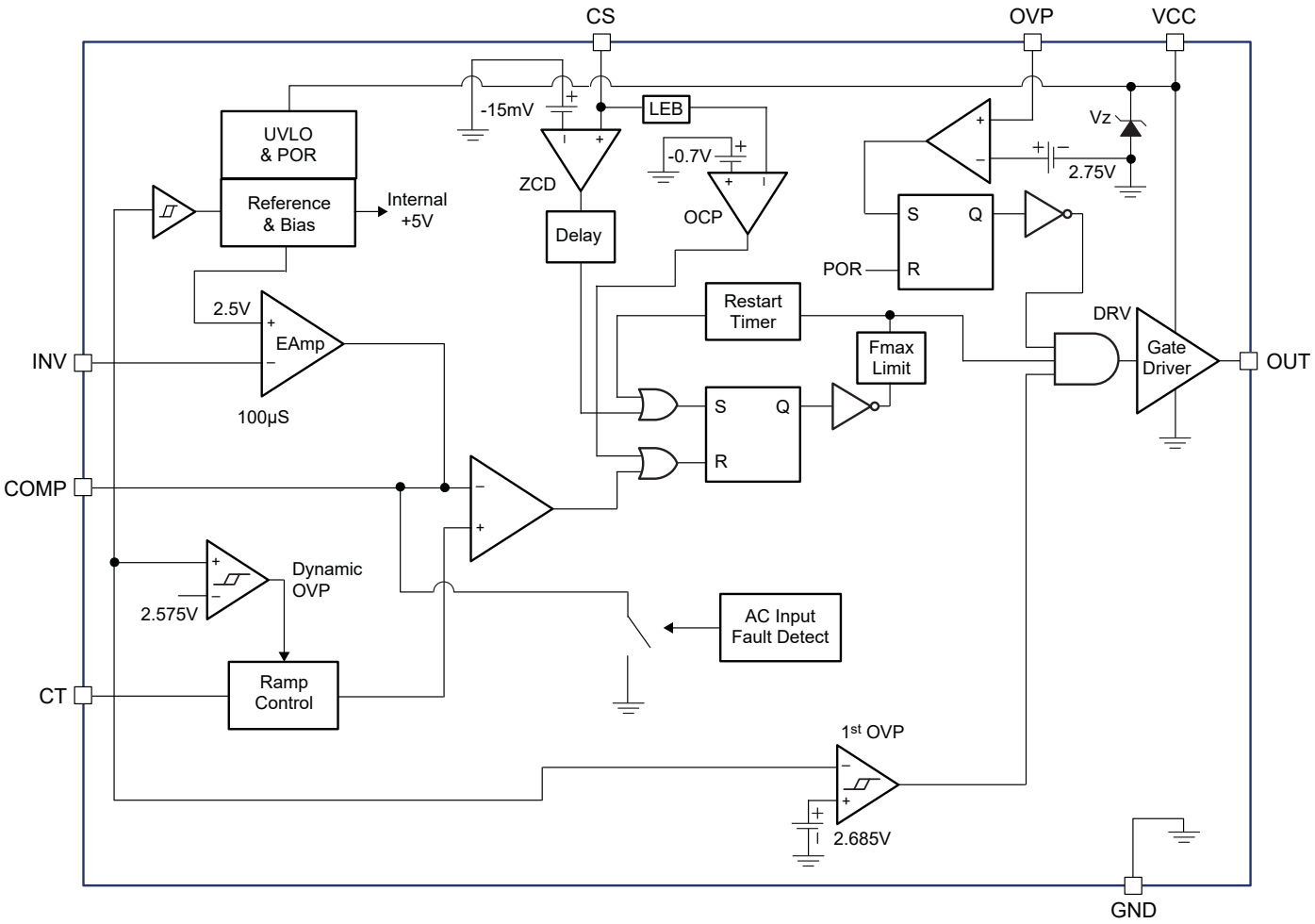
T_A = 25°C, V_{CC} = 14V, unless otherwise specified(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ZERO CURRENT DETECTION						
V_{ZCD-TH}	Zero Current Detection Comparator Threshold		**-24**	-15	**-9**	mV
V_{OCP1}	OCP1 Threshold Voltage (Shutdown Mode)		-0.8	-0.7	-0.6	V
V_{OCP2}	OCP2 Threshold Voltage (Latch Mode)			-1.2		V
$T_{ZCD, D}$	Output Delay from ZCD to Output Turn-On			650		ns
GATE DRIVE						
R_{OH}	Drive Pull-Up Resistance	I_{SOURCE} = 50mA		24	30	Ω
R_{OL}	Drive Pull-Down Resistance	I_{SINK} = 50mA		5	6	Ω
T_{RISE}	Output Rise Time	C_L = 1nF, 10% to 90%		70		ns
T_{FALL}	Output Fall Time	C_L = 1nF, 90% to 10%		25		ns
PROTECTION						
V_{DOVP}	Dynamic OVP Threshold Voltage	T_A = 25°C	2.54	2.575	2.61	V
HV_{OVP_INV}	Dynamic OVP Hysteresis	T_A = 25°C		0.05		V
V_{OVP_INV}	OVP Threshold Voltage @ INV Pin	T_A = 25°C	2.62	2.685	2.75	V
HV_{OVP_INV}	OVP Hysteresis @ INV Pin	T_A = 25°C		0.175		V
V_{OVP}	OVP Threshold Voltage @ OVP Pin	T_A = 25°C	2.65	2.75	2.85	V
V_{EN_INV}	INV Enable Threshold	T_A = 25°C		0.5		V
HY_{EN}	INV Enable Hysteresis	T_A = 25°C	0.01	0.055	0.120	V
OTP	Over-Temperature Shutdown Limit	T_J Rising T_J Falling		150 100		°C
T_{HYS}	Hysteresis Temperature of OTP			50		°C

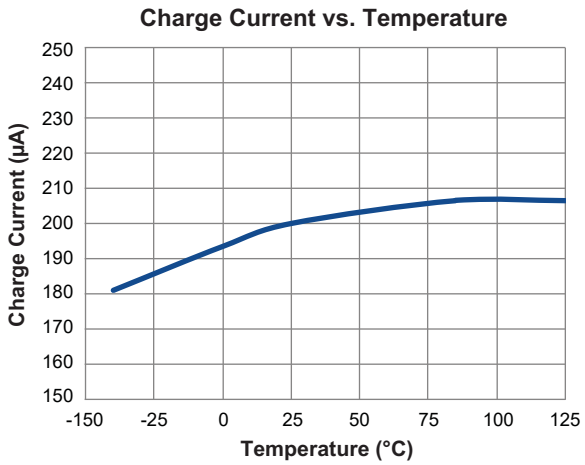
Note:

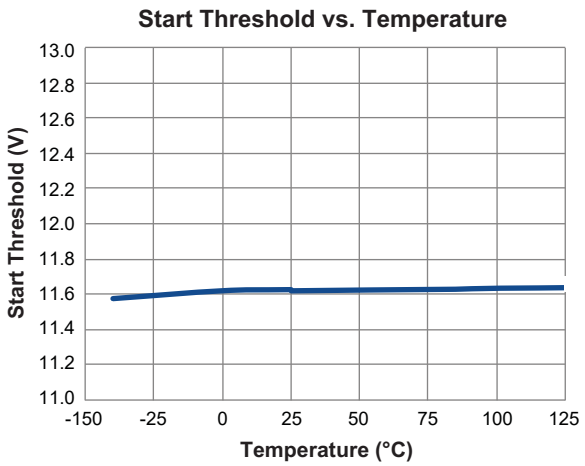
1. Specifications in **BOLD** indicate an ambient temperature range -40°C to +125°C. These specifications are guaranteed by design.

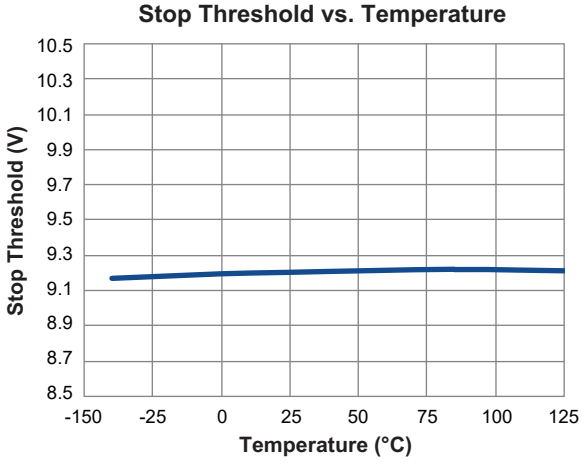
Functional Block Diagram

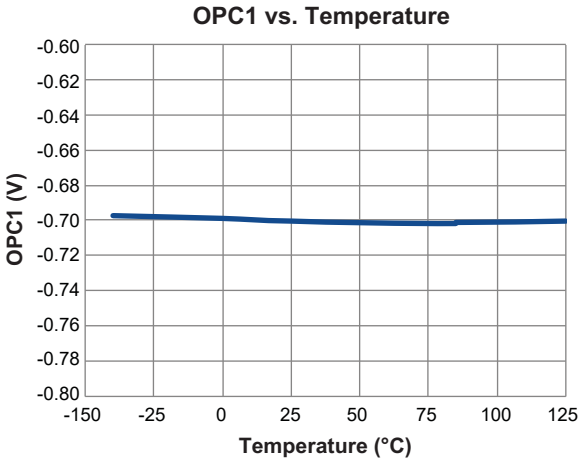


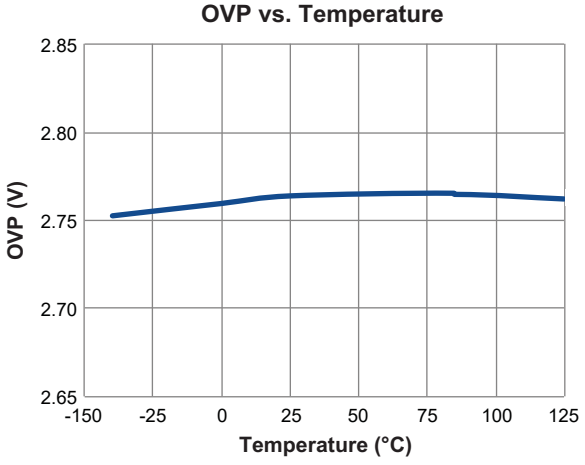
Typical Characteristics

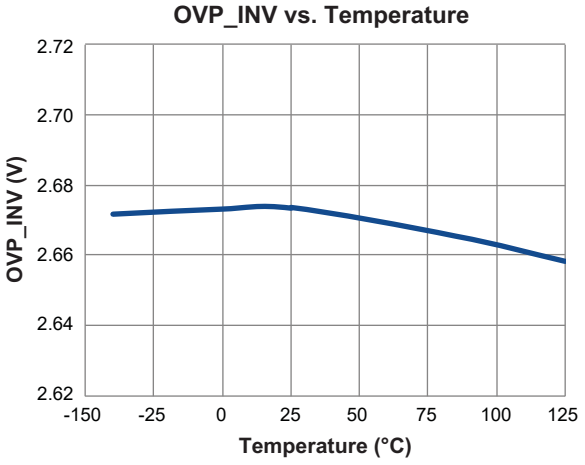




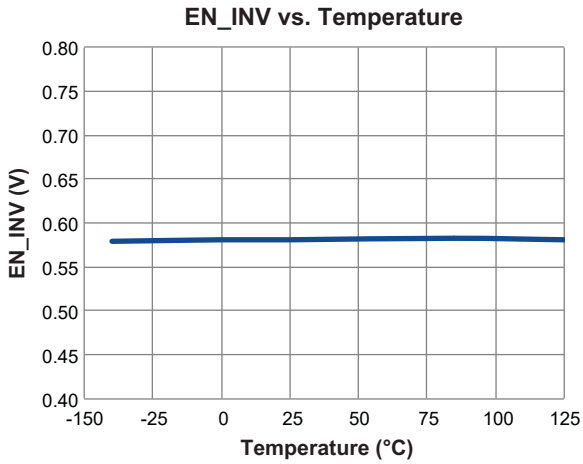


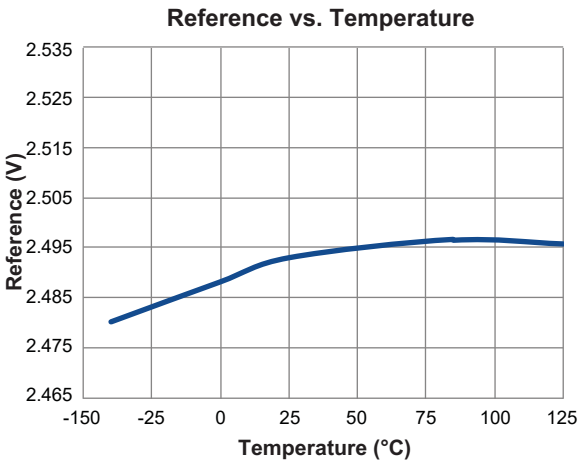


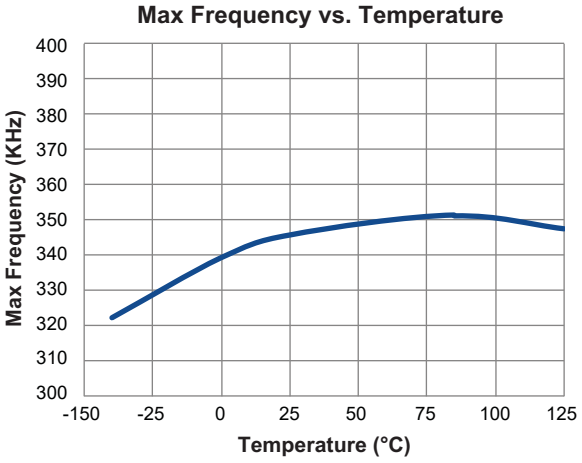


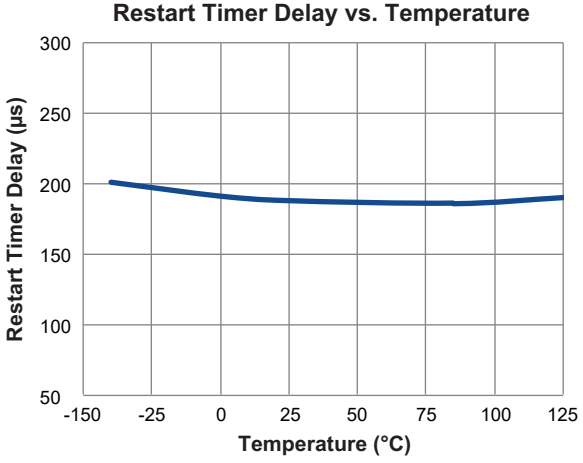


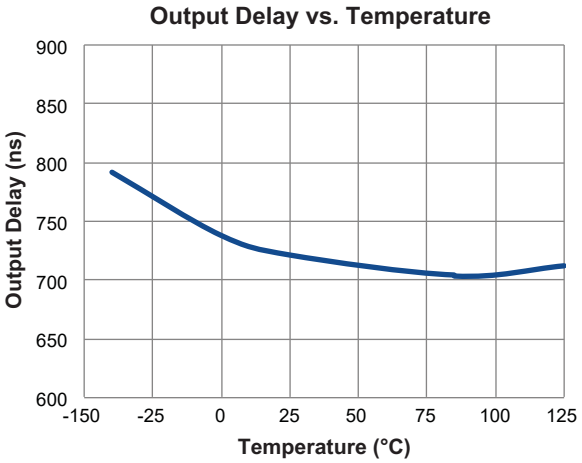
Typical Characteristics *(Continued)*

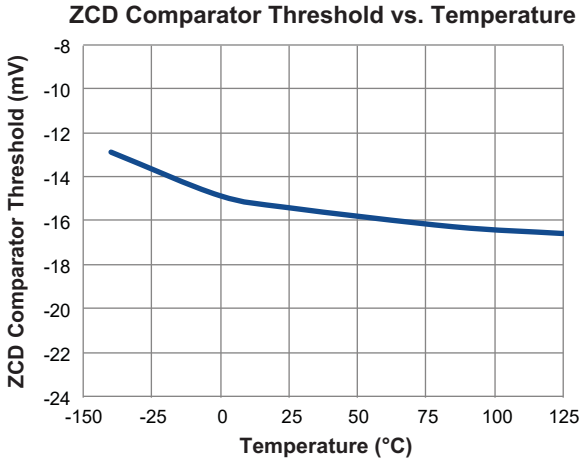












Detailed Description

The AOZ7111 is a voltage mode active power factor correction (PFC) controller designed for cost-effective boost PFC applications that operate in critical conduction mode (CRM). Its voltage mode scheme does not require an AC input line-sensing network, usually necessary for a current mode CRM PFC controller. It gets the ZCD signal pulse from the current sense resistor; therefore, ZCD auxiliary winding is not needed.

AOZ7111 features output over-voltage protection, over-current protection, open-feedback protection, and under-voltage lockout protection. A unique AC input fault detection circuit makes the system more robust during the AC absent test. The additional OVP pin can be used to double check the output voltage if the feedback resistor gets damaged. The controller also implements comprehensive safety features for robust designs.

The AOZ7111 is available in SO-8 package.

Error Amplifier Regulation

AOZ7111 regulates the boost output voltage using an internal transconductance error amplifier (EA) with a typical transconductance value of 100µS. The advantage in using a transconductance error amplifier is that the INV pin voltage is only determined by the resistor divider network connected to the output voltage, not the operation of the amplifier. This enables the INV pin to be used for sensing over-voltage or under-voltage conditions independently of the error amplifier.

The negative terminal of the EA is pinned out to INV, the positive terminal is connected to a 2.5V (±1.8%) reference (V_{REF}), and the EA output is pinned out COMP. The output of the error amplifier (COMP) is connected to the PWM comparator and controls the on-time of the OUT output.

The sink and source current capability of the error amplifier is approximate 10µA during normal operation. When the INV pin voltage is over the normal operating conditions (V_{INV}>2.6V, or V_{INV}<2.4V if the error is large), additional circuitry is activated to enhance the slew-rate of the error amplifier, it enables fast line and load transient response.

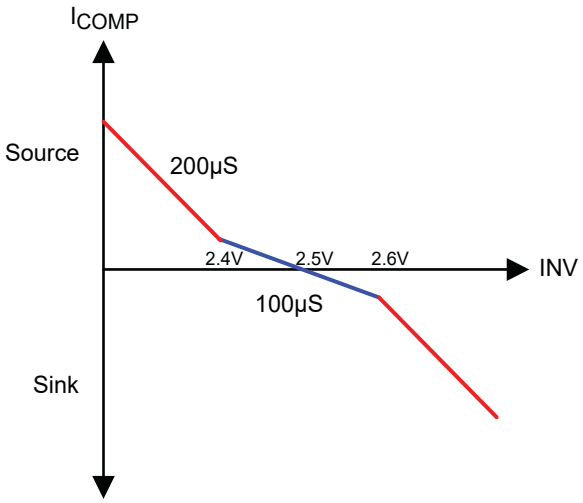


Figure 2. Non-linear Gain Characteristics

The output voltage of PFC contains a high ripple frequency, 2 times the AC power line (50Hz or 60Hz). The V_{OUT} ripple is attenuated by the regulation loop to ensure V_{COMP} is constant during the AC line cycle. In order to obtain a stable operation and ensure V_{COMP} is constant during the AC line cycle, the bandwidth should typically be set below 20Hz so that the regulation block output may be relatively constant over a given AC line cycle.

Soft-Start

AOZ7111 employs an internal soft-start function to suppress inrush current and overshoot of output voltage during the startup. The soft-start circuit works after UVLO and standby are released and before the soft-start cancellation voltage is exceeded. During the soft-start, the OTA supplies a constant 10µA into the compensation network at the COMP pin. The voltage at this pin rises linearly as well as the amplitude of the input current. As soon as the output voltage V_{OUT} reaches 95% of its rated level, the startup procedure is finished and the normal voltage control takes over.

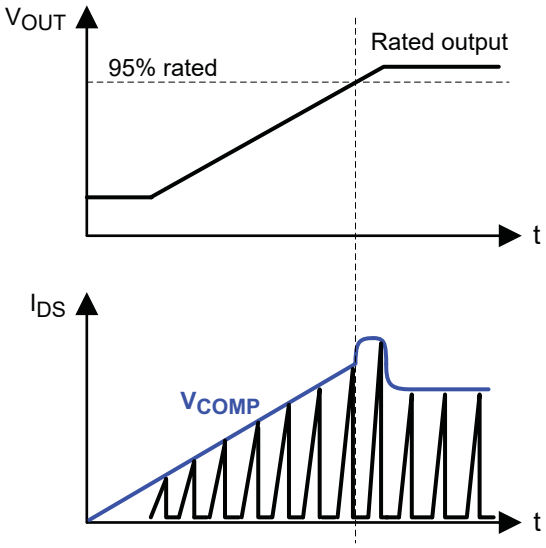


Figure 3. Soft-Start Sequence

On Time Control (Ramp Control Oscillator)

The switching pattern consists of constant on times and variable off times for a given RMS input voltage and output load. The AOZ7111 controls the on-time with the capacitor connected to the Ct pin. A current source charges the Ct capacitor to a voltage derived from the COMP pin voltage ($V_{Ct(off)}$). $V_{Ct(off)}$ is calculated as below:

$$V_{Ct(off)} = V_{COMP} - Ct_{(offset)} = \frac{2 \times P_{OUT} \times L \times I_{charge}}{EFF \times V_{AC}^{2} \times Ct}$$

When $V_{Ct(off)}$ is reached, the drive turns off.

The ramp oscillator consists of three phases:

Charge Phase: The oscillator capacitor voltage grows linearly from its bottom value (ground) until it exceeds V_{COMP} - $Ct_{(offset)}$. At that moment, the PWM latch output gets low and the oscillator discharge sequence is set.

Discharge Phase: The oscillator capacitor is discharged down to its valley value of 0V.

Standby Phase: At the end of the discharge sequence, the oscillator voltage is maintained in a low state until the PWM latch is set again.

V_{COMP} varies with the RMS input voltage and output load, the on time is constant during the AC line cycle if the values of the compensation components are sufficient to filter out the V_{OUT} ripple. The maximum on time of the controller occurs when V_{COMP} is at the maximum. The Ct capacitor is sized to ensure that the required on time is reached at maximum output power and the minimum input voltage condition.

The minimum Ct value is calculated as below:

$$Ct_{(min)} = \frac{2 \times P_{OUT} \times L \times I_{charge}}{EFF \times V_{AC}^{2} \times V_{Ct(max)}}$$

Current Detection Block

The current detection circuit is composed of zero current detection and over-current detection.

The inductor current is converted into a voltage by inserting a ground reference resistor (R_{CS}) series with the input diode bridge and the input filtering capacitor. Therefore, a negative voltage proportional to the inductor current is built:

$$V_{CS} = -R_{CS} \times I_{L}$$

where,
L is the inductor current;
R_{CS} is the current sense resistor;
V_{CS} is the measured voltage.

Zero Current Detection

The zero current detection function guarantees that the MOSFET can not turn on as long as the inductor current has not reached zero.

The negative signal V_{CS} is applied to the current sense at pin 5. The pin 5 voltage is compared to the -15mV threshold so that as long as V_{CS} is lower than this threshold, the current sense comparator resets the PWM latch to force the gate drive signal low state. Consequently, it is not possible to turn on the power MOSFET until the inductor current is measured smaller than ($15mV/R_{CS}$), nearly at zero.

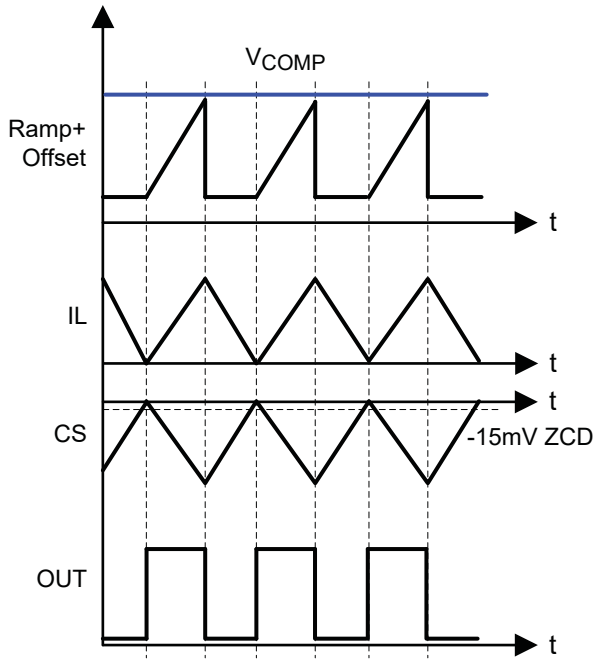


Figure 4. Switching and Current Sense Operation

Over-Current Protection

The over-current detection protective circuit detects the inductor current and protects the power MOSFET by turning off the output driver when it becomes higher than the set current level. With the over-current detection, the voltage across the current detection resistance R_{CS} connected to the GND is fed to the CS pin. If the CS pin voltage compared by the over-current detection comparator becomes lower than -0.7V, it is then regarded as over-current state; therefore, the feed-forward of the output driver is reset to turn off the power MOSFET.

Restart Timer

AOZ7111 utilizes self-oscillation instead of the oscillator with fixed frequency. In steady operation, it turns on the MOSFET with a signal from the zero current detector.

In startup or light load conditions, a trigger signal is required for starting up or stable operation. When the output of the IC continues turn-off (150µs or more), the restart trigger signal is automatically generated.

Maximum Switching Frequency Limit

Because the MOSFET turn-on depends on the CS input, switching frequency may increase to higher than several MHz due to the mis-triggering or noise on the nearby CS pin. If the switching frequency is higher than needed for critical conduction mode, it will enter CCM. In CCM, inductor current can be raised very high, which may exceed the current rating of the power switch or diode. This can seriously damage the power switch and burn it down. To avoid this, the maximum switching frequency limitation is embedded. If the ZCD signal is applied again within 2.9µs after the previous edge of gate signal, this signal is ignored and AOZ7111 waits for another ZCD signal.

Overvoltage Protection (OVP)

It is critical that over voltage protection (OVP) prevents the output voltage exceeding the ratings of PFC stage components. Over-voltage protection (OVP) is embedded by the information at the INV pin. That information comes from the output through the voltage dividing resistors. AOZ7111 has dynamic OVP function to narrow the on time when the INV voltage is higher than 2.575V. When the voltage further rises and exceeds the comparator reference voltage of static OVP (2.685V), the OVP comparator shuts down the output drive pulse. The OVP logic includes hysteresis to ensure that output voltage has sufficient time to discharge before the AOZ7111 driver recovery and also to ensure noise immunity.

Additional OVP detection

Over-voltage protection (OVP) is embedded by the information at the INV pin. That information comes from the output through the voltage dividing resistors. When the upper divider resistor gets damaged and resistance becomes too high the output electrolytic capacitor may explode. To prevent such a catastrophe the additional OVP pin is assigned to double check output voltage.

When the second OVP triggers, switching can be recovered only when the V_{CC} supply voltage falls below V_{STOP} and builds up higher than UVLO again.

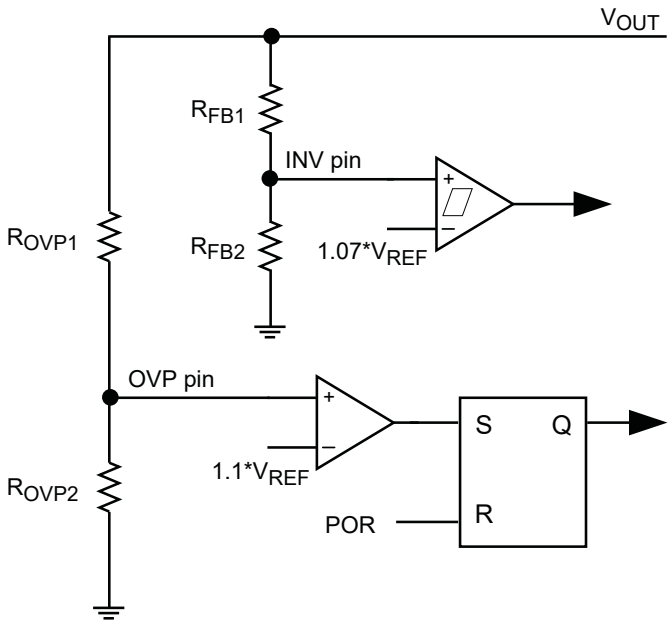


Figure 5. OVP Circuitry Around INV and OVP Pin

AC Input Fault Detection

AOZ7111 does not require an AC input voltage sensing, nor does it need the auxiliary winding with minus current detection. In general, the V_{CC} of PFC controller is supplied by a system standby power supply, a mismatch may occur in a worst case scenario. A worst case scenario could be AC input chattering: the electric AC power source is suddenly absent for two or three additional AC line cycles, V_{CC} is still higher than UVLO (V_{STOP}) during this time, so the voltage control loop tries to compensate for the V_{OUT} drop and V_{COMP} will increase until it reaches its maximum clamp level. During the AC input recovery, high comp leads to very high switching current and severe stress is put on both the MOSFET and boost diode. To ensure that the system is more robust and reliable, AOZ7111 has a unique AC input fault detection circuit to protect against this type of scenario. If the AC input voltage is absent two or three additional cycles, internal soft-start is reset and waits for the AC input recovery again. During the AC input recovery, soft-start manages turn-on time allowing the switching current to increase smoothly.

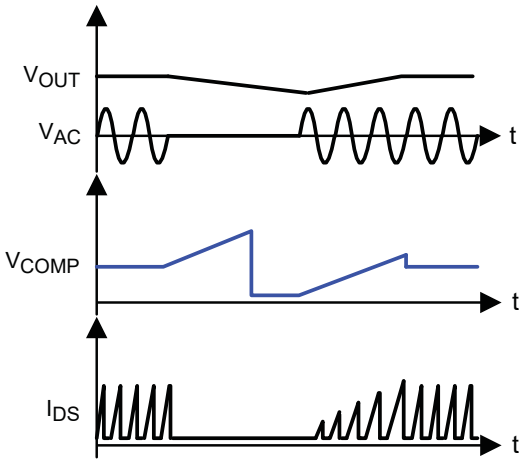


Figure 6. Operation with AC Input Fault Detection

Under Voltage Lock Out (UVLO)

UVLO function is used to prevent controller malfunction when V_{CC} supply voltage drops. When V_{CC} supply voltage reaches 12V (typ), the internal block of the IC is enabled and starts operation. When V_{CC} supply voltage drops below 9.5V (typ), most of the internal circuit is disabled to reduce the IC current consumption.

Under Voltage Protection (UVP)

AOZ7111 detects the under voltage fault if V_{INV} is less than V_{EN_INV}. The UVP comparator disables the operation when $V_{INV\ is}$ less than 0.5V and there is 55mV hysteresis. An external small-signal MOSFET can be used to disables the IC. During disable mode, the current consumption of the IC decreases to 60µA or less.

Application Information

Alpha and Omega Semiconductor provides an EXCEL based design tool, an application note and a demonstration board to help the design of AOZ7111 and reduce the R&D cycle time. All the tools can be download from: www.aosmd.com.

PCB Layout Guide

The following are good PCB layout guideline for a PFC stage:

1. To keep the IC GND pin as clean as possible, the power stage ground and the signal ground must be separated.

2. The PFC MOSFET gate drive loop path should be minimized.

3. Minimize the trace length to INV pin. Since the feedback node is high impedance the trace from the output resistor divider to INV pin should be as short as possible.

4. Switching current sense (CS pin) is very important for the stable operation of PFC stage. Normally, a RC filter is recommended to reduce the noise applied to the CS pin.

5. The V_{CC} decoupling capacitor C_{VCC} need to be placed close to IC V_{CC} and GND pin as much as possible.

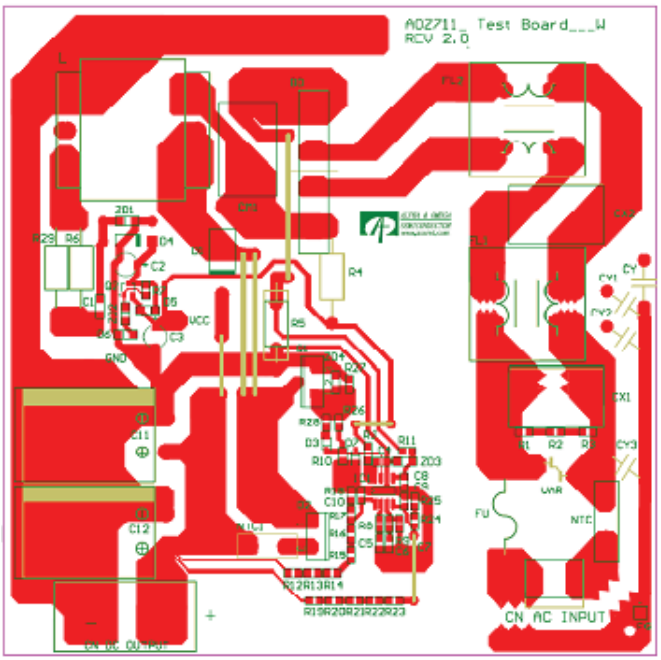
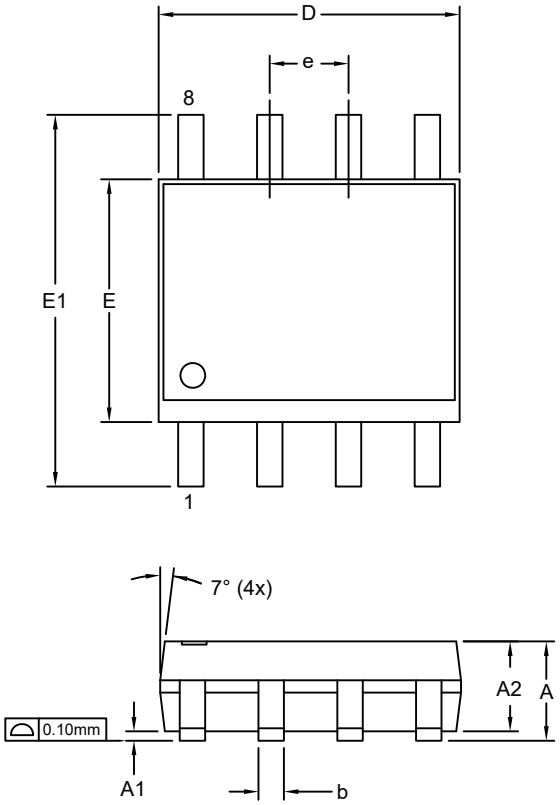
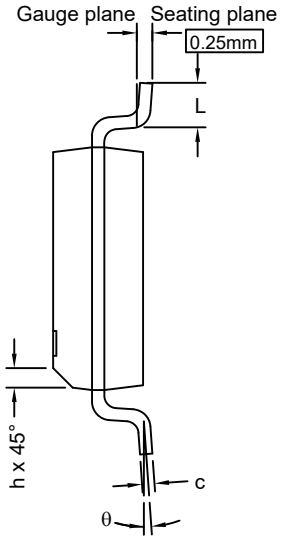


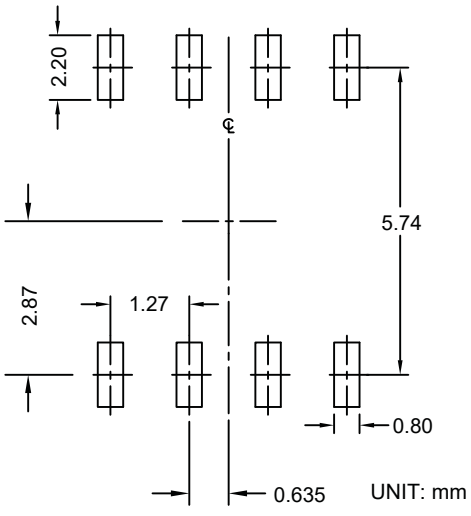
Figure 7. Recommended PCB Layout

Package Dimensions, SO-8L





RECOMMENDED LAND PATTERN



Dimensions in millimeters

Symbols	Min.	Nom.	Max.
A	1.35	1.65	1.75
A1	0.10	—	0.25
A2	1.25	1.50	1.65
b	0.31	—	0.51
c	0.17	—	0.25
D	4.80	4.90	5.00
E	3.80	3.90	4.00
e	1.27 BSC		
E1	5.80	6.00	6.20
h	0.25	—	0.50
L	0.40	—	1.27
θ	0°	—	8°

Dimensions in inches

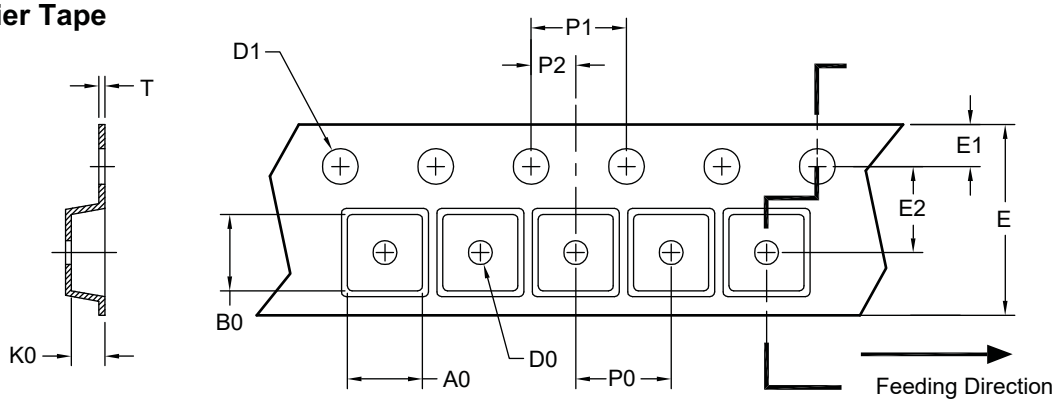
Symbols	Min.	Nom.	Max.
A	0.053	0.065	0.069
A1	0.004	—	0.010
A2	0.049	0.059	0.065
b	0.012	—	0.020
c	0.007	—	0.010
D	0.189	0.193	0.197
E	0.150	0.154	0.157
e	0.050 BSC		
E1	0.228	0.236	0.244
h	0.010	—	0.020
L	0.016	—	0.050
θ	0°	—	8°

Notes:

1. All dimensions are in millimeters.
2. Dimensions are inclusive of plating.
3. Package body size exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 6 mils each.
4. Dimension L is measured in gauge plane.
5. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.

Tape and Reel Dimensions, SO-8L

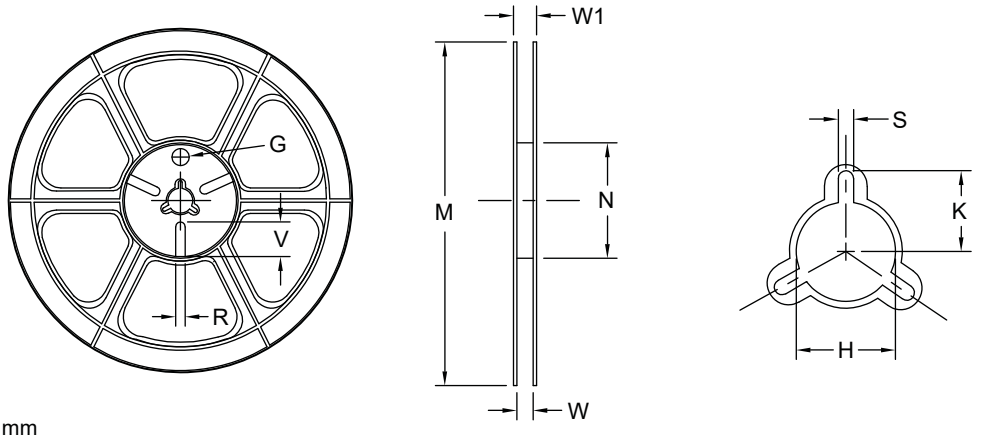
Carrier Tape



UNIT: mm

Package	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
SO-8 (12mm)	6.40 ±0.10	5.20 ±0.10	2.10 ±0.10	1.60 ±0.10	1.50 ±0.10	12.00 ±0.10	1.75 ±0.10	5.50 ±0.10	8.00 ±0.10	4.00 ±0.10	2.00 ±0.10	0.25 ±0.10

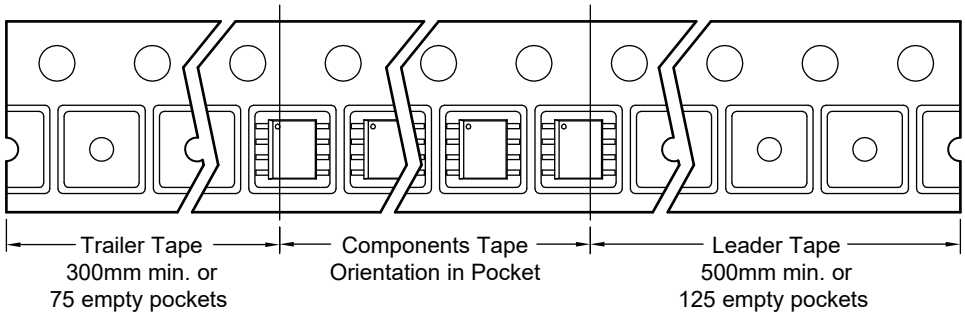
Reel



UNIT: mm

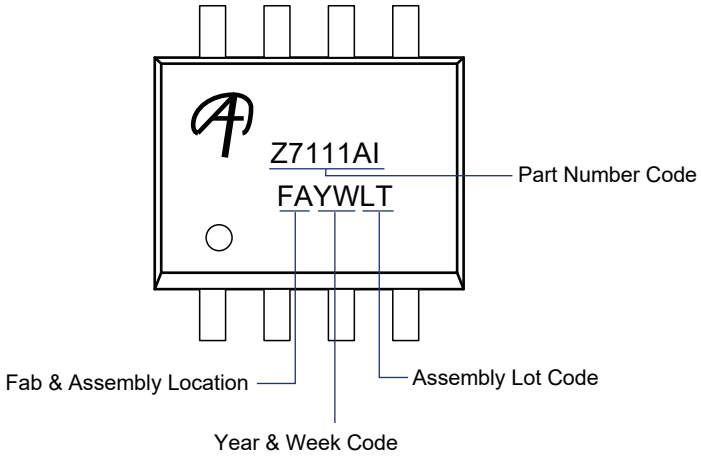
Tape Size	Reel Size	M	N	W	W1	H	K	S	G	R	V
12mm	ø330	ø330.00 ±0.50	ø97.00 ±0.10	13.00 ±0.30	17.40 ±1.00	ø13.00 +0.50/-0.20	10.60	2.00 ±0.50	—	—	—

Leader/Trailer and Orientation



Part Marking

AOZ7111AI
(SO-8)



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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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