AOZ8000

Ultra-Low Capacitance TVS Diode Array

General Description

The AOZ8000 is a transient voltage suppressor array designed to protect high speed data lines from ESD and lightning.

This device incorporates eight surge rated, low capacitance steering diodes and a TVS in a single package. During transient conditions, the steering diodes direct the transient to either the positive side of the power supply line or to ground. They may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4. The TVS diodes provide effective suppression of ESD voltages: ±15kV (air discharge) and ±8kV (contact discharge).

The AOZ8000 comes in SOT-23, DFN-6, and SC-70 packages. They are compatible with both lead free and SnPb assembly techniques. The small size, low capacitance and high ESD protection makes it ideal for protecting high speed video and data communication interfaces.

Features

- ESD protection for high-speed data lines:
  - IEC 61000-4-2, level 4 (ESD) immunity test
  - ±15kV (air discharge) and ±8kV (contact discharge)
  - IEC 61000-4-5 (Lightning) 5A (8/20µs)
  - Human Body Model (HBM) ±15kV
- Small package saves board space
- Low insertion loss
- Protects four I/O lines
- Low capacitance between I/O lines: 0.9pF
- Low clamping voltage
- Low operating voltage: 5.0V

Applications

- USB 2.0 power and data line protection
- Video graphics cards
- Monitors and flat panel displays
- Digital Video Interface (DVI)
- 10/100/1000 Ethernet
- Notebook computers

Green Product

Typical Application

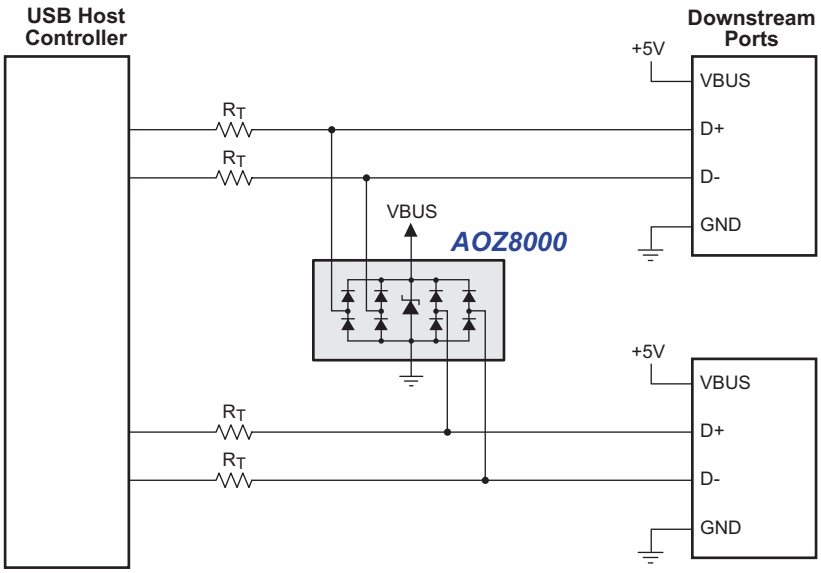


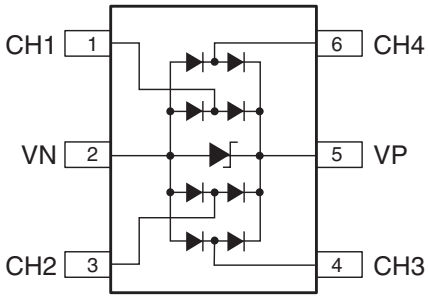
Figure 1. 2 USB High Speed Ports

Ordering Information

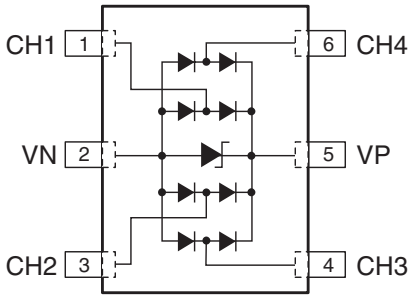
Part Number	Package	Environmental
AOZ8000HIL	SC-70-6	RoHS Compliant Green Prodcut
AOZ8000DIL	DFN-6	
AOZ8000CIL	SOT23-6	

AOS Green Products (with "L" suffix) use reduced levels of Halogens, and are also RoHS compliant.
Please visit www.aosmd.com/web/quality/rohs_compliant.jsp for additional information.

Pin Configuration



SOT23-6/SC-70-6
(Top View)



DFN-6
(Top View)

Absolute Maximum Ratings

Exceeding the Absolute Maximum ratings may damage the device.

Parameter	Rating
VP – VN	6V
Peak Pulse Current (I_{PP}), t_P = 8/20µs	5A
Peak Power Dissipation (8 x 20µs@ 25°C) SC-70 DFN SOT-23	 60W 70W 60W
Storage Temperature (T_S)	-65°C to +150°C
ESD Rating per IEC61000-4-2, Contact(1)	±8kV
ESD Rating per IEC61000-4-2, Air(1)	±15kV
ESD Rating per Human Body Model(2)	±15kV

Notes:
1. IEC 61000-4-2 discharge with $C_{Discharge}$ = 150pF, $R_{Discharge}$ = 330Ω.
2. Human Body Discharge per MIL-STD-883, Method 3015 $C_{Discharge}$ = 100pF, $R_{Discharge}$ = 1.5kΩ.

Maximum Operating Ratings

Parameter	Rating
Junction Temperature (T_J)	-55°C to +125°C

Electrical Characteristics

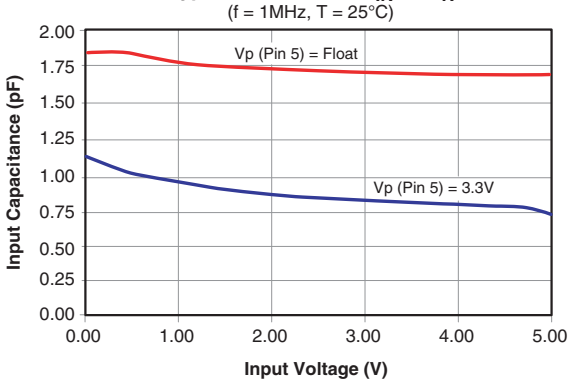
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{RWM}	Reverse Working Voltage	Between pin 5 and 2[4]			5.5	V
V_{BR}	Reverse Breakdown Voltage	I_T = 1mA, between pins 5 and 2[5]	6.6			V
I_R	Reverse Leakage Current	V_{RWM} = 5V, between pins 5 and 2			0.1	µA
V_F	Diode Forward Voltage	I_F = 15mA	0.70	0.85	1	V
V_{CL}	Channel Clamp Voltage Positive Transients Negative Transient	I_{PP} = 1A, tp = 100ns, any I/O pin to Ground[3][6][8]			 10.0 -3.0	 V V
	Channel Clamp Voltage Positive Transients Negative Transient	I_{PP} = 5A, tp = 100ns, any I/O pin to Ground[3][6][8]			 11 -6.0	 V V
	Channel Clamp Voltage Positive Transients Negative Transient	I_{PP} = 12A, tp = 100ns, any I/O pin to Ground[3][6][8]			 15.0 -10.0	 V V
C_j	Junction Capacitance	V_R = 0V, f = 1MHz, any I/O pin to Ground[3][6]		1.85	1.94	pF
		V_R = 0V, f = 1MHz, between I/O pins[3][6]		0.9	0.94	pF
		V_R = 0V, f = 1MHz, any I/O pin to Ground[3][7]		1.0	1.17	pF
ΔC_j	Channel Input Capacitance Matching	V_R = 0V, f = 1MHz, between I/O pins[3][6]			0.03	pF

Notes:

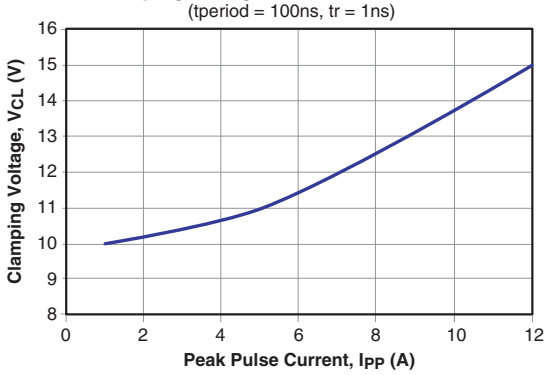
3. These specifications are guaranteed by design.
4. The working peak reverse voltage, V_{RWM}, should be equal to or greater than the DC or continuous peak operating voltage level.
5. V_{BR} is measured at the pulse test current I_T.
6. Measurements performed with no external capacitor on V_P (pin 5 floating).
7. Measurements performed with V_P biased to 3.3 Volts (pin 5 @ 3.3V).
8. Measurements performed using a 100ns Transmission Line Pulse (TLP) system.

Typical Performance Characteristics

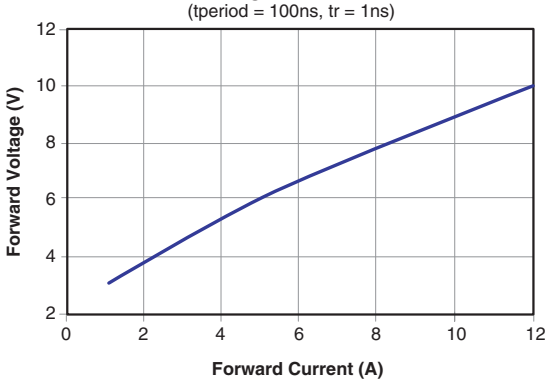
Typical Variation of C_{IN} vs V_R
(f = 1MHz, T = 25°C)



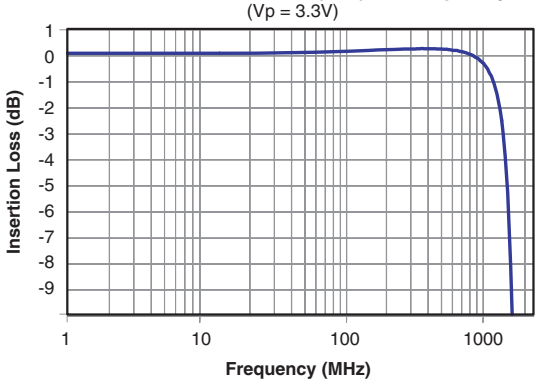
Clamping Voltage vs. Peak Pulse Current
(tperiod = 100ns, tr = 1ns)



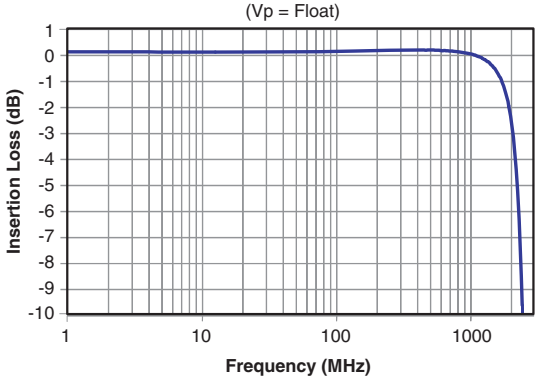
Forward Voltage vs. Forward Current
(tperiod = 100ns, tr = 1ns)



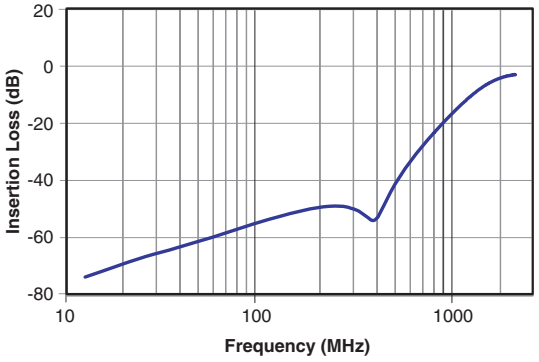
I/O – Gnd Insertion Loss (S21) vs. Frequency
(Vp = 3.3V)



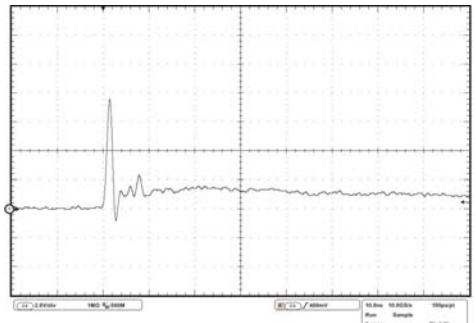
I/O – I/O Insertion Loss (S21) vs. Frequency
(Vp = Float)



Analog Crosstalk (I/O–I/O) vs. Frequency



ESD Clamping
8kV Contact per IEC61000-4-2



Note: Data was taken with a 10X attenuator

Application Information

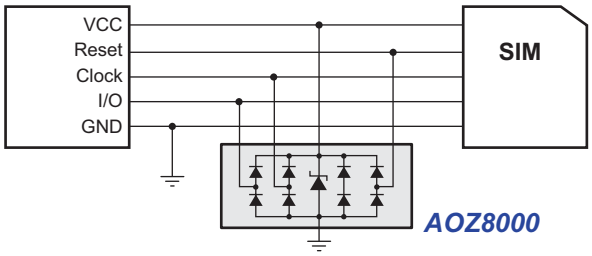
The AOZ8000 TVS is design to protect four data lines from fast damaging transient over-voltage by clamping it to a reference. When the transient on a protected data line exceed the reference voltage the steering diode is forward bias thus, conducting the harmful ESD transient away from the sensitive circuitry under protection.

PCB Layout Guidelines

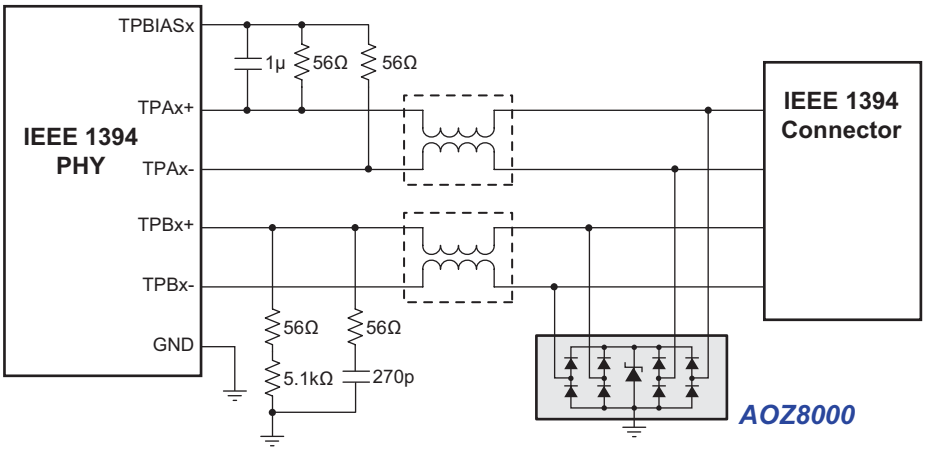
Printed circuit board layout is the key to achieving the highest level of surge immunity on power and data lines. The location of the protection devices on the PCB is the simplest and most important design rule to follow. The AOZ8000 devices should be located as close as possible to the noise source. The placement of the AOZ8000 devices should be used on all data and power lines that enter or exit the PCB at the I/O connector. In most systems, surge pulses occur on data and power lines that enter the PCB through the I/O connector. Placing the AOZ8000 devices as close as possible to the noise source ensures that a surge voltage will be clamped before the pulse can be coupled into adjacent PCB traces. In addition, the PCB should use the shortest possible traces. A short trace length equates to low impedance, which ensures that the surge energy will be dissipated by the AOZ8000 device. Long signal traces will act as antennas to receive energy from fields that are produced by the ESD pulse. By keeping line lengths as short as possible, the efficiency of the line to act as an antenna for ESD related fields is reduced. Minimize interconnecting line lengths by placing devices with the most interconnect as close together as possible. The protection circuits should shunt the surge voltage to either the reference or chassis ground. Shunting the surge voltage directly to the IC's signal ground can cause ground bounce. The clamping performance of TVS diodes on a single ground PCB can be improved by minimizing the impedance with relatively short and wide ground traces. The PCB layout and IC package parasitic inductances can cause significant overshoot to the TVS's clamping voltage. The inductance of the PCB can be reduced by using short trace lengths and multiple layers with separate ground and power planes. One effective method to minimize loop problems is to incorporate a ground plane in the PCB design. The AOZ8000 ultra-low capacitance TVS is designed to protect four high speed data transmission lines from transient over-voltages by clamping them to a fixed reference. The low inductance and construction minimizes voltage overshoot during high current surges. When the voltage on the protected line exceeds the reference voltage the internal steering diodes are forward biased, conducting the transient current away from the sensitive circuitry.

Good circuit board layout is critical for the suppression of ESD induced transients. The following guidelines are recommended:

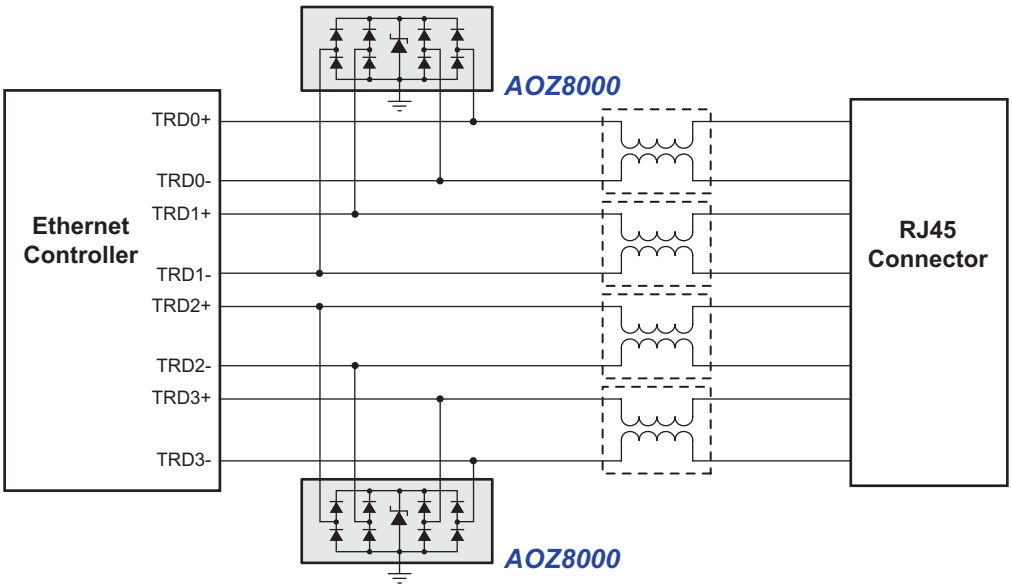
1. Place the TVS near the IO terminals or connectors to restrict transient coupling.
2. Fill unused portions of the PCB with ground plane.
3. Minimize the path length between the TVS and the protected line.
4. Minimize all conductive loops including power and ground loops.
5. The ESD transient return path to ground should be kept as short as possible.
6. Never run critical signals near board edges.
7. Use ground planes whenever possible.
8. Avoid running critical signal traces (clocks, resets, etc.) near PCB edges.
9. Separate chassis ground traces from components and signal traces by at least 4mm.
10. Keep the chassis ground trace length-to-width ratio <5:1 to minimize inductance.
11. Protect all external connections with TVS diodes.



SIM Card Port Connection

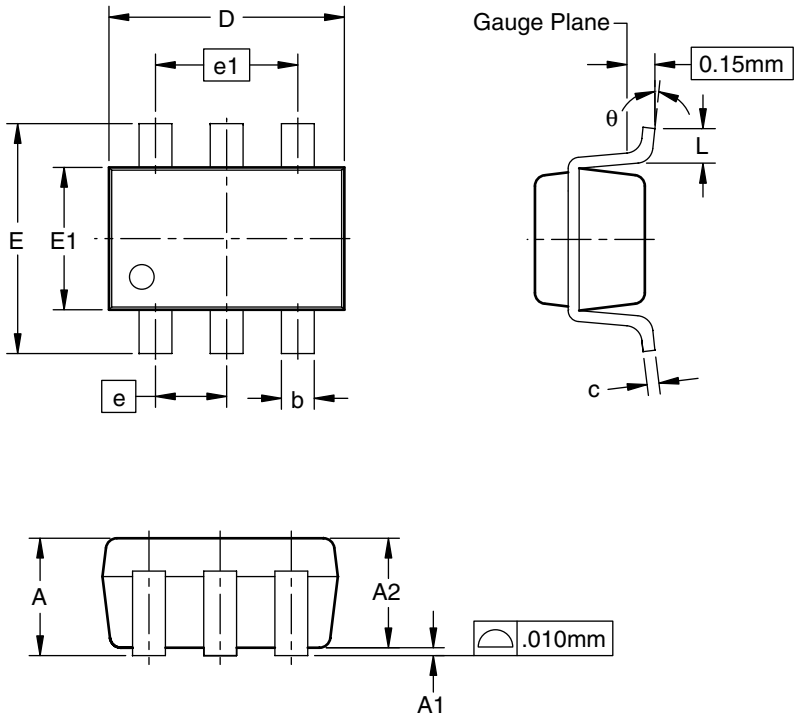


IEEE1394 Port Connection

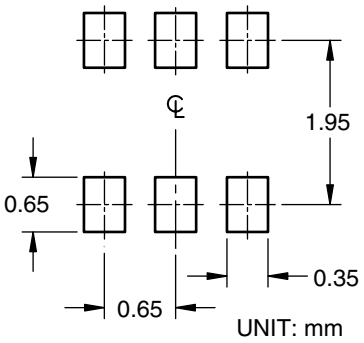


10/100 Ethernet Port Connection

Package Dimensions, SC70-6L



RECOMMENDED LAND PATTERN



Dimensions in millimeters

Symbols	Min.	Nom.	Max.
A		—	1.10
A1	0.00	—	0.10
A2	0.7	0.9	1.00
b	0.15	—	0.30
c	0.08	—	0.22
D	1.85	2.10	2.15
E	1.80	2.30	2.40
e	0.65 BSC		
e1	1.30 BSC		
E1	1.1	1.30	1.4
L	0.26	0.36	0.46
θ	0°	4°	8°

Dimensions in inches

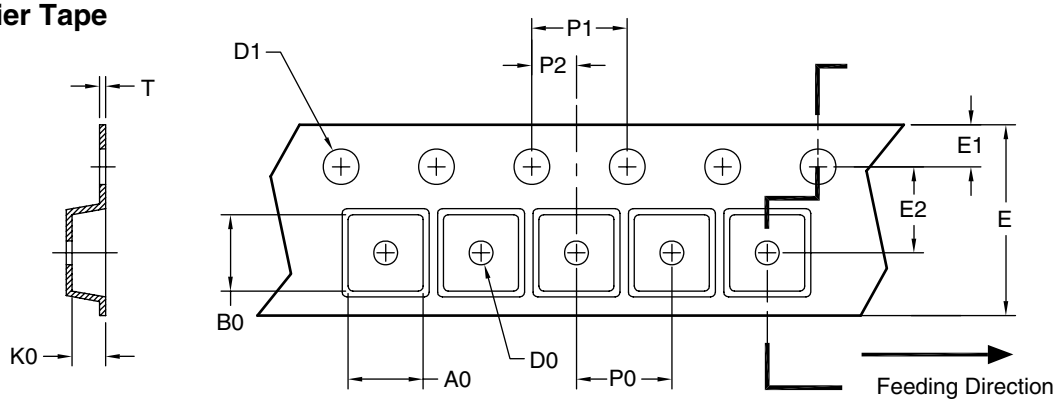
Symbols	Min.	Nom.	Max.
A		—	0.043
A1	0.00	—	0.004
A2	0.028	0.035	0.039
b	0.006	—	0.012
c	0.003	—	0.009
D	0.073	0.083	0.085
E	0.071	0.091	0.094
e	0.026 BSC		
e1	0.051 BSC		
E1	0.043	0.051	0.055
L	0.010	0.014	0.018
θ	0°	4°	8°

Notes:

1. All dimensions are in millimeters.
2. Dimensions are inclusive of plating
3. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 3 mils.
4. Die is facing up for mold and facing down for trim/form; i.e., reverse trim/form.
5. Dimension L is measured in gauge plane.
6. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.

Tape and Reel Dimensions, SC70-6L

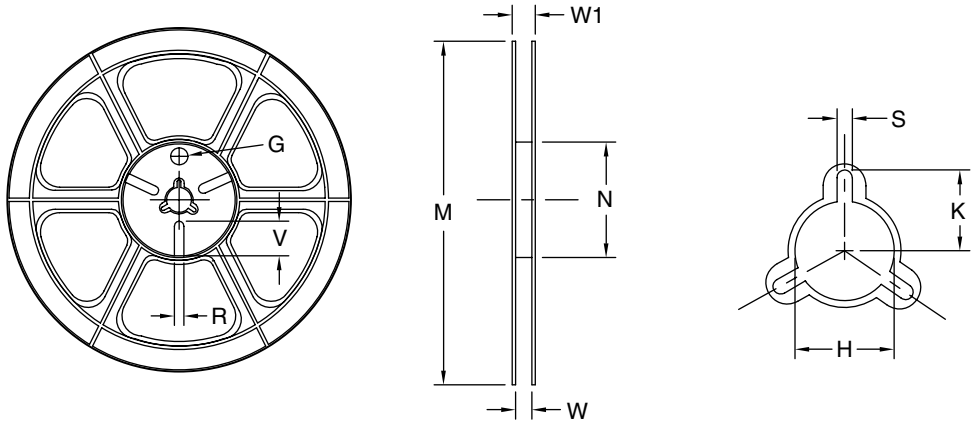
Carrier Tape



UNIT: mm

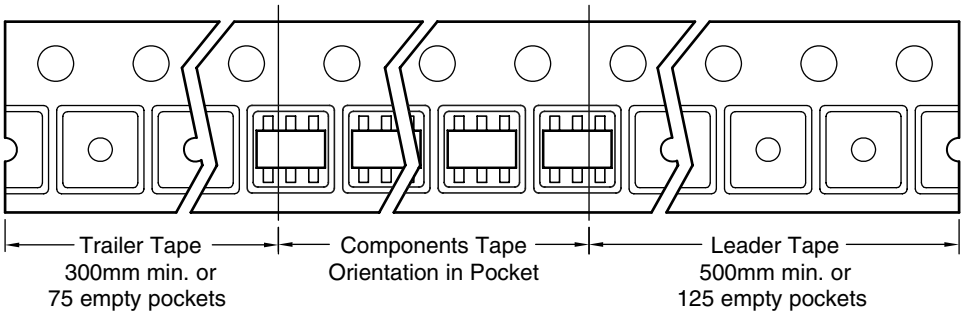
Package	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
SC-70, 6L (8mm)	2.40 ±0.10	2.40 ±0.10	1.19 ±0.10	1.00 Min.	1.55 ±0.05	8.00 ±0.30	1.75 ±0.10	3.50 ±0.05	4.00 ±0.10	4.00 ±0.10	2.00 ±0.05	0.25 ±0.05

Reel

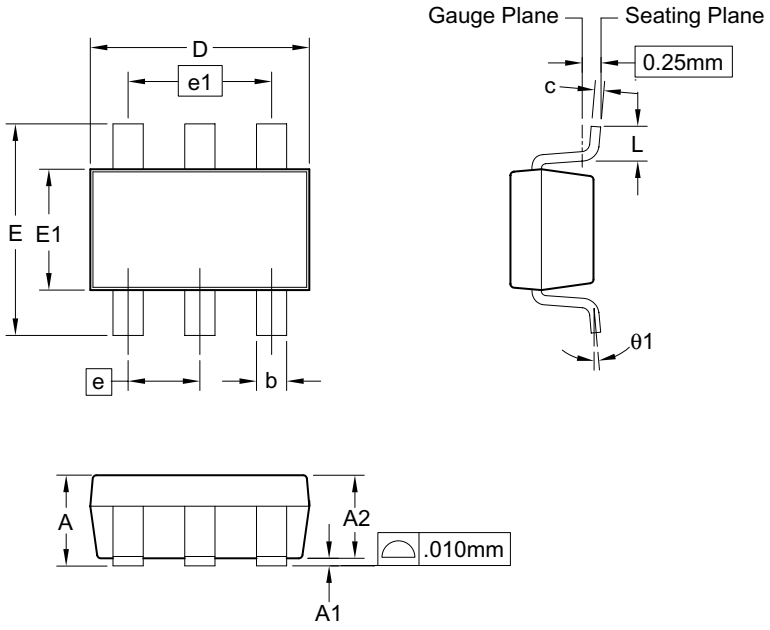


Tape Size	Reel Size	M	N	W	W1	H	K	S	G	R	V
8mm	ø180	ø180.00 ±0.50	ø60.50	9.00 ±0.30	11.40 ±1.00	ø13.00 +0.50/-0.20	10.60	2.00 ±0.50	ø9.00	5.00	18.00

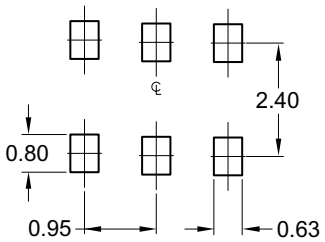
Leader/Trailer and Orientation



Package Dimensions, SOT23-6L



RECOMMENDED LAND PATTERN



UNIT: mm

Dimensions in millimeters

Symbols	Min.	Nom.	Max.
A	0.90	—	1.25
A1	0.00	—	0.15
A2	0.80	1.10	1.20
b	0.30	0.40	0.50
c	0.08	0.13	0.20
D	2.70	2.90	3.10
E	2.50	2.80	3.10
E1	1.50	1.60	1.70
e	0.95 BSC		
e1	1.90 BSC		
L	0.30	—	0.60
θ1	0°	—	8°

Dimensions in inches

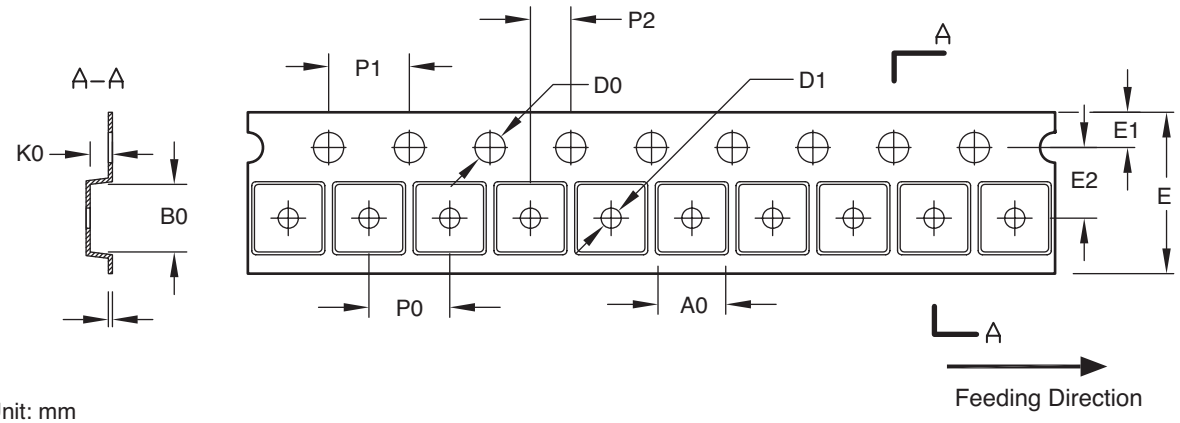
Symbols	Min.	Nom.	Max.
A	0.035	—	0.049
A1	0.00	—	0.006
A2	0.031	0.043	0.047
b	0.012	0.016	0.020
c	0.003	0.005	0.008
D	0.106	0.114	0.122
E	0.098	0.110	0.122
E1	0.059	0.063	0.067
e	0.037 BSC		
e1	0.075 BSC		
L	0.012	—	0.024
θ1	0°	—	8°

Notes:

1. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 5 mils each.
2. Dimension “L” is measured in gauge plane.
3. Tolerance ±0.100mm (4 mil) unless otherwise specified.
4. Followed from JEDEC MO-178C & MO-193C.
6. Controlling dimension is millimeter. Converted inch dimensions are not necessarily exact.

Tape and Reel Dimensions, SOT23-5&6L

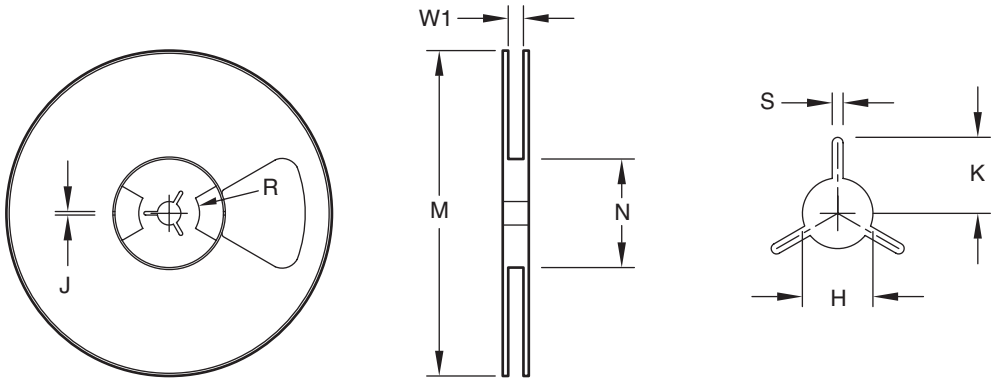
Tape



Unit: mm

Package	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
SOT23-5/6L LP	3.15 ±0.10	3.20 ±0.10	1.40 ±0.10	1.50 ±0.05	1.00 +0.10 / -0	8.00 ±0.30	1.75 ±0.10	3.50 ±0.05	4.00 ±0.10	4.00 ±0.10	2.00 ±0.05	0.23 ±0.03

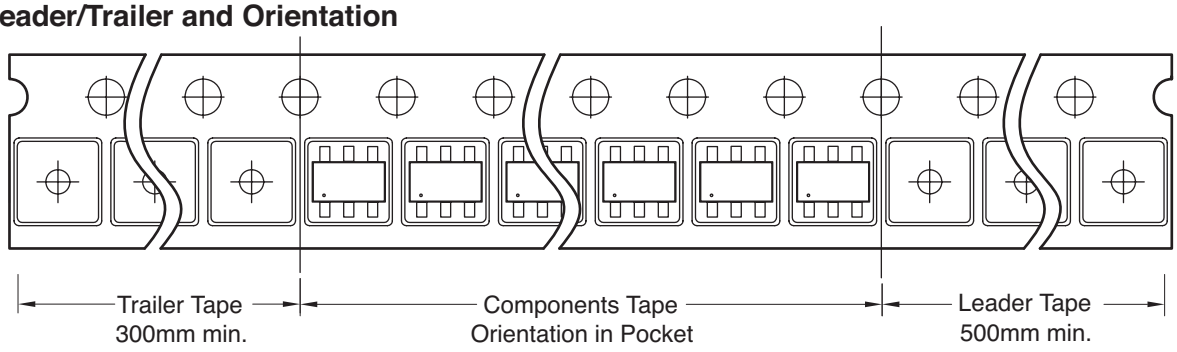
Reel



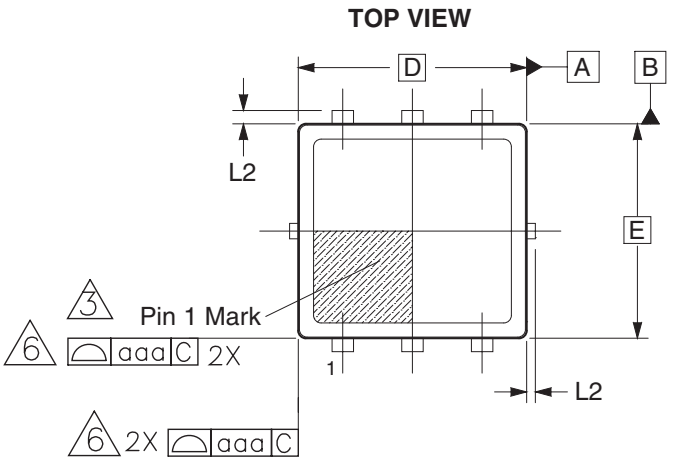
Unit: mm

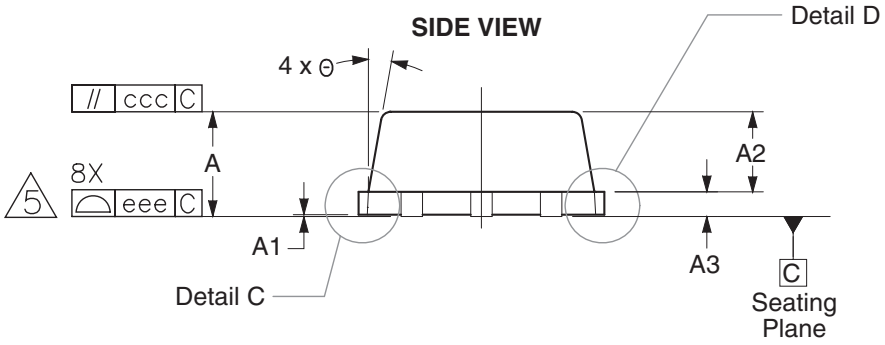
Tape Size	Reel Size	M	N	W1	H	S	K	R	J
8mm	ø177.8	ø177.8 Max.	55.0 Min.	8.4 +1.50 / -0.0	13.0 +0.5 / -0.2	1.5 Min	10.1 Min.	12.7	4.0 ±0.1

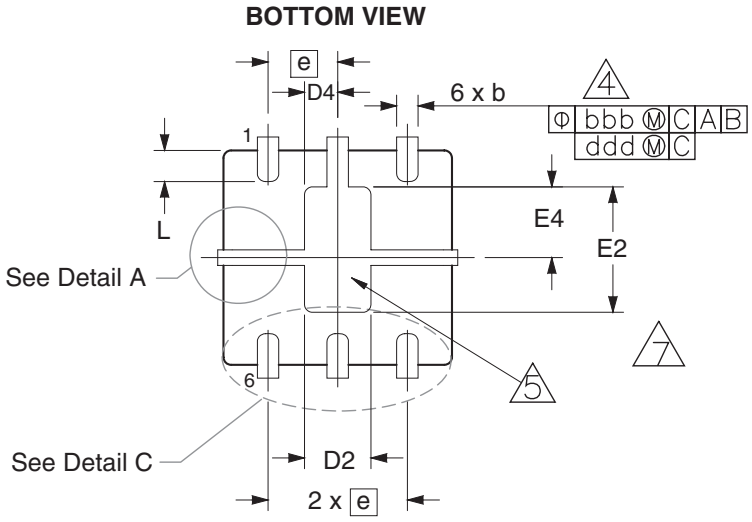
Leader/Trailer and Orientation



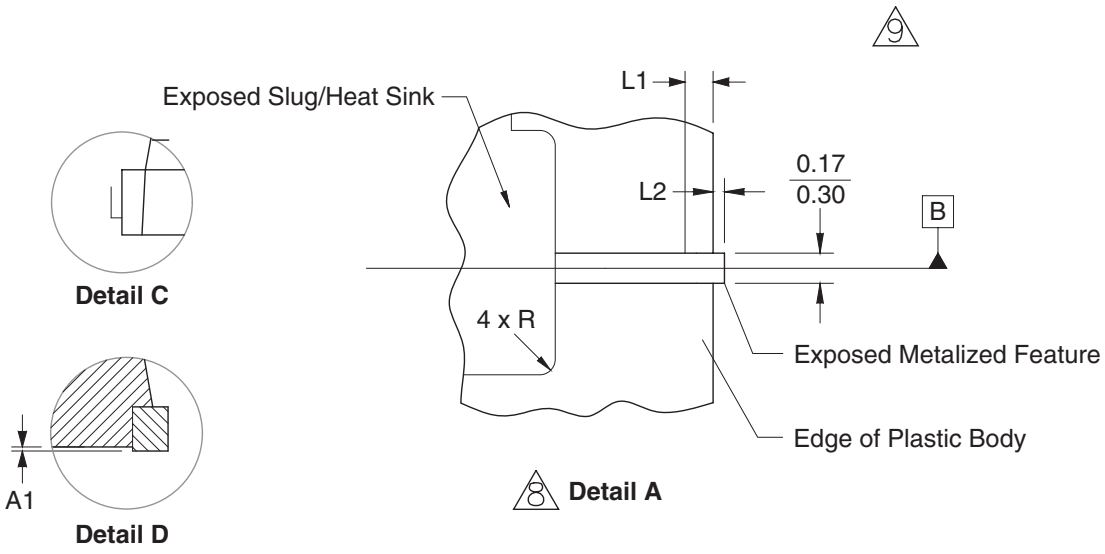
Package Dimensions, DFN 2 x 2 (Page 1 of 3)

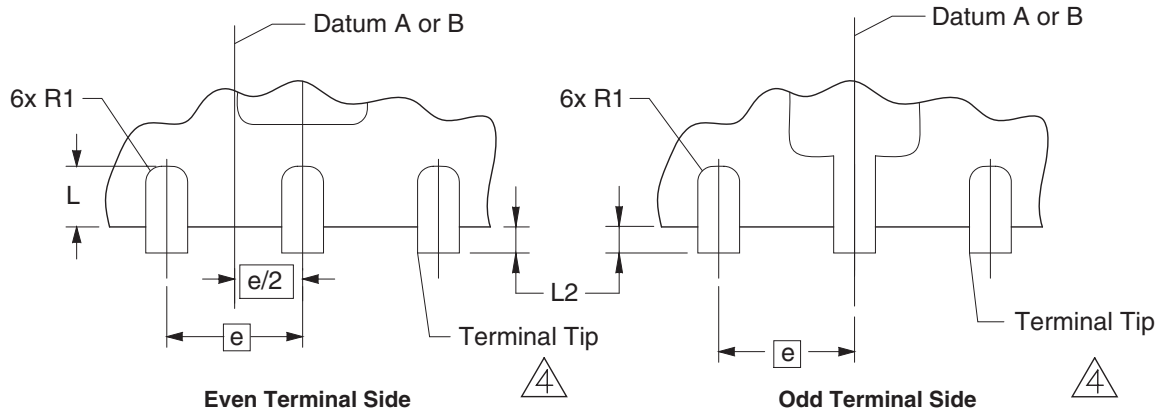






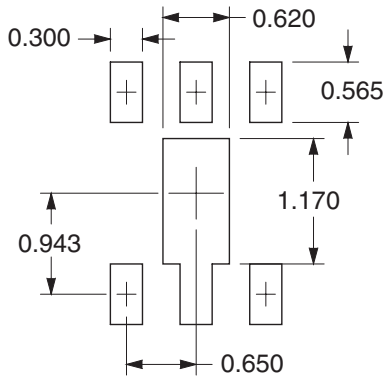
Package Dimensions, DFN 2 x 2 (Page 2 of 3)





Detail B

RECOMMENDED LAND PATTERN



Unit: mm

Package Dimensions, DFN 2 x 2 (Page 3 of 3)

Dimensions in millimeters

Symbols	Min.	Nom.	Max.
A	0.80	0.90	1.00
A1	0.00	0.025	0.05
A2	0.65	0.70	0.75
A3	0.15	0.20	0.25
b	0.18	0.20	0.28
D	2.0 BSC		
E	2.0 BSC		
e	0.65 BSC		
E4	0.56	0.66	0.76
E2	0.84	0.94	1.04
D4	0.21	0.31	0.41
D2	0.52	0.62	0.72
L	0.20	0.29	0.45
L1	—		
L2	—	—	0.125
R	0.075 REF		
R1	0.075 REF		
R2	—		
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
θ	0°	10°	12°

Dimensions in inches

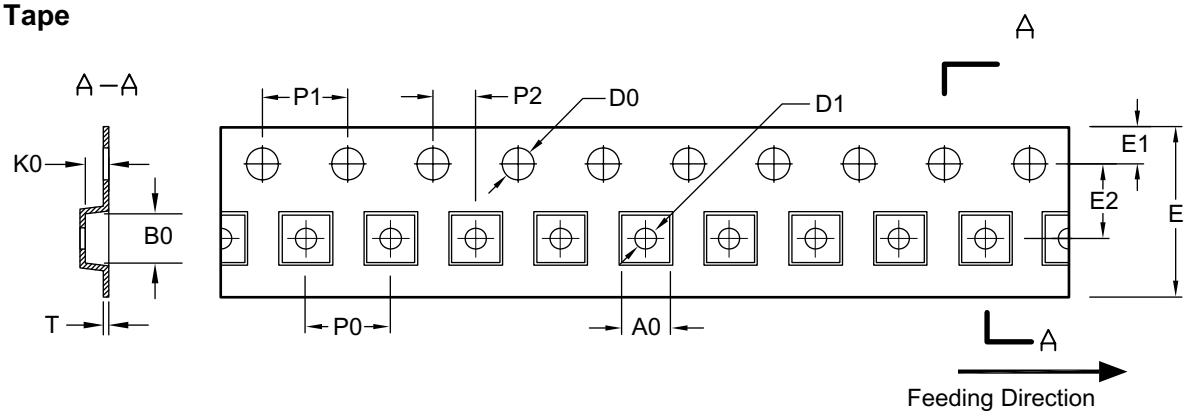
Symbols	Min.	Nom.	Max.
A	0.031	0.035	0.039
A1	0.000	0.001	0.002
A2	0.026	0.028	0.030
A3	0.006	0.008	0.010
b	0.007	0.008	0.011
D	0.079 BSC		
E	0.079 BSC		
e	0.026 BSC		
E4	0.022	0.026	0.030
E2	0.033	0.037	0.041
D4	0.008	0.012	0.016
D2	0.020	0.024	0.028
L	0.008	0.011	0.018
L1	—		
L2	—	—	0.005
R	0.003 REF		
R1	0.003 REF		
R2	—		
aaa	0.004		
bbb	0.004		
ccc	0.004		
ddd	0.002		
eee	0.003		
θ	0°	10°	12°

Notes:

1. Dimensioning and tolerances conform to ASME Y14.5M-1994.
2. All dimensions are in millimeters. All angles are in degrees.
3. The terminal #1 identifier and terminal numbering convention shall conform to JESD 95-1 SPP-012. Details of terminal #1 are optional, but must be located within the zone indicated. The terminal #1 identifier may be a molded, marked, or metalized feature.
4. Dimension b apply to metallized terminal and is measured between 0.15mm and 0.20mm from terminal tip.
5. Coplanarity applies to the exposed heat sink slug as well as the terminal.
6. Profile tolerance (aaa) will be applicable only to the plastic body, and not to the metallized fetures (such as terminal tips and tie bars.) Metallized features may protrude a maximum of L2 from the plastic body profile.
7. Corners will be sharp unless otherwise specified with radius dimensions.
8. This feature applies to both ends of the package.
9. If L1 max. is not called out, the metalized feature will extend to the exposed pad. Thus, the 0.17mm gap does not apply.

Tape and Reel Dimensions, DFN 2 x 2

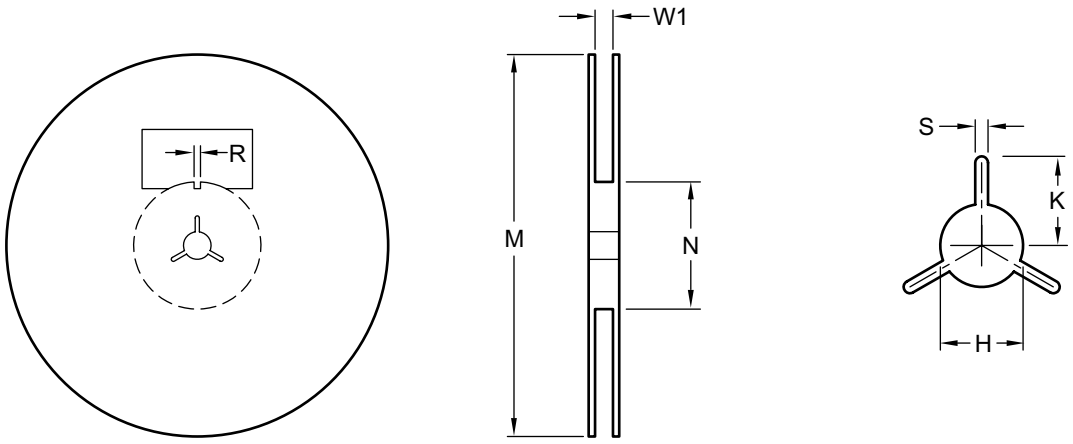
Carrier Tape



UNIT: mm

Package	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
DFN 2x2	2.25 ±0.05	2.25 ±0.05	1.00 ±0.05	1.50 +0.10/-0	1.00 +0.25/-0	8.00 +0.30/-0.10	1.75 ±0.10	3.50 ±0.05	4.00 ±0.10	4.00 ±0.10	2.00 ±0.10	0.254 ±0.02

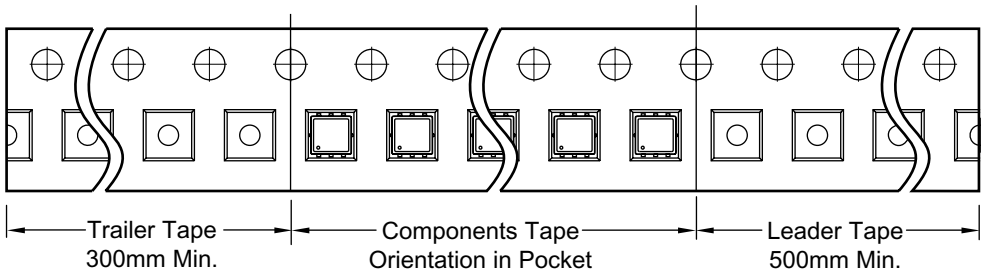
Reel



UNIT: mm

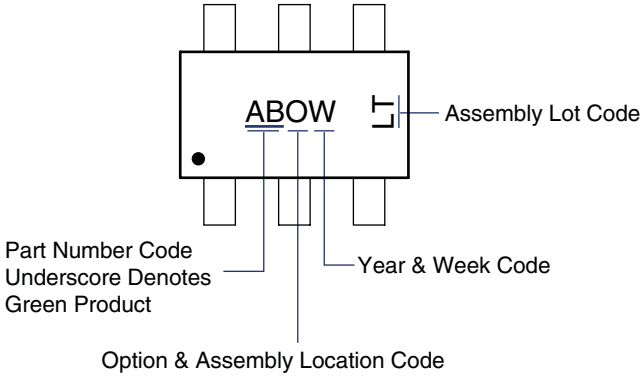
Tape Size	Reel Size	M	N	W1	H	S	K	R
8mm	ø180	ø180.00 ±0.50	60.0 ±0.50	8.4 +1.5/-0.0	13.0 ±0.20	1.5 Min.	13.5 Min.	3.0 ±0.50

Leader / Trailer & Orientation

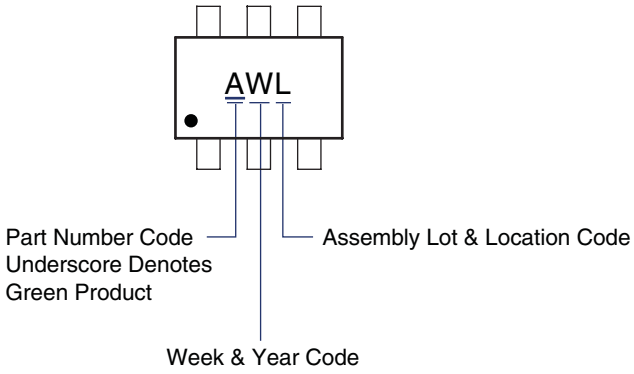


Part Marking

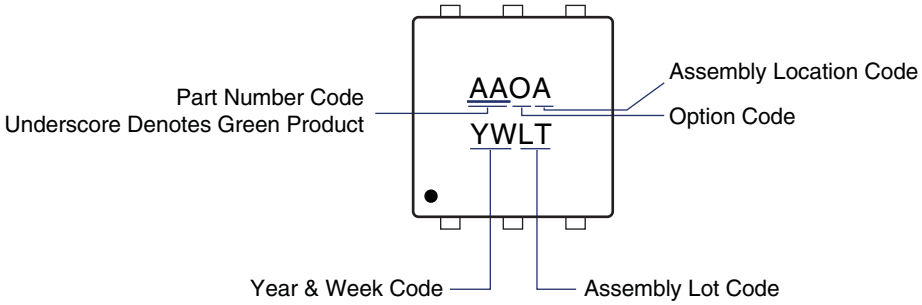
AOZ8000CIL
(SOT-23)



AOZ8000HIL
(SC70-6)



AOZ8000DIL
(DFN 2x2)



This datasheet contains preliminary data; supplementary data may be published at a later date.
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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.

2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.