AOZ8001K

Ultra-Low Capacitance TVS Diode Array

General Description

The AOZ8001K is a transient voltage suppressor array designed to protect high speed data lines from ESD and lightning.

This device incorporates four surge rated, low capacitance steering diodes and a TVS in a single package. During transient conditions, the steering diodes direct the transient to either the positive side of the power supply line or to ground. They may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4. The TVS diodes provide effective suppression of ESD voltages: ±15kV (air discharge) and ±8kV (contact discharge).

The AOZ8001K comes in a RoHS compliant SC-89 package and is rated over a -40°C to +85°C ambient temperature range. It is compatible with both lead free and SnPb assembly techniques.

The very small 1.7 x 1.7 x 0.6mm SC-89 package makes it ideal for applications where PCB space is a premium. The SC-89 has a flow through package design for an optimal and user friendly PCB layout design. The small size, low capacitance and high ESD protection makes it ideal for protecting high speed video and data communication interfaces.

Features

- ESD protection for high-speed data lines:
  - IEC 61000-4-2, level 4 (ESD) immunity test
  - ±15kV (air discharge) and ±8kV (contact discharge)
  - IEC 61000-4-5 (Lightning) 5A (8/20µs)
  - Human Body Model (HBM) ±15kV
- Small package saves board space
- Low insertion loss
- Protects four I/O lines
- Low capacitance from IO to Ground: 1.0pF
- Low clamping voltage
- Low operating voltage: 5.0V
- Pb-free device
- Green product

Applications

- USB 2.0 power and data line protection
- Video graphics cards
- Monitors and flat panel displays
- Digital Video Interface (DVI)
- 10/100/1000 Ethernet
- Notebook computers

Typical Application

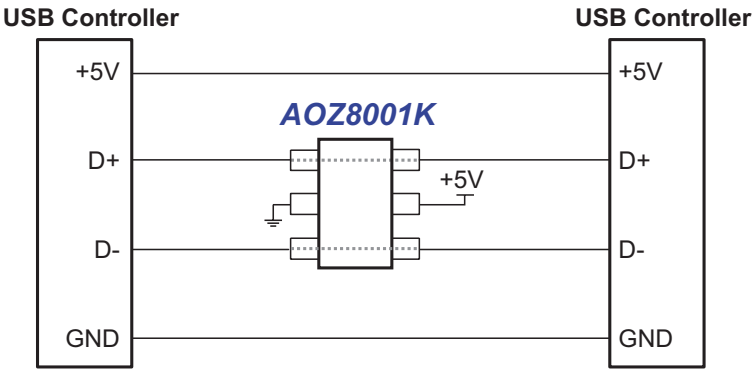


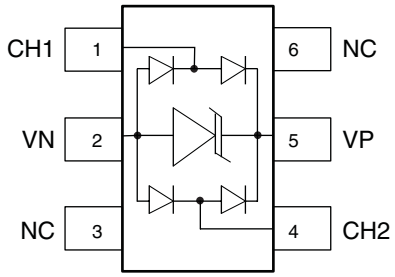
Figure 1. USB 2.0 High Speed Port

Ordering Information

Part Number	Ambient Temperature Range	Package	Environmental
AOZ8001KI	-40°C to +85°C	SC-89	RoHS Compliant
AOZ8001KIL			RoHS Compliant Green Product

All AOS Products are offering in packaging with Pb-free plating and compliant to RoHS standards.
Please visit www.aosmd.com/web/quality/rohs_compliant.jsp for additional information.

Pin Configuration



SC-89
(Top View)

Absolute Maximum Ratings

Exceeding the Absolute Maximum ratings may damage the device.

Parameter	Rating
VP – VN	6V
Peak Pulse Current (I_{PP}), t_P = 8/20µs	5A
Storage Temperature (T_S)	-65°C to +150°C
ESD Rating per IEC61000-4-2, Contact(1)	±8kV
ESD Rating per IEC61000-4-2, Air(1)	±15kV
ESD Rating per Human Body Model(2)	±15kV

Notes:
1. IEC 61000-4-2 discharge with $C_{Discharge}$ = 150pF, $R_{Discharge}$ = 330Ω.
2. Human Body Discharge per MIL-STD-883, Method 3015 $C_{Discharge}$ = 100pF, $R_{Discharge}$ = 1.5kΩ.

Maximum Operating Ratings

Parameter	Rating
Junction Temperature (T_J)	-40°C to +125°C

Electrical Characteristics

T_A = 25°C unless otherwise specified. Specifications in **BOLD** indicate a temperature range of -40°C to +85°C.

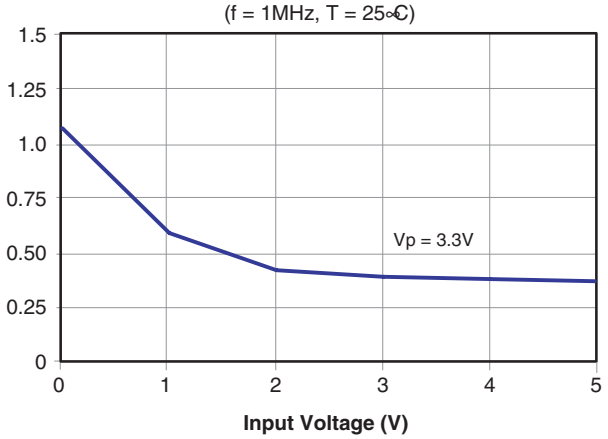
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{RWM}	Reverse Working Voltage	Between pin 5 and 2[3]			5.5	V
V_{BR}	Reverse Breakdown Voltage	I_T = 1mA, between pins 5 and 2[4]	**6.6**			V
I_R	Reverse Leakage Current	V_{RWM} = 5V, between pins 5 and 2			**1.0**	µA
V_F	Diode Forward Voltage	I_F = 15mA	**0.70**	**0.85**	**1**	V
V_{CL}	Channel Clamp Voltage Positive Transients Negative Transient	I_{PP} = 1A, tp = 100ns, any I/O pin to Ground[5][7]			 10.00 -2.00	 V V
	Channel Clamp Voltage Positive Transients Negative Transient	I_{PP} = 5A, tp = 100ns, any I/O pin to Ground[5][7]			 11.00 -5.00	 V V
	Channel Clamp Voltage Positive Transients Negative Transient	I_{PP} = 12A, tp = 100ns, any I/O pin to Ground[5][7]			 14.50 -10.50	 V V
C_j	Junction Capacitance	V_R = 0V, f = 1MHz, between I/O pins[6]		0.1	0.12	pF
		V_R = 0V, f = 1MHz, any I/O pin to Ground[6]		1.0	1.17	pF
ΔC_j	Channel Input Capacitance Matching	V_R = 0V, f = 1MHz, between I/O pins[5]			0.03	pF

Notes:

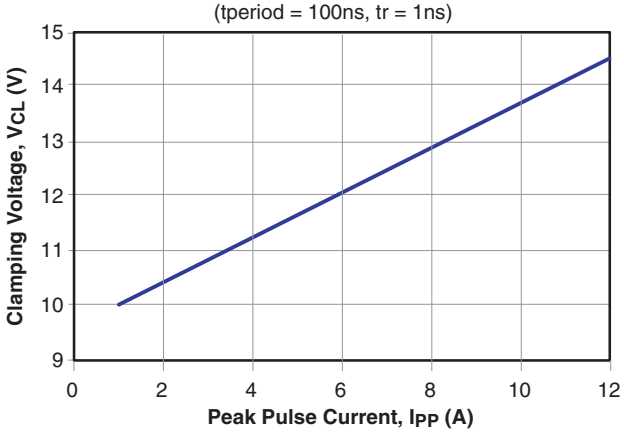
3. The working peak reverse voltage, V_{RWM}, should be equal to or greater than the DC or continuous peak operating voltage level.
4. V_{BR} is measured at the pulse test current I_T.
5. Measurements performed with no external capacitor on V_P (pin 5 floating).
6. Measurements performed with V_P biased to 3.3 Volts (pin 5 @ 3.3V).
7. Measurements performed using a 100ns Transmission Line Pulse (TLP) system.

Typical Performance Characteristics

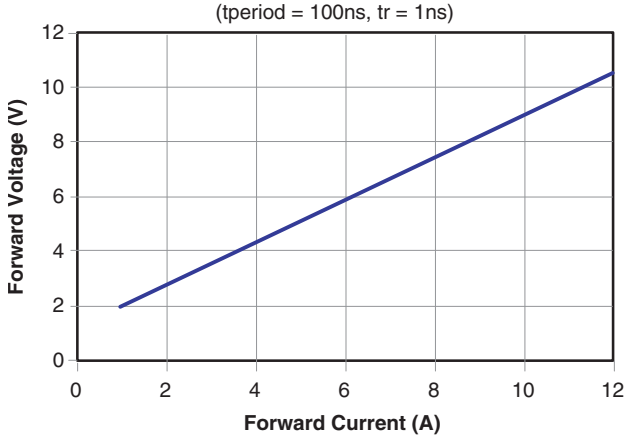
Typical Variation of C_{IN} vs V_R
(f = 1MHz, T = 25°C)



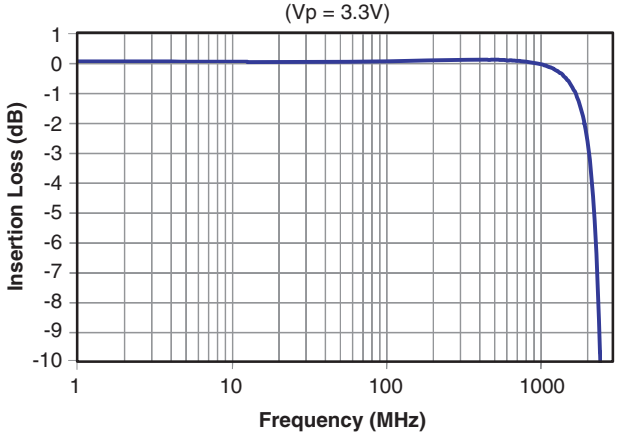
Clamping Voltage vs. Peak Pulse Current
(tperiod = 100ns, tr = 1ns)



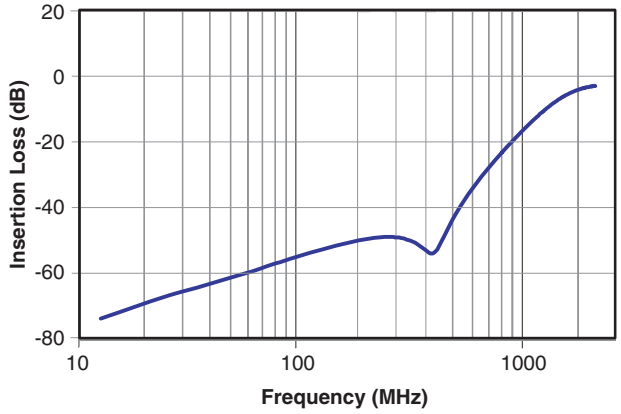
Forward Voltage vs. Forward Current
(tperiod = 100ns, tr = 1ns)



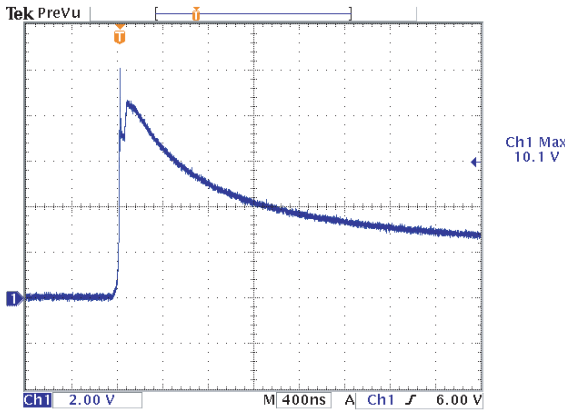
I/O – Gnd Insertion Loss (S21) vs. Frequency
(Vp = 3.3V)



Analog Crosstalk (I/O–I/O) vs. Frequency



ESD Response (8kV Contact per IEC61000-4-2)



Application Information

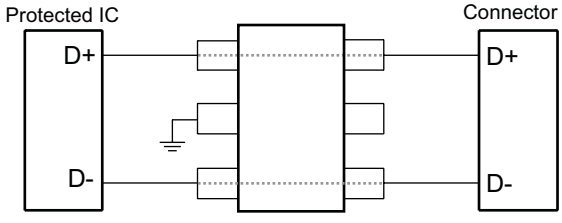
The AOZ8001K TVS is design to protect two data lines from fast damaging transient over-voltage by clamping it to a reference. When the transient on a protected data line exceed the reference voltage the steering diode is forward bias thus, conducting the harmful ESD transient away from the sensitive circuitry under protection.

PCB Layout Guidelines

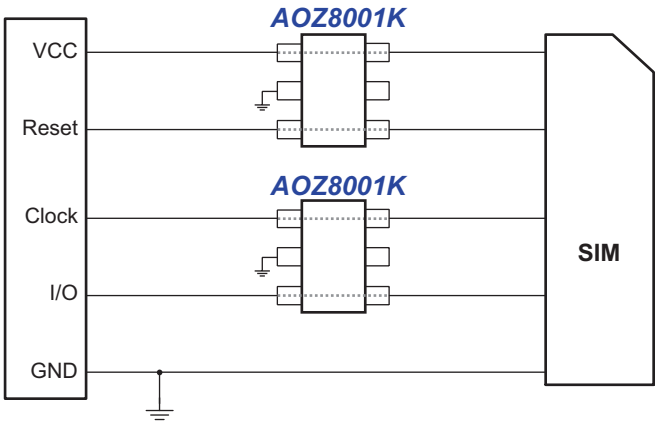
Printed circuit board layout is the key to achieving the highest level of surge immunity on power and data lines. The location of the protection devices on the PCB is the simplest and most important design rule to follow. The AOZ8001K devices should be located as close as possible to the noise source. The placement of the AOZ8001K devices should be used on all data and power lines that enter or exit the PCB at the I/O connector. In most systems, surge pulses occur on data and power lines that enter the PCB through the I/O connector. Placing the AOZ8001K devices as close as possible to the noise source ensures that a surge voltage will be clamped before the pulse can be coupled into adjacent PCB traces. In addition, the PCB should use the shortest possible traces. A short trace length equates to low impedance, which ensures that the surge energy will be dissipated by the AOZ8001K device. Long signal traces will act as antennas to receive energy from fields that are produced by the ESD pulse. By keeping line lengths as short as possible, the efficiency of the line to act as an antenna for ESD related fields is reduced. Minimize interconnecting line lengths by placing devices with the most interconnect as close together as possible. The protection circuits should shunt the surge voltage to either the reference or chassis ground. Shunting the surge voltage directly to the IC's signal ground can cause ground bounce. The clamping performance of TVS diodes on a single ground PCB can be improved by minimizing the impedance with relatively short and wide ground traces. The PCB layout and IC package parasitic inductances can cause significant overshoot to the TVS's clamping voltage. The inductance of the PCB can be reduced by using short trace lengths and multiple layers with separate ground and power planes. One effective method to minimize loop problems is to incorporate a ground plane in the PCB design. The AOZ8001K ultra-low capacitance TVS is designed to protect four high speed data transmission lines from transient over-voltages by clamping them to a fixed reference. The low inductance and construction minimizes voltage overshoot during high current surges. When the voltage on the protected line exceeds the reference voltage the internal steering diodes are forward biased, conducting the transient current away from the sensitive circuitry.

Good circuit board layout is critical for the suppression of ESD induced transients. The following guidelines are recommended:

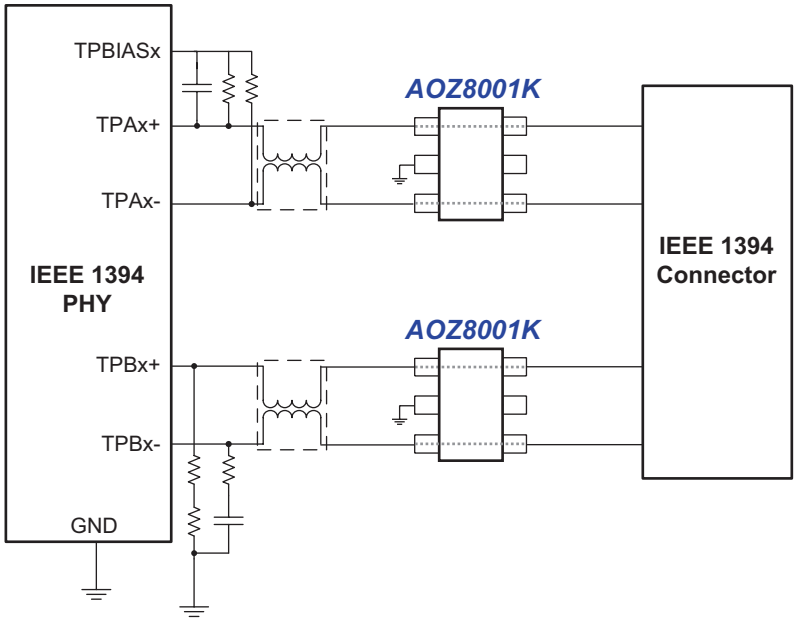
1. Place the TVS near the IO terminals or connectors to restrict transient coupling.
2. Fill unused portions of the PCB with ground plane.
3. Minimize the path length between the TVS and the protected line.
4. Minimize all conductive loops including power and ground loops.
5. The ESD transient return path to ground should be kept as short as possible.
6. Never run critical signals near board edges.
7. Use ground planes whenever possible.
8. Avoid running critical signal traces (clocks, resets, etc.) near PCB edges.
9. Separate chassis ground traces from components and signal traces by at least 4mm.
10. Keep the chassis ground trace length-to-width ratio <5:1 to minimize inductance.
11. Protect all external connections with TVS diodes.



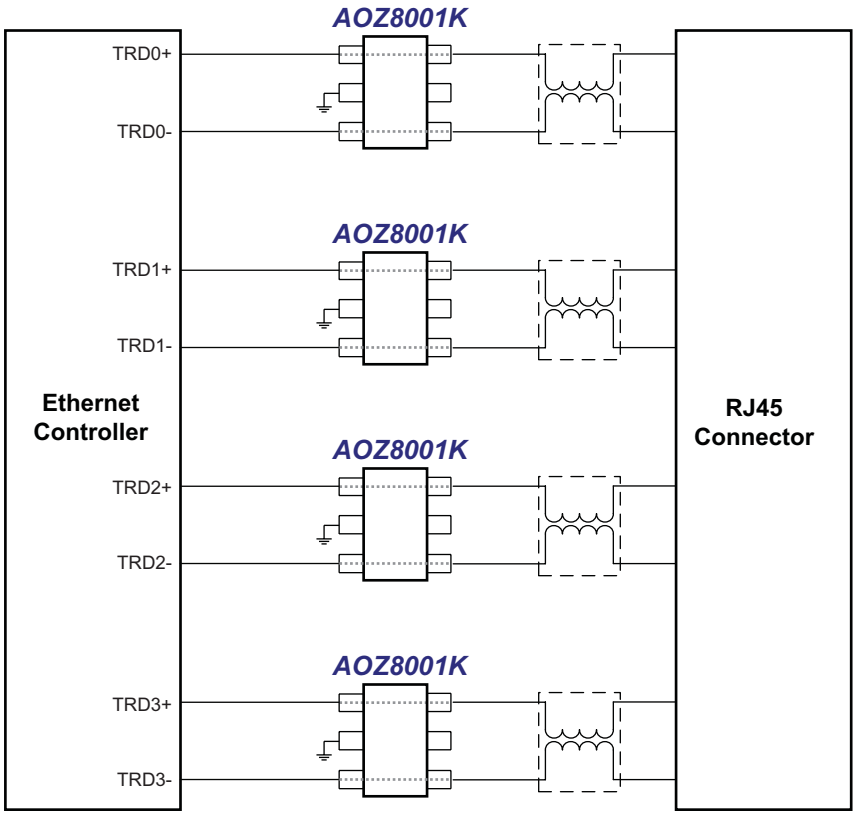
Flow Through Layout



SIM Card Port Connection

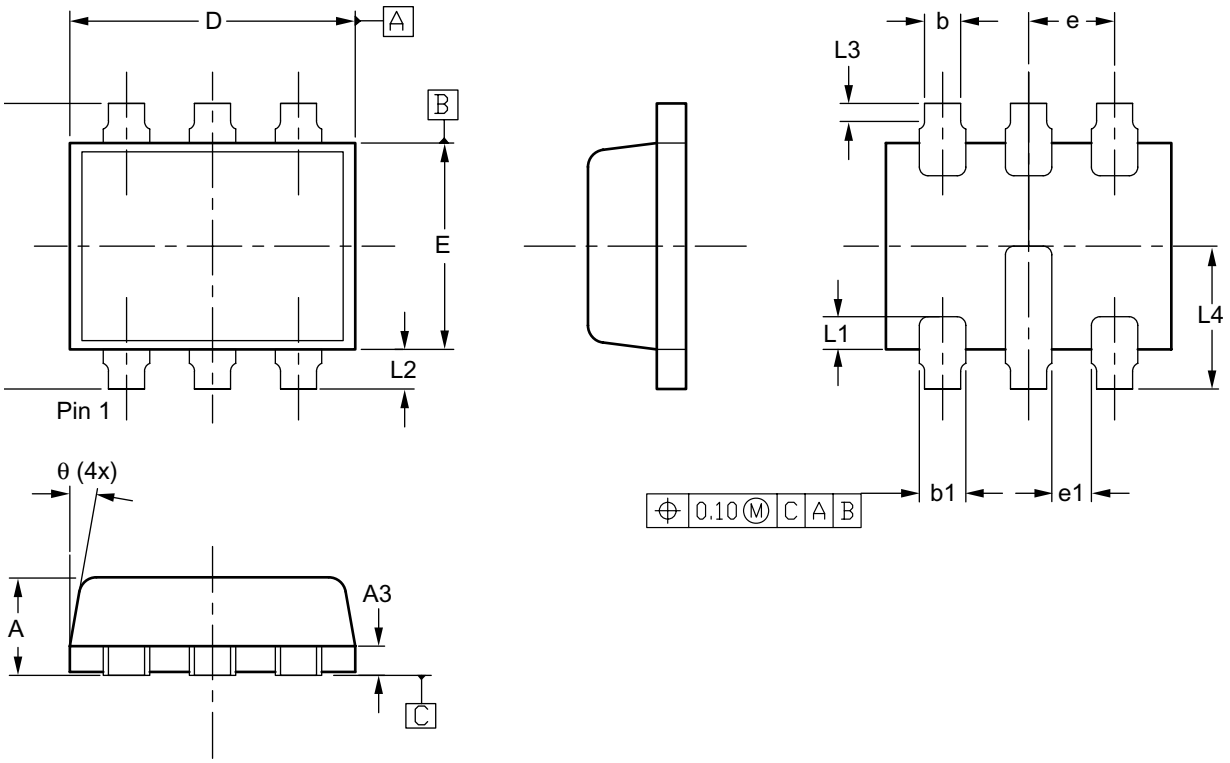


IEEE1394 Port Connection

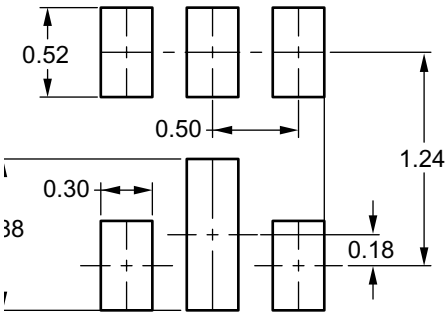


10/100 Ethernet Port Connection

Package Dimensions, SC-89



RECOMMENDED LAND PATTERN



UNIT: mm

Dimensions in millimeters

Symbols	Min.	Nom.	Max.
A	0.53	0.57	0.60
A3	0.13	0.17	0.18
b	0.17	—	0.25
D	1.50	1.66	1.70
E1	1.50	1.65	1.70
e		0.50 BSC	
E	1.10	1.20	1.30
L1	0.11	0.19	0.26
L2	0.10	0.23	0.30
L3	0.05	0.10	—
L4		0.83 REF	
b1	—	0.27	0.34
e1	0.20	—	—
θ	8°	10°	12°

Dimensions in inches

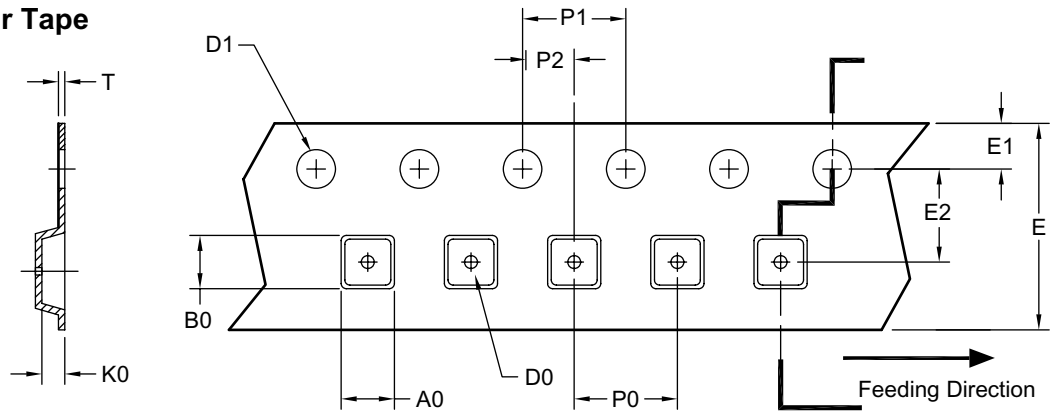
Symbols	Min.	Nom.	Max.
A	0.021	0.022	0.024
A3	0.005	0.007	0.007
b	0.007	—	0.010
D	0.060	0.065	0.067
E1	0.060	0.065	0.067
e		0.020 BSC	
E	0.043	0.047	0.051
L1	0.004	0.007	0.010
L2	0.004	0.009	0.012
L3	0.002	0.004	—
L4		0.033 REF	
b1	—	0.011	0.013
e1	0.008	—	—
θ	8°	10°	12°

Notes:

1. All dimensions are in millimeters.
2. Dimension are inclusive of plating.
3. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 3 mils each.
4. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.

Tape and Reel Dimensions, SC-89

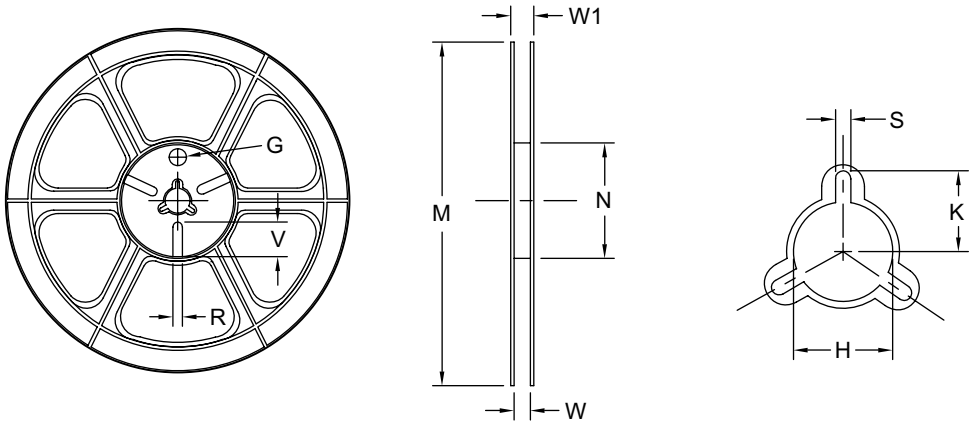
Carrier Tape



UNIT: mm

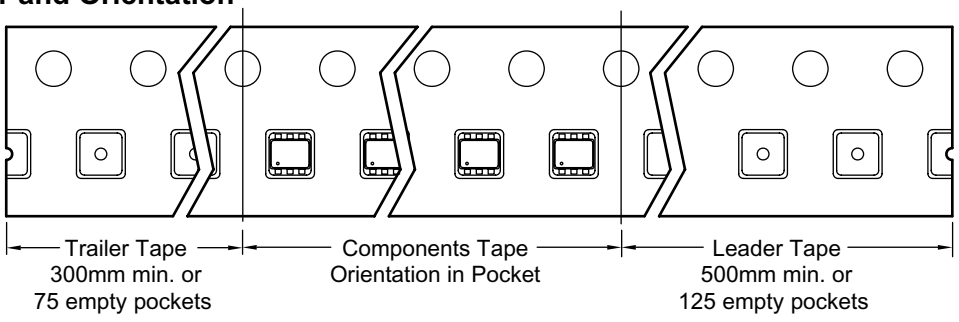
Package	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
SC-89, 6L (8mm)	1.78 ±0.05	1.78 ±0.05	0.89 ±0.05	0.50 ±0.05	1.50 ±0.10	8.00 +0.30/-0.10	1.75 ±0.10	3.50 ±0.05	4.00 ±0.10	4.00 ±0.10	2.00 ±0.05	0.25 ±0.05

Reel



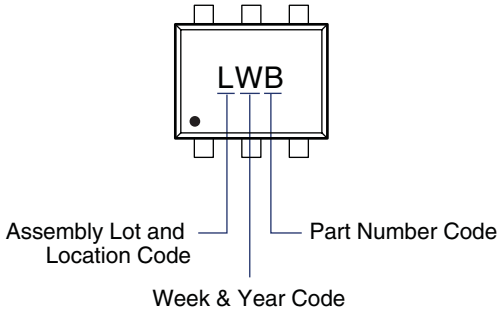
Tape Size	Reel Size	M	N	W	W1	H	K	S	G	R	V
8mm	ø180	ø180.00 ±0.50	ø60.50	9.00 ±0.30	11.40 ±1.00	ø13.00 +0.50/-0.20	10.60	2.00 ±0.50	ø9.00	5.00	18.00

Leader/Trailer and Orientation

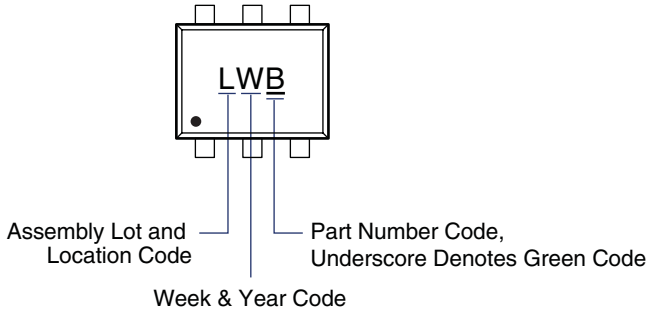


Part Marking

AOZ8001KI
(SC-89)



AOZ8001KIL
(SC-89)



Alpha & Omega Semiconductor reserves the right to make changes at any time without notice.

LIFE SUPPORT POLICY

ALPHA & OMEGA SEMICONDUCTOR PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.

2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

单击下面可查看定价，库存，交付和生命周期等信息

>>AOS(万代)