AOZ9510QI

30V/20A Smart Motor Module

General Description

The AOZ9510QI is an integrated half-bridge gate driver with smart functions. The device includes one half-bridge gate driver, capable of driving high-side and low-side N-channel MOSFETs. Using two AOZ9510QI for single phase motor driver and three AOZ9510QI for three phase motor drivers.

The device features multiple protection functions such as VCC UVLO, and over temperature protection. Moreover, AOZ9510QI provides adjustable gate drive sink and source current control. By doing this control, user can optimize performances of EMI and efficiency.

The AOZ9510QI is available in a 4mm×4mm QFN-23L package and is rated over a -40°C to +85°C ambient temperature range.

Features

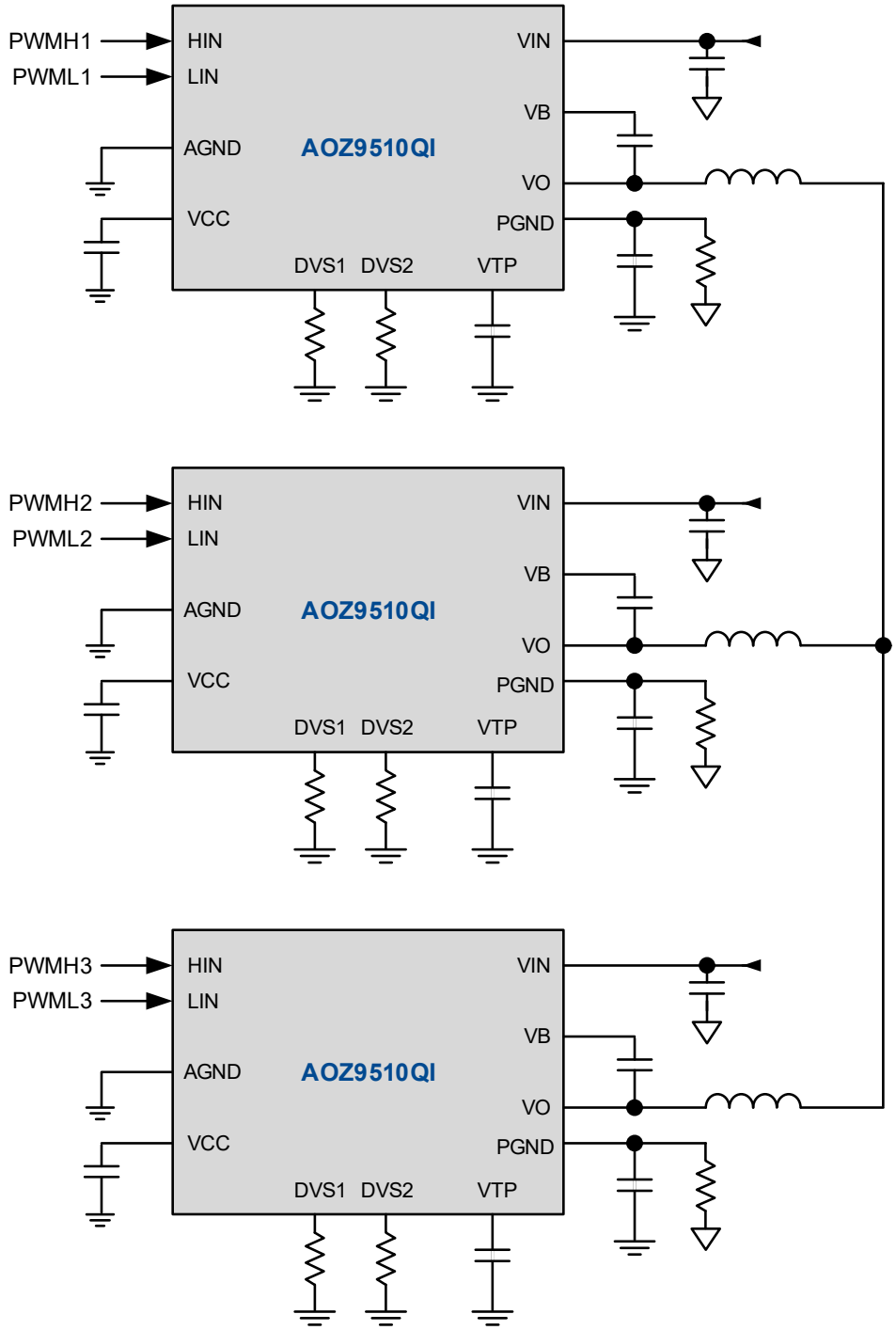
- Input voltage range:
  - 10.8V to 30V
- Maximum output current 20A
- Adjustable gate drive sink/source current
- Junction temperature monitor
- Support 100% PWM operation
- Integrated bootstrap diode
- Low $R_{DS(ON)}$ internal NFETs
  - 6mΩfor both HS/LS
- Thermal protection
- VCC UVLO
- Thermally enhanced 23-pin 4×4 QFN

Applications

- BLDC motor drive
- Fans and pumps
- Power tools

Green Product

Typical Application

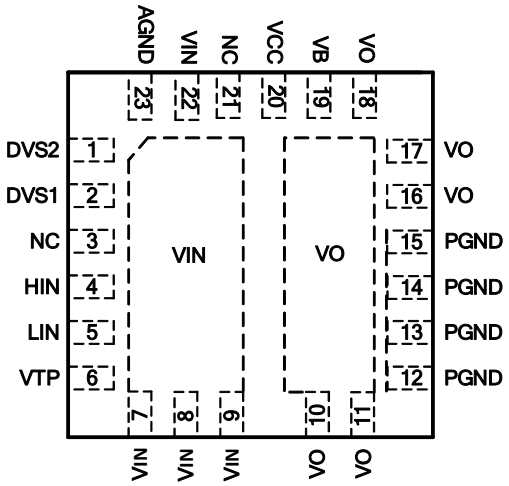


Ordering Information

Part Number	Ambient Temperature Range	Package	Environmental
AOZ9510QI	-40°C to +85°C	23-Pin 4x4 QFN	RoHS

All AOS Products are offering in packaging with Pb-free plating and compliant to RoHS standards. Please visit www.aosmd.com/media/AOSGreenPolicy.pdf for additional information.

Pin Configuration



23-Pin 4mm x 4mm QFN

Pin Description

Pin Number	Pin Name	Pin Function
1	DVS2	Adjustable gate drive sink current.
2	DVS1	Adjustable gate drive source current.
3	NC	No connect
4	HIN	PWM input for high-side MOSFET.
5	LIN	PWM input for low-side MOSFET.
6	VTP	Junction temperature monitor
7, 8, 9, 22	VIN	Supply input. All IN pins must be connected together.
10,11,16,17,18	VO	Motor drive output.
12, 13, 14, 15	PGND	Power ground. Reserved one 0603 X7R ceramic capacitor (0.1uF~1uF) between PGND and AGND is needed.
19	VB	Bootstrap capacitor connection. Connect an external capacitor between VB and VO for supplying high-side MOSFET.
20	VCC	Supply input for analog functions. Bypass VCC to AGND with a 0.1uF~10uF ceramic capacitor and as close to VCC pin as possible.
21	NC	No connect
23	AGND	Analog ground.

Absolute Maximum Ratings[1]

Exceeding the Absolute Maximum ratings may damage the device.

Parameter	Rating
VIN to AGND	-0.3V to 30V
VO to AGND	-0.3V to 30V
VB to AGND	-0.3V to 40V
DVS1, DVS2, ERR, VCC to AGND	-0.3V to 13.2V
HIN, LIN to AGND	-0.3V to 5.5V
PGND to AGND[3]	-0.3V to +1V
Junction Temperature (T_J)	+150°C
Storage Temperature (T_S)	-65°C to +150°C
ESD Rating	2kV

Notes:

1. Exceeding the Absolute Maximum ratings may damage the device.
2. The device is not guaranteed to operate beyond the Maximum Operating ratings.
3. PGND to AGND transient (t<100ns) ----- -6.5V to 6.5V.

Maximum Operating Ratings[2]

The device is not guaranteed to operate beyond the Maximum Operating Ratings.

Parameter	Rating
Supply Voltage (V_{IN})	10.8V to 30V
Ambient Temperature (T_A)	-40°C to +85°C
Package Thermal Resistance	
(Θ_{JA})	32°C/W
(Θ_{JC})	4°C/W

Electrical Characteristics

T_A = -40°C to 85°C unless otherwise specified.

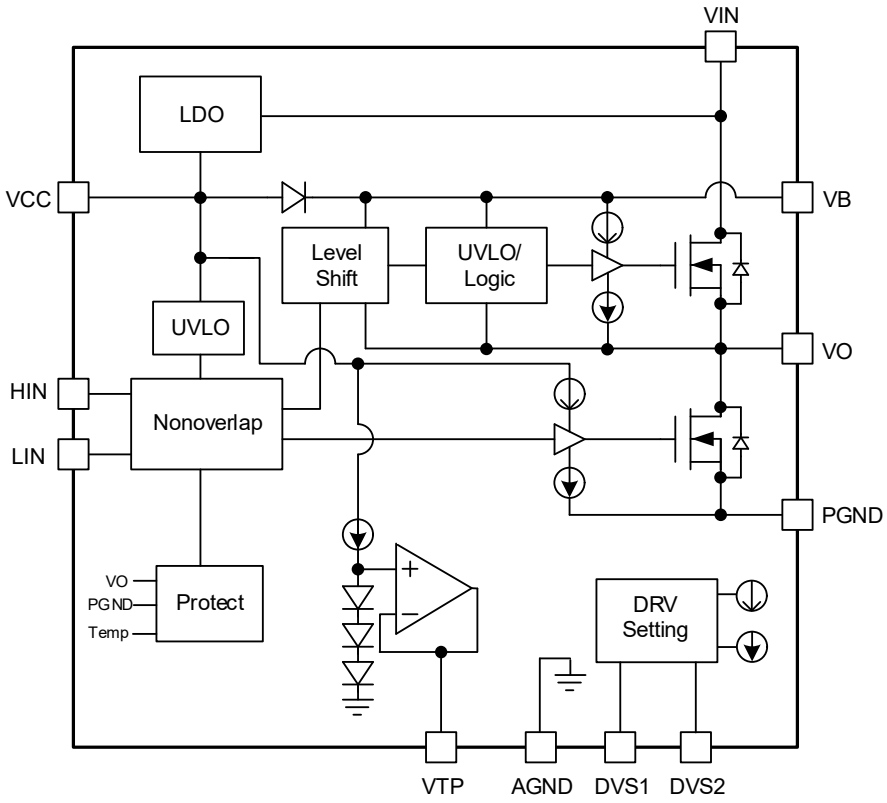
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{CC}	V_{CC}	VIN =12V, HIN/LIN=0V	7.8	8	8.2	V
	Line Regulation	VIN =12V ~ 24V, HIN/LIN=0V		0.1		%/V
I_{VCC_short}	Ivcc Short Current	VIN =12V, HIN/LIN=0V, Monitor I_{VCC}		1		mA
V_{UVLO_R}	Vcc UVLO Rising	VIN=12V, Vcc increase, Monitor DVS1 from low to high	7	7.5	8	V
V_{UVLO_F}	Vcc UVLO Falling	VIN=12V, Vcc decrease, Monitor DVS1 from high to low		5.2		V
VB_{UVLO_R}	VB-VO UVLO Rising	VIN=20V, VB-VO increase, HIN = High Monitor VO from low to high	6.7	7.2	7.7	V
VB_{UVLO_F}	VB-VO UVLO Falling	VIN=20V, VB-VO decrease, HIN = High Monitor VO from high to low	5.2	5.5	5.8	V
I_{VIN_QC}	I_{VIN}Quiescent Current	HIN/LIN=0V, Monitor VIN Current		2.4		mA
$I_{VB\text{-}VO\_QC}$	$I_{VB\text{-}VO}$Quiescent Current	VIN = 10.8V, HIN/LIN = 0V, VO = Floating, VB-VO = 10V, Monitor VB-VO Current		25		µA
V_{HLIN_L}	HIN/LIN Logic Low Voltage	VIN =12V			1.2	V
V_{HLIN_H}	HIN/LIN Logic High Voltage	VIN =12V	2.2			V
R_{HLIN_IN}	HIN/LIN Input Pull Low Impedance			280		kΩ
t_{HIN_RP}	HIN Rising Propagation Delay	VIN = 10.8V, DVS = 20kΩ, VO to GND = 100Ω, HIN = Low to High, Monitor HIN High TH to 10% VO		42		ns
t_{HIN_FP}	HIN Falling Propagation Delay	VIN = 10.8V, DVS = 20kΩ, VO to GND = 100Ω, HIN = High to Low, Monitor HIN Low TH to 90% VO		87		ns
t_{LIN_RP}	LIN Rising Propagation Delay	VIN= 10.8V, DVS=20kΩ, VO to VIN=100Ω, LIN=Low to High, Monitor LIN High TH to 90% VO		52		ns

Electrical Characteristics

T_A = -40°C to 85°C unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
t_{LIN_FP}	LIN Falling Propagation Delay	VIN=10.8V, DVS= 20kΩ, VO to VIN=100Ω, LIN= High to Low, Monitor LIN Low TH to 10% VO		88.5		ns
T_{DM_R}	Delay Matching Rising	Difference between t_{HIN_RP} and t_{LIN_RP}		10		ns
T_{DM_F}	Delay Matching Falling	Difference between t_{HIN_FP} and t_{LIN_FP}		1.5		ns
V_{DVS}	DVS	VIN = 12V, DVS to GND=20kΩ	0.97	1	1.03	V
I_{DVS_MIN}	DVS Min. Source Current	VIN = 12V, DVS = 4V		0.5		µA
I_{DVS_MAX}	DVS Max. Source Current	VIN = 10.8V, DVS = 0.8V		140		µA
SR_{HIN_R}	HIN Rising Slew Rate (DVS = 20kΩ)	VIN = 10.8V, VO to GND = 100Ω, HIN = Low to High, Monitor Vo Rising Slew Rate		1.43		V/ns
SR_{HIN_F}	HIN Falling Slew Rate (DVS = 20kΩ)	VIN = 10.8V, VO to GND =100Ω, HIN = High to Low, Monitor Vo Falling Slew Rate		0.022		V/ns
SR_{LIN_R}	LIN Rising Slew Rate (DVS = 20kΩ)	VIN = 10.8V, VO to VIN = 100Ω, LIN = High to Low Monitor Vo Rising Slew Rate		0.027		V/ns
SR_{LIN_F}	LIN Falling Slew Rate (DVS = 20kΩ)	VIN = 10.8V, VO to VIN = 100Ω, LIN = Low to High, Monitor Vo Falling Slew Rate		1.02		V/ns
R_{H_ON}	VIN-VO RON	VIN = 12V, HIN = 5V, VB-VO = 8V, IVO = 1A		6		mΩ
R_{L_ON}	VO-PGND RON	VIN = 12V, LIN = 5V, PGND=0, IVO = 1A		6		mΩ
V_{SD}	Boost Diode Forward Voltage	Forward Current = 2mA		0.15		V
T_{OTP}	Over Temperature Protection	VIN = 12V		150		°C
VTP	$V_{TP\_25°C}$	VIN=12V at 25°C	1.86	1.9	1.94	V
	$V_{TP\_125°C}$	VIN=12V at 125°C	1.26	1.3	1.34	V

Functional Block Diagram



Typical Performance Characteristics

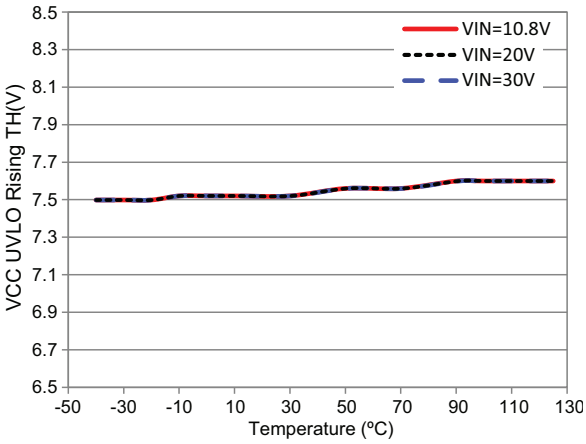


Figure 1. VCC UVLO Rising Threshold

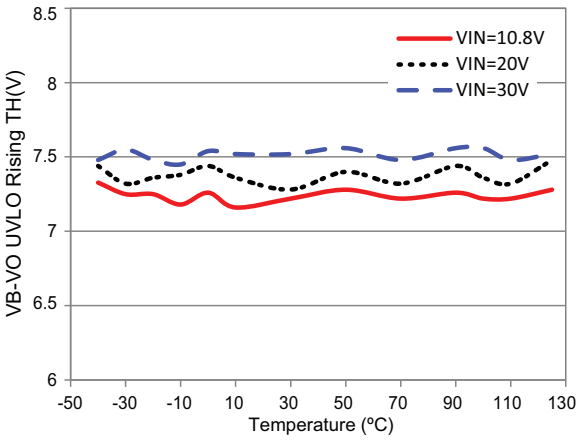


Figure 2. VB-VO UVLO Rising Threshold

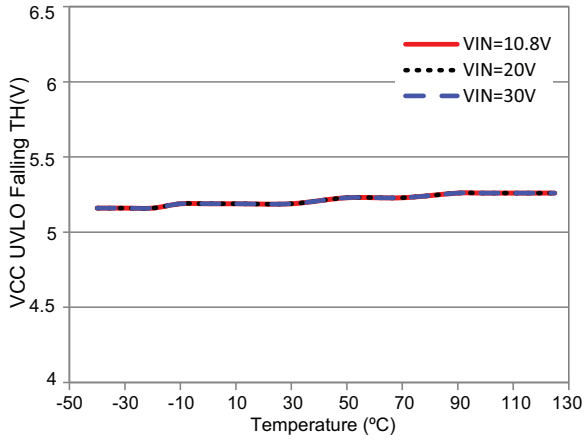


Figure 3. VCC UVLO Falling Threshold

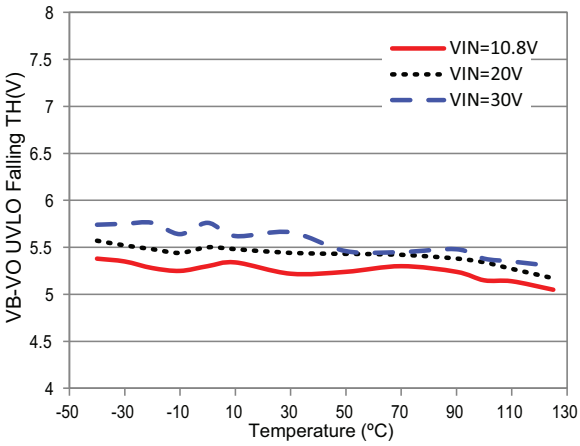


Figure 4. VB-VO UVLO Falling Threshold

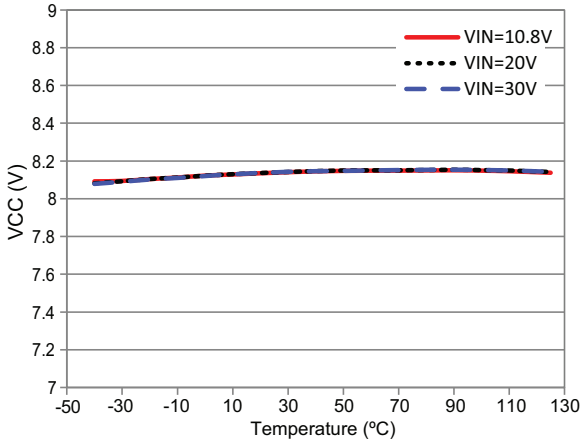


Figure 5. VCC Regulation

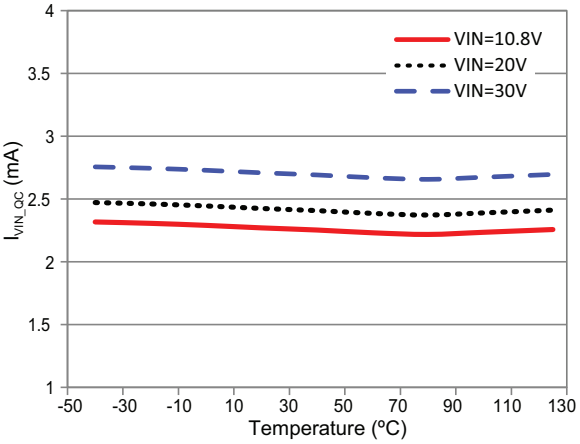


Figure 6. Input Quiescent Current (mA)

Typical Performance Characteristics *(Continued)*

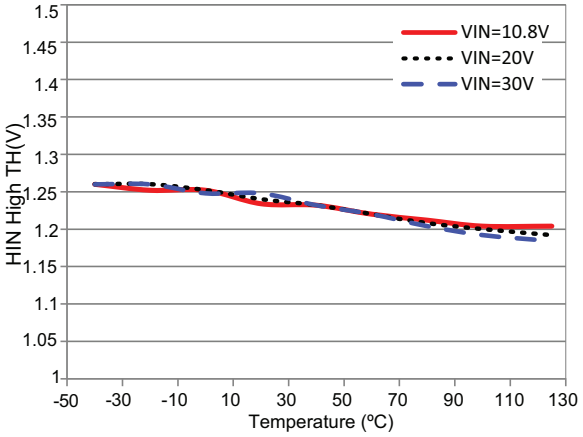


Figure 7. HIN High Threshold

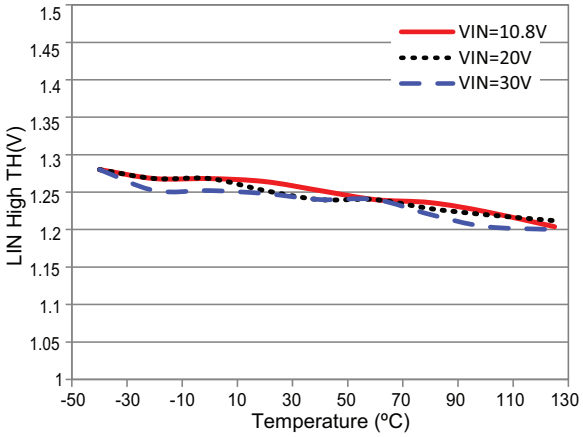


Figure 8. LIN High Threshold

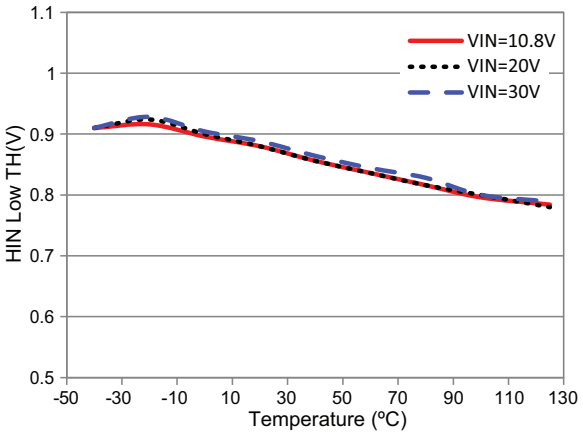


Figure 9. HIN Low Threshold

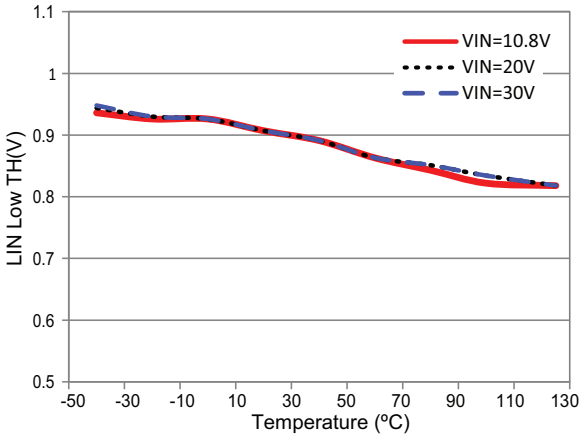


Figure 10. LIN Low Threshold

Detailed Description

The AOZ9510QI is an integrated half-bridge gate driver for motor drive applications. The device includes one half-bridge gate driver, capable of driving high-side and low-side N-channel MOSFETs. The AOZ9510QI provides adjustable source/sink current of both high/low-side gate drive output current which can optimize performances of EMI and efficiency on different PCB layout and applications.

In addition, the AOZ9510QI provides several fault protections, such as UVLO, OTP and non-overlapping mechanism.

The AOZ9510QI is available in 23-pin 4mm×4mm QFN package.

Input Power Architecture

The AOZ9510QI integrates an internal linear regulator to generate 8V (2.5%) VCC from input pins. If input voltage is lower than 5.2V, the linear regulator will be triggered VB-VO UVLO. The VCC maximum source current is 1mA. Therefore, extra external source is needed when operation switching frequency exceeds 30kHz.

Non-overlapping

For forbidding shoot-through, HIN or LIN is invalid when HIN or LIN goes high state before other one. For example, low-side gate state keeps low regardless of the state of LIN when HIN is high at first, and vice versa.

Thermal Monitor

The junction temperature can be monitored by using internal current mirror pass through internal diodes. The related V_{TP} equation can be approximated as below,

$$V_{TP} = 1.9V - (Temp - 25^{o}C) \times 6mV$$

Adjustable Source/Sink Current

It's hard to meet all of EMI specifications in different applications. So, AOZ9510QI provides external adjustable resistors for tuning gate drive source and sink current.

DSV1 and DVS2 are used to tune gate drive source and sink current, respectively. A resistor connects between each DVS pin and GND to setting gate drive source /sink current by internal current mirror, as illustrated Figure 11‘ Source and sink current use maximum capability to drive when DVS pins are floating or the voltage on DVS pins exceed 4V. User can get the same source and sink capability by using DVS1 to design and DVS2 floating. The suggestion range of R_{DVS} is 20kΩ~100kΩ.

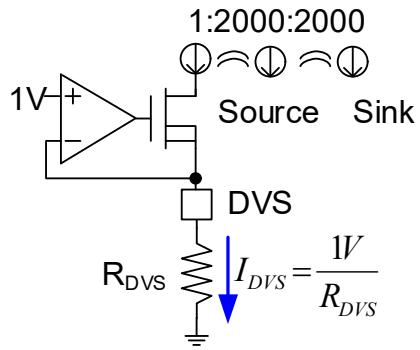


Figure 11. Source / Sink Current Setting

In addition, source and sink current controls are implemented only during MOSFET Miller effect and VGS >1V, as illustrated Figure 12.

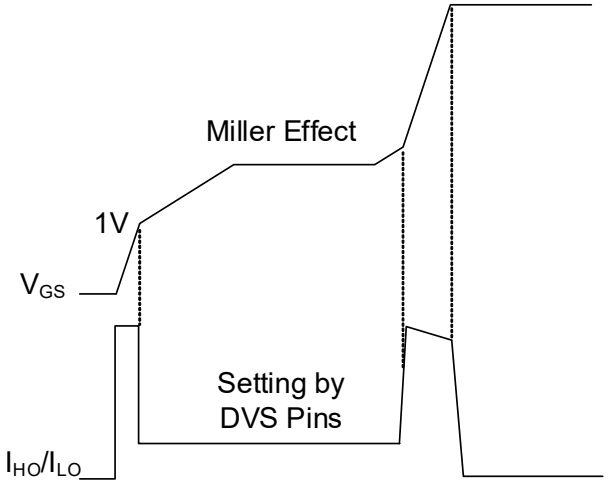


Figure 12. Source/Sink Current Implement Waveform

Layout Considerations

Several layout tips are listed below for the best electric and thermal performance.

1. The VIN pins and pad are connected to internal high side switch drain. They are also low resistance thermal conduction path. Connected a large copper plane to VIN pins to help thermal dissipation.
2. Input capacitors should be connected to the VIN pins and the PGND pins as close as possible to reduce the switching spikes.
3. The VO pins and pad are connected to internal low side switch drain. They are low resistance thermal conduction path and most noisy switching node. Connected a large copper plane to VO pins to help thermal dissipation.
4. Decoupling capacitor C_{VCC} should be connected to V_{CC} and AGND as close as possible.
5. Bootstrap capacitor C_B should be connected to VB and VO as close as possible.
6. A ground plane is preferred; PGND and AGND must be connected to the ground plane through vias.
7. Keep sensitive signal traces such as feedback trace and digital signals far away from the VO pins.

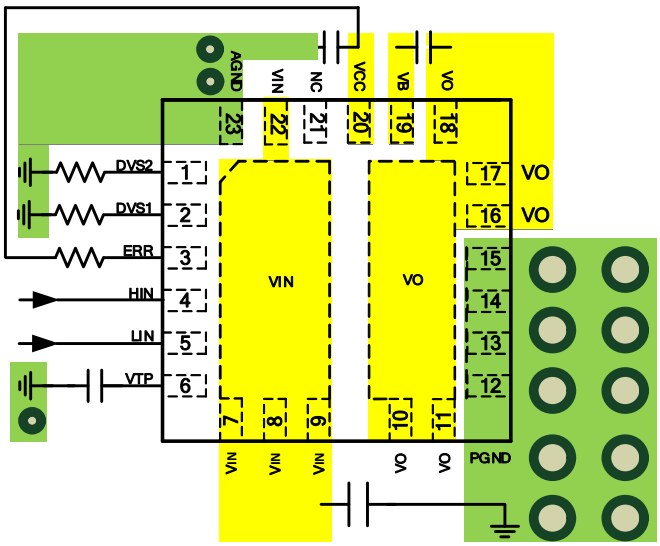
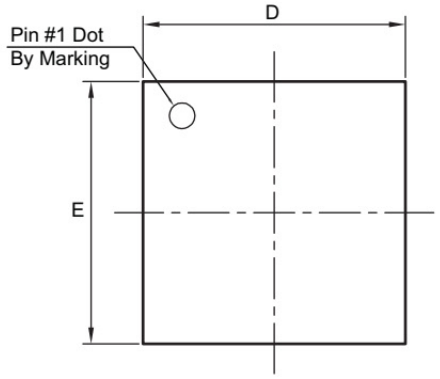
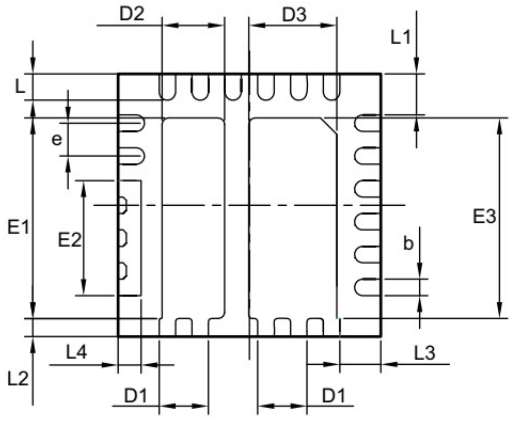


Figure 13. Layout Placement

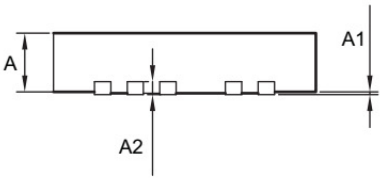
Package Dimensions, QFN 4x4B-23L



TOP VIEW

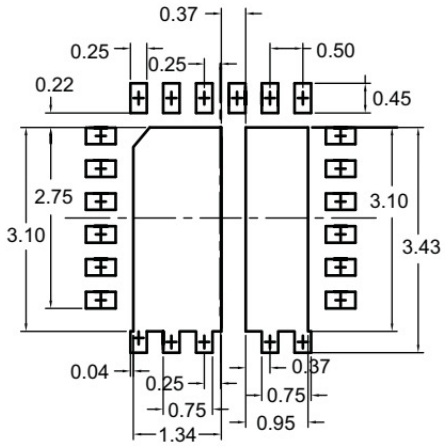


BOTTOM VIEW



SIDE VIEW

RECOMMENDED LAND PATTERN



UNIT: MM

Dimensions in millimeters

Symbols	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0.00	—	0.05
A2		0.2 REF	
E	3.90	4.00	4.10
E1	2.95	3.05	3.15
E2	1.65	1.75	1.85
E3	2.95	3.05	3.15
D	3.90	4.00	4.10
D1	0.65	0.75	0.85
D2	0.85	0.95	1.05
D3	1.24	1.34	1.44
L	0.35	0.40	0.45
L1	0.57	0.62	0.67
L2	0.23	0.28	0.33
L3	0.57	0.62	0.67
L4	0.30	0.35	0.40
b	0.20	0.25	0.30
e		0.50 BSC	

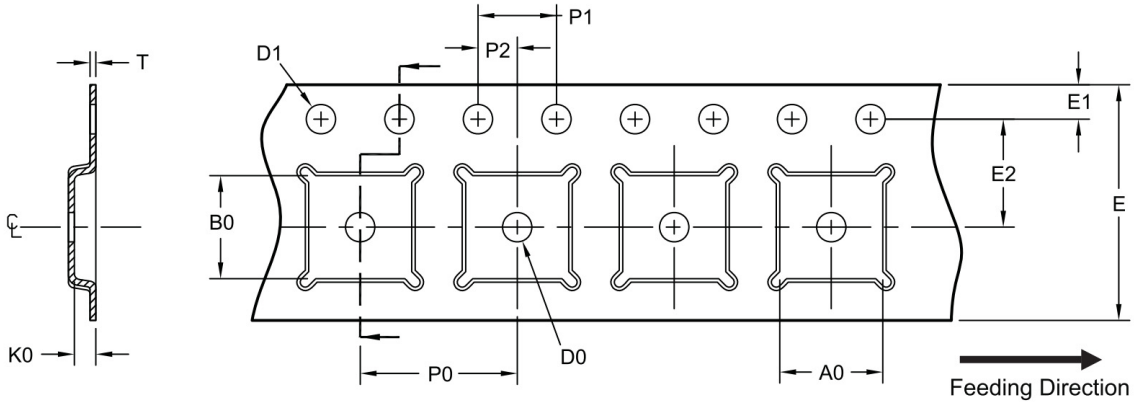
Dimensions in inches

Symbols	Min.	Typ.	Max.
A	0.031	0.035	0.039
A1	0.000	—	0.002
A2		0.008 REF	
E	0.153	0.157	0.161
E1	0.116	0.120	0.124
E2	0.065	0.069	0.073
E3	0.116	0.120	0.124
D	0.153	0.157	0.161
D1	0.026	0.030	0.034
D2	0.033	0.037	0.041
D3	0.049	0.053	0.057
L	0.014	0.016	0.018
L1	0.022	0.024	0.026
L2	0.009	0.011	0.013
L3	0.022	0.024	0.026
L4	0.012	0.014	0.016
b	0.008	0.010	0.012
e		0.020 BSC	

Notes:
1. Controlling dimensions are in millimeters. Converted inch dimensions are not necessarily exact.
2. Tolerance: ± 0.05 unless otherwise specified.
3. Radius on all corners is 0.152 max., unless otherwise specified.
4. Package wrapage: 0.012 max.
5. No plastic flash allowed on the top and bottom lead surface.
6. Pad planarity: ± 0.102
7. Crack between plastic body and lead is not allowed.

Tape and Reel Drawing, QFN 4x4B-23L

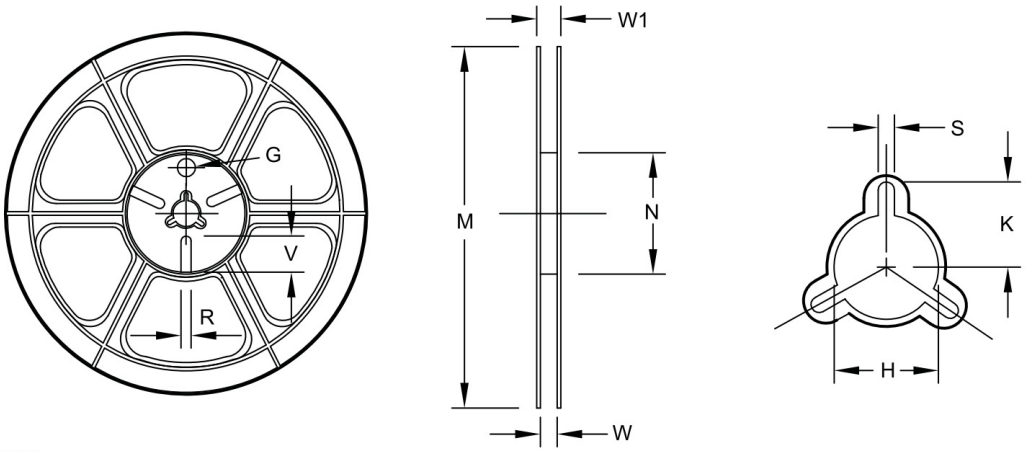
Carrier Tape



UNIT: mm

Package	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
QFN 4x4 (12mm)	4.35 ±0.10	4.35 ±0.10	1.10 ±0.10	1.50 Min.	1.50 +0.10/-0	12.00 ±0.30	1.75 ±0.10	5.50 ±0.05	8.00 ±0.10	4.00 ±0.10	2.00 ±0.05	0.30 ±0.05

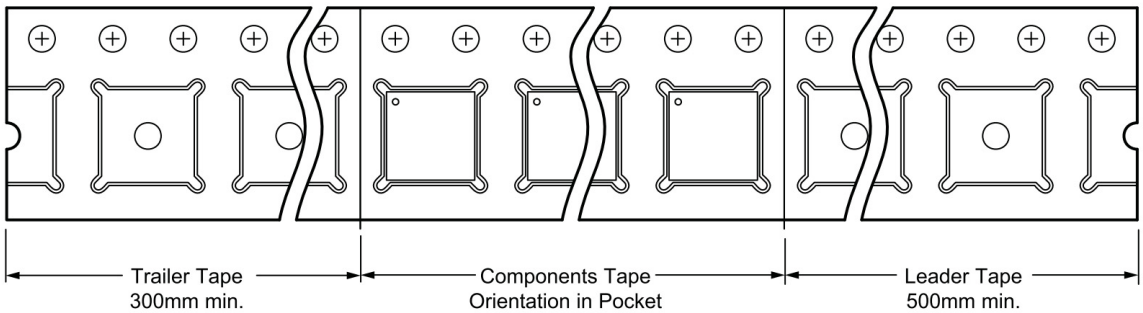
Reel



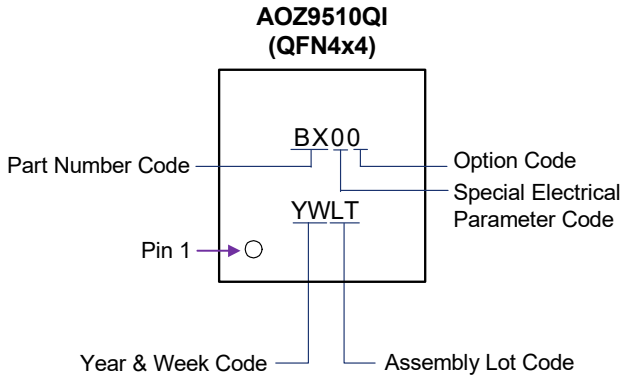
UNIT: mm

Tape Size	Reel Size	M	N	W	W1	H	K	S	G	R	V
12mm	ø330	ø330.0 ±2.0	ø79.0 ±1.0	12.4 +2.0/-0.0	17.0 +2.6/-1.2	ø13.0 ±0.5	10.5 ±0.2	2.0 ±0.5	—	—	—

Leader/Trailer and Orientation



Part Marking



Note:
Assembly Location - YWLT/YWL$\underline{T}$/YWL$\overline{T}$

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