

## 30V N-Channel Enhancement Mode MOSFET

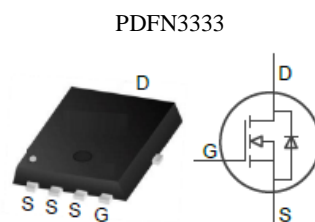
### General Features

- Low  $R_{DS(ON)}$
- Low Gate Charge
- Advanced High Cell Density Trench Technology
- RoHS Compliant
- Halogen-free available
- 100% Avalanche Tested

$BV_{DSS}$	$R_{DS(ON)}$ @ $V_{GS}=10V$	$R_{DS(ON)}$ @ $V_{GS}=4.5V$
30V	3.9m $\Omega$	5.2 m $\Omega$
$I_D$	59A	

### Applications

- High Efficiency DC/DC Converters
- Synchronous Rectification
- UPS Inverter
- Power Management
- Battery Powered System



### Ordering Information

Part Number	Package	Marking	Remark
AKF30N5P0SX	PDFN3333	30N5P0SX	Halogen Free

### Absolute Maximum Ratings

 $T_C=25^{\circ}C$  unless otherwise specified

Symbol	Parameter	Rating	Unit	
$V_{DSS}$	Drain-to-Source Voltage <sup>[1]</sup>	30	V	
$V_{GSS}$	Gate-to-Source Voltage	$\pm 20$	V	
$I_D$	Continuous Drain Current	$T_C=25^{\circ}C$	59	A
		$T_C=70^{\circ}C$	47	A
$I_{DM}$	Pulsed Drain Current at $V_{GS}=10V$ <sup>[2]</sup>	177	A	
$E_{AS}$	Single Pulse Avalanche Energy ( $V_{DD}=25V$ , $V_{GS}=10V$ , $R_G=25\Omega$ , $L=1mH$ )	32	mJ	
$P_D$	Power Dissipation	28	W	
$T_J$ and $T_{STG}$	Operating and Storage Temperature Range	-55 to 150	$^{\circ}C$	

Caution: Stresses greater than those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device.

### Thermal Characteristics

Symbol	Parameter	Rating	Unit
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	45	$^{\circ}C/W$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	4.5	

## Electrical Characteristics

### OFF Characteristics

 $T_J=25^{\circ}\text{C}$  unless otherwise noted

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$BV_{DSS}$	Drain-to-Source Breakdown Voltage	30	--	--	V	$V_{GS}=0V, I_D=250\mu A$
$I_{DSS}$	Drain-to-Source Leakage Current	--	--	1	$\mu A$	$V_{DS}=30V, V_{GS}=0V$
$I_{GSS}$	Gate-to-Source Leakage Current	--	--	100	nA	$V_{GS}=20V, V_{DS}=0V$
		--	--	-100	nA	$V_{GS}=-20V, V_{DS}=0V$

### On Characteristics

 $T_J=25^{\circ}\text{C}$  unless otherwise noted

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance <sup>[3]</sup>	--	3.9	5.0	m $\Omega$	$V_{GS}=10V, I_D=8A$
		--	5.2	7.0	m $\Omega$	$V_{GS}=4.5V, I_D=5A$
$V_{GS(TH)}$	Gate Threshold Voltage	1.0	--	2.0	V	$V_{DS} = V_{GS}, I_D=250\mu A$

### Dynamic Characteristics

Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$C_{iss}$	Input Capacitance	--	1527	--	pF	$V_{GS}=0V$ $V_{DS}=15V$ $f=1.0MHz$
$C_{oss}$	Output Capacitance	--	187	--		
$C_{rss}$	Reverse Transfer Capacitance	--	151	--		
$Q_g$	Total Gate Charge	--	33	--	nC	$V_{DD}=15V$ $V_{GS}=10V$ $I_D=6.5A$
$Q_{gs}$	Gate-to-Source Charge	--	7.4	--		
$Q_{gd}$	Gate-to-Drain (Miller) Charge	--	7.1	--		

### Resistive Switch Characteristics

Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$t_{d(on)}$	Turn-on Delay Time	--	17	--	ns	$V_{DD}=15V$ $V_{GS}=10V$ $R_G=3.3\Omega$ $R_L=2.3\Omega$
$t_{rise}$	Rise Time	--	51	--		
$t_{d(off)}$	Turn-off Delay Time	--	42	--		
$t_{fall}$	Fall Time	--	16	--		

**Source-Drain Diode Characteristics** $T_J=25^{\circ}\text{C}$  unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$I_{SD}$	Continuous Source Current	--	--	28	A	Maximum Ratings
$V_{SD}$	Diode Forward Voltage	--	--	1.0	V	$I_S=1.0\text{A}, V_{GS}=0\text{V}$

**NOTE:**[1]  $T_J=25^{\circ}\text{C}$  to  $150^{\circ}\text{C}$ 

[2] Repetitive rating, pulse width limited by maximum junction temperature.

[3] Pulse width  $\leq 380\mu\text{s}$ ; duty cycle  $\leq 2\%$ .

### Typical Characteristics

Figure 1. On Resistance vs. Junction Temperature

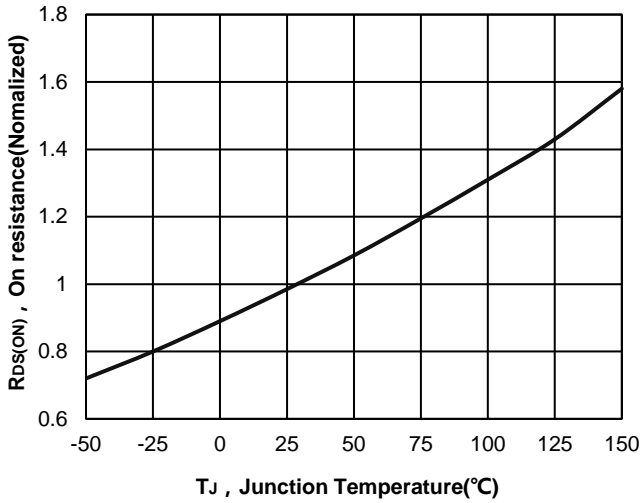


Figure 2. On Resistance vs. Drain Current

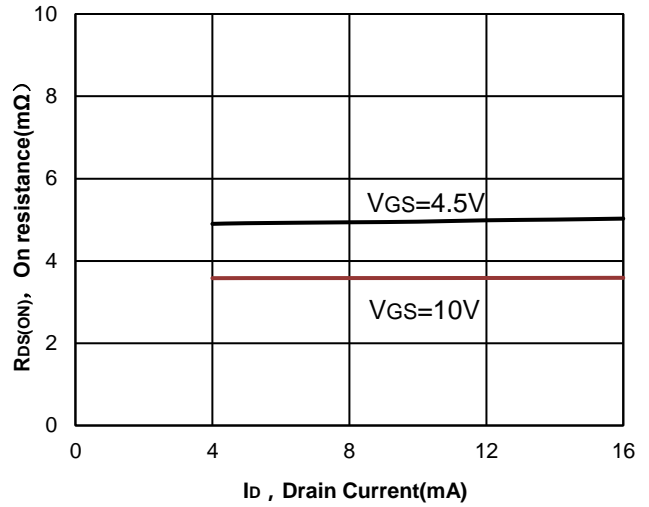


Figure 3. Typical Capacitance vs. Drain-to-Source Voltage

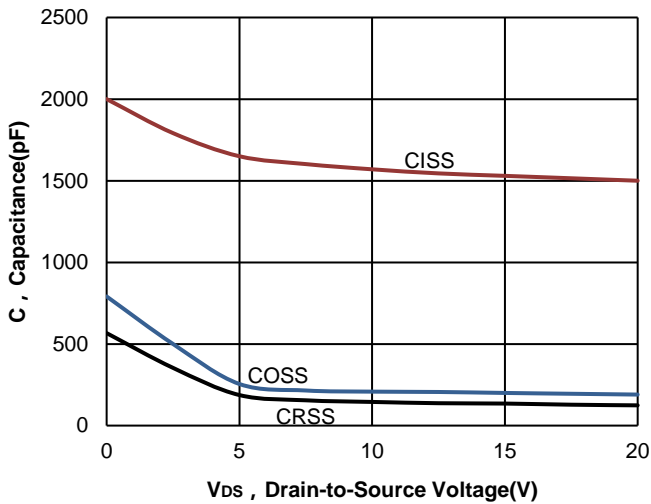


Figure 4. On Resistance vs. Gate-to-Source Voltage

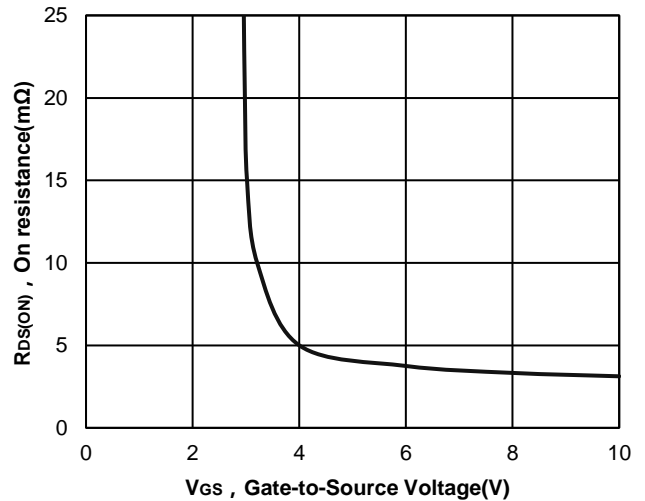


Figure 5. Body-diode Characteristics

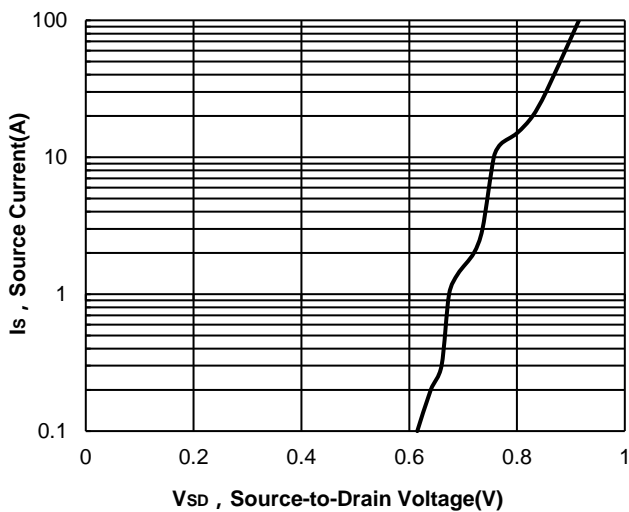


Figure 6. Typical Output Characteristics

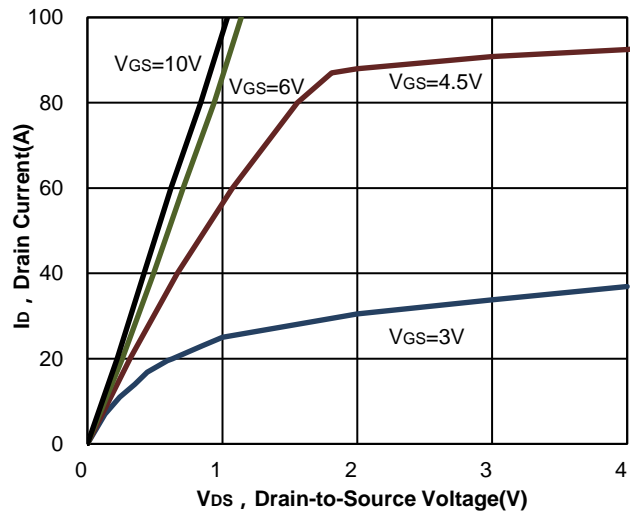


Figure 7. Typical Gate Charge vs. Gate-to-Source Voltage

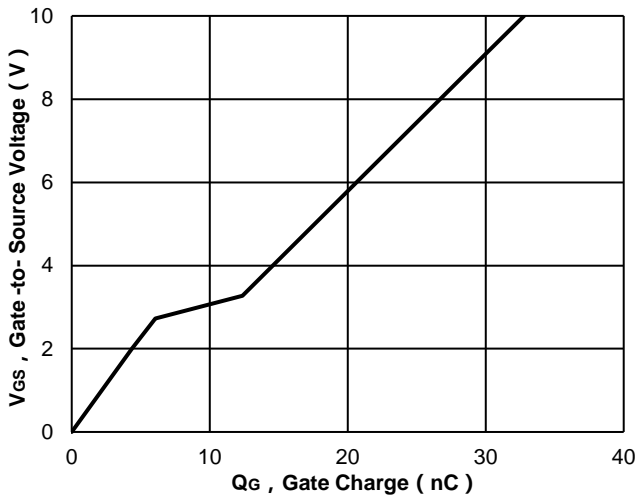


Figure 8. Maximum Forward Biased Safe Operating Area

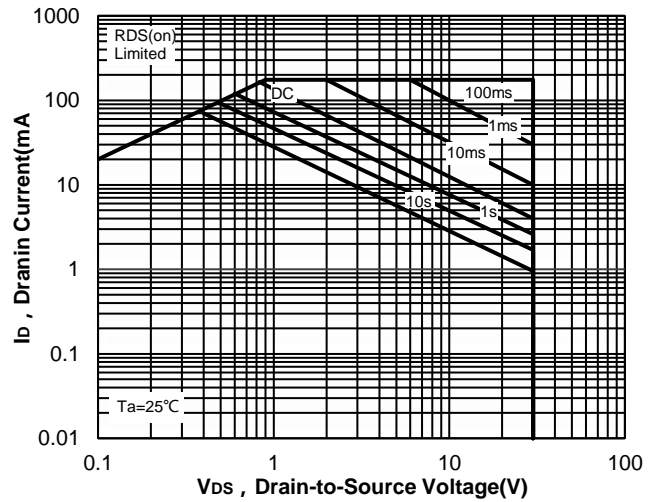
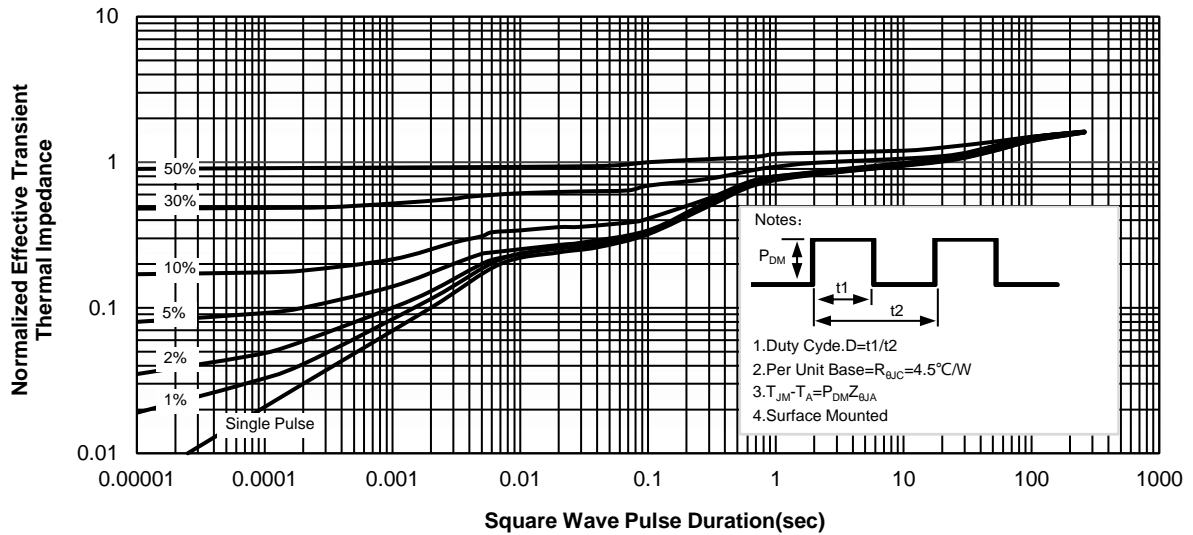
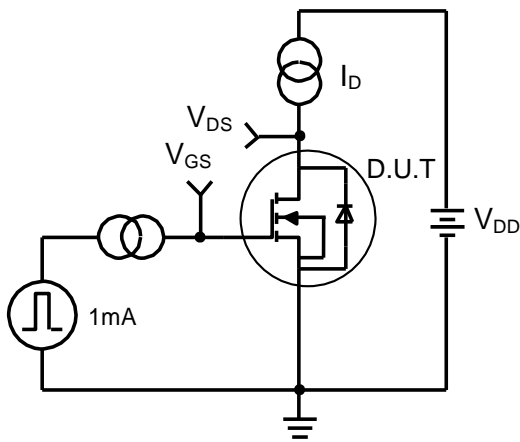
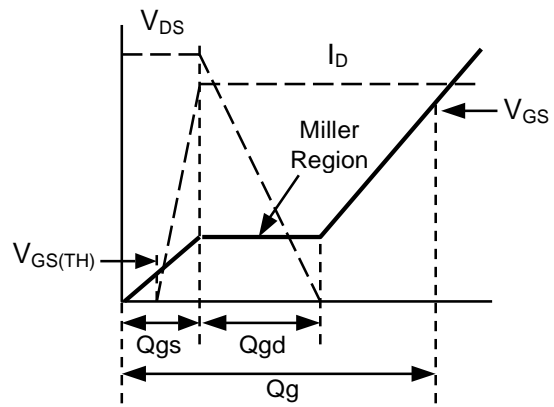
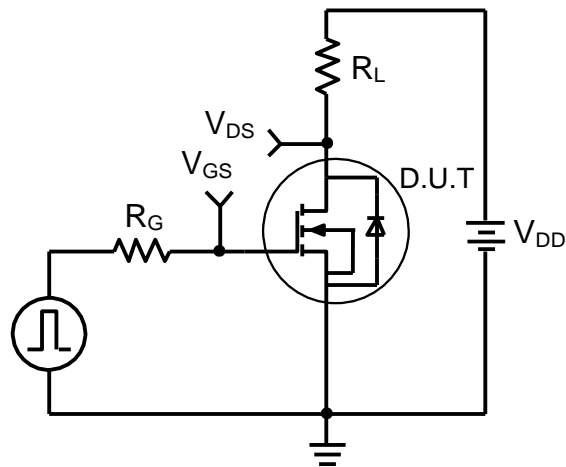
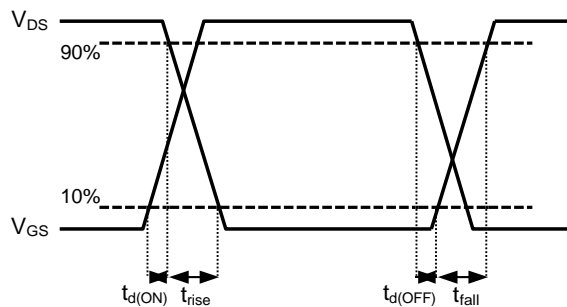
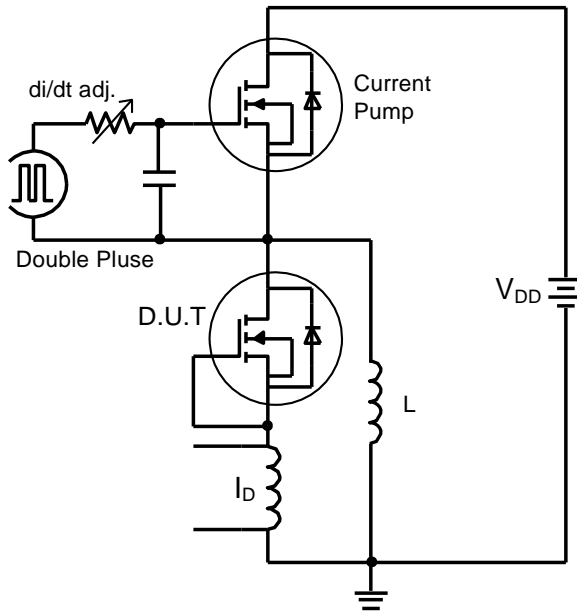
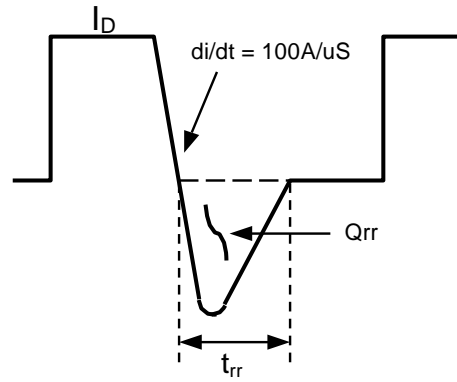
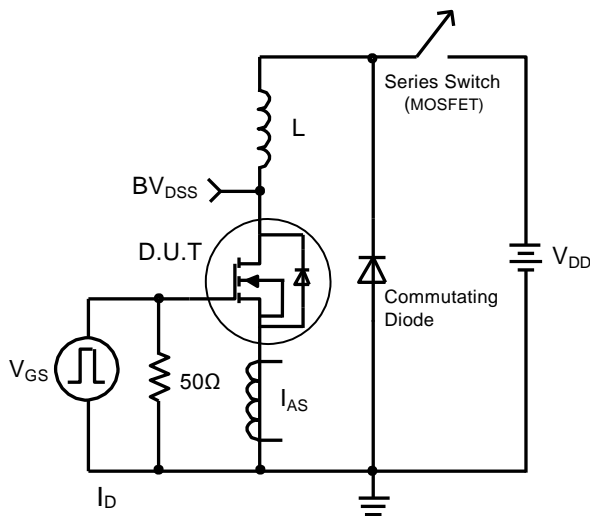
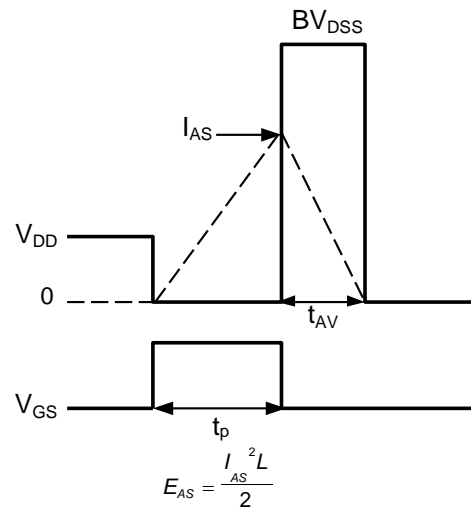


Figure 9. Normalized Thermal Transient Impedance, Junction-to-Case

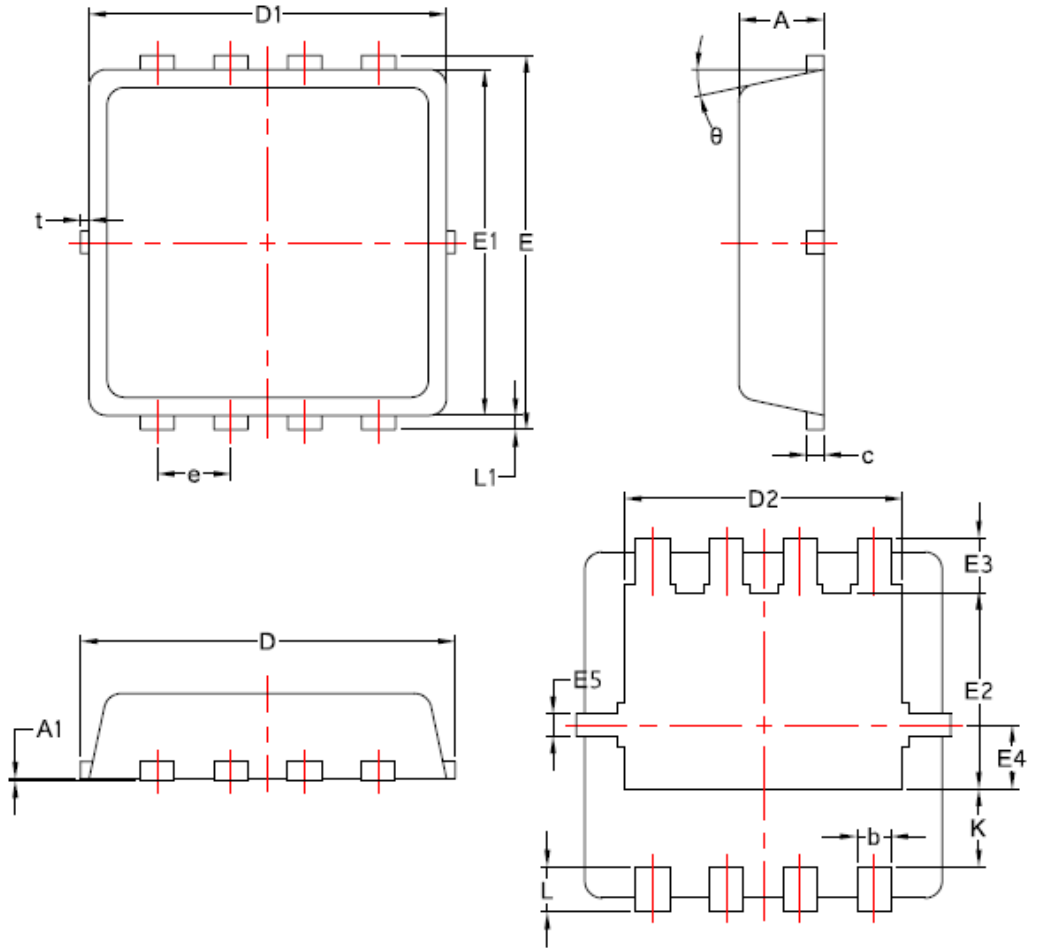


**Test Circuit**

**Figure 10. Gate Charge Test Circuit**

**Figure 11. Gate Charge Waveform**

**Figure 12. Resistive Switching Test Circuit**

**Figure 13. Resistive Switching Waveforms**


**Figure 14. Diode Reverse Recovery Test Circuit**

**Figure 15. Diode Reverse Recovery Waveform**

**Figure 16. Unclamped Inductive Switching Test Circuit**

**Figure 17. Unclamped Inductive Switching Waveforms**

**Package Dimensions**
**PDFN3333**

SYMBOL	COMMON		
	MM		
	MIN	NOM	MAX
A	0.70	0.75	0.85
A1	/	/	0.05
b	0.20	0.30	0.40
c	0.10	0.152	0.25
D	3.15	3.30	3.45
D1	3.00	3.15	3.25
D2	2.29	2.45	2.65
E	3.15	3.30	3.45
E1	2.90	3.05	3.20
E2	1.54	1.74	1.94
E3	0.28	0.48	0.65
E4	0.37	0.57	0.77
E5	0.10	0.20	0.30
e	0.60	0.65	0.70
K	0.59	0.69	0.89
L	0.30	0.40	0.50
L1	0.06	0.125	0.20
t	0	0.075	0.13
$\theta$	10°	12°	14°





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