AC7840x Datasheet

Supports the following:

AC78407YGLA，AC78407LGLA，AC78407HGLA，
AC78406YGLA，AC78406LGLA，AC78406HGLA，
AC78405YGLA，AC78405LGLA，AC78405HGLA，
AC78403YGLA，AC78403LGLA，AC78403HGLA，
AC78407LFLA，AC78407HFLA，
AC78406YFLA，AC78406LFLA，AC78406HFLA

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Document Revision History

Revision	Date	Author	Description
0.5	2022-06-08	AutoChips	Initial version(design parameters and some estimated parameters are used)
1.0	2022-12-28	AutoChips	Formal version(actual test parameters are used)
1.1	2023-03-16	AutoChips	Added DFlash lifetime parameter (Section 7.3);Added PFlash dual Bank information(Section 1)
1.2	2023-06-25	AutoChips	Add New Part Number

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1 Key features

- **Automotive grade**
  - AEC-Q100 Grade 1 qualified
  - ISO26262 ASIL-B qualified
- **Performance**
  - Up to 120 MHz ARM® Cortex-M4F core
  - Integrated DSP
  - Float Point Unit(FPU)
  - Fast I/O access port
- **Memories and memory interfaces**
  - On-chip Flash, including PFlash up to 1 MB(Including 2 banks, 512KB+512KB)and DFlash up to 128 KB, both PFlash and DFlash support ECC
  - Up to 124 KB SRAM, ECC is supported
  - 4 KB FlexRAM
- **CSE(Cryptographic Services Engine)**
  - Support AES-128 ECB, CBC, CMAC
  - Support secure boot mode
  - Comply with SHE specification
  - Support TRNG, PRNG
  - Secure cryptographic key storage (Support up to 17 user keys)
- **Clocks**
  - oscillator (OSC) - supports 4 MHz to 30 MHz quartz crystal resonator; choice of low power or high gain oscillators, or up to 50MHz external input clock
  - System PLL - internal PLL with internal or external reference to to generate 120 MHz system clock
  - Internal 128 kHz low-power oscillator (LSI)
  - High Speed Internal Clock (HSI) — internal RC oscillator provides 8 MHz clock source
  - Ultra High Speed Internal Clock(VHSI) — internal RC oscillator provides 48 MHz clock source
- **Power Management**
  - Power Management Module (PMC) with five power modes: RUN、STOP1、STOP2、VLPR、VLPS
  - Low-voltage detection with reset (LVD/LVR)
- **System peripherals**
  - Watchdog with independent clock source(WDOG/External WDG(EWDG))
  - Programmable cyclic redundancy check module(CRC)
  - JTAG/SWD debug interface

- One 16-channel DMA

- **Human-machine interface**
  - Up to 128 general-purpose input/output (GPIO)
  - External interrupt (IRQ)

- **Analog modules**
  - Two ADC , each up to 28-channel(outer 24 channels, inner 4 channels) , 1Msps@12 bit/1.33Msps@10 bit/1.46Msps@8 bit SAR ADC, optional hardware trigger (ADC)
  - One analog comparators(ACMP) containing a 8-bit DAC and programmable reference input

- **Timer**
  - Up to six 8-channel complementary PWM
  - One 4-channel periodic interrupt timer (TIMER)
  - One 16-bit pulse counter(PCT)
  - One real-time counter (RTC)
  - Two programmable delay timer (PDT)

- **Communication interfaces**
  - Up four CAN-FD modules, compatible with CAN 2.0B
  - Four UART modules (supporting 4-ch Software LIN)
  - Three SPI modules
  - One I2C module
  - One EIO module, supporting up to 4 Timers and 4 Shifters

- **Operating characteristics**
  - Voltage range: 2.7 to 5.5 V
  - Temperature range(ambient): -40 to 125°C

- **Package**
  - 144-pin LQFP
  - 100-pin LQFP
  - 64-pin LQFP

2 Block diagram

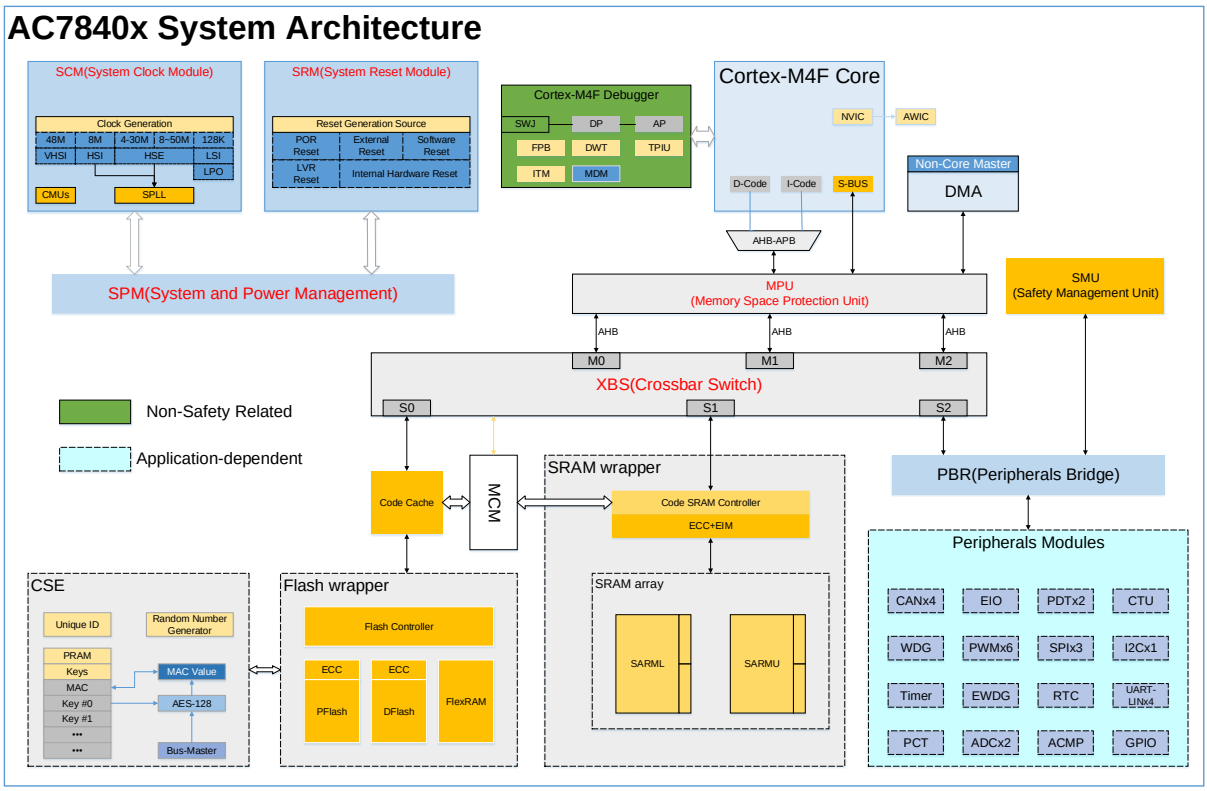


Figure 2-1 AC7840x Block Diagram

3 Part Identification

3.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

3.2 Format

Part numbers for this device have the following format:

AC## GTUFPN

3.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid).

Table 3-1 Fields

Field	Description	Value
AC	AutoChips	• AC
7	AutoChips MCU family	• 7
8	General Purpose Automotive MCU	• 8
4	Core Platform	• 4 = Cortex-M4
0	Specific Function Bit	• 0 = performance/version bit • 7/6/5/3 = Product subfamily 7: 4-ch CAN-FD, Crypto is supported,support ISELED 6: 4-ch CAN-FD, Crypto is supported 5: 3-ch CAN-FD, Crypto is supported 3: 3-ch CAN-FD, Crypto is not supported
6		
Y	Pin Count	• H = 64 • L = 100 • Y = 144
G	Flash Memory Size	• F = 512KB • G = 1024KB
L	Package type	• L = LQFP • Q = QFN • T = TSSOP
A	Temperature range (°C)	• A = AEC-Q100 Grade 1(-40~125°C)

		• I = -40~105°C C= -40~85°C

3.4 Example

This is an example part number: AC78406YGLA.

4 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the following classification is used and the parameters are tagged accordingly in the tables where appropriate.

Table 4-1 Parameter classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

5 Rating

5.1 Thermal handling ratings

Table 5-1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
TSTG	Storage temperature	–55	150	°C	1
TSDR	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, High Temperature Storage Life.

2. Determined according to IPC/JEDEC Standard J-STD-020, Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.

5.2 Moisture handling ratings

Table 5-2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.

5.3 ESD handling ratings

Table 5-3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	–4000	4000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	–750	750	V	2
I_{LAT}	Latch-up current at ambient temperature of 125°C	–100	100	mA	3

1. Determined according to AEC-Q100-002-D,HUMAN BODY MODEL ELECTROSTATIC DISCHARGE TEST.

2. Determined according to AEC-Q100-011-C1,CHARGED DEVICE MODEL (CDM) ELECTROSTATIC DISCHARGE TEST.

3. Determined according to AEC-Q100-004-D, IC LATCH-UP TEST.

- Test was performed at 125 °C case temperature (Class II).
- Supply groups pass 1.5 Vccmax

5.4 Voltage and current operating ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in the following table may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this document.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pullup resistor associated with the pin is enabled.

Table 5-4 Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V_{DD1}	Digital supply voltage	–0.3	5.5	V
V_{DD2}	Digital supply voltage	–0.3	5.5	V
V_{DD3}	Digital supply voltage	–0.3	5.5	V
V_{DD4}	Digital supply voltage	–0.3	5.5	V
V_{DD5}	Digital supply voltage	–0.3	5.5	V
V_{DD6}	Digital supply voltage	–0.3	5.5	V
I_{DD}	Maximum current into V_{DD}	—	120	mA
V_{IN}	Input voltage except true open drain pins	–0.3	V_{DD} + 0.1 [1]	V
	Input voltage of true open drain pins	–0.3	V_{DD} + 0.1 [1]	V
I_D	Instantaneous maximum current single pin limit (applies to all port pins)	–20	20	mA
V_{DDA}	Analog supply voltage	V_{DD} – 0.1	V_{DD} + 0.1	V

[1] Maximum rating of V_{DD} also applies to V_{IN}.

6 General

6.1 Nonswitching electrical specifications

6.1.1 Power and ground pins

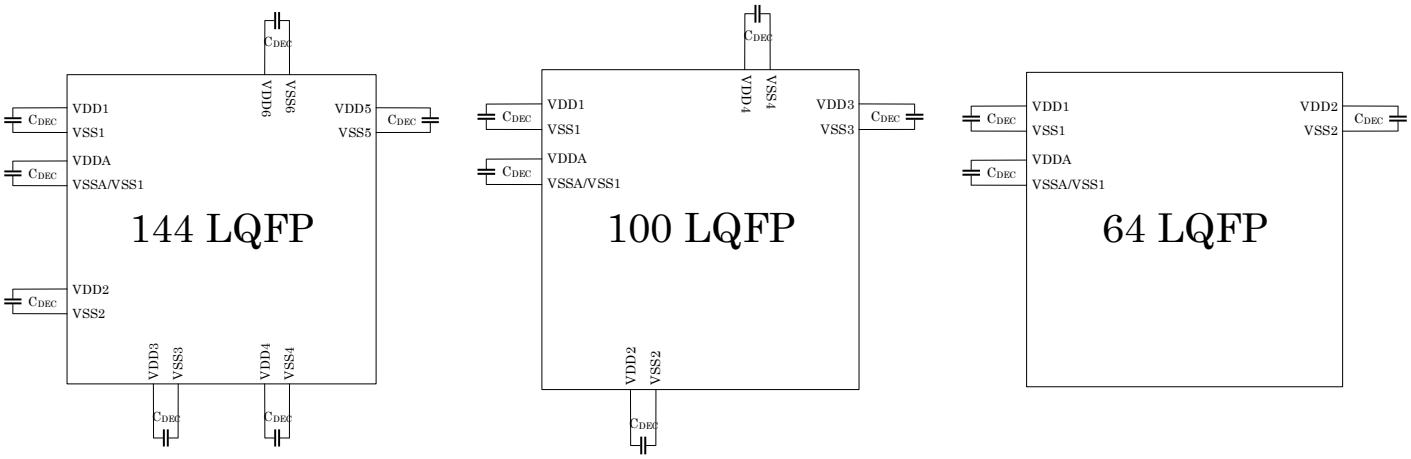


Figure 6-1 Pinout decoupling

1. VDDx and VDDA must be shorted to a common source on PCB.
2. All decoupling capacitors must be low ESR ceramic capacitors (X7R type) , the recommended value is 0.1 uF.
3. For improved performance, it is recommended to use 10 uF, 0.1 uF and 1 nF capacitors in parallel.
4. All decoupling capacitors should be placed as close as possible to the corresponding power and ground pins.

6.1.2 DC characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 6-1 DC characteristics

Symbol	C	Description			Min.	Typ.	Max.	Unit
VDD	P	Operating voltage		—	2.7	—	5.5	V
V_{OH}	P	Output high voltage	drive strength	I_{load} = -5, -20mA	V_{DD} - 0.8	—	—	V
I_{OH}	D		Maximum	5 V	20	—	—	mA
				3.3 V	14	—	—	

		Output high voltage	output high current of single IO -- $I_{OH,}$ high drive configuration					
			Maximum output high current of single IO -- $I_{OH,}$ low drive configuration	5 V	5	—	—`	mA
				3.3 V	3.5	—	—	
I_{OHT}	D	Output high voltage	Max total I_{OH} for all IO ports	—	—	—	100	mA
V_{OL}	P	Output low voltage	drive strength	I_{load}= 5, 20mA	—	—	0.8	V
I_{OL}	D	Output low voltage	Maximum output low current of single IO -- $I_{OL,}$ high drive configuration	5 V	20	—	—	mA
				3.3 V	12	—	—	
			Maximum output low current of single IO -- $I_{OL,}$ low drive configuration	5 V	5	—	—	mA
				3.3 V	3	—	—	
V_{IH}	P	Input high voltage	All digital inputs	4.0≤V_{DD}<5.5 V	0.65×V_{DD}	—	V_{DD} + 0.3	V
				2.7≤V_{DD}<4.0 V	0.70×V_{DD}	—	V_{DD} + 0.3	
V_{IL}	P	Input low voltage	All digital inputs	4.0≤V_{DD}<5.5 V	-0.3	—	0.35×V_{DD}	V
				2.7≤V_{DD}<4.0 V	-0.3	—	0.30×V_{DD}	
V_{hys}	C	Input hysteresis	All digital inputs	—	—	0.03×V_{DD}	—	mV

$\|I_{In}\|$	P	Input leakage current	Per pin (pins in high impedance input mode)	$V_{IN} = V_{DD}$ or V_{SS}	-1	0.1	1	µA
R_{PU}	P	Pullup resistors	All digital inputs and enables internal pullup	$4.0 \le V_{DD} < 5.5$ V	20	—	70	kΩ
				$2.7 \le V_{DD} < 4.0$ V	20	—	70	
R_{PD}	P	Pulldown resistors	All digital inputs and enables internal pulldown	$4.0 \le V_{DD} < 5.5$ V	20	—	70	kΩ
				$2.7 \le V_{DD} < 4.0$ V	20	—	70	
I_{IC}	D	DC injection current	Single pin limit	$V_{IN} < V_{SS}$, $V_{IN} > V_{DD}$	-3	—	3	mA
			Total MCU limit, including sum of all stressed pins		—	—	30	
C_{In}	C	Input capacitance, all pins		—	—	5	7	pF

Table 6-2 LVD /POR / AVDD Voltage warning specification

Symbol	C	Description	Min.	Typ.	Max.	Unit
V_{POR}	D	POR reset voltage [1]	1.6	1.8	2	V
V_{LVDL}	C	Falling edge low-voltage detect threshold—low gear	2.8	2.9	3.0	V
V_{LVDH}	C	Falling edge low-voltage detect threshold—high gear [2]	4.4	4.5	4.65	V
V_{HYSLVD}	C	low-voltage detect hysteresis	—	50	—	mV
V_{LVRH}	C	Falling edge low-voltage reset threshold (RUN /STOP/VLPR)	2.5	2.6	2.7	V
V_{LVRH}	C	Falling edge low-voltage reset threshold (VLPS)	1.97	2.22	2.44	V
V_{HYSPVD}	C	High-gear low-voltage detect hysteresis	—	50	—	mV
V_{BG}	P	Buffered bandgap output [3]	1.18	1.2	1.22	V

[1] Maximum is the highest voltage that POR is guaranteed.

[2] Rising thresholds are falling threshold + hysteresis.

[3] Voltage Factory trimmed at V_{DD} = 5.0 V, T_{emp} = 25 °C.

6.1.3 Power mode

The device supports RUN, STOP1, STOP2, VLPR and VLPS modes.

- RUN - CPU clocks can be run at full speed. After MCU reset, the default operating mode is RUN mode, using VHSI as the system clock.
- STOP1- CPU enters into deep sleep mode, core clock , system clocks and bus clock are disabled.
- STOP2 - CPU enters into deep sleep mode, core clock and system clocks are disabled, bus clock is enabled.
- VLPR - CPU can be run in low speed state. PLL, VHSI and outer HSE are disabled in ths mode, and HSI can only be used as system clock.
- VLPS – CPU enters into deep sleep mode and it is the lowest power mode in AC7840x.

6.1.4 Supply current characteristics

Table 6-3 Supply current characteristics

Power Mode	Scenario	VDD (V)	-40℃	25℃	125℃	Unit
RUN@120MHz	Peripherals off	5	11.625	12.428	73.156	mA
		3.3	11.265	12.074	67.731	
	Peripherals on	5	32.288	31.778	95.944	
		3.3	30.350	30.737	88.369	
RUN@80MHz	Peripherals off	5	11.625	12.429	73.156	
		3.3	11.264	12.075	67.725	
	Peripherals on	5	26.059	25.381	89.056	
		3.3	24.103	24.457	81.825	
RUN@64MHz	Peripherals off	5	11.624	12.429	73.150	
		3.3	11.264	12.074	67.750	
	Peripherals on	5	23.470	22.798	86.200	
		3.3	21.532	21.917	79.113	
RUN@48MHz	Peripherals off	5	11.624	12.429	73.125	
		3.3	11.264	12.075	67.725	
	Peripherals on	5	20.213	19.480	82.294	
		3.3	18.310	18.661	75.419	
STOP1	—	5	4.171	4.953	65.606	mA
		3.3	4.015	4.856	60.875	
STOP2	—	5	4.482	5.264	65.913	mA
		3.3	4.323	5.164	61.175	
VLPR	Peripherals on 1	5	2.888	2.625	62.050	mA
		3.3	2.223	2.539	57.506	

	Peripherals on 2	5	4.158	3.005	63.431	mA
		3.3	3.034	2.909	58.138	
	Peripherals off	5	2.217	2.612	62.000	mA
		3.3	2.065	2.526	57.475	
VLPS	Peripherals off	5	—	—	—	—
		3.3	—	—	—	
	Timer on	5	—	—	—	—
		3.3	—	—	—	
IDD/MHz[1]	—	5	145.313	155.363	914.450	uA/MHz
	—	3.3	140.800	150.938	846.563	

[1] This value is measured at RUN@80MHz and the peripheral are off

The detailed descriptions of the measurement scene are shown in the table below.

Table 6-4 Test scenarios detailed description

Module	**VLPS(Peripherals off)**	**VLPS(TIMER off)**	**VLPR(Peripherals off)**	**VLPR (Peripherals on 1)**	**VLPR (Peripherals on 2)**	**STOP1**	**STOP2**	**RUN(48/64/80/120MHz) (Peripherals off)**	**RUN(48/64/80/120MHz) (Peripherals on)**
Core module									
NVIC	OFF	OFF	ON	ON	ON	OFF	OFF	ON	ON
System module									
SPM/PMC	ON	ON	ON	ON	ON	ON	ON	ON	ON
Voltage regulator	Stop	Stop	Stop	Stop	Stop	Run	Run	Run	Run
LVD/LVR	LVD OFF/LVR ON	LVD OFF/LVR ON	LVD OFF/LVR ON	LVD OFF/LVR ON	LVD OFF/LVR ON	LVD/LVR ON	LVD/LVR ON	LVD/LVR ON	LVD/LVR ON`
BOD	ON	ON	ON	ON	ON	ON	ON	ON	ON

DMA	OFF	OFF	OFF	OFF	DMA:ON, DMA from SRAML to SRAMU once each 8ms	OFF	OFF	OFF	DMA:ON, DMA from Flash to SRAMU once each 8ms
WDG	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF
EWDG	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
Clock module									
128kHz LSI	OFF	ON	ON	ON	ON	ON	ON	ON	ON
PLL	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON RUN@48MHz: OFF	ON RUN@48MHz: OFF
HSI	OFF	OFF	ON(8MHz)	ON(8MHz)	ON(8MHz)	ON(8MHz)	ON(8MHz)	OFF	OFF
VHSI	OFF	OFF	OFF	OFF	OFF	ON(48MHz)	ON(48MHz)	ON(48MHz)	ON(48MHz)
HSE	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON
SCG	LSI as clock source	LSI as clock source of TIMER	HSI as clock source	HSI as clock source	HSI as clock source	All clock source	All clock source	All clock source, HSI off	All clock source, HSI off

Core Clock	OFF	OFF	4 MHz (HSI as clock source)	4 MHz (HSI as clock source)	1 MHz (HSI as clock source)	OFF	OFF	Run@80 MHz:80 MHz(PLL as clock source, HSE:8 MHz) Run@64 MHz:64 MHz(PLL as clock source, HSE:8 MHz) Run@48 MHz:48 MHz (48MHz as clock source)	Run@80 MHz:80 MHz(PLL as clock source, HSE:8 MHz) Run@64 MHz:64 MHz(PLL as clock source, HSE:8 MHz) Run@48 MHz:48 MHz (48MHz as clock source)
System Clock	OFF	OFF	4MHz(HSI as clock source)	4MHz(HSI as clock source)	1MHz(HSI as clock source)	OFF	OFF	Run@80 MHz:80 MHz(PLL as clock source, HSE:8 MHz)	Run@80 MHz:80 MHz(PLL as clock source, HSE:8 MHz)

								Run@64 MHz:64 MHz(PLL as clock source, HSE:8 MHz) Run@48 MHz:48 MHz (48MHz as clock source)	Run@64 MHz:64 MHz(PLL as clock source , HSE:8 MHz) Run@48 MHz:48 MHz (48MHz as clock source)
Bus Clock	OFF	OFF	2MHz(HIS as clock source)	2MHz(HSI as clock source)	1MHz(HSI as clock source)	OFF	48MHz(VHSI as clock source)	Run@80 MHz:40 MHz Run@64 MHz:32 MHz Run@48 MHz:48 MHz	Run@80 MHz:40 MHz Run@64 MHz:32 MHz Run@48 MHz:48 MHz
Flash Clock	OFF	OFF	1MHz(HSI as clock source)	1MHz(HSI as clock source)	1MHz(HSI as clock source)	OFF	24MHz(VHSI as clock source)	Run@80 MHz:20 MHz Run@64 MHz:16 MHz Run@48 MHz:24 MHz	Run@80 MHz:20 MHz Run@64 MHz:16 MHz Run@48 MHz:24 MHz
Memory and memory interfaces									

Flash Memory	Low power(non-read/program/erase)	Low power(non-read/program/erase)	Low power(non-read/program/erase)	Low power(non-read/program/erase)	ON(maximum read 1 MHz, non-program/erase)	Low power(non-read/program/erase)	Low power(non-read/program/erase)	ON	ON
Flash pre-fetch	N/A	N/A	OFF	OFF	OFF	ON	ON	ON	ON
System RAM(SRAMU and SRAML)	Low power(non-read/program/erase)	Low power(non-read/program/erase)	Low power (read& write)	Low power (read& write)	Low power (read& write)	Low power (read& write)	Low power (read& write)	ON	ON
Cache	OFF	OFF	OFF	OFF	OFF	Low power (non-read&non-write)	Low power (non-read&non-write)	ON	ON
Flex Memory	Low power (non-read&non-write)	Low power (non-read&non-write)	Low power (read& write	Low power (read& write	Low power (read& write	Low power (non-read&non-write)	Low power (non-read&non-write)	ON	ON
Communication module									

UART	OFF	OFF	OFF	OFF	3xUART , transmit at the baudrate 19200 each 100ms	OFF	OFF	OFF	3xUART, transmit at the baudrate 19200 each 100ms
SPI	OFF	OFF	OFF	OFF	SPI0/1/2, transmit once at the baudrate 500kps each 5ms	OFF	OFF	OFF	SPI0@Run@80MHz:20Mbps RUN@64 and 48MHz, transmit once at the baudrate 16Mbps each 5ms SPI1/2, transmit once at the baudrate 1Mbps each 5ms

I2C	OFF	OFF	OFF	OFF	1xLPI2C, transmit once each 100 ms	OFF	OFF	OFF	1xLPI2C, transmit once each 100 ms
EIO	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
CAN	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	3xFlexCAN@500Kbps
Security Module									
CRC	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
Timer Module									
PWM	OFF	OFF	OFF	OFF	PWM0 CH0-7 400Hz PWM PWM1 CH0-7 200Hz PWM FMT2 CH5 20KHz PWM PWM3 CH0-7 200Hz PWM	OFF	OFF	OFF	PWM0 CH0-7 400Hz PWM PWM1 CH0-7 200Hz PWM FMT2 CH5 20KHz PWM PWM3 CH0-7 200Hz PWM
Timer	OFF	OFF	OFF	OFF	LPIT:ON,	OFF	OFF	OFF	LPIT:ON,

					an interrupt is generated every 1ms				an interrupt is generated every 1ms
PDT	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
PCT	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF
RTC	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
Analog Module									
12-bit ADC	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ADC0 7CH ON@48 MHz, convert once every 3ms ADC1 7CH ON@48 MHz, convert once every 3ms
ACMP	OFF	OFF	OFF	OFF	ACMP 2 Ch ON	OFF	OFF	OFF	ACMP 2 Ch ON@48 MHz
PAD interface									

IOs Enable	OFF	OFF	OFF	PC6,PC7,PC8,PC9,PC10,PC11,PC12,PC13	PC6,PC7,PC8,PC9,PC10,PC11,PC12,PC13, , the corresponding peripheral IOs are enabled	OFF	OFF	OFF	The corresponding peripheral IOs are enabled

6.1.5 Behavior of power mode transition

All specifications in Table 6-5 use the following clocking configuration.

- RUN
  - Clock source: VHSI
  - SYS_CLK/CORE_CLK = 48 MHz
  - BUS_CLK = 48 MHz
- VLPR
  - Clock source: HSI
  - SYS_CLK/CORE_CLK = 8 MHz
  - BUS_CLK = 8 MHz
- STOP1/STOP2
  - Clock source: VHSI
  - SYS_CLK/CORE_CLK = OFF
  - BUS_CLK = 48 MHz
- VLPS: all clock sources are turned off.

Table 6-5 Bahaviors of power mode transition

Symbol	Description	Min.	Typ.	Max.	Unit
t_{POR}	After a POR event, the time length between when VDD reaches 2.7 V and when the first instruction is executed within the operating temperature range of the chip.	—	325	—	μs
—	VLPS → RUN	14	—	21	μs
—	STOP1 → RUN	0.5	—	1.46	μs
—	STOP2 → RUN	0.5	—	1.46	μs
—	VLPR → RUN	—	1.5	—	μs

—	VLPS → VLPR	—	20	—	µs
—	RUN → STOP1	—	0.4	—	µs
—	RUN → STOP2	—	0.4	—	µs
—	RUN → VLPS	—	35	—	µs
—	RUN → VLPR	—	0.9	—	µs
—	Pin reset → code execution	—	214	—	µs

6.2 Switching specifications

6.2.1 Control timing

Table 6-6 Control timing

No.	Symbol	C	Rating		Min.	Typ.[1]	Max.	Unit
1	f_{Sys}	D	System and core clock (t_{sys} = 1/f_{Sys})		DC	—	120	MHz
2	f_{Bus}	P	Bus frequency (t_{cyc} = 1/f_{sys})		DC	—	60	MHz
3	f_{LSI}	P	Internal low power oscillator frequency		—	128	—	KHz
4	t_{extrst}	D	External reset pulse width [2]		1.5 × t_{sys}	—	—	ns
5	t_{ILIH}/ t_{IHIL}	D	IRQ pulse width	RUN [3]	1.5 × t_{sys}	—	—	ns
	—	—		VLPR	1.5 × t_{sys}	—	—	—
	—	—		STOP1	1.5 × t_{sys}	—	—	—
	—	—		STOP2	1.5 × t_{sys}	—	—	—
	t_{ILIH}/t_{IHIL}	D		VLPS	1.5 × t_{sys}	—	—	—
6	t_{Rise}	C	Port rise and fall time - Normal drive strength (load = 50 pF) [4]	—	—	10.2	—	ns
	t_{Fall}	C			—	9.5	—	ns
	t_{Rise}	C	Port rise and fall time - high drive strength (load = 50 pF) [4]	—	—	3	—	ns
	t_{Fall}	C			—	3	—	ns

[1] Typical values are based on characterization data at V_{DD}=5.0 V, 25 °C unless otherwise stated.

[2] This is the shortest pulse that is guaranteed to be recognized as a RESET_B pin request.

[3] This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized.

[4] Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature ranges -40 °C to 125 °C.

6.2.2 PWM module timing

Synchronizer circuits determine the shortest input pulses that can be recognized. These synchronizers operate from the PWM clock.

Table 6-7 PWM input timing

No.	Symbol	C	Description	Min.	Max.	Unit
1	f_{PWM}	D	Timer clock frequency	—	120M	Hz
2	f_{Tclk}	D	Outer clock frequency	0	$f_{PWM}/4$	Hz
3	t_{Tclk}	D	Outer clock cycle	4	—	t_{PWM} [1]
4	t_{clkh}	D	Outer clock high level	1.5	—	t_{PWM}
5	t_{clkl}	D	Outer clock low level	1.5	—	t_{PWM}
6	t_{ICPW}	D	Input capture pulse width	1.5	—	t_{PWM}

[1] $t_{PWM}=1/f_{PWM}$.

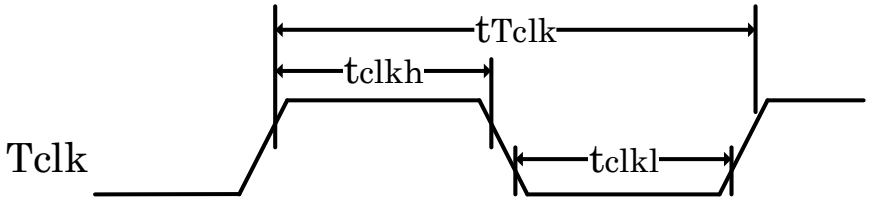


Figure 6-2 Timer outer clock

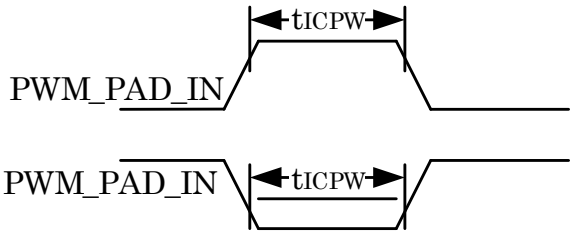


Figure 6-3 Timer outer input capture pulse

PWM_PAD_IN represents the chip pin input corresponding to PWM.

6.3 Thermal specifications

6.3.1 Thermal characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin.

Table 6-8 Thermal characteristics

Board type	Symbol	Description	144 LQFP	100 LQFP	64 LQFP	Unit	Notes
Dual-layer (1s1p)	θ_{JA}	Thermal resistance, junction to ambient (natural convection)	46.0	64.59	64.83	°C/W	1, 2
Four-layer (2s2p)	θ_{JA}	Thermal resistance, junction to ambient (natural convection)	38.13	48.22	45.41	°C/W	1, 3
—	θ_{JB}	Thermal resistance, junction to board	26.13	28.74	23.46	°C/W	4
—	θ_{JC}	Thermal resistance, junction to case	11.6	16.3	13.2	°C/W	5
Dual-layer (1s1p)	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center(natural convection)	24.66	27.26	19.5	°C/W	6
Four-layer (2s2p)	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center(natural convection)	24.46	27.04	19.33	°C/W	6
Dual-layer (1s1p)	Ψ_{JB}	Thermal characterization parameter, junction to package bottom outside center(natural convection)	25.06	27.78	20.75	°C/W	7
Four-layer (2s2p)	Ψ_{JB}	Thermal characterization parameter, junction to package bottom outside center(natural convection)	25.03	27.93	21.33	°C/W	7
Dual-layer (1s1p)	θ_{JMA}	Thermal resistance, junction to ambient (200 ft./min. air speed)	37.73	46.81	49.0	°C/W	1, 3
Four-layer (2s2p)	θ_{JMA}	Thermal resistance, junction to ambient (200 ft./min. air speed)	31.93	40.14	37.5	°C/W	1, 3

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with natural convection for horizontally oriented board. Board meets JESD51-3 specification for 1s board.
3. Per JEDEC JESD51-6 with forced convection for horizontally oriented board. Board meets JESD51-7 specification for 1s or 2s2p board, respectively.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the package bottom plate, ignore contact thermal resistance.
6. Thermal characterization parameter indicating the temperature difference between

package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

7. Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA})$$

Wherein, T_A = Ambient temperature, the unit is °C.

θ_{JA} is package thermal resistance, junction-to-ambient, the unit is °C/W.

$$P_D = P_{int} + P_{I/O}$$

Chip internal power, the unit is Watts.

$$P_{int} = I_{DD} \times V_{DD}$$

$P_{I/O}$: power dissipation on input and output pins - user determined.

For most applications, $P_{I/O} \ll P_{int}$ and can be neglected.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273\,°C)$$

Solving the equations above for K gives:

$$K = P_D \times (T_A + 273\,°C) + \theta_{JA} \times (P_D)^2$$

where K is a constant pertaining to the particular part.

K can be determined by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving the above equations iteratively for any value of T_A.

7 Peripheral operating requirements and behaviors

7.1 Core modules

7.1.1 SWD electricals

Table 7-1 SWD full voltage range electrical

Symbol	Description	Min.	Max.	Unit
—	Operating voltage	2.7	5.5	V
J1	SWD_CLK operation frequency • Serial wire debug	0	12	MHz
J2	SWD_CLK cycle period	1/J1	—	ns
J3	SWD_CLK clock pulse width • Serial wire debug	20	—	ns
J4	SWD_CLK rise and fall times	—	3	ns
J9	SWD_DIO input data setup time to SWD_CLK rise	5	—	ns
J10	SWD_DIO input data hold time after SWD_CLK rise	5	—	ns
J11	SWD_CLK high to SWD_DIO data valid	—	41	ns

7.2 External oscillator (OSC) and ICS characteristics

7.2.1 External oscillator(OSC) characteristics

Table 7-2 OSC specifications (temperature ranges from -40 to 125 °C ambient)

No.	Symbol	C	Description	Min.	Typ.	Max.	Unit
1	f_{hi}	C	Crystal frequency	4	—	30	MHz
2	CL1, CL2	D	Load capacitors	Refer to note [1]			—
3	R_S	D	Series resistor	—	0	—	KΩ
4	t_{CST}	C	Crystal start-up time	—	3	—	ms

[1] For CL1 and CL2, it is recommended to use high-quality external ceramic capacitors designed for high-frequency applications, and selected to match the requirements of the crystal. CL1 and CL2 are usually the same size. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing CL1 and CL2.

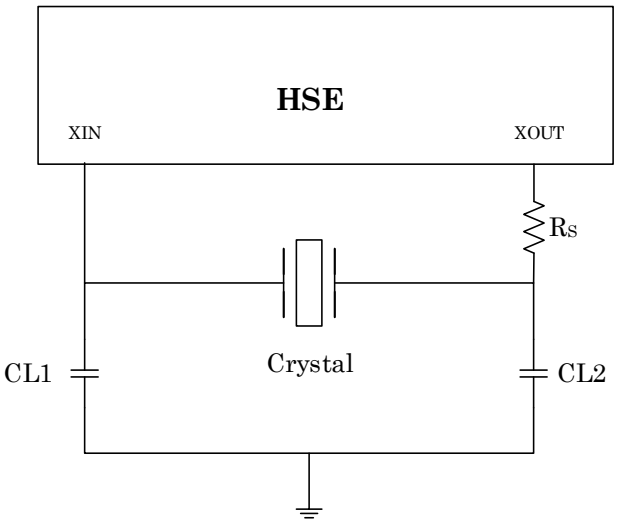


Figure 7-1 Typical crystal or resonator circuit

7.2.2 Internal RC characteristics

Table 7-3 OSC and ICS specifications (temperature range from -40 to 125 °C ambient)

No.	Symbol	C	Characteristics		Min.	Typ.	Max.	Unit
1	f_{HSI}	P	HSI output frequency range	Over temperature range from -40 °C to 125°C	7.9	8	8.1	MHz
2	f_{VHSI}	P	VHSI output frequency range	Over temperature range from -40 °C to 125°C	47.28	48	48.72	MHz
3	f_{LSI}	P	LSI output frequency range	Over temperature range from -40 °C to 125°C	108	128	147	KHz

7.2.3 PLL characteristics

Table 7-4 PLL characteristics

No.	Symbol	C	Parameter	Min.	Typ.	Max.	Unit
1	f_{PLL_IN}	D	PLL input clock frequency	4	—	48	MHz
2	f_{PLL_REF}	D	PLL reference clock frequency	—	—	12	MHz
3	f_{PLL_OUT}	D	PLL output clock frequency	9	—	120	MHz
4	f_{VCO_OUT}	D	VCO output frequency	500	—	1500	MHz
Operating temperature: -40~125°C $f_{PLL\_REF} = f_{PLL\_IN}$ /Prediv, Prediv can be 1,2,4							

No.	Symbol	C	Parameter	Min.	Typ.	Max.	Unit
$f_{VCO\_OUT} = f_{PLL\_REF}$ *Fbkdiv, Fbkdiv can be 5,6,7,...,254,255 $f_{PLL\_OUT} = f_{VCO\_OUT}$ /Postdiv, Postdiv can be 2,4,6,...,60,62							

7.3 Embedded Flash specifications

This section provides details about program/erase time and frequency for the Flash memory.

Table 7-5 Flash characteristics

Symbol		C	Description	Min.	Typ.	Max.	Unit
$V_{Prog/Erase}$		D	Supply voltage for program/erase at temperature from - 40°C to 125 °C	2.7	—	5.5	V
f_{SYS}		D	Flash bus frequency	8	48	120	MHz
t_{RDONCE}		D	Time for Flash read once	4	4	6	t_{cyc}[1]
t_{MER}		D	Mass erase (all main block pages)	—	32	—	ms
t_{MERPF}		D	Mass erase pflash	—	28	—	ms
t_{MERDF}		D	Mass erase dflash	—	26	—	ms
t_{PER}		D	Page erase (one page)	—	820	—	us
t_{MERV}		D	Mass erase verify(all main block pages)	295000	—	590000	t_{cyc} [1]
t_{MERVPF}		D	Mass erase verify pflash	262200	—	524400	t_{cyc}[1]
t_{MERVDF}		D	Mass erase verify dflash	32800	—	65600	t_{cyc}[1]
t_{PERV}		D	Periodical verify(n × 64bit)	2 × n	—	4 × n	t_{cyc}[1]
t_{PRG1}		D	Single program Flash (64bit)	—	95	—	us
t_{PRGn}	n≤8	D	Periodical program Flash (n × 64bit)	—	200	—	us
t_{PRGn}	n>8	D		—	(n/8 + 1) ×200	—	us
n_{EDR}		C	PFlash endurance(erase cycle times – program cycle times) at temperature from - 40°C to 125 °C	10 k	—	—	cycle
		C	DFlash endurance(erase cycle times – program cycle times) at temperature from - 40°C to 125 °C	100 k	—	—	cycle
t_{RET}		C	PFlash data retention time at an average junction temperature of TJavg = 85°C after up to 10,000 program/erase cycles	10	—	—	year
		C	DFlash data retention time at an average junction temperature of TJavg = 85°C after up to 100,000 program/erase cycles	10	—	—	year

[1] $t_{cyc} = 1/ f_{SYS}$.

7.4 Analog

7.4.1 ADC characteristics

Table 7-6 12 bit ADC and Tsensor operating conditions and characteristics

Symbol	C	Description	Condition	Min.	Typ.	Max.	Unit
V_{AVDD}	D	Supply Voltage	Absolute value	2.7	—	5.5	V
V_{REFH}	D	Positive reference input	Absolute value	2.7	—	V_{AVDD}	V
V_{REFL}	D	Negative reference input	Absolute value	—	0	—	V
V_{IN}	D	Input Voltage Range	—	0	—	V_{AVDD}/ V_{REFH}	V
R_{IN}	D	Input source impedance	Refer to the formula [1]	—	—	—	Ω
C_{ADC}	D	Internal Sampling Capacitor	—	—	2.4	—	pF
R_{ADC}	D	Sampling switch resistance	—	—	—	3.1	KΩ
f_{ADC}	D	ADC clock frequency	—	—	—	30	MHz
Ts	D	ADC sampling cycle	—	5/10/15/23/35/45/85/185			cycle
f_{sample}	D	Sampling time	—	—	Ts/f_{ADC}	—	s
f_{trig}	D	Conversion rate(including sampling time)	12bit: f_{ADC}=30MHz; Ts=15 cycles	—	1	—	MHz
			10bit: f_{ADC}=30MHz; Ts=10 cycles	—	1.33	—	MHz
			8bit: f_{ADC}=30MHz; Ts=10 cycles	—	1.46	—	MHz
INL	C	Integral non-linearity[2]	12bit	-3	1.5	3	LSB
DNL	C	Differential non-linearity[2]	12bit	-1	1.5	3	LSB
TUE	C	Total Unadjustable Error[2]	12bit	-8		8	LSB
CH	D	External channels	—	—	—	24	—

[1] The relationship between input source impedance and sampling time must satisfy the formula: $R_{IN} < \frac{T_s}{f_{ADC} * C_{ADC} * ln(2^{N+2})} - R_{ADC}$, N is the ADC bits, ADC sampling duration must meet the settling accuracy of 0.25LSB, and the parasitic capacitance of the PAD terminal is not considered in the formula.

[2] The test conditions of INL, DNL, and TUE are: 12bit, the conversion rate is 1MSPS, and the power supply and reference voltage are greater than 3V.

Table 7-7 12 bit ADC and Tsensor operating conditions and characteristics(continue)

Symbol	C	Description	Condition	Min.	Typ.	Max.	Unit
Slope	D	Temperature sensor slope	-40 °C–125 °C	—	1.788	—	mV/°C
V_{TEMP25}	D	Temperature sensor voltage	25 °C	—	0.673	—	V

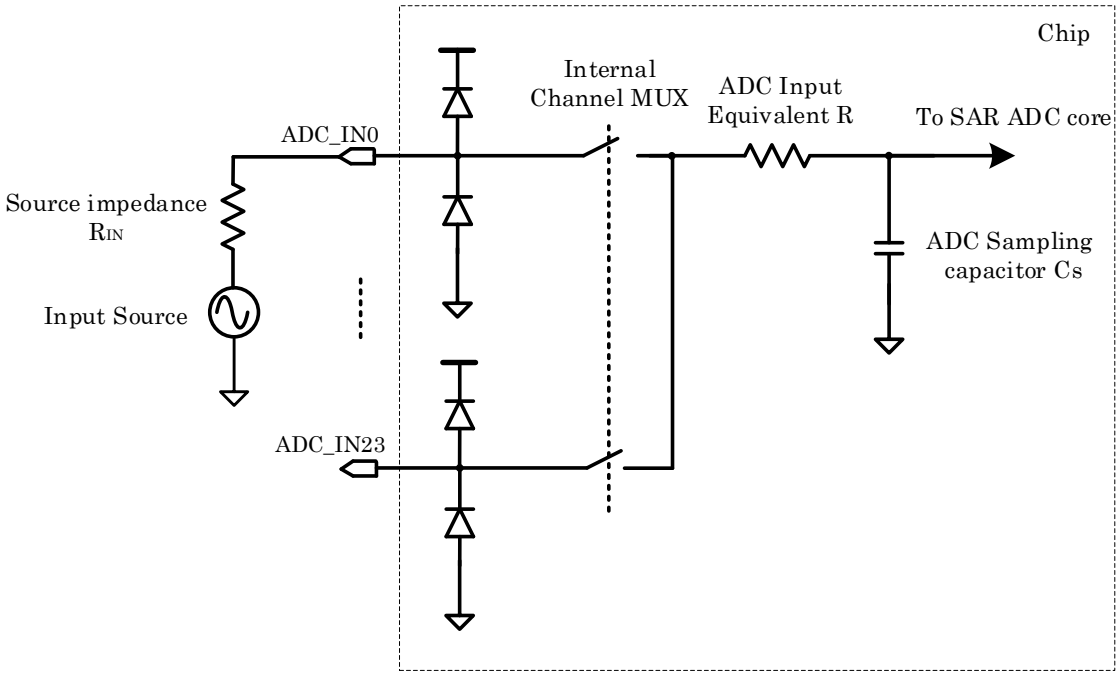


Figure 7-2 ADC input equivalent diagram

7.4.2 Analog comparator (ACMP) electricals

Table 7-8 Comparator electrical specifications

Symbol	C	Description	Min.	Typ.	Max.	Unit
V_{AVDD}	D	Supply voltage	2.7	—	5.5	V
I_{DDA}	T	Supply current (Operation mode)	—		20	μA
V_{AIN}	D	Analog input voltage	0	—	V_{AVDD}	V
V_{AIO}	P	Analog input offset voltage	-30	—	30	mV
V_{HYS}	C	Analog comparator hysteresis (HYST=0)	—	0/10/20/40	—	mV
I_{DDAOFF}	D	Supply current (Off mode)	—	—	100	nA
t_D	C	Propagation delay	—	0.4	1	μs

7.5 Communication interfaces

7.5.1 SPI specifications

The serial peripheral interface(SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes. See the SPI chapter of the chip's reference manual for information about the modified transfer formats used for communicating with slower peripheral devices. All timing is shown with respect to 20% V_{DD} and 80% V_{DD}. All timing assumes slew rate control is disabled and high-drive strength is enabled for SPI output pins.

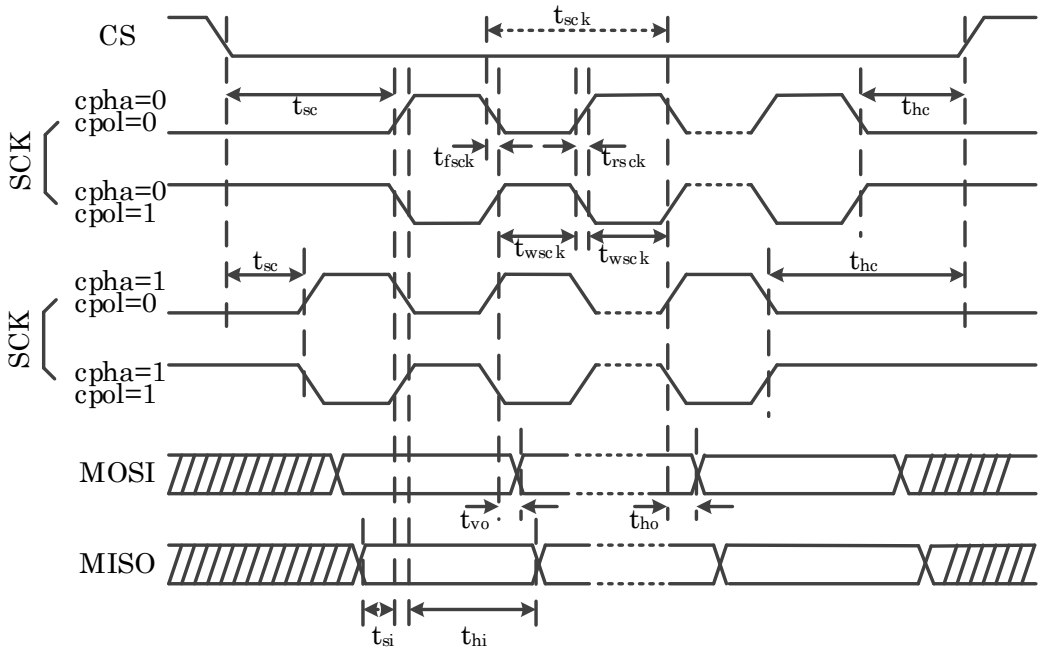


Figure 7-3 SPI timing diagram —master

Table 7-9 SPI characteristics – master

Symbol	Description	Min.	Max.	Unit	Note
f_{op}	Operation frequency	f_{clk}/512	15	MHz	f_{clk} is SPI functional clock
t_{sc}	CS setup time	1×t_{clk}	256×t_{clk}	ns	Time from Negative edge of CS to the first SCK edge(t_{clk} is the SPI functional clock cycle)
t_{hc}	CS hold time	1×t_{clk}	256×t_{clk}	ns	Time from last SCK edge to positive edge of CS
t_{wsck}	SCK high or low level time	1×t_{clk}	256×t_{clk}	ns	No considering t_{rsck} and t_{fsck}
t_{si}	Data input setup time	10	—	ns	—
t_{hi}	Data input hold time	5	—	ns	—
t_{vo}	Data output valid time	—	5	ns	—
t_{ho}	Data output hold time	-5	—	ns	—

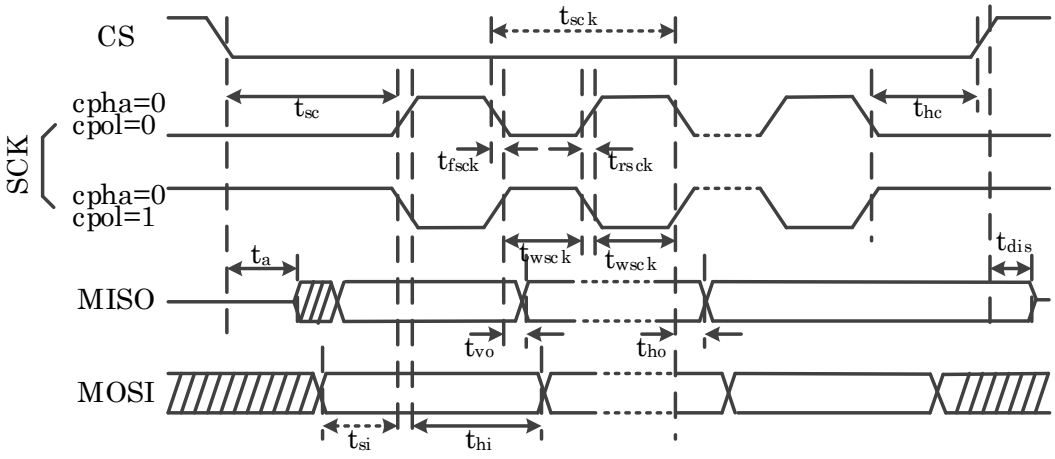


Figure 7-4 SPI timing diagram –slave(cpha=0)

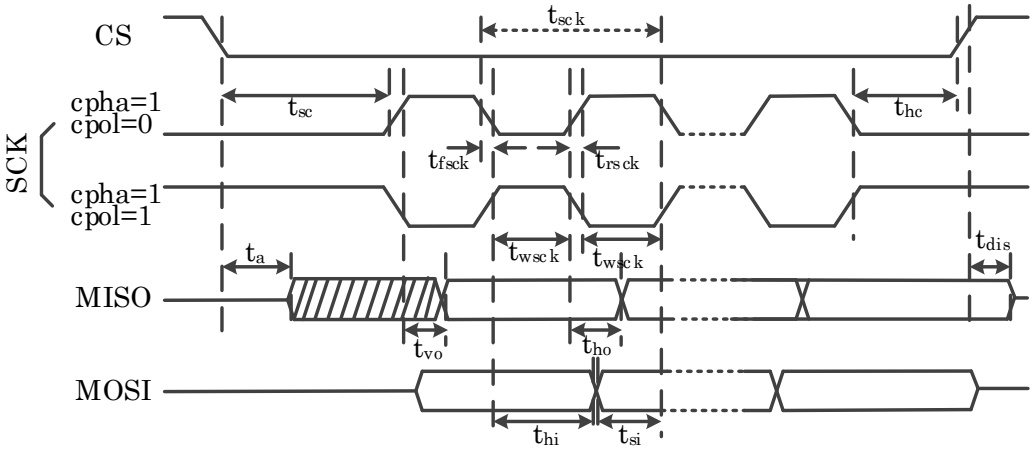


Figure 7-5 SPI timing diagram –slave(cpha=1)

Table 7-10 SPI characteristicss– master

Symbol	Descriptiom	Min.	Max.	Unit	Note
f_{op}	Operation frequency	—	15M	Hz	—
t_{sc}	CS setup time	$2\times t_{bus}$	—	ns	Time from negative edge of CS to the first SCK edge(t_{bus} is SPI APB bus clock)
t_{hc}	CS hold time	$2\times t_{bus}$	—	ns	Time from last SCK edge to positive edge of CS
t_a	Slave access time	—	15	ns	Data from “Z” to effective
t_{dis}	Slave MISO disable time	—	12	ns	Data from effective to “Z”
t_{si}	Data input setup time	15	—	ns	—
t_{hi}	Data input hold time	12	—	ns	—
t_{vo}	Data output valid time	—	30	ns	—
t_{ho}	Data output hold time	16	—	ns	—

7.5.2 CAN specifications

Table 7-11 CAN wake-up pulse characteristics

Symbol	Description	Min.	Typ.	Max.	Unit
t_{WUP}	CAN dominant wakeup pulse parameter filtered	—	—	0.9	µs
t_{WUP}	CAN dominant wakeup pulse parameter effective	4.7	—	—	µs

7.5.3 UART specifications

Basic function of Universal Asynchronous Receiver/Transmitter (UART) is to transmit and receive the serial data bit by bit. In order to support transmitting break field, sync field and data, additional Soft Local Interconnect Network(LIN) is included in the AC7840x chips. The main parameters of UART is introduced as below:

1. Up to 4 UART function channels and all of which support soft LIN functions (the uart function and soft LIN function of the same UART cannot be used at the same time).
2. UART can transmit or receive data with the range of baud rate from 600 bps to 3 Mbps, and the tolerance of real baud rate with ideal baud rate is less than 1%.
3. The minimum GPIO pin interrupt pulse width is 133 ns. Because of that these pins do not have a passive filter on the inputs, this is the shortest pulse width that is guaranteed to be recognized.
4. The maximum baud rate supported in soft LIN function is 20 Kbps.
5. Auto baud rate detection is selectable open or not in soft LIN function. The tolerance of received baud rate is from -20%(+/-2%) to +23% (+/-2%) in this case.
6. For the 4 UART function channels, only 0~2 channels support the function of hardware flow control.

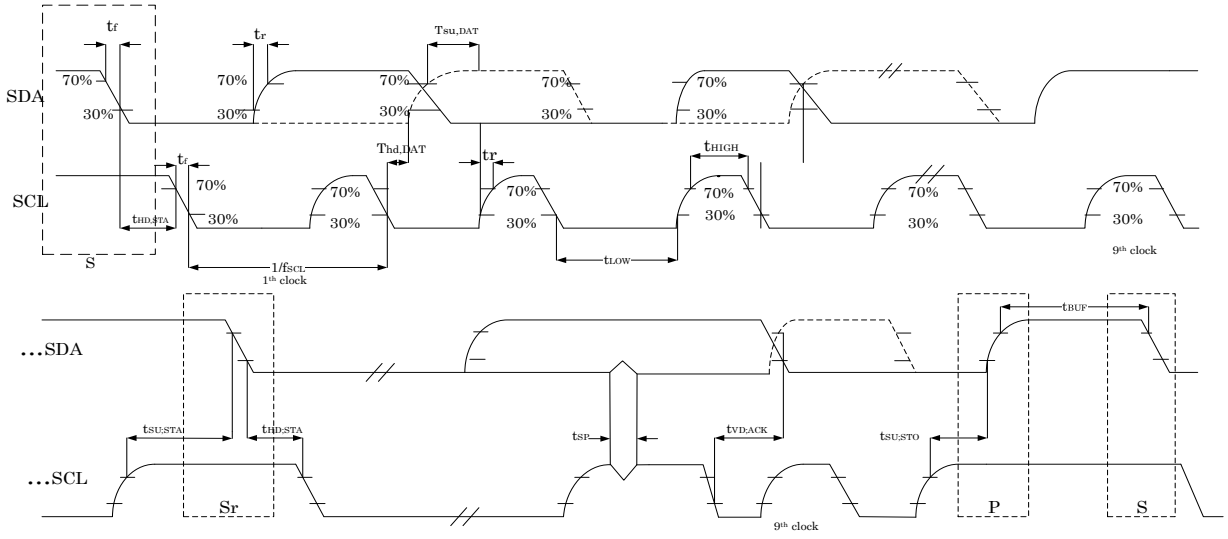
7.5.4 I2C specifications

Table 7-12 Characteristics of the I2C bus lines for different mode[1]

Symbol	Description	Standard-mode		Fast-mode		Fast-mode Plus		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{SCL}	SCL clock frequency	0	100	0	400	0	1000	KHz
$t_{HD;STA}$	hold time (repeated) START condition	4	—	0.6	—	0.26	—	µs
t_{LOW}	LOW period of the SCL clock	4.7	—	1.3	—	0.5	—	µs
t_{HIGH}	HIGH period of the SCL clock	4	—	0.6	—	0.26	—	µs

$t_{SU;STA}$	set-up time for a repeated START condition	4.7	—	0.6	—	0.26	—	µs
$t_{HD;DAT}$	Data hold time	0	—	0	—	0	—	µs
$t_{SU;DAT}$	Data setup time	250	—	100	—	50	—	ns
t_r	Rise time of both SDA and SCL signals	—	1000	20	300	—	120	ns
t_f	Fall time of both SDA and SCL signals	—	300	20 × (V_{DD} / 5.5 V)	300	20 × (V_{DD} / 5.5 V)	120	ns
$t_{SU;STO}$	Set-up time for STOP condition	4	—	0.6	—	0.26	—	µs
t_{BUF}	Bus free time between a STOP and START condition	4.7	—	1.3	—	0.5	—	µs
C_b	Capacitive load for each bus line	—	400	—	400	—	550	pF
$t_{VD;DAT}$	Data valid time	—	3.45	—	0.9	—	0.45	µs
$t_{VD;ACK}$	Data valid acknowledge time	—	3.45	—	0.9	—	0.45	µs
V_{nL}	Noise margin at the LOW level	0.1V_{DD}	—	0.1V_{DD}	—	0.1V_{DD}	—	V
V_{nH}	Noise margin at the HIGH level	0.2V_{DD}	—	0.2V_{DD}	—	0.2V_{DD}	—	V

[1]:I2C supports three modes: standard mode, fast mode and fast mode plus.



V_{IL}=0.3V_{DD}
V_{IH}=0.7V_{DD}

Figure 7-6 Timing for F/S-mode devices on the I2C-bus

7.5.5 EIO specifications

EIO (Enhanced IO) is a highly configurable module that provides a wide range of functions, including:

- Emulate various serial communication protocols
- Four flexible 16-bit timers supporting trigger, reset, enable and disable conditions
- Four configurable 32-bit shifters supporting transmit, receive and match memory

With 4 timers and 4 shifters, the EIO module can support a wide range of protocols, including but not limited to:

- UART transmit and receive
- I2C master
- SPI master and slave
- I2S master and slave
- PWM waveform generation

8 Dimensions

8.1 LQFP144 package information

8.1.1 LQFP144 package dimension information

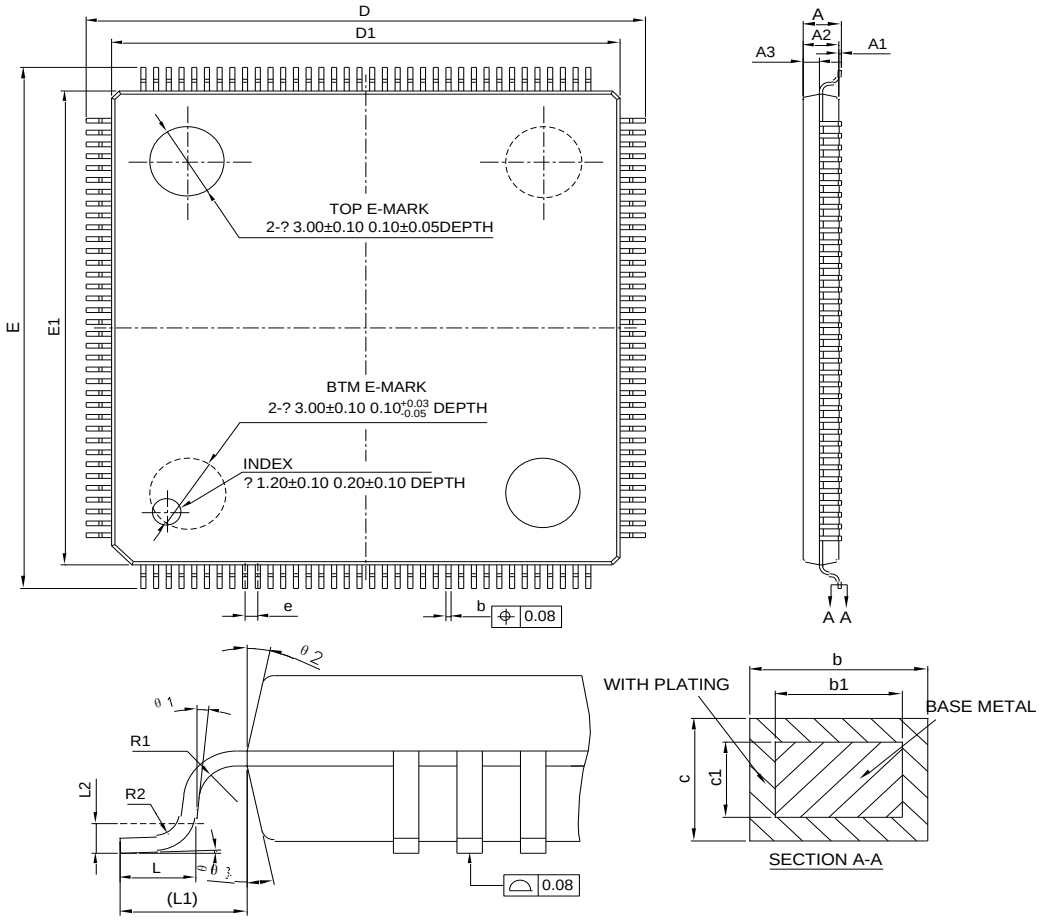


Figure 8-1 LQFP144 – 144 pin, 20*20 mm Low Profile Quad Flat Package Outline [1]

[1] Drawing is not to scale.

Table 8-1 LQFP144 – 144 pin, 20*20 mm Low Profile Quad Flat Package Mechanical Data [1]

Item	Symbol	Min.	Nom.	Max.
Total height	A	—	—	1.60
Stand off	A1	0.05	—	0.15
Mold thickness	A2	1.35	1.40	1.45
Leadframe to mold height	A3	0.59	0.64	0.69

Item		Symbol	Min.	Nom.	Max.
Lead width		b	0.17	—	0.27
Lead width without plating		b1	0.17	0.20	0.23
Leadframe thickness		c	0.127	—	0.18
Leadframe thickness without plating		c1	0.119	0.127	0.134
Outer lead distance	X	D	21.80	22.00	22.20
	Y	E	21.80	22.00	22.20
Package size	X	D1	19.90	20.00	20.10
	Y	E1	19.90	20.00	20.10
Lead pitch		e	0.40	0.50	0.60
L		L	0.45	0.60	0.75
Lead length		L1	1.00 REF		
L2		L2	0.25 BSC		
Lead forming arc radius R1		R1	0.08	—	—
Lead forming arc radius R2		R2	0.08	—	—
Angle 1		Θ	0°	—	7°
Angle 2		Θ1	0°	—	—
Angle 3		Θ2	11°	12°	13°
Angle 4		Θ3	11°	12°	13°

[1] Dimensions are expressed in millimeter.

8.1.2 LQFP144 device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

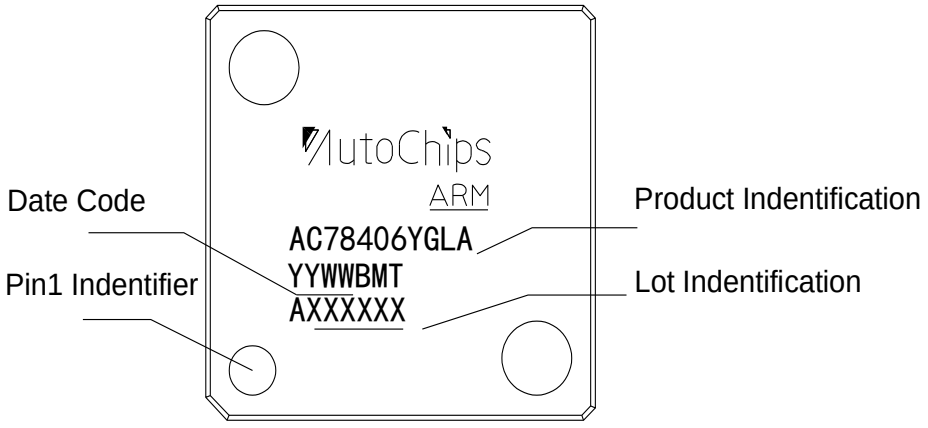


Figure 8-2 LQFP144 marking example (package top view)

8.2 LQFP100 package information

8.2.1 LQFP100 package dimension information

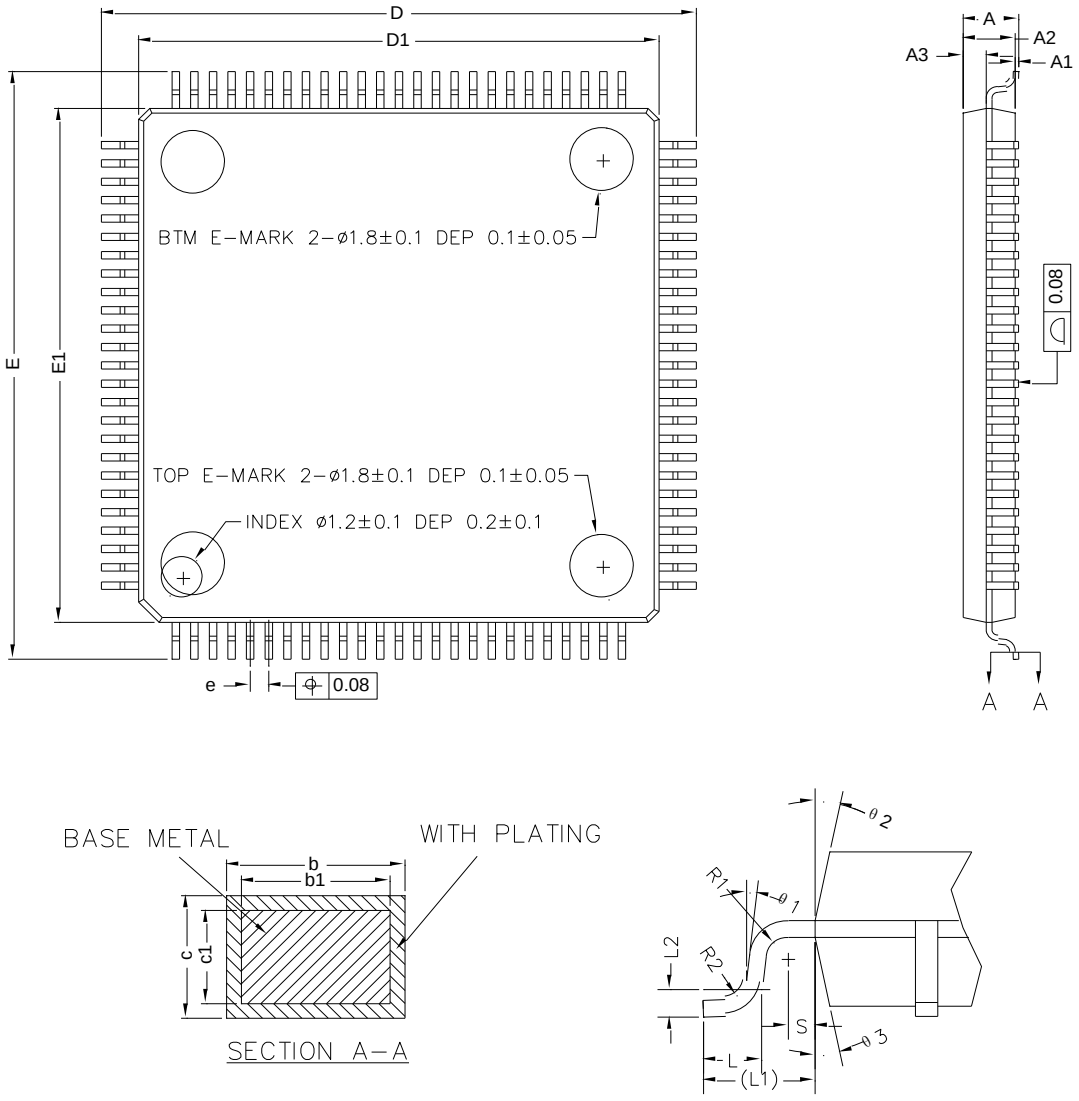


Figure 8-3 LQFP100 – 100 pin, 14x 14 mm Low Profile Quad Flat Package Outline [1]

[1] Drawing is not to scale.

Table 8-2 LQFP100 – 100 pin, 14*14 mm Low Profile Quad Flat Package Mechanical Data [1]

Item	Symbol	Min.	Nom.	Max.
Total height	A	—	—	1.60
Stand off	A1	0.05	—	0.15
Mold thickness	A2	1.35	1.40	1.45
Leadframe to mold height	A3	0.59	0.64	0.69

Item		Symbol	Min.	Nom.	Max.
Lead width		b	0.18	—	0.27
Lead width without plating		b1	0.17	0.20	0.23
Leadframe thickness		c	0.13	—	0.18
Leadframe thickness without plating		c1	0.12	0.127	0.134
Outer lead distance	X	D	15.80	16.00	16.20
	Y	E	15.80	16.00	16.20
Package size	X	D1	13.90	14.00	14.10
	Y	E1	13.90	14.00	14.10
Lead pitch		e	0.40	0.50	0.60
L		L	0.45	0.60	0.75
Lead length		L1	1.00 REF		
L2		L2	0.25 BSC		
Lead forming arc radius R1		R1	0.08	—	—
Lead forming arc radius R2		R2	0.08	—	0.20
Angle 1		Θ	0°	3.5°	7°
Angle 2		Θ1	0°	—	—
Angle 3		Θ2	11°	12°	13°
Angle 4		Θ3	11°	12°	13°

[1] Dimensions are expressed in millimeter.

8.2.2 LQFP100 device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

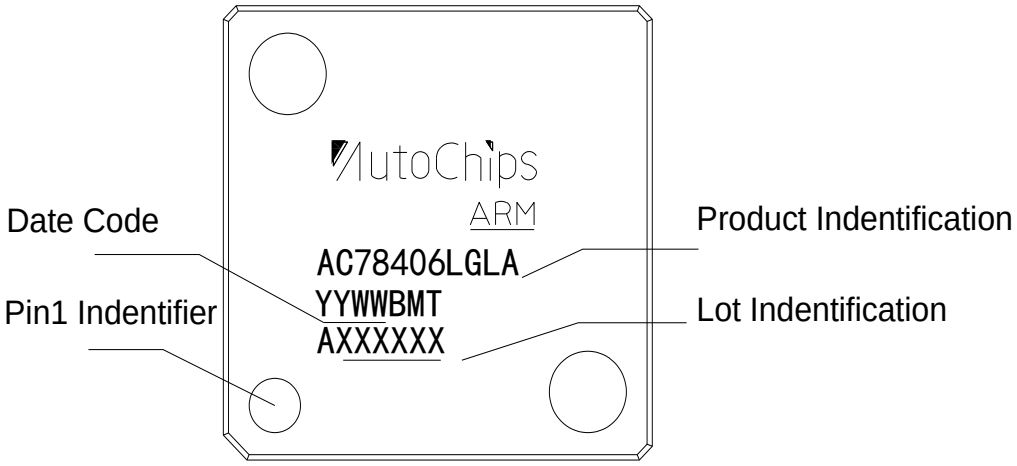


Figure 8-4 LQFP100 marking example (package top view)

8.3 LQFP64 package information

8.3.1 LQFP64 package dimension information

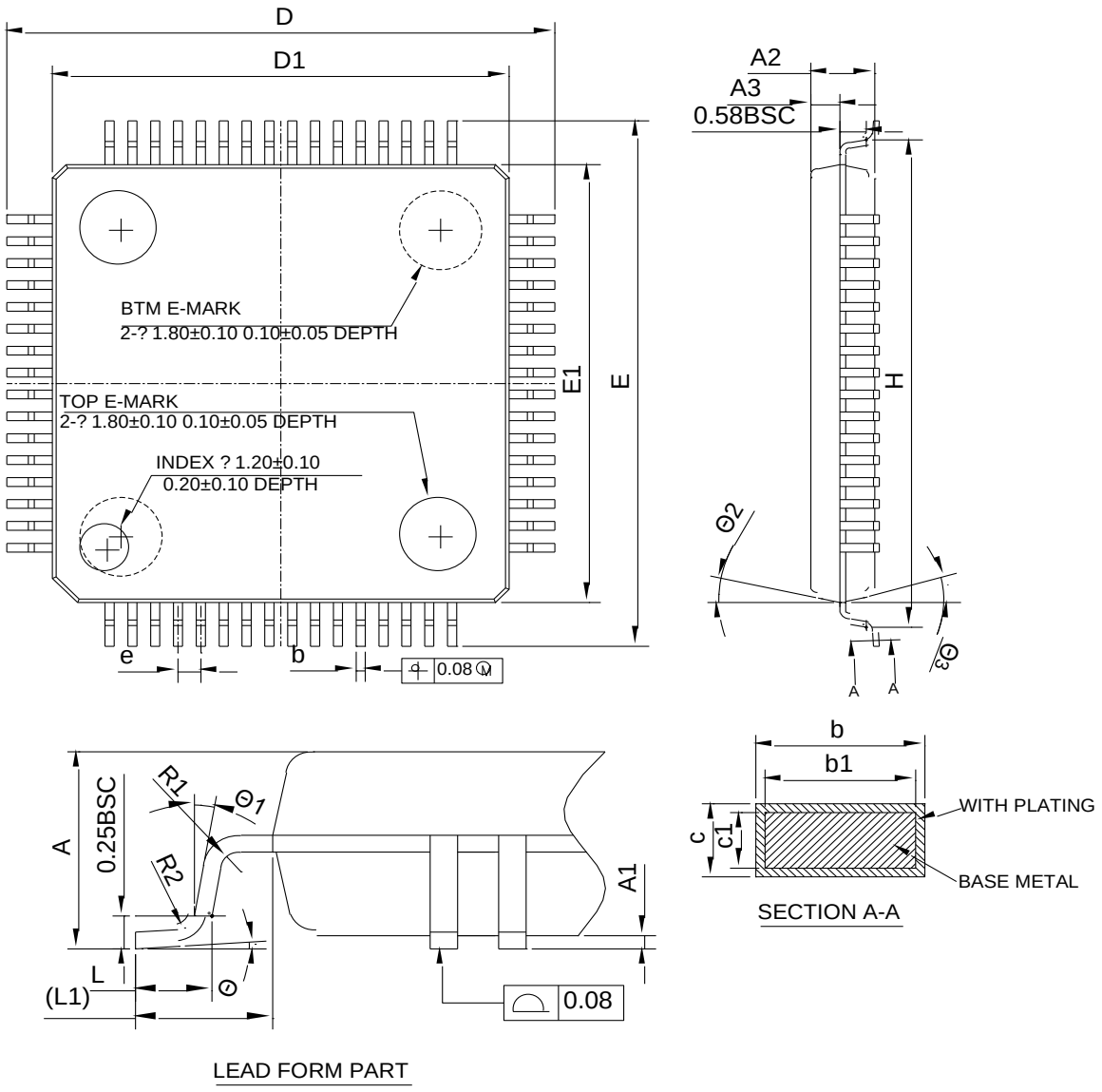


Figure 8-5 LQFP64 – 64 pin, 10 x 10 mm Low Profile Quad Flat Package Outline [1]

[1] Drawing is not to scale.

Table 8-3 LQFP64 – 64 pin, 10 x10 mm Low Profile Quad Flat Package mechanical data [1]

Item	Symbol	Min.	Nom.	Max.
Total height	A	—	—	1.60
Stand off	A1	0.05	—	0.15
Mold thickness	A2	1.35	1.40	1.45

Item		Symbol	Min.	Nom.	Max.
Leadframe to mold height		A3	0.59	0.64	0.69
Lead width		b	0.18	—	0.27
Lead width without plating		b1	0.17	0.20	0.23
Leadframe thickness		c	0.13	—	0.18
Leadframe thickness without plating		c1	0.117	0.127	0.137
Outer lead distance	X	D	11.95	12.00	12.05
	Y	E	11.95	12.00	12.05
Package size	X	D1	9.90	10.00	10.10
	Y	E1	9.90	10.00	10.10
Lead pitch		e	0.40	0.50	0.60
H		H	11.09	11.13	11.17
L		L	0.53	—	0.70
Lead length		L1	1.00 REF		
Lead forming arc radius R1		R1	0.15REF		
Lead forming arc radius R2		R2	0.13REF		
Angle 1		Θ	0°	3.5°	7°
Angle 2		Θ1	0°	—	—
Angle 3		Θ2	11°	12°	13°
Angle 4		Θ3	11°	12°	13°

[1] Dimensions are expressed in millimeters.

8.3.2 LQFP64 device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

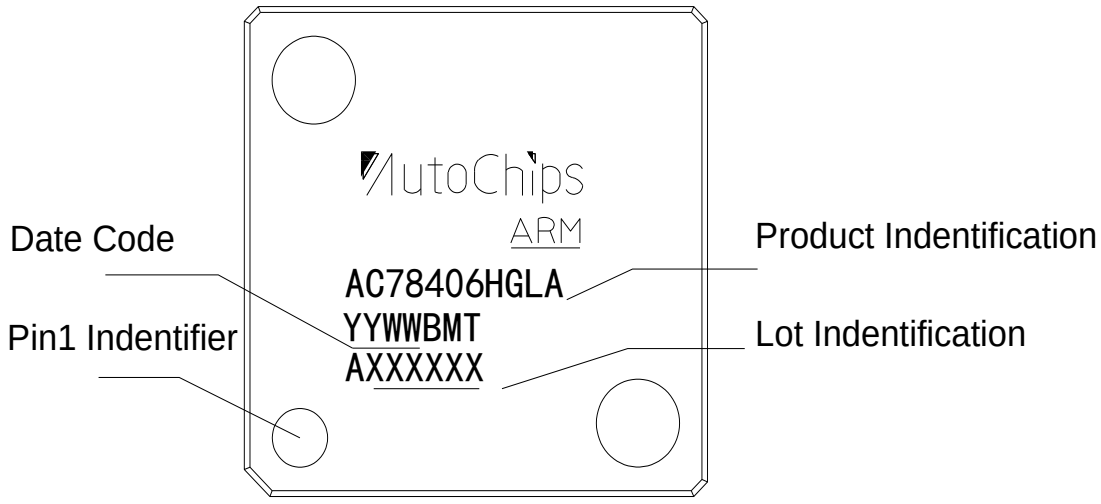


Figure 8-6 LQFP64 marking example (package top view)

9 Pin Assignments

9.1 Signal multiplexing and pin assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

Table 9-1 Signal multiplexing and pin assignments

144 PIN LQFP	100 PIN LQFP	64 PIN LQFP	Pin Name	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	GPIO
1	1	—	PE16	HIGH_Z	GPIO	UART1_RTS	SPI2_SIN	PWM2_CH7	PWM4_FLT0	EIO_D3	TRGMUX_OUT7	144
2	2	—	PE15	HIGH_Z	GPIO	UART1_CTS	SPI2_SCK	PWM2_CH6	PWM4_FLT1	EIO_D2	TRGMUX_OUT6	143
3	3	1	PD1	HIGH_Z	GPIO	PWM0_CH3	SPI1_SIN	PWM2_CH1	HIGH_Z	EIO_D1	TRGMUX_OUT2	97
4	4	2	PD0	HIGH_Z	GPIO	PWM0_CH2	SPI1_SCK	PWM2_CH0	HIGH_Z	EIO_D0	TRGMUX_OUT1	96
5	5	3	PE11	HIGH_Z	GPIO	SPI2_CS0	PCT0_ALT1	PWM2_CH5	HIGH_Z	EIO_D5	TRGMUX_OUT5	139
6	6	4	PE10	HIGH_Z	GPIO	CLKOUT	SPI2_CS1	PWM2_CH4	CAN0_STB	EIO_D4	TRGMUX_OUT4	138
7	7	—	PE13	HIGH_Z	GPIO	PWM4_CH5	SPI2_CS2	PWM2_FLT0	HIGH_Z	HIGH_Z	HIGH_Z	141
8	8	5	PE5	HIGH_Z	GPIO	PWM_CLK2	PWM2_CH0	PWM2_CH3	CAN0_TX	EIO_D7	EWDG_IN	133
9	9	6	PE4	HIGH_Z	GPIO	HIGH_Z	PWM2_CH1	PWM2_CH2	CAN0_RX	EIO_D6	EWDG_OUT_b	132
10	—	—	PA25	HIGH_Z	GPIO	PWM5_CH0	HIGH_Z	HIGH_Z	HIGH_Z	HIGH_Z	HIGH_Z	25
11	10	7	VDD	—	—	—	—	—	—	—	—	—
12	—	—	VSS	—	—	—	—	—	—	—	—	—
13	11	8	VDDA	—	—	—	—	—	—	—	—	—
14	12	9	VREFH	—	—	—	—	—	—	—	—	—
15	13	—	VREFL	—	—	—	—	—	—	—	—	—
16	14	10	VSS	—	—	—	—	—	—	—	—	—
17	15	11	PB7	HSE_IN[1]	gpio	I2C0_SCL	HIGH_Z	HIGH_Z	HIGH_Z	HIGH_Z	HIGH_Z	39
18	16	12	PB6	HSE_OUT[2]	gpio	I2C0_SDA	HIGH_Z	HIGH_Z	HIGH_Z	HIGH_Z	HIGH_Z	38
19	—	—	PA26	HIGH_Z	gpio	PWM5_CH1	SPI1_CS0	SPI0_CS0	HIGH_Z	HIGH_Z	HIGH_Z	26
20	17	—	PE14	HIGH_Z	gpio	PWM0_FLT1	HIGH_Z	PWM2_FLT1	HIGH_Z	HIGH_Z	HIGH_Z	142
21	18	13	PE3	HIGH_Z	gpio	PWM0_FLT0	UART2_RTS	PWM2_FLT0	CAN3_TX	TRGMUX_IN6	ACMP0_OUT	131
22	—	—	PA27	HIGH_Z	gpio	PWM5_CH2	SPI1_SOUT	UART0_TX	CAN0_TX	HIGH_Z	HIGH_Z	27
23	19	—	PE12	HIGH_Z	gpio	PWM0_FLT3	UART2_TX	PWM5_FLT0	CAN3_RX	HIGH_Z	HIGH_Z	140
24	—	—	PA28	HIGH_Z	gpio	PWM5_CH3	SPI1_SCK	UART0_RX	CAN0_RX	HIGH_Z	HIGH_Z	28
25	20	—	PD17	HIGH_Z	gpio	PWM0_FLT2	UART2_RX	PWM5_FLT1	CAN3_STB	HIGH_Z	HIGH_Z	113
26	—	—	PA29	HIGH_Z	gpio	PWM5_CH4	HIGH_Z	UART2_TX	SPI1_SIN	HIGH_Z	HIGH_Z	29

27	—	—	PA30	HIGH_Z	gpio	PWM5_CH5	UART2_RX	SPI0_SOUT	CAN0_STB	HIGH_Z	HIGH_Z	30
28	21	14	PD16	HIGH_Z	gpio	PWM0_CH1	HIGH_Z	SPI0_SIN	ACMP0_RRT	HIGH_Z	HIGH_Z	112
29	22	15	PD15	HIGH_Z	gpio	PWM0_CH0	HIGH_Z	SPI0_SCK	HIGH_Z	HIGH_Z	HIGH_Z	111
30	23	16	PE9	HIGH_Z	gpio	PWM0_CH7	UART2_CTS	HIGH_Z	HIGH_Z	HIGH_Z	HIGH_Z	137
31	—	—	VSS	—	—	—	—	—	—	—	—	—
32	—	—	VDD	—	—	—	—	—	—	—	—	—
33	—	—	PA31	HIGH_Z	gpio	PWM5_CH6	HIGH_Z	SPI0_CS1	HIGH_Z	HIGH_Z	HIGH_Z	31
34	24	—	PD14	HIGH_Z	gpio	PWM2_CH5	UART1_TX	HIGH_Z	HIGH_Z	HIGH_Z	CLKOUT	110
35	25	—	PD13	HIGH_Z	gpio	PWM2_CH4	UART1_RX	HIGH_Z	HIGH_Z	HIGH_Z	RTC_CLKOUT	109
36	—	—	PB18	ADC0_IN16	gpio	PWM5_CH7	HIGH_Z	SPI1_CS1	HIGH_Z	HIGH_Z	HIGH_Z	50
37	—	—	PB20	ADC0_IN17	gpio	HIGH_Z	HIGH_Z	UART3_TX	HIGH_Z	HIGH_Z	HIGH_Z	52
38	—	—	PB21	ADC0_IN18	gpio	HIGH_Z	HIGH_Z	UART3_RX	HIGH_Z	HIGH_Z	HIGH_Z	53
39	26	17	PE8	ACMP0_IN3	gpio	PWM0_CH6	CAN0_STB	HIGH_Z	HIGH_Z	HIGH_Z	HIGH_Z	136
40	27	18	PB5	HIGH_Z	gpio	PWM0_CH5	SPI0_CS1	SPI0_CS0	CLKOUT	TRGMUX_IN0	HIGH_Z	37
41	28	19	PB4	HIGH_Z	gpio	PWM0_CH4	SPI0_SOUT	HIGH_Z	HIGH_Z	TRGMUX_IN1	HIGH_Z	36
42	29	20	PC3	ADC0_IN11/ ACMP0_IN4	gpio	PWM0_CH3	CAN0_TX	UART0_TX	HIGH_Z	HIGH_Z	HIGH_Z	67
43	30	21	PC2	ADC0_IN10 /ACMP0_IN5	gpio	PWM0_CH2	CAN0_RX	UART0_RX	HIGH_Z	HIGH_Z	HIGH_Z	66
44	31	22	PD7	ACMP0_IN6	gpio	UART2_TX	HIGH_Z	PWM2_FLT3	HIGH_Z	HIGH_Z	HIGH_Z	103
45	32	23	PD6	ACMP0_IN7	gpio	UART2_RX	HIGH_Z	PWM2_FLT2	HIGH_Z	HIGH_Z	HIGH_Z	102
46	33	24	PD5	HIGH_Z	gpio	PWM2_CH3	PCT0_ALT2	PWM2_FLT1	HIGH_Z	TRGMUX_IN7	HIGH_Z	101
47	34	—	PD12	HIGH_Z	gpio	PWM2_CH2	HIGH_Z	HIGH_Z	HIGH_Z	UART2_RTS	HIGH_Z	108
48	35	—	PD11	HIGH_Z	gpio	PWM2_CH1	PWM2_CH0	HIGH_Z	HIGH_Z	UART2_CTS	HIGH_Z	107
49	36	—	PD10	HIGH_Z	gpio	PWM2_CH0	PWM2_CH1	HIGH_Z	HIGH_Z	CLKOUT	HIGH_Z	106
50	37	—	VSS	—	—	—	—	—	—	—	—	—
51	38	—	VDD	—	—	—	—	—	—	—	—	—
52	39	25	PC1	ADC0_IN9	gpio	PWM0_CH1	SPI2_SOUT	HIGH_Z	HIGH_Z	PWM1_CH7	HIGH_Z	65
53	40	26	PC0	ADC0_IN8	gpio	PWM0_CH0	SPI2_SIN	HIGH_Z	HIGH_Z	PWM1_CH6	HIGH_Z	64
54	41	—	PD9	HIGH_Z	gpio	HIGH_Z	EIO_D0	PWM2_FLT3	HIGH_Z	PWM1_CH5	HIGH_Z	105
55	42	—	PD8	HIGH_Z	gpio	HIGH_Z	HIGH_Z	PWM2_FLT2	EIO_D1	PWM1_CH4	HIGH_Z	104
56	43	27	PC17	ADC0_IN15	gpio	PWM1_FLT3	CAN2_TX	HIGH_Z	HIGH_Z	UART3_TX	HIGH_Z	81
57	44	28	PC16	ADC0_IN14	gpio	PWM1_FLT2	CAN2_RX	HIGH_Z	HIGH_Z	UART3_RX	HIGH_Z	80
58	—	—	PB22	ADC0_IN19	gpio	HIGH_Z	HIGH_Z	HIGH_Z	UART1_TX	HIGH_Z	HIGH_Z	54
59	45	29	PC15	ADC0_IN13	gpio	PWM1_CH3	SPI2_SCK	HIGH_Z	CAN2_STB	TRGMUX_IN8	HIGH_Z	79

60	—	—	PB23	ADC0_IN20	gpio	HIGH_Z	UART1_RX	HIGH_Z	HIGH_Z	HIGH_Z	HIGH_Z	55
61	46	30	PC14	ADC0_IN12	gpio	PWM1_CH2	SPI2_CS0	HIGH_Z	HIGH_Z	TRGMUX_IN9	HIGH_Z	78
62	—	—	PB25	ADC0_IN21	gpio	HIGH_Z	HIGH_Z	HIGH_Z	SPI2_CS0	HIGH_Z	HIGH_Z	57
63	47	31	PB3	ADC0_IN7	gpio	PWM1_CH1	SPI0_SIN	PWM1_CH0	PWM2_CH2	TRGMUX_IN2	HIGH_Z	35
64	—	—	PB27	ADC0_IN22	gpio	HIGH_Z	HIGH_Z	HIGH_Z	SPI2_SOUT	HIGH_Z	HIGH_Z	59
65	—	—	PB28	ADC0_IN23	gpio	HIGH_Z	HIGH_Z	HIGH_Z	SPI2_SIN	HIGH_Z	HIGH_Z	60
66	—	—	VSS	—	—	—	—	—	—	—	—	—
67	—	—	VDD	—	—	—	—	—	—	—	—	—
68	48	32	PB2	ADC0_IN6	gpio	PWM1_CH0	SPI0_SCK	PWM1_CH1	HIGH_Z	TRGMUX_IN3	HIGH_Z	34
69	—	—	PB29	HIGH_Z	gpio	HIGH_Z	HIGH_Z	HIGH_Z	SPI2_SCK	HIGH_Z	HIGH_Z	61
70	49	—	PC13	HIGH_Z	gpio	PWM3_CH7	PWM2_CH7	UART2_RTS	CAN3_TX	HIGH_Z	HIGH_Z	77
71	50	—	PC12	HIGH_Z	gpio	PWM3_CH6	PWM2_CH6	UART2_CTS	CAN3_RX	HIGH_Z	HIGH_Z	76
72	—	—	PC19	HIGH_Z	gpio	HIGH_Z	HIGH_Z	HIGH_Z	SPI2_CS1	HIGH_Z	HIGH_Z	83
73	—	—	PC23	HIGH_Z	gpio	SPI0_SCK	HIGH_Z	HIGH_Z	HIGH_Z	HIGH_Z	HIGH_Z	87
74	51	—	PC11	HIGH_Z	gpio	PWM3_CH5	PWM4_CH2	HIGH_Z	CAN3_STB	TRGMUX_IN10	HIGH_Z	75
75	52	—	PC10	HIGH_Z	gpio	PWM3_CH4	HIGH_Z	HIGH_Z	HIGH_Z	TRGMUX_IN11	HIGH_Z	74
76	—	—	PC27	HIGH_Z	gpio	PWM4_CH4	HIGH_Z	HIGH_Z	HIGH_Z	HIGH_Z	HIGH_Z	91
77	53	33	PB1	ADC0_IN5/ADC1_INTERLEAVE1[3]	gpio	UART0_TX	SPI0_SOUT	PWM_CLK0	CAN0_TX	PWM4_CH5	HIGH_Z	33
78	54	34	PB0	ADC0_IN4/ADC1_INTERLEAVE0[3]	gpio	UART0_RX	SPI0_CS0	PCT0_ALT3	CAN0_RX	PWM4_CH6	HIGH_Z	32
79	—	—	PC28	HIGH_Z	gpio	PWM4_CH7	HIGH_Z	HIGH_Z	HIGH_Z	HIGH_Z	HIGH_Z	92
80	55	35	PC9	HIGH_Z	gpio	UART1_TX	PWM1_FLT1	PWM5_CH0	CAN0_STB	UART0_RTS	HIGH_Z	73
81	56	36	PC8	HIGH_Z	gpio	UART1_RX	PWM1_FLT0	PWM5_CH1	HIGH_Z	UART0_CTS	HIGH_Z	72
82	—	—	PC29	HIGH_Z	gpio	PWM5_CH2	HIGH_Z	HIGH_Z	HIGH_Z	HIGH_Z	HIGH_Z	93
83	57	37	PA7	ADC0_IN3	gpio	PWM0_FLT2	PWM5_CH3	RTC_CLKIN	HIGH_Z	UART1_RTS	HIGH_Z	7
84	—	—	PC30	HIGH_Z	gpio	PWM5_CH4	EIO_D0	HIGH_Z	HIGH_Z	HIGH_Z	HIGH_Z	94
85	58	38	PA6	ADC0_IN2	gpio	PWM0_FLT1	SPI1_CS1	PWM5_CH5	HIGH_Z	UART1_CTS	HIGH_Z	6
86	—	—	PC31	HIGH_Z	gpio	PWM5_CH6	EIO_D1	HIGH_Z	HIGH_Z	HIGH_Z	HIGH_Z	95
87	59	39	PE7	HIGH_Z	gpio	PWM0_CH7	PWM3_FLT0	HIGH_Z	HIGH_Z	HIGH_Z	HIGH_Z	135
88	—	—	PD18	ADC1_IN16	gpio	PWM5_CH7	EIO_D2	HIGH_Z	HIGH_Z	HIGH_Z	HIGH_Z	114
89	—	—	PD19	ADC1_IN17	gpio	HIGH_Z	EIO_D3	HIGH_Z	HIGH_Z	HIGH_Z	HIGH_Z	115
90	60	40	VSS	—	—	—	—	—	—	—	—	—
91	61	41	VDD	—	—	—	—	—	—	—	—	—
92	62	—	PA17	HIGH_Z	gpio	PWM0_CH6	PWM3_FLT0	EWDG_OUT_b	PWM5_FLT0	HIGH_Z	HIGH_Z	17

93	63	—	PB17	HIGH_Z	gpio	PWM0_CH5	SPI1_CS3	PWM5_FLT1	HIGH_Z	HIGH_Z	HIGH_Z	49
94	64	—	PB16	ADC1_IN15	gpio	PWM0_CH4	SPI1_SOUT	UART3_TX	HIGH_Z	HIGH_Z	HIGH_Z	48
95	65	—	PB15	ADC1_IN14	gpio	PWM0_CH3	SPI1_SIN	UART3_RX	HIGH_Z	HIGH_Z	HIGH_Z	47
96	66	—	PB14	ADC1_IN9 / ADC0_INTERLEAVE1[3]	gpio	PWM0_CH2	SPI1_SCK	HIGH_Z	HIGH_Z	HIGH_Z	HIGH_Z	46
97	67	42	PB13	ADC1_IN8 / ADC0_INTERLEAVE0[3]	gpio	PWM0_CH1	PWM3_FLT1	CAN2_TX	HIGH_Z	HIGH_Z	HIGH_Z	45
98	68	43	PB12	ADC1_IN7	gpio	PWM0_CH0	PWM3_FLT2	CAN2_RX	HIGH_Z	HIGH_Z	HIGH_Z	44
99	—	—	PD22	ADC1_IN18	gpio	HIGH_Z	HIGH_Z	CAN3_TX	HIGH_Z	HIGH_Z	HIGH_Z	118
100	69	44	PD4	ADC1_IN6	gpio	PWM0_FLT3	PWM3_FLT3	HIGH_Z	CAN2_STB	HIGH_Z	HIGH_Z	100
101	70	45	PD3	ADC1_IN3	gpio	PWM3_CH5	SPI1_CS0	EIO_D5	EIO_D7	TRGMUX_IN4	NMI_b	99
102	71	46	PD2	ADC1_IN2	gpio	PWM3_CH4	SPI1_SOUT	EIO_D4	EIO_D6	TRGMUX_IN5	HIGH_Z	98
103	—	—	PD23	ADC1_IN19	gpio	HIGH_Z	HIGH_Z	CAN3_RX	HIGH_Z	HIGH_Z	HIGH_Z	119
104	72	47	PA3	ADC1_IN1	gpio	PWM3_CH1	I2C0_SCL	EWDG_IN	EIO_D5	UART0_TX	HIGH_Z	3
105	73	48	PA2	ADC1_IN0	gpio	PWM3_CH0	I2C0_SDA	EWDG_OUT_b	EIO_D4	UART0_RX	HIGH_Z	2
106	—	—	PD24	ADC1_IN20	gpio	HIGH_Z	HIGH_Z	CAN3_STB	HIGH_Z	HIGH_Z	HIGH_Z	120
107	74	—	PB11	HIGH_Z	gpio	PWM3_CH3	HIGH_Z	HIGH_Z	HIGH_Z	HIGH_Z	HIGH_Z	43
108	75	—	PB10	HIGH_Z	gpio	PWM3_CH2	I2C0_SDA	HIGH_Z	UART3_TX	HIGH_Z	HIGH_Z	42
109	76	—	PB9	HIGH_Z	gpio	PWM3_CH1	I2C0_SCL	HIGH_Z	UART3_RX	HIGH_Z	HIGH_Z	41
110	—	—	PD27	ADC1_IN21	gpio	HIGH_Z	HIGH_Z	HIGH_Z	HIGH_Z	HIGH_Z	HIGH_Z	123
111	77	—	PB8	HIGH_Z	gpio	PWM3_CH0	HIGH_Z	HIGH_Z	HIGH_Z	HIGH_Z	HIGH_Z	40
112	—	—	PD28	ADC1_IN22	gpio	HIGH_Z	HIGH_Z	HIGH_Z	HIGH_Z	HIGH_Z	HIGH_Z	124
113	78	49	PA1	ADC0_IN1 / ACMP0_IN1	gpio	PWM1_CH1	PWM2_CH2	EIO_D3	PWM1_CH0	UART0_RTS	TRGMUX_OUT0	1
114	—	—	PD29	ADC1_IN23	gpio	HIGH_Z	HIGH_Z	HIGH_Z	HIGH_Z	HIGH_Z	HIGH_Z	125
115	79	50	PA0	ADC0_IN0 / ACMP0_IN0	gpio	PWM2_CH1	HIGH_Z	EIO_D2	PWM2_CH0	UART0_CTS	TRGMUX_OUT3	0
116	—	—	PD30	HIGH_Z	gpio	HIGH_Z	HIGH_Z	HIGH_Z	HIGH_Z	HIGH_Z	HIGH_Z	126
117	80	51	PC7	ADC1_IN5	gpio	UART1_TX	CAN1_TX	PWM3_CH3	HIGH_Z	PWM1_CH0	HIGH_Z	71
118	81	52	PC6	ADC1_IN4	gpio	UART1_RX	CAN1_RX	PWM3_CH2	HIGH_Z	PWM1_CH1	HIGH_Z	70
119	82	—	PA16	ADC1_IN13	gpio	PWM1_CH3	SPI1_CS2	HIGH_Z	HIGH_Z	HIGH_Z	HIGH_Z	16
120	83	—	PA15	ADC1_IN12	gpio	PWM1_CH2	SPI0_CS3	SPI2_CS3	HIGH_Z	HIGH_Z	HIGH_Z	15
121	84	53	PE6	ADC1_IN11	gpio	SPI0_CS2	HIGH_Z	PWM3_CH7	CAN1_STB	UART1_RTS	HIGH_Z	134
122	85	54	PE2	ADC1_IN10	gpio	SPI0_SOUT	PCT0_ALT3	PWM3_CH6	HIGH_Z	UART1_CTS	HIGH_Z	130
123	86	—	VSS	—	—	—	—	—	—	—	—	—
124	87	—	VDD	—	—	—	—	—	—	—	—	—
125	—	—	PE19	HIGH_Z	gpio	HIGH_Z	HIGH_Z	HIGH_Z	HIGH_Z	HIGH_Z	HIGH_Z	147

126	—	—	PE20	HIGH_Z	gpio	PWM4_CH0	HIGH_Z	HIGH_Z	HIGH_Z	HIGH_Z	HIGH_Z	148
127	88	—	PA14	HIGH_Z	gpio	PWM0_FLT0	PWM3_FLT1	EWDG_IN	HIGH_Z	PWM1_FLT0	HIGH_Z	14
128	—	—	PE21	HIGH_Z	gpio	PWM4_CH1	HIGH_Z	HIGH_Z	HIGH_Z	HIGH_Z	HIGH_Z	149
129	—	—	PE22	HIGH_Z	gpio	PWM4_CH2	HIGH_Z	HIGH_Z	HIGH_Z	HIGH_Z	HIGH_Z	150
130	89	55	PA13	HIGH_Z	gpio	PWM1_CH7	CAN1_TX	HIGH_Z	HIGH_Z	PWM2_CH0	HIGH_Z	13
131	—	—	PE23	HIGH_Z	gpio	PWM4_CH3	CAN2_STB	HIGH_Z	HIGH_Z	HIGH_Z	HIGH_Z	151
132	—	—	PE24	HIGH_Z	gpio	PWM4_CH4	CAN2_TX	HIGH_Z	HIGH_Z	HIGH_Z	HIGH_Z	152
133	—	—	PE25	HIGH_Z	gpio	PWM4_CH5	CAN2_RX	HIGH_Z	HIGH_Z	HIGH_Z	HIGH_Z	153
134	90	56	PA12	HIGH_Z	gpio	PWM1_CH6	CAN1_RX	HIGH_Z	HIGH_Z	PWM2_CH1	HIGH_Z	12
135	91	57	PA11	HIGH_Z	gpio	PWM1_CH5	CAN1_STB	EIO_D1	ACMP0_RRT	HIGH_Z	HIGH_Z	11
136	92	58	PA10	HIGH_Z	gpio	PWM1_CH4	HIGH_Z	EIO_D0	HIGH_Z	HIGH_Z	JTAG_TDO [1]	10
137	93	59	PE1	HIGH_Z	gpio	SPI0_SIN	HIGH_Z	HIGH_Z	SPI1_CS0	PWM1_FLT1	HIGH_Z	129
138	94	60	PE0	HIGH_Z	gpio	SPI0_SCK	PWM_CLK1	HIGH_Z	SPI1_SOUT	PWM1_FLT2	HIGH_Z	128
139	95	61	PC5	HIGH_Z	gpio	PWM2_CH0	RTC_CLKOUT	HIGH_Z	HIGH_Z	PWM2_CH1	JTAG_TDI [1]	69
140	96	62	PC4	ACMP0_IN2	gpio	PWM1_CH0	RTC_CLKOUT	HIGH_Z	EWDG_IN	PWM1_CH1	JTAG_TCLK [1]	68
141	97	63	PA5	HIGH_Z	gpio	HIGH_Z	PWM_CLK1	HIGH_Z	HIGH_Z	HIGH_Z	RESET_b[1]	5
142	98	64	PA4	HIGH_Z	gpio	HIGH_Z	HIGH_Z	ACMP0_OUT	EWDG_OUT_b	HIGH_Z	JTAG_TMS [1]	4
143	99	—	PA9	HIGH_Z	gpio	UART2_TX	SPI2_CS0	EIO_D7	PWM3_FLT2	PWM1_FLT3	PWM4_FLT0	9
144	100	—	PA8	HIGH_Z	gpio	UART2_RX	SPI2_SOUT	EIO_D6	PWM3_FLT3	PWM4_FLT1	HIGH_Z	8

[1]: This functions as default function.

[2]: All the pins are default as Function 0 on the first time power on except some dedicated pins.

[3]: ADC0_INTERLEAVE0, ADC0_INTERLEAVE1, ADC1_INTERLEAVE0, ADC1_INTERLEAVE1 are partial channel multiplexing of ADC0 and ADC1 to implement functions such as safety detection and clock interleaving of ADC0 input channel and ADC1 input channel.

9.2 Device pin assignment

9.2.1 LQFP144 package

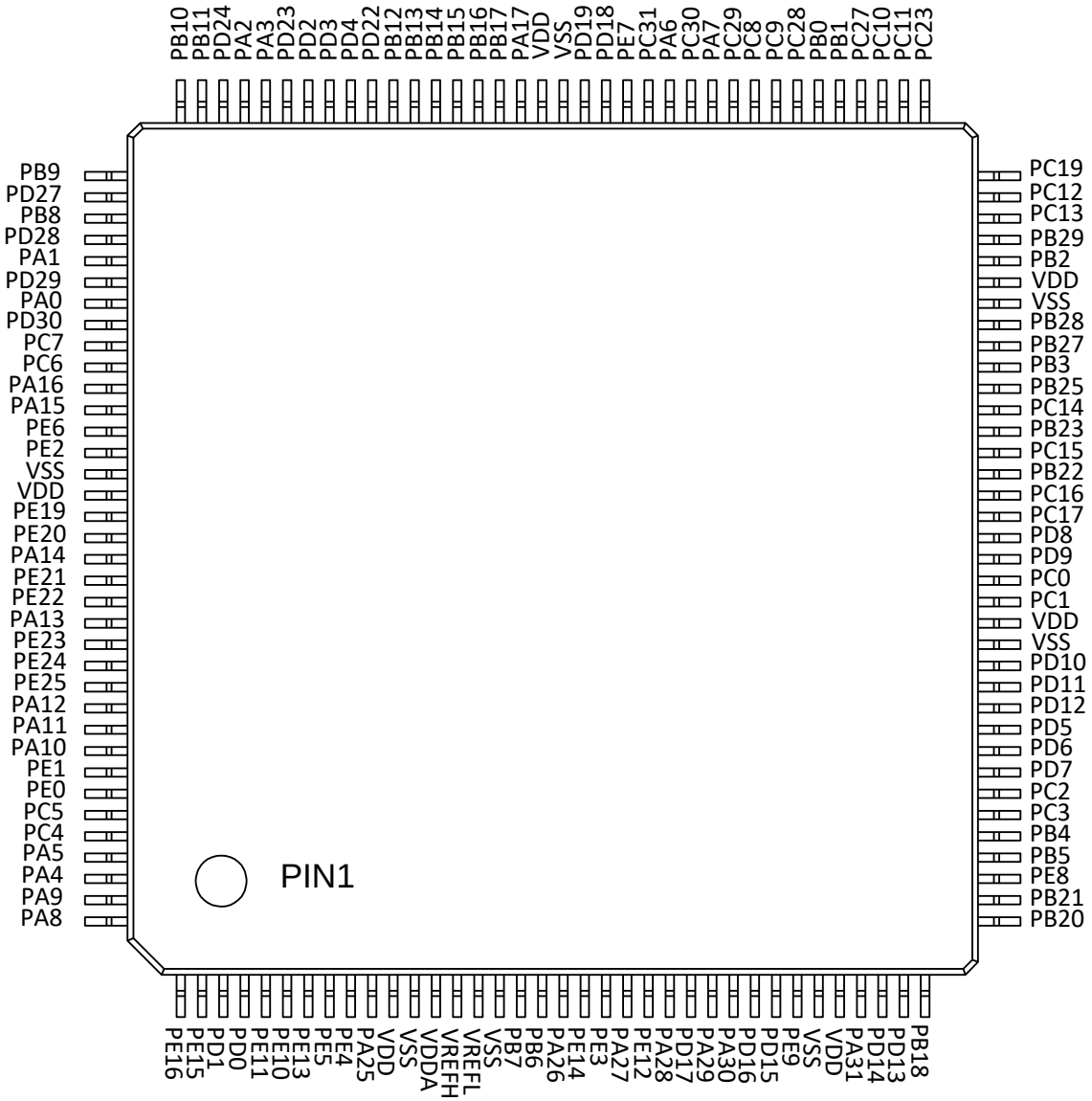


Figure 9-1 LQFP144 package

9.2.2 LQFP100 package

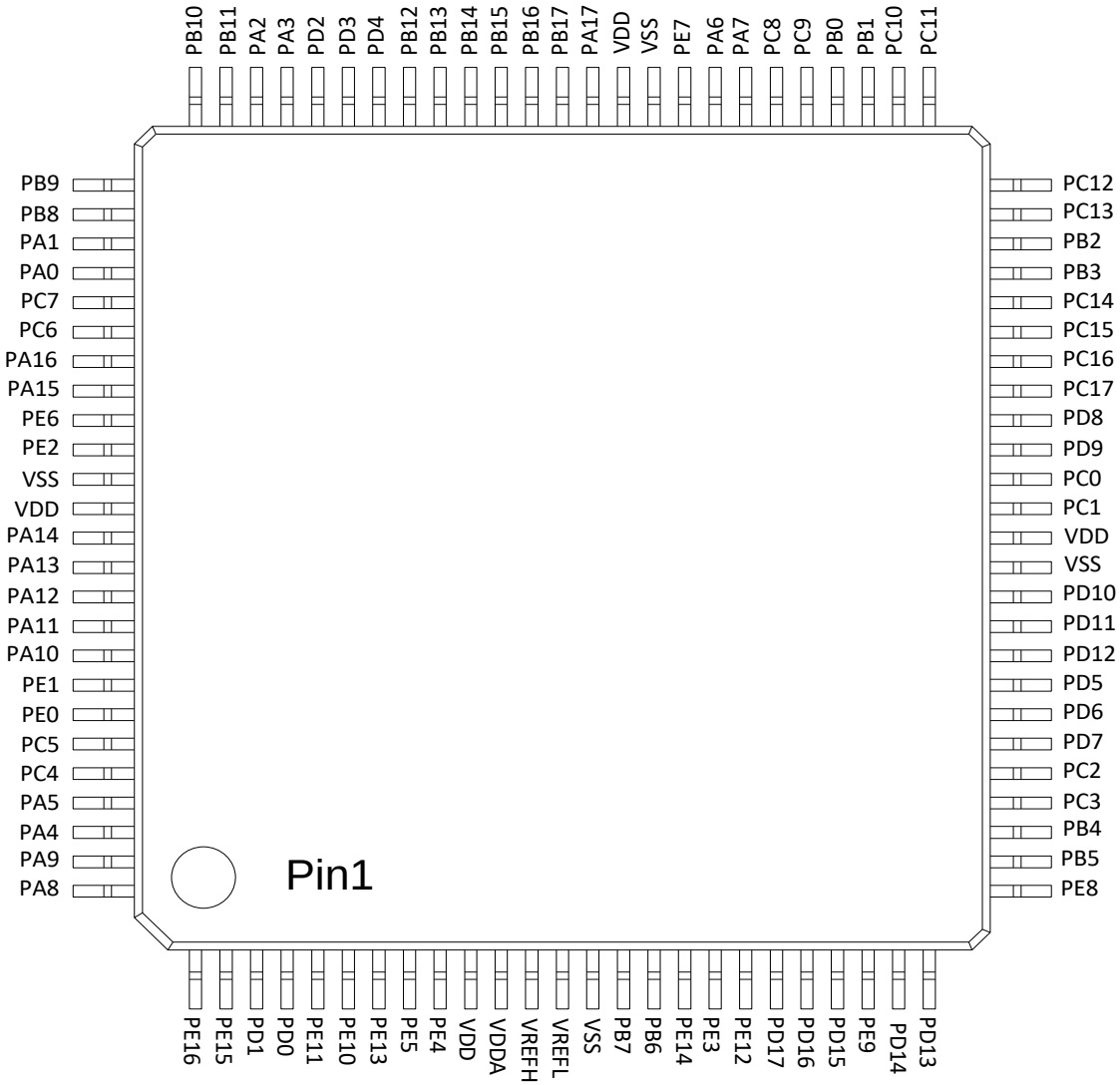


Figure 9-2 LQFP100 package

9.2.3 LQFP64 package

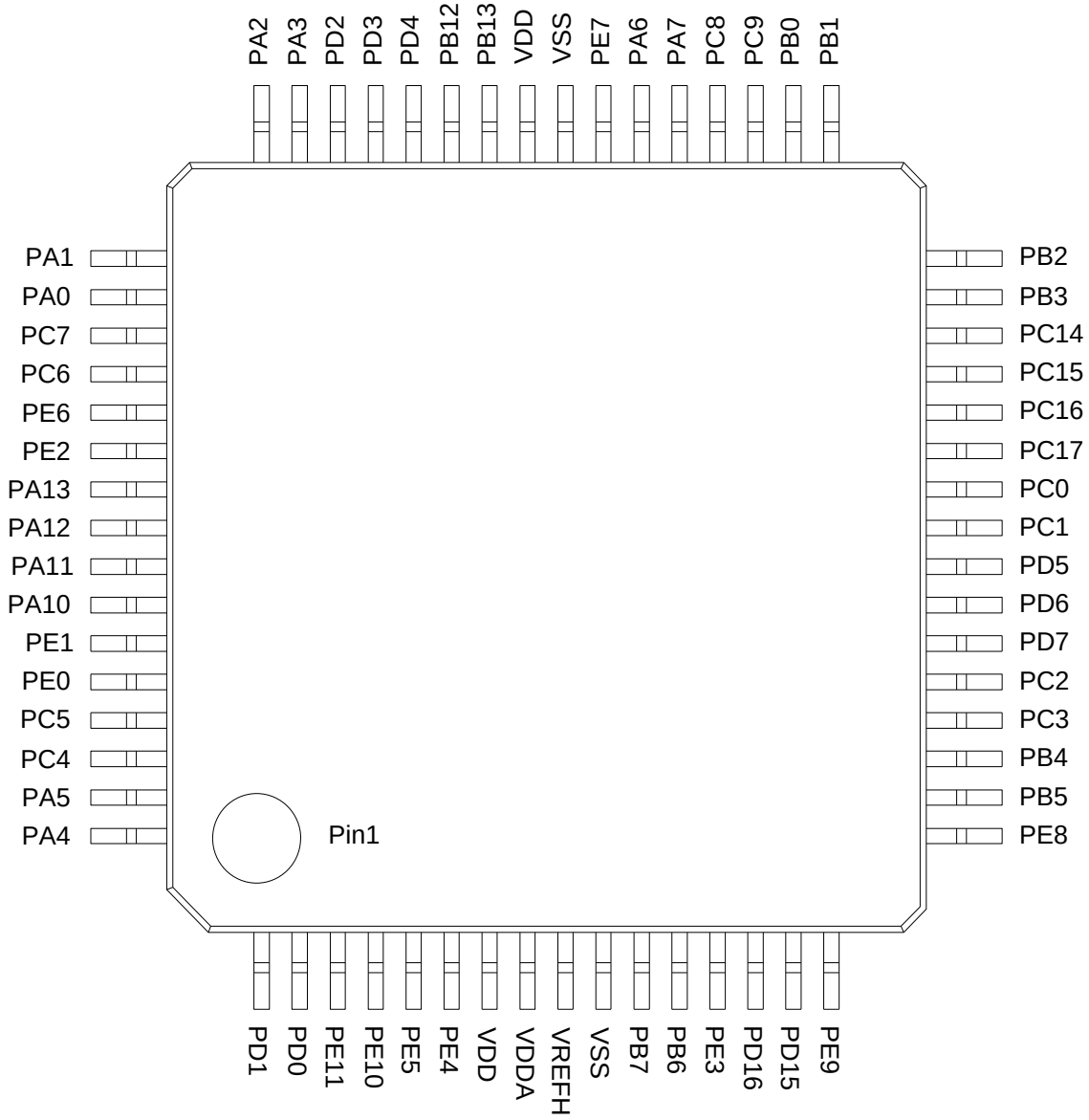


Figure 9-3 LQFP64 package

单击下面可查看定价，库存，交付和生命周期等信息

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