AC7840x Datasheet

Supports the following:

AC78409YGLA，AC78409LGLA，AC78409HGLA，
AC78409LFLA，AC78409HFLA，
AC78408YGLA，AC78408LGLA，AC78408HGLA，
AC78408YFLA，AC78408LFLA，AC78408HFLA，
AC78407YGLA，AC78407LGLA，AC78407HGLA，
AC78407LFLA，AC78407HFLA，
AC78406YGLA，AC78406LGLA，AC78406HGLA，
AC78406YFLA，AC78406LFLA，AC78406HFLA

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Document Revision History

Revision	Date	Author	Description
1.0	2022-12-28	AutoChips	Formal version(actual test parameters are used)
1.1	2023-03-16	AutoChips	Added DFlash lifetime parameter (Section 7.3);Added PFlash dual Bank information(Section 1)
1.2	2023-06-25	AutoChips	Add New Part Number
1.3	2024-03-12	AutoChips	1. Cover page, delete AC78405/3 and add AC78408/9 serial number 2. Section 3.3, update 7840 subseries description according to “Selection Guide” 3. Section 6.1.3-6.2.1， add Standby mode parameters 4. Section 7.4.1, add ADC VREFH/L usage note 5. Section 8, add marking information of AC78408/9 subseries 6. Section 9.1, update PINMUX table

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1 Key features

- **Automotive grade**
  - AEC-Q100 Grade 1 qualified
  - ISO26262 ASIL-B qualified
- **Performance**
  - Up to 120 MHz ARM® Cortex-M4F core
  - Integrated DSP
  - Float Point Unit(FPU)
  - Fast I/O access port
- **Memories and memory interfaces**
  - On-chip Flash, including PFlash up to 1 MB(Including 2 banks, 512KB+512KB)and DFlash up to 128 KB, both PFlash and DFlash support ECC
  - Up to 124 KB SRAM, ECC is supported
  - 4 KB FlexRAM
- **CSE(Cryptographic Services Engine)**
  - Support AES-128 ECB, CBC, CMAC
  - Support secure boot mode
  - Comply with SHE specification
  - Support TRNG, PRNG
  - Secure cryptographic key storage (Support up to 17 user keys)
- **Clocks**
  - oscillator (OSC) - supports 4 MHz to 30 MHz quartz crystal resonator; choice of low power or high gain oscillators, or up to 50MHz external input clock
  - System PLL - internal PLL with internal or external reference to to generate 120 MHz system clock
  - Internal 128 kHz low-power oscillator (LSI)
  - High Speed Internal Clock (HSI) — internal RC oscillator provides 8 MHz clock source
  - Ultra High Speed Internal Clock(VHSI) — internal RC oscillator provides 48 MHz clock source
- **Power Management**
  - Power Management Module (PMC) with six power modes: RUN, STOP1, STOP2, VLPR, VLPS, Standby
  - Low-voltage detection with reset (LVD/LVR)
- **System peripherals**
  - Watchdog with independent clock source(WDOG/External WDG(EWDG))
  - Programmable cyclic redundancy check module(CRC)
  - JTAG/SWD debug interface

- One 16-channel DMA

- **Human-machine interface**
  - Up to 128 general-purpose input/output (GPIO)
  - External interrupt (IRQ)

- **Analog modules**
  - Two ADC , each up to 28-channel(outer 24 channels, inner 4 channels) , 1Msps@12 bit/1.33Msps@10 bit/1.46Msps@8 bit SAR ADC, optional hardware trigger (ADC)
  - One analog comparators(ACMP) containing a 8-bit DAC and programmable reference input

- **Timer**
  - Up to six 8-channel complementary PWM
  - One 4-channel periodic interrupt timer (TIMER)
  - One 16-bit pulse counter(PCT)
  - One real-time counter (RTC)
  - Two programmable delay timer (PDT)

- **Communication interfaces**
  - Up four CAN-FD modules, compatible with CAN 2.0B
  - Four UART modules (supporting 4-ch Software LIN)
  - Three SPI modules
  - One I2C module
  - One EIO module, supporting up to 4 Timers and 4 Shifters

- **Operating characteristics**
  - Voltage range: 2.7 to 5.5 V
  - Temperature range(ambient): -40 to 125°C

- **Package**
  - 144-pin LQFP
  - 100-pin LQFP
  - 64-pin LQFP

2 Block diagram

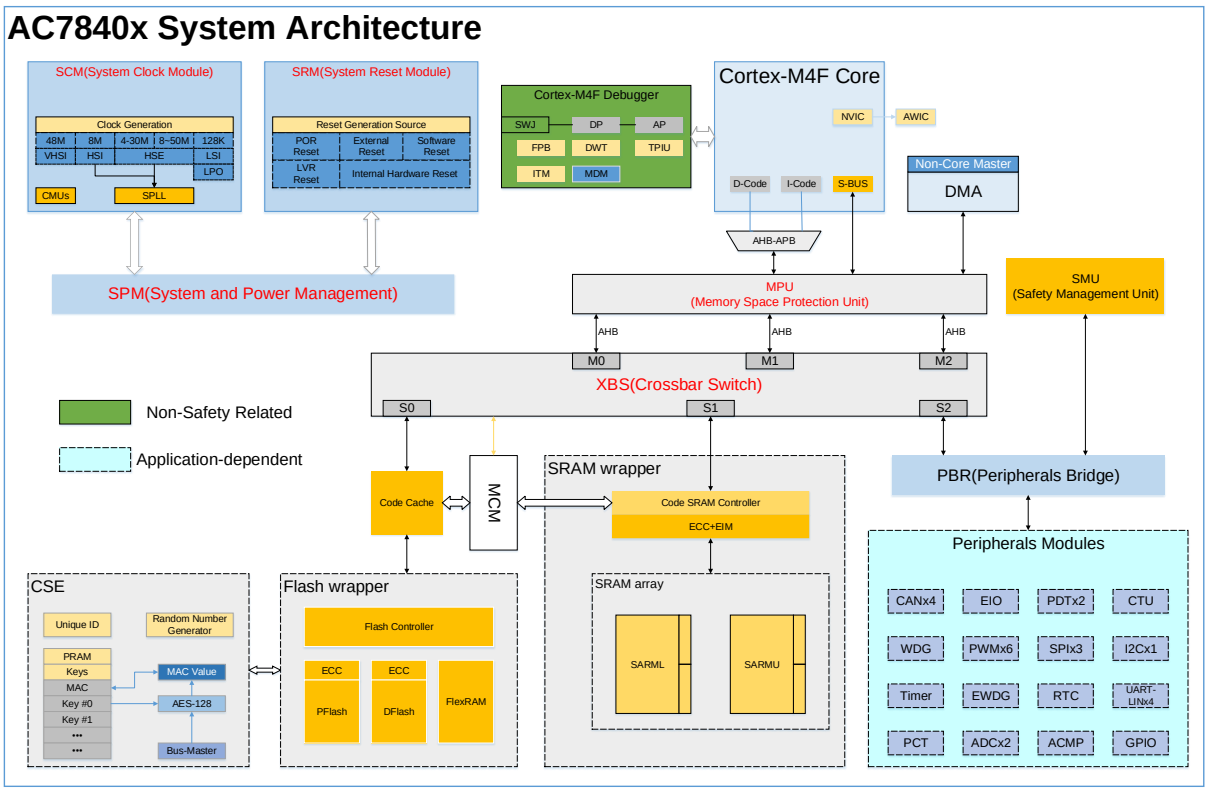

Figure 2-1 AC7840x Block Diagram

3 Part Identification

3.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

3.2 Format

Part numbers for this device have the following format:

AC## GTUFPN

3.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid).

Table 3-1 Fields

Field	Description	Value
AC	AutoChips	• AC
7	AutoChips MCU family	• 7
8	General Purpose Automotive MCU	• 8
4	Core Platform	• 4 = Cortex-M4
0 6	Specific Function Bit	• 0 = platform series • 9/8/7/6 = Product subfamily 9: support Crypto, support ISELED, Standby mode 8: support Crypto, Standby mode 7: Crypto is supported, support ISELED 6: Crypto is supported
Y	Pin Count	• H = 64 • L = 100 • Y = 144
G	Flash Memory Size	• F = 512KB • G = 1024KB
L	Package type	• L = LQFP • Q = QFN • T = TSSOP
A	Temperature range (°C)	• A = AEC-Q100 Grade 1(-40~125°C) • I = -40~105°C C= -40~85°C

3.4 Example

This is an example part number: AC78406YGLA.

4 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the following classification is used and the parameters are tagged accordingly in the tables where appropriate.

Table 4-1 Parameter classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

5 Rating

5.1 Thermal handling ratings

Table 5-1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
TSTG	Storage temperature	–55	150	°C	1
TSDR	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, High Temperature Storage Life.

2. Determined according to IPC/JEDEC Standard J-STD-020, Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.

5.2 Moisture handling ratings

Table 5-2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.

5.3 ESD handling ratings

Table 5-3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	–4000	4000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	–750	750	V	2
I_{LAT}	Latch-up current at ambient temperature of 125°C	–100	100	mA	3

1. Determined according to AEC-Q100-002-D,HUMAN BODY MODEL ELECTROSTATIC DISCHARGE TEST.

2. Determined according to AEC-Q100-011-C1,CHARGED DEVICE MODEL (CDM) ELECTROSTATIC DISCHARGE TEST.

3. Determined according to AEC-Q100-004-D, IC LATCH-UP TEST.

- Test was performed at 125 °C case temperature (Class II).
- Supply groups pass 1.5 Vccmax

5.4 Voltage and current operating ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maximam is not guaranteed. The following table is the designed operation ratings, and stress beyond the limits specified in the following table may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this document.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pullup resistor associated with the pin is enabled.

Table 5-4 Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V_{DD}[1]	Digital supply voltage	–0.3	5.5	V
I_{DD}	Maximum current into V_{DD}	—	120	mA
V_{IN}	Input voltage except true open drain pins	–0.3	V_{DD} + 0.1[2]	V
	Input voltage of true open drain pins	–0.3	V_{DD} + 0.1[2]	V
I_D	Instantaneous maximum current single pin limit (applies to all port pins)	–20	20	mA
V_{DDA}	Analog supply voltage	V_{DD} – 0.1	V_{DD} + 0.1	V

[1] All 6 VDD in section 9.1 should compliant with these limits.

[2] Maximum rating of V_{DD} also applies to V_{IN}.

6 General

6.1 Nonswitching electrical specifications

6.1.1 Power and ground pins

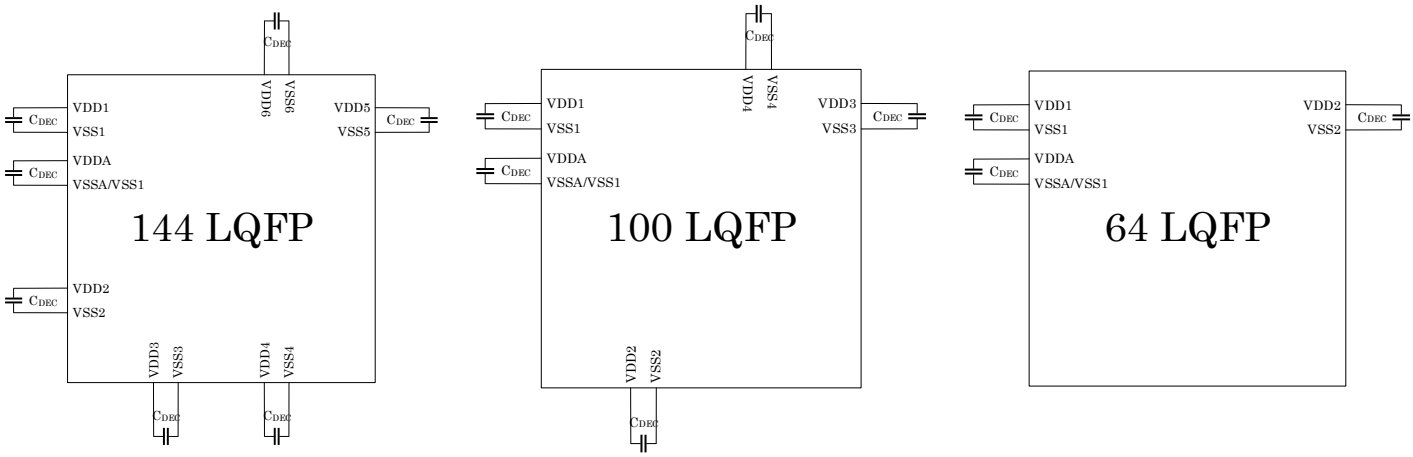

Figure 6-1 Pinout decoupling

1. All 6 VDDx and VSSx here corspending to the 6 VDD and VSS in section 9.1.
2. VDDx and VDDA must be shorted to a common source on PCB.
3. All decoupling capacitors must be low ESR ceramic capacitors (X7R type) , the recommended value is 0.1 uF.
4. For improved performance, it is recommended to use 10 uF, 0.1 uF and 1 nF capacitors in parallel.
5. All decoupling capacitors should be placed as close as possible to the corresponding power and ground pins.

6.1.2 DC characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 6-1 DC characteristics

Symbol	C	Description			Min.	Typ.	Max.	Unit
VDD	C	Operating voltage		—	2.7[1]	—	5.5	V
V_{OH}	C	Output high voltage	drive strength	I_{load} = -5, -20mA	V_{DD} - 0.8	—	—	V

I_{OH}	P	Output high voltage	Maximum output high current of single IO -- I_{OH}, high drive configuration[2]	5 V	20	—	—	mA
	C			3.3 V	14	—	—	
	P		Maximum output high current of single IO -- I_{OH}, low drive configuration[2]	5 V	5	—	—	mA
	C			3.3 V	3.5	—	—	
I_{OHT}	D	Output high voltage	Max total I_{OH} for all IO ports	—	—	—	100	mA
V_{OL}	C	Output low voltage	drive strength	I_{load}= 5, 20mA	—	—	0.8	V
I_{OL}	P	Output low voltage	Maximum output low current of single IO -- I_{OL}, high drive configuration	5 V	20	—	—	mA
	C			3.3 V	12	—	—	
	P		Maximum output low current of single IO -- I_{OL}, low drive configuration	5 V	5	—	—	mA
	C			3.3 V	3	—	—	
V_{IH}	P	Input high voltage	All digital inputs	4.0≤V_{DD}<5.5 V	0.65×V_{DD}	—	V_{DD} + 0.3	V
				2.7≤V_{DD}<4.0 V	0.70×V_{DD}	—	V_{DD} + 0.3	
V_{IL}	P	Input low voltage	All digital inputs	4.0≤V_{DD}<5.5 V	-0.3	—	0.35×V_{DD}	V
				2.7≤V_{DD}<4.0 V	-0.3	—	0.30×V_{DD}	
V_{hys}	P	Input hysteresis	All digital inputs	—	0.06×V_{DD}	—	—	mV

$\|I_{In}\|$	P	Input leakage current	Per pin (pins in high impedance input mode)	$V_{IN} = V_{DD}$ or V_{SS}	-1	0.1	1	μA
R_{PU}	P	Pullup resistors	All digital inputs and enables internal pullup	4.0≤V_{DD}<5.5 V	20	—	70	kΩ
				2.7≤V_{DD}<4.0 V	20	—	80	
R_{PD}	P	Pulldown resistors	All digital inputs and enables internal pulldown	4.0≤V_{DD}<5.5 V	20	—	70	kΩ
				2.7≤V_{DD}<4.0 V	20	—	80	
I_{IC}	D	DC injection current	Single pin limit	V_{IN} < V_{SS}, V_{IN} > V_{DD}	-3	—	3	mA
			Total MCU limit, including sum of all stressed pins		—	—	30	
C_{In}	D	Input capacitance, all pins		—	—	5	7	pF

[1] Some modules under 2.7V can't guarantee the performance, only guarantee the functionality, please see section 7 for more information.

[2] The specific register setting, please refer to "ATC_AC7840x_ReferenceManual_EN".

Table 6-2 LVD /POR / AVDD Voltage warning specification

Symbol	C	Description	Min.	Typ.	Max.	Unit
V_{POR}	D	POR reset voltage [1]	1.6	1.8	2	V
V_{LVDL}	C	Falling edge low-voltage detect threshold—low gear	2.8	2.9	3.0	V
V_{LVDH}	C	Falling edge low-voltage detect threshold—high gear [2]	4.36	4.5	4.65	V
V_{HYSLVD}	C	low-voltage detect hysteresis	—	50	—	mV
V_{LVRH}	C	Falling edge low-voltage reset threshold (RUN /STOP/VLPR)	2.5	2.6	2.7	V
V_{LVRH}	C	Falling edge low-voltage reset threshold (VLPS)	1.97	2.22	2.44	V
V_{HYSPVD}	C	High-gear low-voltage detect hysteresis	—	50	—	mV
V_{BG}	P	Buffered bandgap output [3]	1.18	1.2	1.22	V

[1] Maximum is the highest voltage that POR is guaranteed.

[2] Rising thresholds are falling threshold + hysteresis.

[3] Voltage Factory trimmed at V_{DD} = 5.0 V, T_{emp} = 25 °C.

6.1.3 Power mode

The device supports RUN, STOP1, STOP2, VLPR and VLPS modes. AC7840(8/9) additionally support Standby mode，which other subseries not support。

- RUN - CPU clocks can be run at full speed. After MCU reset, the default operating mode is RUN mode, using VHSI as the system clock.
- STOP1- CPU enters into deep sleep mode, core clock , system clocks and bus clock are disabled.
- STOP2 - CPU enters into deep sleep mode, core clock and system clocks are disabled, bus clock is enabled.
- VLPR - CPU can be run in low speed state. PLL, VHSI and outer HSE are disabled in ths mode, and HSI can only be used as system clock.
- VLPS - CPU enters into deep sleep mode and it is the lowest power mode in AC7840x.
- Standby - CPU is power off, support wakeup by 15 GPIO and RTC, keep 32KB SRAM from power off (Standby mode only supported by AC7840(8/9) subseries)

6.1.4 Supply current characteristics

Table 6-3 Supply current characteristics

Power Mode	Scenario	VDD (V)	-40℃	25℃	125℃	Unit
RUN@120MHz	Peripherals off	5	21.266	22.079	36.891	mA
		3.3	20.842	21.650	35.686	
	Peripherals on	5	30.022	30.383	45.828	
		3.3	28.555	29.449	43.939	
RUN@80MHz	Peripherals off	5	16.362	17.100	31.759	
		3.3	15.979	16.725	30.640	
	Peripherals on	5	24.174	24.409	39.700	
		3.3	22.753	23.563	38.071	
RUN@64MHz	Peripherals off	5	14.529	15.240	29.834	
		3.3	14.162	14.891	28.760	
	Peripherals on	5	21.809	21.990	37.215	
		3.3	20.396	21.180	35.667	
RUN@48MHz	Peripherals off	5	11.222	11.931	26.414	
		3.3	10.880	11.606	25.409	
	Peripherals on	5	18.607	18.765	33.867	
		3.3	17.236	18.001	32.349	

STOP1	—	5	4.506	5.204	19.744	mA
		3.3	4.371	5.106	19.041	
STOP2	—	5	4.196	4.889	19.489	mA
		3.3	4.063	4.792	18.709	
VLPR	Peripherals off	5	2.141	2.603	16.632	mA
		3.3	2.018	2.523	15.983	
	Peripherals on 1	5	2.699	2.619	16.661	mA
		3.3	2.084	2.535	16.005	
	Peripherals on 2	5	3.094	2.998	16.983	mA
		3.3	2.494	2.905	16.414	
VLPS	Peripherals off	5	0.060	0.282	7.574	mA
		3.3	0.053	0.269	7.383	
	Timer on	5	0.060	0.282	7.611	mA
		3.3	0.053	0.271	7.402	
Standby	Peripherals off	5	0.025	0.037	0.485	mA
		3.3	0.022	0.034	0.471	
	Timer on	5	0.025	0.038	0.483	mA
		3.3	0.022	0.034	0.472	
IDD/MHz[1]	—	5	204.522	213.746	396.989	uA/MHz
	—	3.3	199.735	209.067	382.994	

[1] This value is measured at RUN@80MHz and the peripheral are off

The data above is guaranteed as classification T.

The detailed descriptions of the measurement scenes are shown in the attachment "AC7840x_Power_Modes_Configuration_EN.xlsx".

6.1.5 Behavior of power mode transition

All specifications in Table 6-4 use the following clocking configuration.

- RUN
  - Clock source: VHSI
  - SYS_CLK/CORE_CLK = 48 MHz
  - BUS_CLK = 48 MHz
- VLPR
  - Clock source: HSI
  - SYS_CLK/CORE_CLK = 8 MHz
  - BUS_CLK = 8 MHz
- STOP1/STOP2
  - Clock source: VHSI
  - SYS_CLK/CORE_CLK = OFF
  - BUS_CLK = 48 MHz
- VLPS

- Clock source: LSI, other clocks are turned off

- Standby
  - Clock source: LSI

Table 6-4 Bahaviors of power mode transition

Symbol	Description	Min.	Typ.	Max.	Unit
t_{POR}	After a POR event, the time length between when VDD reaches 2.7 V and when the first instruction is executed within the operating temperature range of the chip.	—	300	—	µs
—	VLPS → RUN	14	—	21	µs
—	STOP1 → RUN	0.5	—	1.46	µs
—	STOP2 → RUN	0.5	—	1.46	µs
—	VLPR → RUN	—	1.5	—	µs
—	Standby → RUN	—	500	—	µs
—	VLPS → VLPR	—	20	—	µs
—	RUN → STOP1	—	0.4	—	µs
—	RUN → STOP2	—	0.4	—	µs
—	RUN → VLPS	—	35	—	µs
—	RUN → Standby	—	75	—	µs
—	RUN → VLPR	—	0.9	—	µs
—	Pin reset → code execution	—	200	—	µs

6.2 Switching specifications

6.2.1 Control timing

Table 6-5 Control timing

No.	Symbol	C	Rating		Min.	Typ.[1]	Max.	Unit
1	f_{Sys}	D	System and core clock (t_{sys} = 1/f_{Sys})		DC	—	120	MHz
2	f_{Bus}	P	Bus frequency (t_{cyc} = 1/f_{sys})		DC	—	60	MHz
3	t_{extrst}	D	External reset pulse width [2]		1.5 × t_{sys}	—	—	ns
4	t_{ILIH}/t_{IHIL}	D	IRQ pulse width	RUN [3]	1.5 × t_{sys}	—	—	ns
	t_{ILIH}/t_{IHIL}	D		VLPR	1.5 × t_{sys}	—	—	—
	t_{ILIH}/t_{IHIL}	D		STOP1	1.5 × t_{sys}	—	—	—

	t_{ILIH}/t_{IHIL}	D		STOP2	1.5 × t_{sys}	—	—	—
	t_{ILIH}/t_{IHIL}	D		VLPS	1.5 × t_{sys}	—	—	—
	t_{ILIH}/t_{IHIL}	D		STDBY	1.5 × t_{sys}	—	—	—
5	t_{Rise}	C	Port rise and fall time - Normal drive strength (load = 50 pF) [4]	—	—	10.2	—	ns
	t_{Fall}	C			—	9.5	—	ns
	t_{Rise}	C	Port rise and fall time - high drive strength (load = 50 pF) [4]	—	—	5.4	—	ns
	t_{Fall}	C			—	4.6	—	ns

[1] Typical values are based on characterization data at V_{DD}=5.0 V, 25 °C unless otherwise stated.

[2] This is the shortest pulse that is guaranteed to be recognized as a RESET_B pin request.

[3] This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized.

[4] Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels.

6.2.2 PWM module timing

Synchronizer circuits determine the shortest input pulses that can be recognized. These synchronizers operate from the PWM clock.

Table 6-6 PWM input timing

No.	Symbol	C	Description	Min.	Max.	Unit
1	f_{PWM}	D	Timer clock frequency	—	120M	Hz
2	f_{Tclk}	D	Outer clock frequency	0	$f_{PWM}/4$	Hz
3	t_{Tclk}	D	Outer clock cycle	4	—	t_{PWM} [1]
4	t_{clkh}	D	Outer clock high level	1.5	—	t_{PWM}
5	t_{clkl}	D	Outer clock low level	1.5	—	t_{PWM}
6	t_{ICPW}	D	Input capture pulse width	1.5	—	t_{PWM}

[1] $t_{PWM}=1/f_{PWM}$.

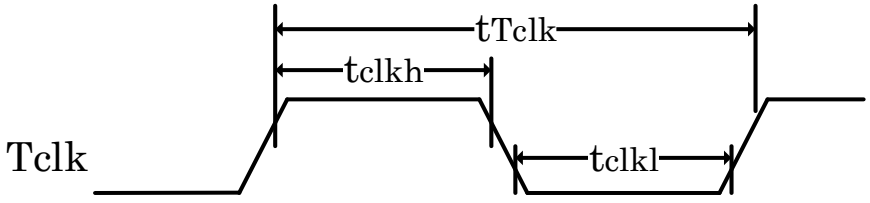

Figure 6-2 Timer outer clock

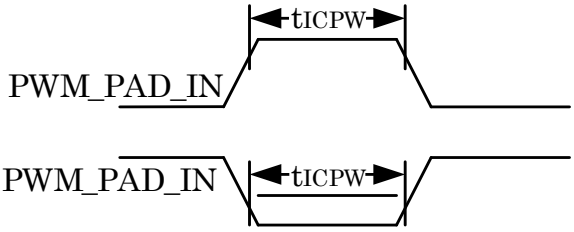

Figure 6-3 Timer outer input capture pulse

PWM_PAD_IN represents the chip pin input corresponding to PWM.

6.3 Thermal specifications

6.3.1 Thermal characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin.

Table 6-7 Thermal characteristics

Board type	Symbol	Description	144 LQFP	100 LQFP	64 LQFP	Unit	Notes
Dual-layer (1s1p)	θ_{JA}	Thermal resistance, junction to ambient (natural convection)	46.0	64.59	64.83	°C/W	1, 2
Four-layer (2s2p)	θ_{JA}	Thermal resistance, junction to ambient (natural convection)	38.13	48.22	45.41	°C/W	1, 3
—	θ_{JB}	Thermal resistance, junction to board	26.13	28.74	23.46	°C/W	4
—	θ_{JC}	Thermal resistance, junction to case	11.6	16.3	13.2	°C/W	5
Dual-layer (1s1p)	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center(natural convection)	24.66	27.26	19.5	°C/W	6
Four-layer (2s2p)	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center(natural convection)	24.46	27.04	19.33	°C/W	6
Dual-layer (1s1p)	Ψ_{JB}	Thermal characterization parameter, junction to package bottom outside center(natural convection)	25.06	27.78	20.75	°C/W	7

Four-layer (2s2p)	Ψ_{JB}	Thermal characterization parameter, junction to package bottom outside center(natural convection)	25.03	27.93	21.33	°C/W	7
Dual-layer (1s1p)	θ_{JMA}	Thermal resistance, junction to ambient (200 ft./min. air speed)	37.73	46.81	49.0	°C/W	1, 3
Four-layer (2s2p)	θ_{JMA}	Thermal resistance, junction to ambient (200 ft./min. air speed)	31.93	40.14	37.5	°C/W	1, 3

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with natural convection for horizontally oriented board. Board meets JESD51-3 specification for 1s board.
3. Per JEDEC JESD51-6 with forced convection for horizontally oriented board. Board meets JESD51-7 specification for 1s or 2s2p board, respectively.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the package bottom plate, ignore contact thermal resistance.
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.
7. Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA})$$

Wherein, T_A = Ambient temperature, the unit is °C.

θ_{JA} is package thermal resistance, junction-to-ambient, the unit is °C/W.

$$P_D = P_{int} + P_{I/O}$$

Chip internal power, the unit is Watts.

$$P_{int} = I_{DD} \times V_{DD}$$

$P_{I/O}$: power dissipation on input and output pins - user determined.

For most applications, $P_{I/O} \ll P_{int}$ and can be neglected.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273\,°C)$$

Solving the equations above for K gives:

$$K = P_D \times (T_A + 273\,°C) + \theta_{JA} \times (P_D)^2$$

where K is a constant pertaining to the particular part.

K can be determined by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving the above equations iteratively for any value of T_A.

7 Peripheral operating requirements and behaviors

7.1 Core modules

7.1.1 SWD electricals

The folloing table describe the typical timing characters of SWD timing mode. These characteristics are SWD standard parameters, and guaranteed by GPIO characteristics and SWD internal circile design.

Table 7-1 SWD full voltage range electrical

Symbol	Description	Min.	Max.	Unit
—	Operating voltage	2.7	5.5	V
J1	SWD_CLK operation frequency • Serial wire debug	0	12	MHz
J2	SWD_CLK cycle period	1/J1	—	ns
J3	SWD_CLK clock pulse width • Serial wire debug	20	—	ns
J4	SWD_CLK rise and fall times	—	3	ns
J9	SWD_DIO input data setup time to SWD_CLK rise	5	—	ns
J10	SWD_DIO input data hold time after SWD_CLK rise	5	—	ns
J11	SWD_CLK high to SWD_DIO data valid	—	50	ns

7.2 External oscillator (OSC) and ICS characteristics

7.2.1 External oscillator(OSC) characteristics

Table 7-2 OSC specifications (temperature ranges from -40 to 125 °C ambient)

No.	Symbol	C	Description	Min.	Typ.	Max.	Unit
1	f_{hi}	C	Crystal frequency	4	—	30	MHz
2	CL1, CL2	D	Load capacitors	Refer to note [1]			—
3	R_S	D	Series resistor	—	0	—	KΩ
4	t_{CST}	C	Crystal start-up time	—	3	—	ms

[1] For CL1 and CL2, it is recommended to use high-quality external ceramic capacitors designed for high-frequency applications, and selected to match the requirements of the crystal. CL1 and CL2 are usually the same size. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing CL1 and CL2.

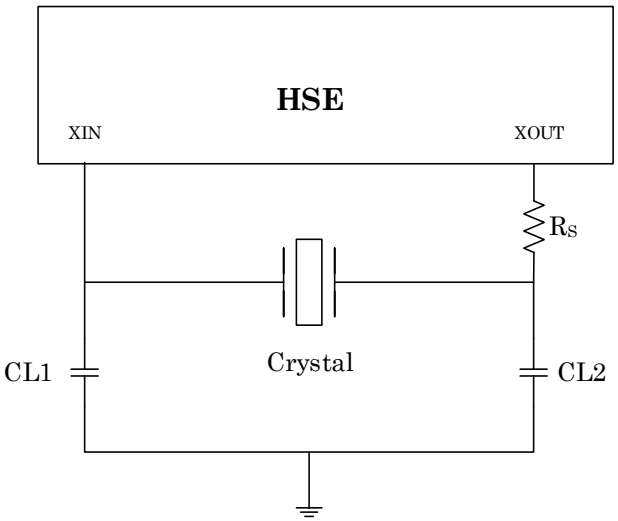

Figure 7-1 Typical crystal or resonator circuit

7.2.2 Internal RC characteristics

Table 7-3 OSC and ICS specifications (temperature range from -40 to 125 °C ambient)

No.	Symbol	C	Characteristics		Min.	Typ.	Max.	Unit
1	f_{HSI}	P	HSI output frequency range	Over temperature range from -40 °C to 125°C	7.9	8	8.1	MHz
2	f_{VHSI}	P	VHSI output frequency range	Over temperature range from -40 °C to 125°C	47.28	48	48.72	MHz
3	f_{LSI}	P	LSI output frequency range	Over temperature range from -40 °C to 125°C	108	128	147	KHz

7.2.3 PLL characteristics

Table 7-4 PLL characteristics

No.	Symbol	C	Parameter	Min.	Typ.	Max.	Unit
1	f_{PLL_IN}	D	PLL input clock frequency	4	—	48	MHz
2	f_{PLL_REF}	D	PLL reference clock frequency	—	—	12	MHz
3	f_{PLL_OUT}	D	PLL output clock frequency	9	—	120	MHz
4	f_{VCO_OUT}	D	VCO output frequency	500	—	1500	MHz
Operating temperature: -40~125°C $f_{PLL\_REF} = f_{PLL\_IN}$ /Prediv, Prediv can be 1,2,4							

No.	Symbol	C	Parameter	Min.	Typ.	Max.	Unit
$f_{VCO\_OUT} = f_{PLL\_REF}$ *Fbkdiv, Fbkdiv can be 5,6,7,...,254,255 $f_{PLL\_OUT} = f_{VCO\_OUT}$ /Postdiv, Postdiv can be 2,4,6,...,60,62							

7.3 Embedded Flash specifications

This section provides details about program/erase time and frequency for the Flash memory.

Table 7-5 Flash characteristics

Symbol		C	Description	Min.	Typ.	Max.	Unit
$V_{Prog/Erase}$		D	Supply voltage for program/erase at temperature from - 40°C to 125 °C	2.7	—	5.5	V
f_{SYS}		D	Flash bus frequency	8	48	120	MHz
t_{RDONCE}		D	Time for Flash read once	4	4	6	t_{cyc}[1]
t_{MER}		D	Mass erase (all main block pages)	—	32	—	ms
t_{MERPF}		D	Mass erase pflash	—	28	—	ms
t_{MERDF}		D	Mass erase dflash	—	26	—	ms
t_{PER}		D	Page erase (one page)	—	820	—	us
t_{MERV}		D	Mass erase verify(all main block pages)	295000	—	590000	t_{cyc} [1]
t_{MERVPF}		D	Mass erase verify pflash	262200	—	524400	t_{cyc}[1]
t_{MERVDF}		D	Mass erase verify dflash	32800	—	65600	t_{cyc}[1]
t_{PERV}		D	Periodical verify(n × 64bit)	2 × n	—	4 × n	t_{cyc}[1]
t_{PRG1}		D	Single program Flash (64bit)	—	95	—	us
t_{PRGn}	n≤8	D	Periodical program Flash (n × 64bit)	—	200	—	us
t_{PRGn}	n>8	D		—	(n/8 + 1) ×200	—	us
n_{EDR}		C	PFlash endurance(erase cycle times – program cycle times) at temperature from - 40°C to 125 °C	10 k	—	—	cycle
		C	DFlash endurance(erase cycle times – program cycle times) at temperature from - 40°C to 125 °C	100 k	—	—	cycle
t_{RET}		C	PFlash data retention time at an average junction temperature of TJavg = 85°C after up to 10,000 program/erase cycles	10	—	—	year
		C	DFlash data retention time at an average junction temperature of TJavg = 85°C after up to 100,000 program/erase cycles	10	—	—	year

[1] $t_{cyc} = 1/ f_{SYS}$.

7.4 Analog

7.4.1 ADC characteristics

Table 7-6 12 bit ADC and Tsensor operating conditions and characteristics

Symbol	C	Description	Condition	Min.	Typ.	Max.	Unit
V_{AVDD}	D	Supply Voltage	Absolute value	2.7	—	5.5	V
V_{REFH}	D	Positive reference input [1]	Absolute value	2.7	—	V_{AVDD}	V
V_{REFL}	D	Negative reference input [1]	Absolute value	—	0	—	V
V_{IN}	D	Input Voltage Range	—	0	—	V_{AVDD}/ V_{REFH}	V
R_{IN}	D	Input source impedance	Refer to the formula [2]	—	—	—	Ω
C_{ADC}	D	Internal Sampling Capacitor	—	—	2.4	—	pF
R_{ADC}	D	Sampling switch resistance	—	—	—	3.1	KΩ
f_{ADC}	D	ADC clock frequency	—	—	—	30	MHz
Ts	D	ADC sampling cycle	—	5/10/15/23/35/45/85/185			cycle
f_{sample}	D	Sampling time	—	—	Ts/f_{ADC}	—	s
f_{trig}	D	Conversion rate(including sampling time)	12bit: f_{ADC}=30MHz; Ts=15 cycles	—	1	—	MHz
			10bit: f_{ADC}=30MHz; Ts=10 cycles	—	1.33	—	MHz
			8bit: f_{ADC}=30MHz; Ts=10 cycles	—	1.46	—	MHz
INL	C	Integral non-linearity[3]	12bit	-3	1.5	3	LSB
DNL	C	Differential non-linearity[3]	12bit	-1	1.5	3	LSB
TUE	C	Total Unadjustable Error[3]	12bit	-8		8	LSB
CH	D	External channels	—	—	—	24	—

[1] If it's supposed to use VREFH/VREFL as ADC reference, an external voltage should be forced to VREFH and VREFL should be connected to the ground.

[2] The relationship between input source impedance and sampling time must satisfy the formula: $R_{IN} < \frac{T_s}{f_{ADC}*C_{ADC}*ln(2^{N+2})} - R_{ADC}$, N is the ADC bits, ADC sampling duration must meet the settling accuracy of 0.25LSB, and the parasitic capacitance of the PAD terminal is not considered in the formula.

[3] The test conditions of INL, DNL, and TUE are: 12bit, the conversion rate is 1MSPS, and the power supply and reference voltage are greater than 3V.

Table 7-7 12 bit ADC and Tsensor operating conditions and characteristics(continue)

Symbol	C	Description	Condition	Min.	Typ.	Max.	Unit
Slope	D	Temperature sensor slope	-40 °C–125 °C	—	1.788	—	mV/°C
V_{TEMP25}	D	Temperature sensor voltage	25 °C	—	0.673	—	V

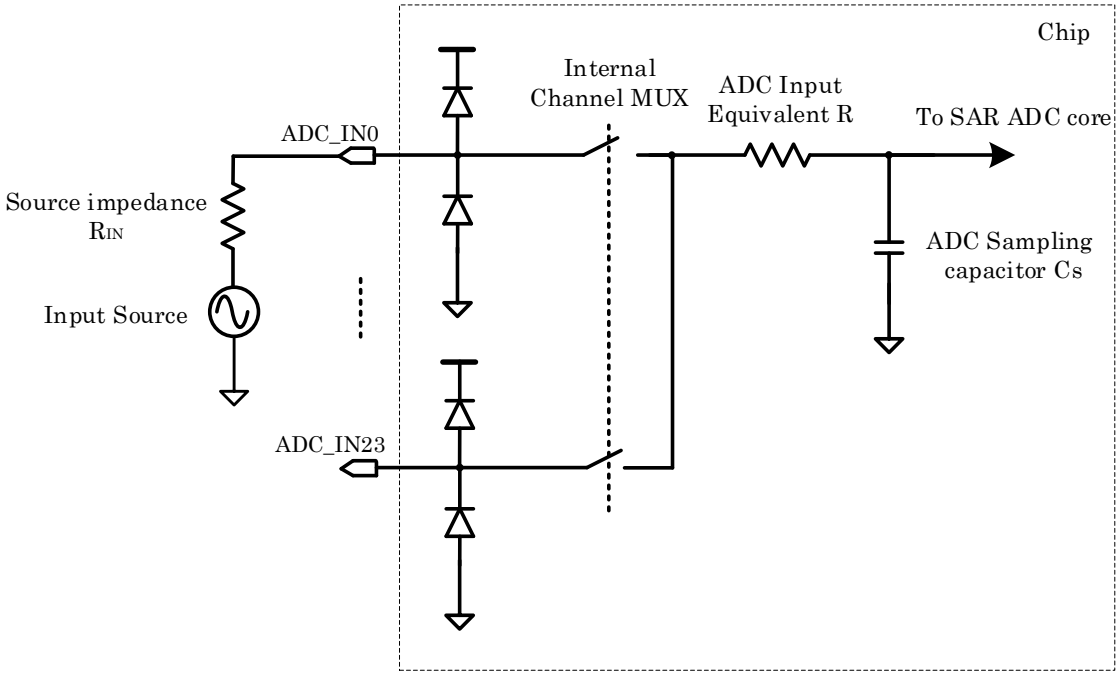

Figure 7-2 ADC input equivalent diagram

7.4.2 Analog comparator (ACMP) electricals

Table 7-8 Comparator electrical specifications

Symbol	C	Description	Min.	Typ.	Max.	Unit
V_{AVDD}	D	Supply voltage	2.7	—	5.5	V
I_{DDA}	T	Supply current (Operation mode)	—		20	μA
V_{AIN}	D	Analog input voltage	0	—	V_{AVDD}	V
V_{AIO}	P	Analog input offset voltage	-30	—	30	mV
V_{HYS}	C	Analog comparator hysteresis (HYST=0)	—	0/10/20/40	—	mV
I_{DDAOFF}	D	Supply current (Off mode)	—	—	100	nA
t_D	C	Propagation delay	—	0.4	1	μs

7.5 Communication interfaces

7.5.1 SPI specifications

The serial peripheral interface(SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes. See the SPI chapter of the chip's reference manual "ATC_AC7840x_ReferenceManual_EN" for information about the modified transfer formats used for communicating with slower peripheral devices. All timing is shown with respect to 20% V_{DD} and 80% V_{DD}. All timing assumes slew rate control is disabled and high-drive strength is enabled for SPI output pins.

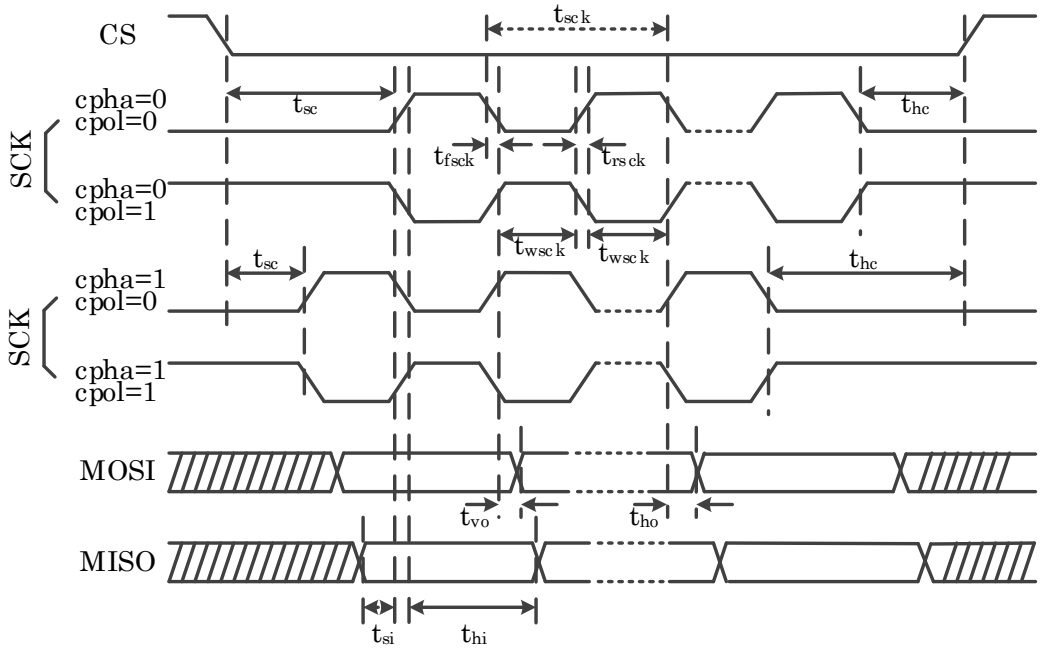

Figure 7-3 SPI timing diagram —master

Table 7-9 SPI characteristics – master

Symbol	Description	Min.	Max.	Unit	Note
f_{op}	Operation frequency	f_{clk}/512	15	MHz	f_{clk} is SPI functional clock
t_{sc}	CS setup time	1×t_{clk}	256×t_{clk}	ns	Time from Negative edge of CS to the first SCK edge(t_{clk} is the SPI functional clock cycle)
t_{hc}	CS hold time	1×t_{clk}	256×t_{clk}	ns	Time from last SCK edge to positive edge of CS
t_{wsck}	SCK high or low level time	1×t_{clk}	256×t_{clk}	ns	No considering t_{rsck} and t_{fsck}
t_{si}	Data input setup time	17	—	ns	—
t_{hi}	Data input hold time	13	—	ns	—

Symbol	Description	Min.	Max.	Unit	Note
t_{vo}	Data output valid time	—	5	ns	—
t_{ho}	Data output hold time	-3	—	ns	—

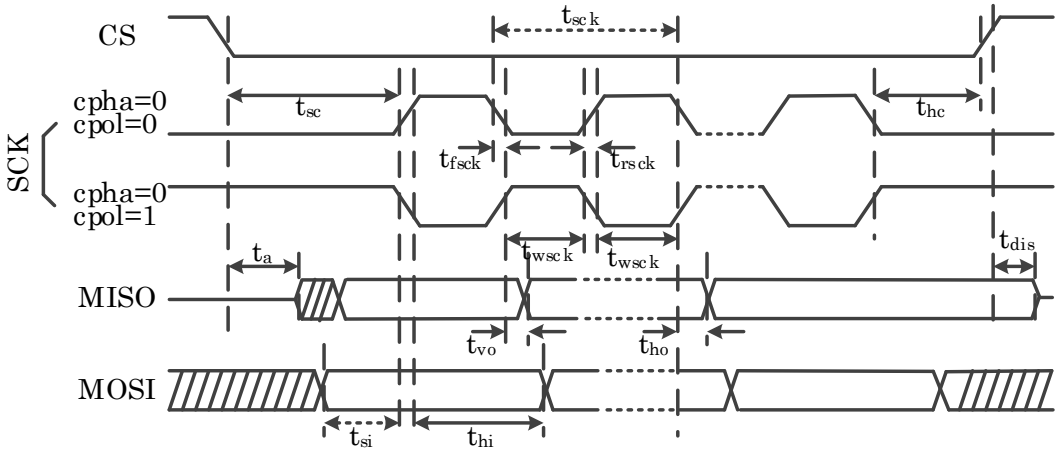

Figure 7-4 SPI timing diagram –slave(cpha=0)

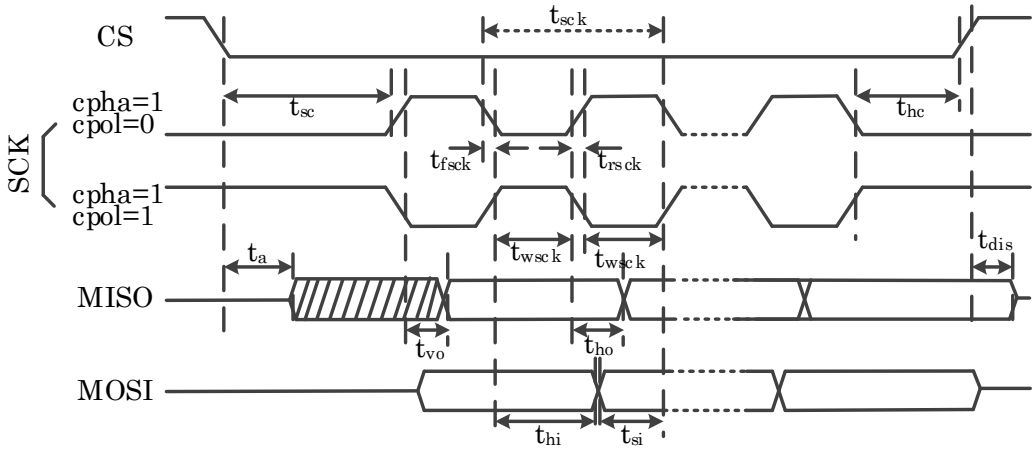

Figure 7-5 SPI timing diagram –slave(cpha=1)

Table 7-10 SPI characteristicss– master

Symbol	Descriptiom	Min.	Max.	Unit	Note
f_{op}	Operation frequency	—	15M	Hz	—
t_{sc}	CS setup time	$2\times t_{bus}$	—	ns	Time from negative edge of CS to the first SCK edge(t_{bus} is SPI APB bus clock)
t_{hc}	CS hold time	$2\times t_{bus}$	—	ns	Time from last SCK edge to positive edge of CS
t_a	Slave access time	—	35	ns	Data from “Z” to effective
t_{dis}	Slave MISO disable time	—	35	ns	Data from effective to “Z”
t_{si}	Data input setup time	16	—	ns	—
t_{hi}	Data input hold time	12	—	ns	—
t_{vo}	Data output valid time	—	30	ns	—
t_{ho}	Data output hold time	6	—	ns	—

7.5.2 CAN specifications

Table 7-11 CAN wake-up pulse characteristics

Symbol	C	Description	Min.	Typ.	Max.	Unit
t_{WUP}	D	CAN dominant wakeup pulse parameter filtered	—	—	0.9	µs
t_{WUP}	D	CAN dominant wakeup pulse parameter effective	4.7	—	—	µs

7.5.3 UART specifications

Basic function of Universal Asynchronous Receiver/Transmitter (UART) is to transmit and receive the serial data bit by bit. In order to support transmitting break field, sync field and data, additional Soft Local Interconnect Network(LIN) is included in the AC7840x chips. The main parameters of UART is introduced as below:

1. Up to 4 UART function channels and all of which support soft LIN functions (the uart function and soft LIN function of the same UART cannot be used at the same time).
2. UART can transmit or receive data with the range of baud rate from 600 bps to 3 Mbps, and the tolerance of real baud rate with ideal baud rate is less than 1%.
3. The minimum GPIO pin interrupt pulse width is 133 ns. Because of that these pins do not have a passive filter on the inputs, this is the shortest pulse width that is guaranteed to be recognized.
4. The maximum baud rate supported in soft LIN function is 20 Kbps.
5. Auto baud rate detection is selectable open or not in soft LIN function. The tolerance of received baud rate is from -20%(+/-2%) to +23% (+/-2%) in this case.
6. For the 4 UART function channels, only 0~2 channels support the function of hardware flow control.

7.5.4 I2C specifications

The following table and figure describe the timing characteristics of I2C. These parameters are refer to I2C standard requirement, and guaranteed by GPIO parameters, I2C internal circle design and user configuration.

Table 7-12 Characteristics of the I2C bus lines for different mode[1]

Symbol	Description	Standard-mode		Fast-mode		Fast-mode Plus		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{SCL}	SCL clock frequency	0	100	0	400	0	1000	KHz
$t_{HD;STA}$	hold time (repeated) START condition	4	—	0.6	—	0.26	—	µs
t_{LOW}	LOW period of the SCL clock	4.7	—	1.3	—	0.5	—	µs

t_{HIGH}	HIGH period of the SCL clock	4	—	0.6	—	0.26	—	µs
$t_{SU;STA}$	set-up time for a repeated START condition	4.7	—	0.6	—	0.26	—	µs
$t_{HD;DAT}$	Data hold time	0	—	0	—	0	—	µs
$t_{SU;DAT}$	Data setup time	250	—	100	—	50	—	ns
t_r	Rise time of both SDA and SCL signals	—	1000	20	300	—	120	ns
t_f	Fall time of both SDA and SCL signals	—	300	20 × (V_{DD} / 5.5 V)	300	20 × (V_{DD} / 5.5 V)	120	ns
$t_{SU;STO}$	Set-up time for STOP condition	4	—	0.6	—	0.26	—	µs
t_{BUF}	Bus free time between a STOP and START condition	4.7	—	1.3	—	0.5	—	µs
C_b	Capacitive load for each bus line	—	400	—	400	—	550	pF
$t_{VD;DAT}$	Data valid time	—	3.45	—	0.9	—	0.45	µs
$t_{VD;ACK}$	Data valid acknowledge time	—	3.45	—	0.9	—	0.45	µs
V_{nL}	Noise margin at the LOW level	$0.1V_{DD}$	—	$0.1V_{DD}$	—	$0.1V_{DD}$	—	V
V_{nH}	Noise margin at the HIGH level	$0.2V_{DD}$	—	$0.2V_{DD}$	—	$0.2V_{DD}$	—	V

[1]:I2C supports three modes: standard mode, fast mode and fast mode plus.

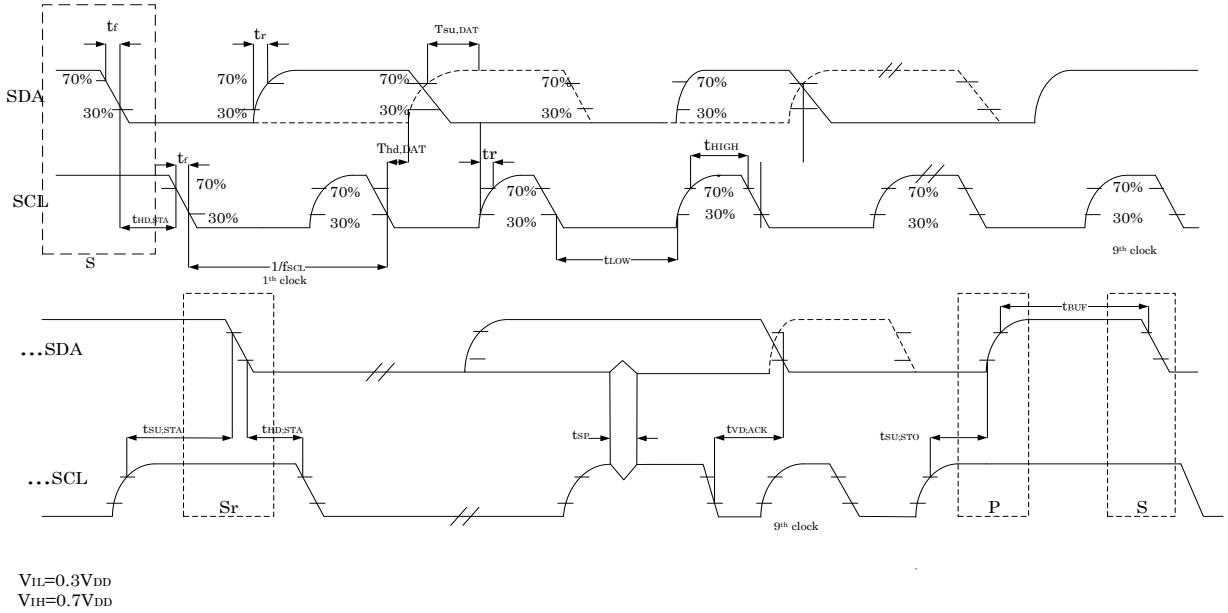

Figure 7-6 Timing for F/S-mode devices on the I2C-bus

7.5.5 EIO specifications

EIO (Enhanced IO) is a highly configurable module that provides a wide range of functions, including:

- Emulate various serial communication protocols
- Four flexible 16-bit timers supporting trigger, reset, enable and disable conditions
- Four configurable 32-bit shifters supporting transmit, receive and match memory

With 4 timers and 4 shifters, the EIO module can support a wide range of protocols, including but not limited to:

- UART transmit and receive
- I2C master
- SPI master and slave
- I2S master and slave
- PWM waveform generation

8 Dimensions

8.1 LQFP144 package information

8.1.1 LQFP144 package dimension information

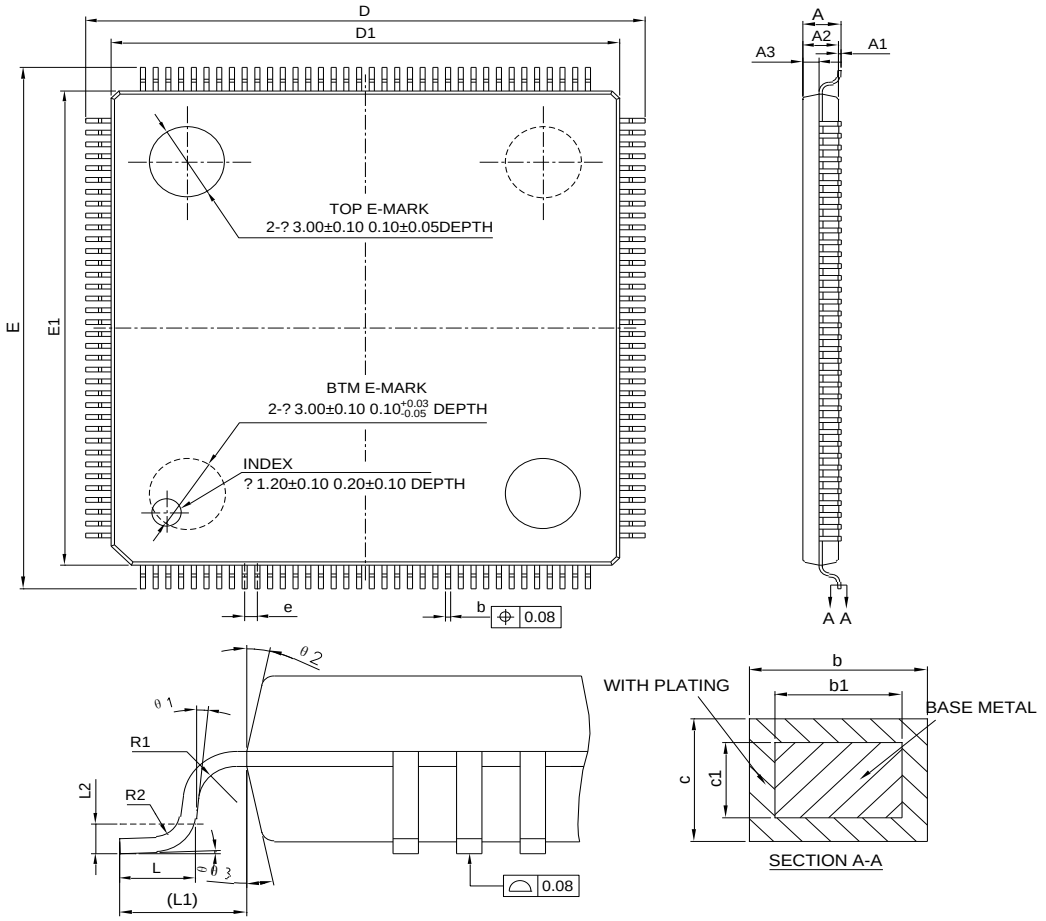

Figure 8-1 LQFP144 – 144 pin, 20*20 mm Low Profile Quad Flat Package Outline [1]

[1] Drawing is not to scale.

Table 8-1 LQFP144 – 144 pin, 20*20 mm Low Profile Quad Flat Package Mechanical Data [1]

Item	Symbol	Min.	Nom.	Max.
Total height	A	—	—	1.60
Stand off	A1	0.05	—	0.15
Mold thickness	A2	1.35	1.40	1.45
Leadframe to mold height	A3	0.59	0.64	0.69

Item		Symbol	Min.	Nom.	Max.
Lead width		b	0.17	—	0.27
Lead width without plating		b1	0.17	0.20	0.23
Leadframe thickness		c	0.127	—	0.18
Leadframe thickness without plating		c1	0.119	0.127	0.134
Outer lead distance	X	D	21.80	22.00	22.20
	Y	E	21.80	22.00	22.20
Package size	X	D1	19.90	20.00	20.10
	Y	E1	19.90	20.00	20.10
Lead pitch		e	0.40	0.50	0.60
L		L	0.45	0.60	0.75
Lead length		L1	1.00 REF		
L2		L2	0.25 BSC		
Lead forming arc radius R1		R1	0.08	—	—
Lead forming arc radius R2		R2	0.08	—	—
Angle 1		Θ	0°	—	7°
Angle 2		Θ1	0°	—	—
Angle 3		Θ2	11°	12°	13°
Angle 4		Θ3	11°	12°	13°

[1] Dimensions are expressed in millimeter.

8.1.2 LQFP144 device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

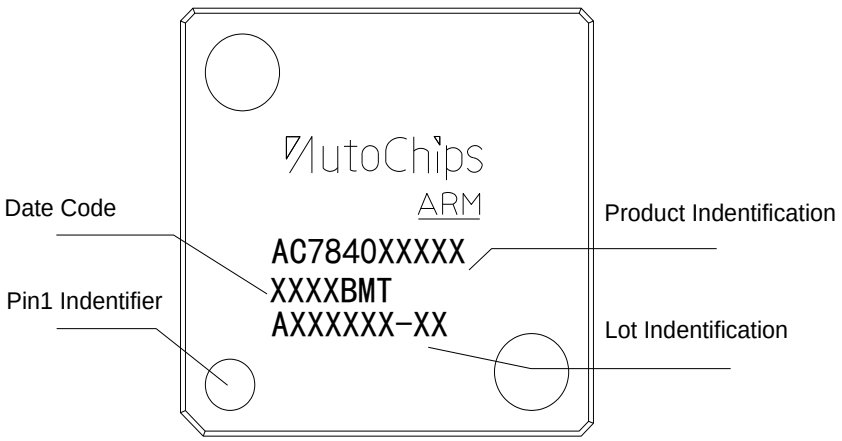

Figure 8-2 AC7840(6/7)XXXX LQFP144 marking example (package top view)

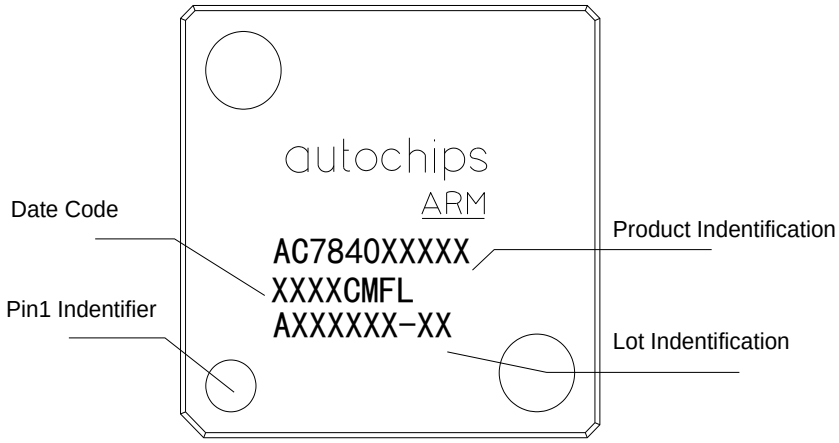

Figure 8-3 AC7840(8/9)XXXX LQFP144 marking example (package top view)

8.2 LQFP100 package information

8.2.1 LQFP100 package dimension information

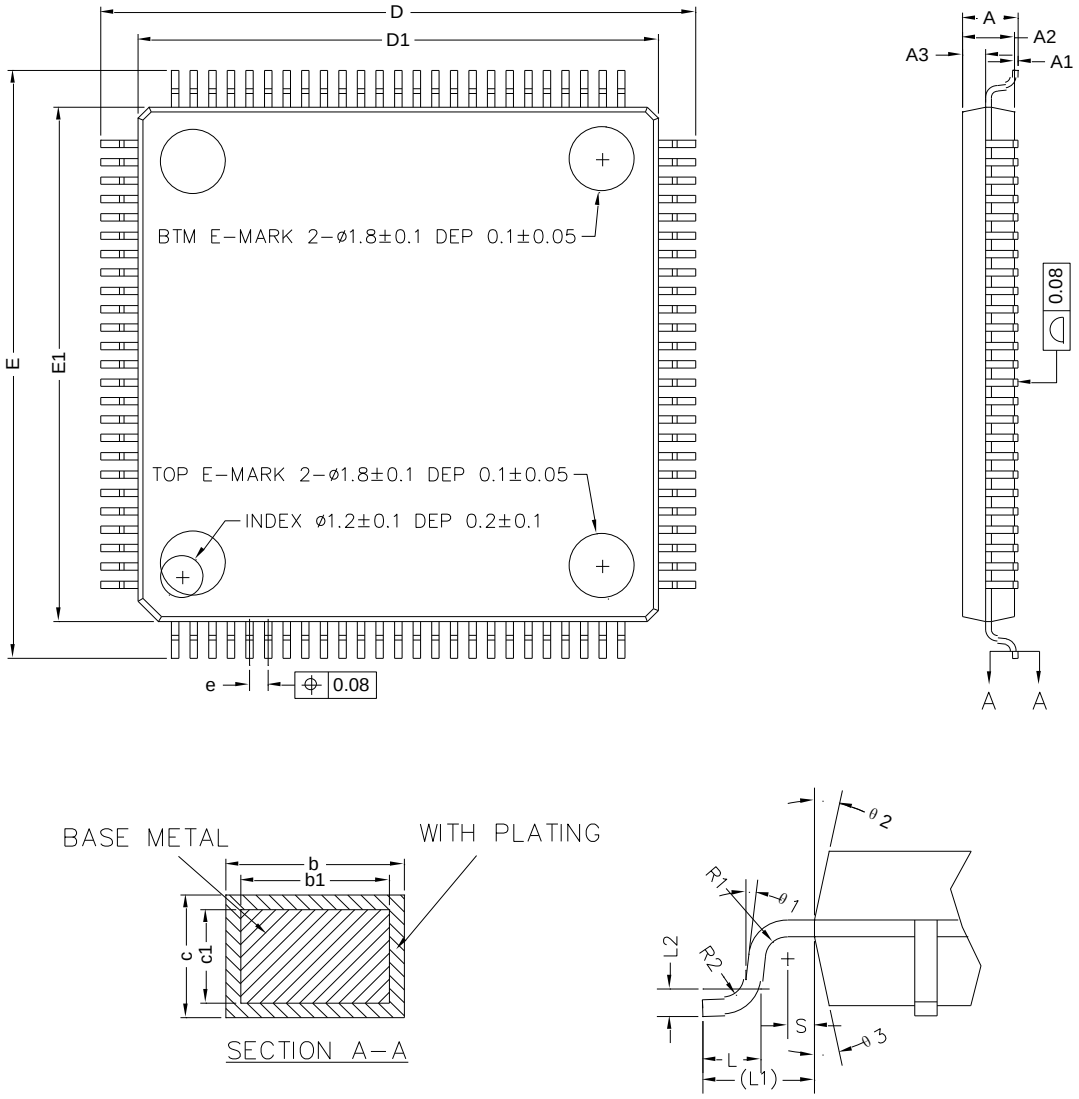

Figure 8-4 LQFP100 – 100 pin, 14x 14 mm Low Profile Quad Flat Package Outline [1]

[1] Drawing is not to scale.

Table 8-2 LQFP100 – 100 pin, 14*14 mm Low Profile Quad Flat Package Mechanical Data [1]

Item	Symbol	Min.	Nom.	Max.
Total height	A	—	—	1.60
Stand off	A1	0.05	—	0.15
Mold thickness	A2	1.35	1.40	1.45
Leadframe to mold height	A3	0.59	0.64	0.69

Item		Symbol	Min.	Nom.	Max.
Lead width		b	0.18	—	0.27
Lead width without plating		b1	0.17	0.20	0.23
Leadframe thickness		c	0.13	—	0.18
Leadframe thickness without plating		c1	0.12	0.127	0.134
Outer lead distance	X	D	15.80	16.00	16.20
	Y	E	15.80	16.00	16.20
Package size	X	D1	13.90	14.00	14.10
	Y	E1	13.90	14.00	14.10
Lead pitch		e	0.40	0.50	0.60
L		L	0.45	0.60	0.75
Lead length		L1	1.00 REF		
L2		L2	0.25 BSC		
Lead forming arc radius R1		R1	0.08	—	—
Lead forming arc radius R2		R2	0.08	—	0.20
Angle 1		Θ	0°	3.5°	7°
Angle 2		Θ1	0°	—	—
Angle 3		Θ2	11°	12°	13°
Angle 4		Θ3	11°	12°	13°

[1] Dimensions are expressed in millimeter.

8.2.2 LQFP100 device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

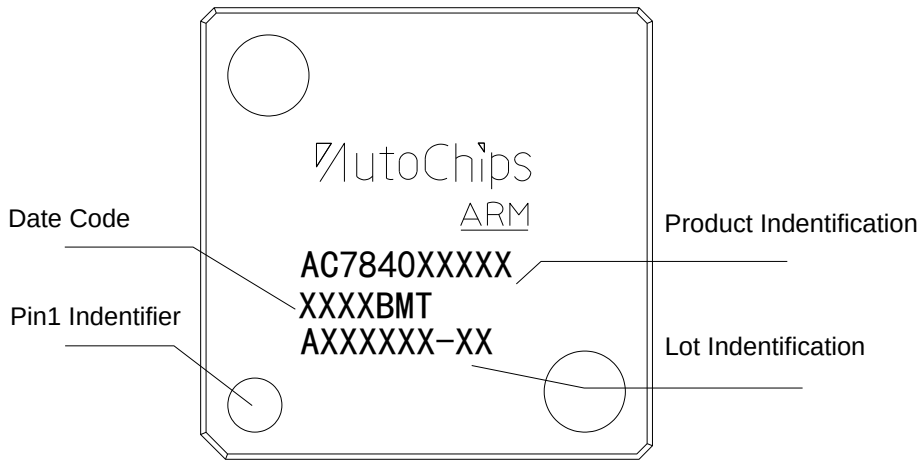

Figure 8-5 AC7840(6/7)XXXX LQFP100 marking example (package top view)

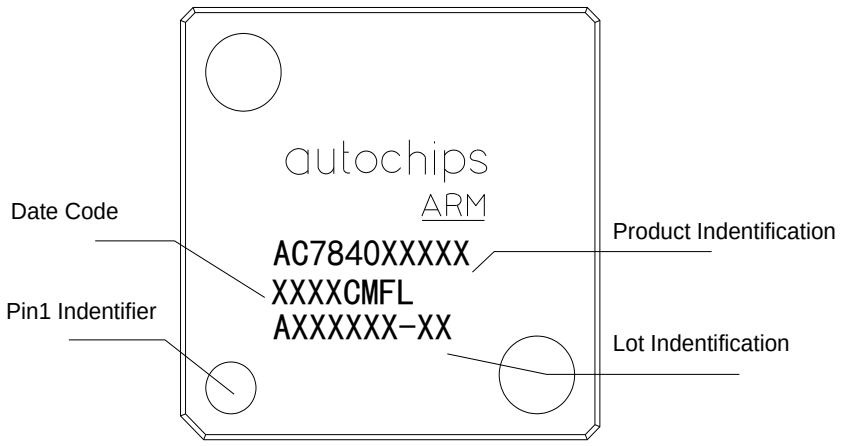

Figure 8-6 AC7840(8/9)XXXX LQFP100 marking example (package top view)

8.3 LQFP64 package information

8.3.1 LQFP64 package dimension information

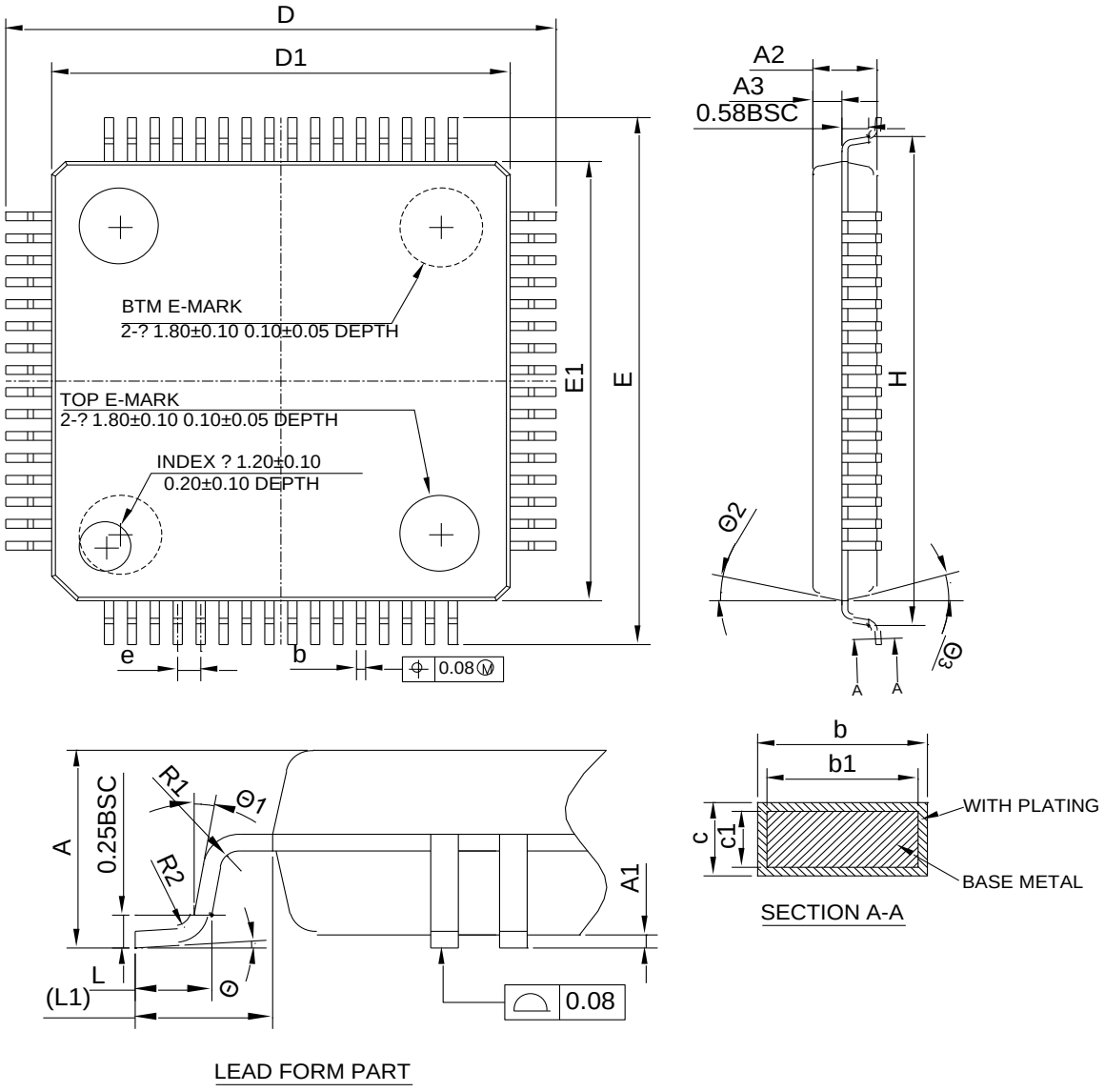

Figure 8-7 LQFP64 – 64 pin, 10 x 10 mm Low Profile Quad Flat Package Outline [1]

[1] Drawing is not to scale.

Table 8-3 LQFP64 – 64 pin, 10 x10 mm Low Profile Quad Flat Package mechanical data [1]

Item	Symbol	Min.	Nom.	Max.
Total height	A	—	—	1.60
Stand off	A1	0.05	—	0.15
Mold thickness	A2	1.35	1.40	1.45

Item		Symbol	Min.	Nom.	Max.
Leadframe to mold height		A3	0.59	0.64	0.69
Lead width		b	0.18	—	0.27
Lead width without plating		b1	0.17	0.20	0.23
Leadframe thickness		c	0.13	—	0.18
Leadframe thickness without plating		c1	0.117	0.127	0.137
Outer lead distance	X	D	11.95	12.00	12.05
	Y	E	11.95	12.00	12.05
Package size	X	D1	9.90	10.00	10.10
	Y	E1	9.90	10.00	10.10
Lead pitch		e	0.40	0.50	0.60
H		H	11.09	11.13	11.17
L		L	0.53	—	0.70
Lead length		L1	1.00 REF		
Lead forming arc radius R1		R1	0.15REF		
Lead forming arc radius R2		R2	0.13REF		
Angle 1		Θ	0°	3.5°	7°
Angle 2		Θ1	0°	—	—
Angle 3		Θ2	11°	12°	13°
Angle 4		Θ3	11°	12°	13°

[1] Dimensions are expressed in millimeters.

8.3.2 LQFP64 device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

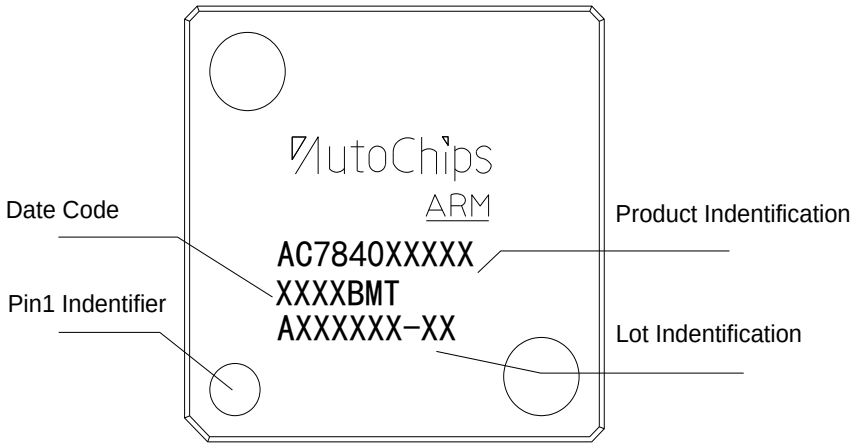

Figure 8-8 AC7840(6/7)XXXX LQFP64 marking example (package top view)

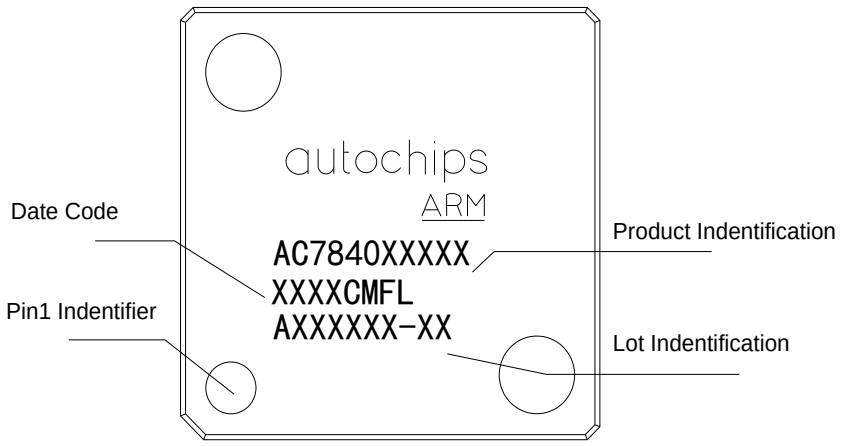

Figure 8-9 AC7840(8/9)XXXX LQFP64 marking example (package top view)

9 Pin Assignments

9.1 Signal multiplexing and pin assignments

For more information about the signals available on each pin and the locations of these pins on the devices, please refer to the “ATC_AC7840x_PINMUX.xlsx”.

The General-Purpose Input/Output (GPIO) module is responsible for selecting which ALT functionality is available on each pin. For more information, see chapter GPIO in “ATC_AC7840x_ReferenceManual_EN”.

9.2 Device pin assignment

9.2.1 LQFP144 package

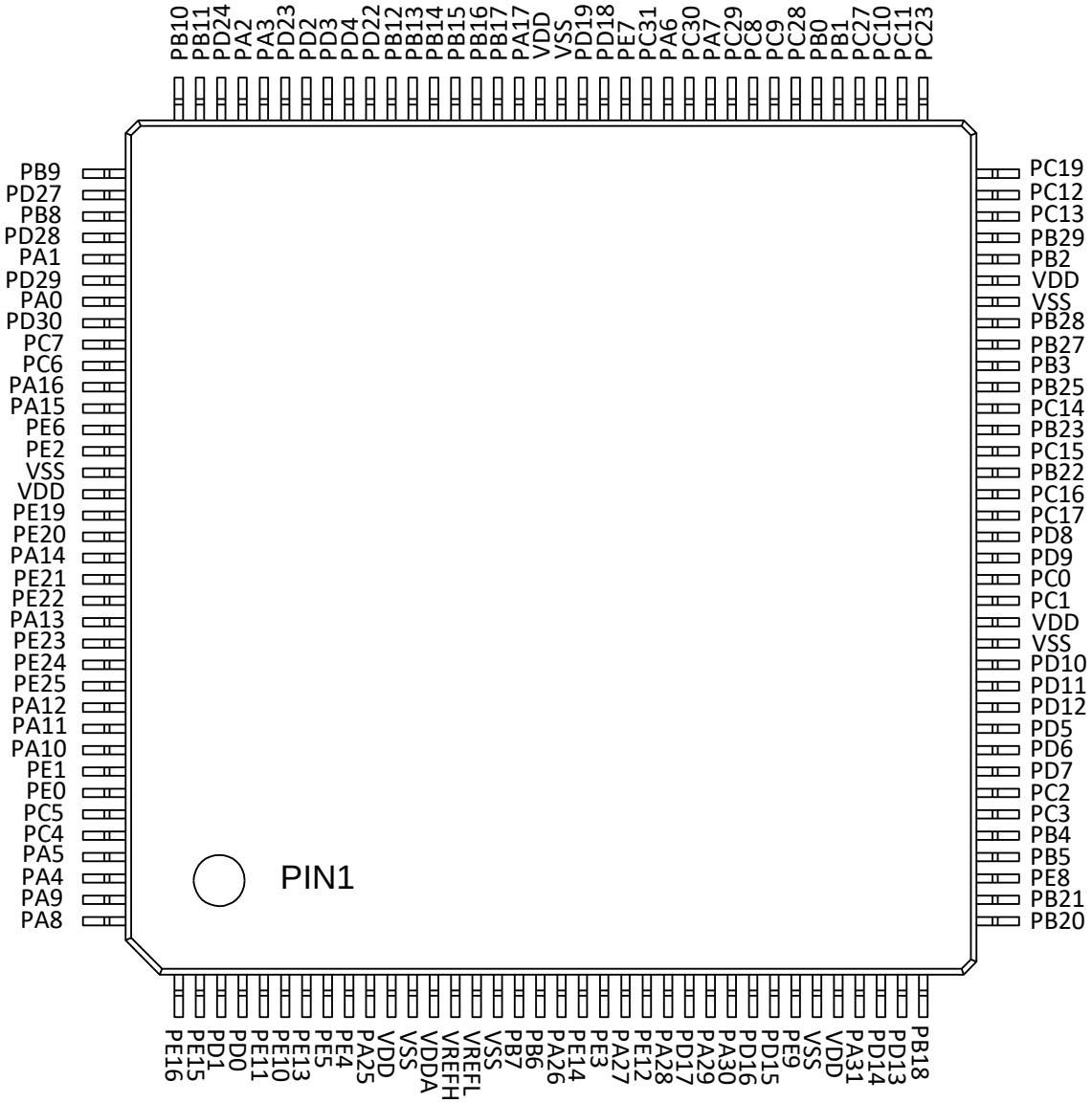

Figure 9-1 LQFP144 package

9.2.2 LQFP100 package

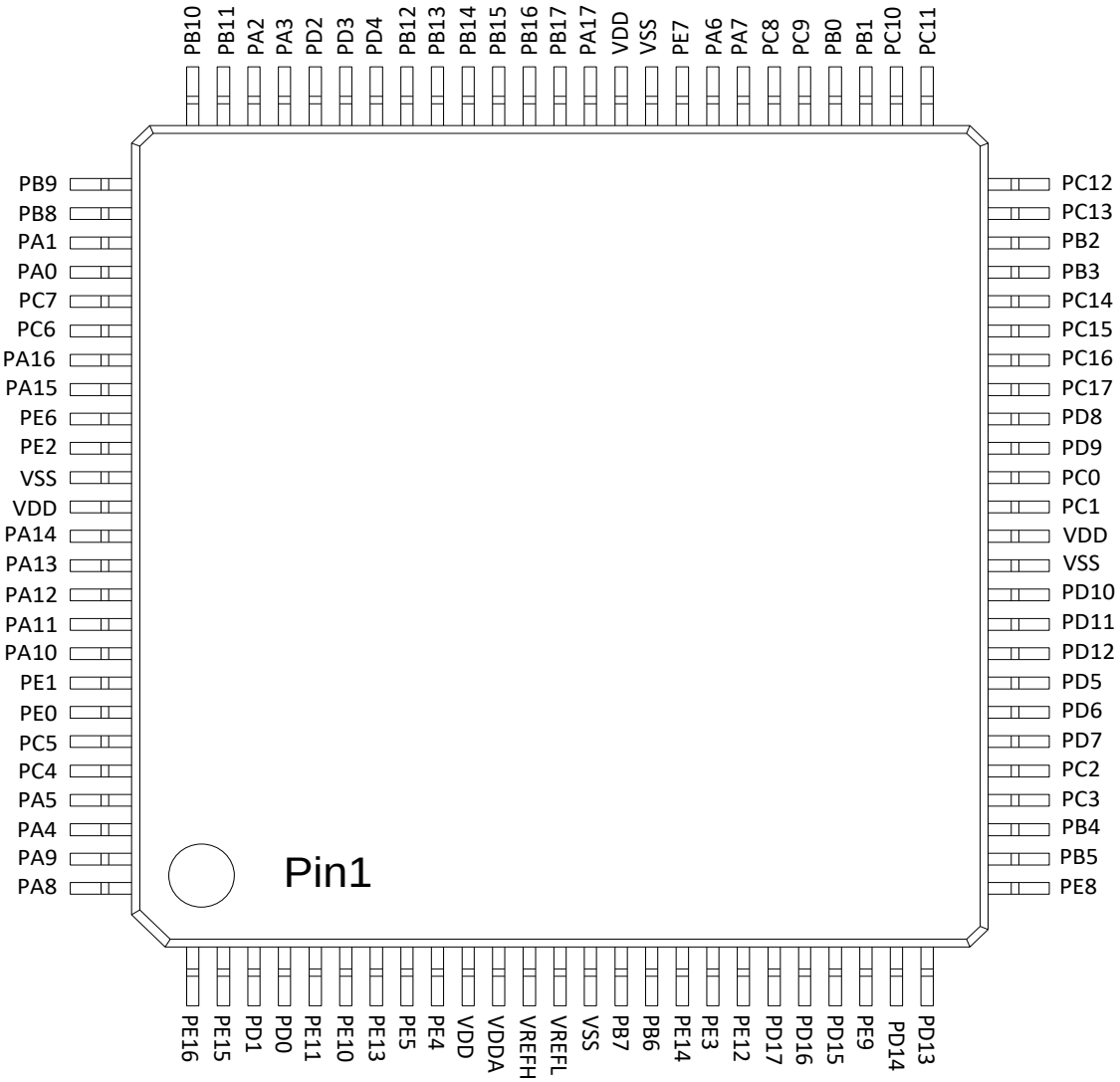

Figure 9-2 LQFP100 package

9.2.3 LQFP64 package

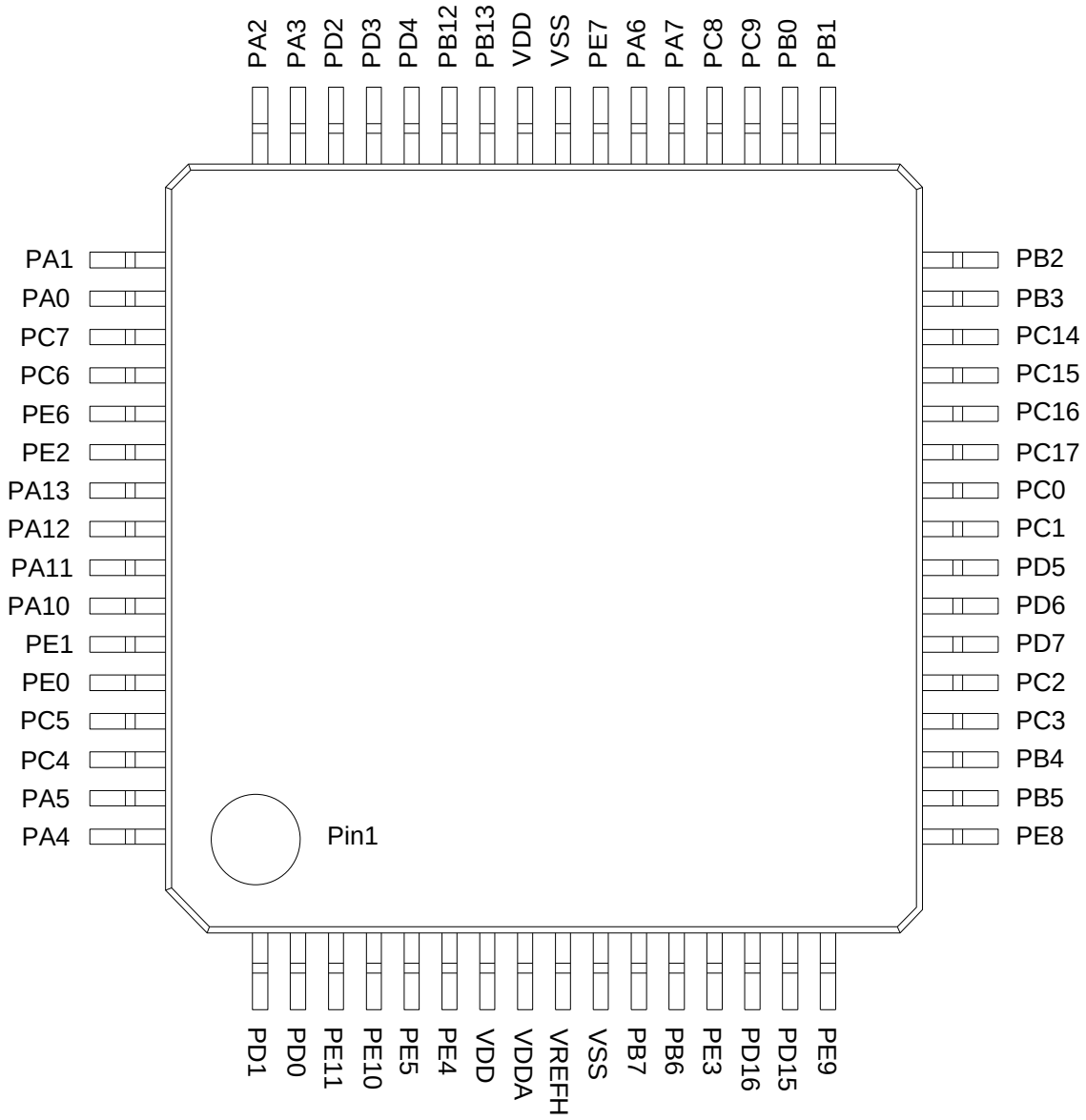

Figure 9-3 LQFP64 package

单击下面可查看定价，库存，交付和生命周期等信息

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