# I$^2$S/TDM Input, High Efficiency, 10.25V BOOST Digital Smart K Audio Amplifier

## FEATURES

- **Integrates SKTune Algorithm**
  - **Soundness Enhancement**
  - **Audio Path Parametric Equalizer**
  - **Multi-Band Dynamic Range Compressor**
  - **Programmable Power Control**
  - **Anti-Clip Voltage Limiter**
- **Smart BOOST with total efficiency up to 80%**
- **High RF noise suppression, eliminate the TDD noise completely**
- **Low noise: 12uV**
- **THD+N: 0.02%**
- Supports 6Ω Speaker
- Extensive Pop-Click Suppression
- Volume control(from -96dB to 0dB)
- I$^2$S/TDM interface：
  - I$^2$S, Left-Justified and Right-Justified
  - Supports four slots TDM
  - Input Sample Rates from 8kHz to 96kHz
  - Data Width: 16, 20, 24, 32 Bits
- I$^2$C-bus control interface(400kHz)
- Power Supplies：
  - VDD：3.0V-5.5V
  - DVDD: 1.65V-1.95V
  - VDDIO: 1.65V-3.6V
- Short-Circuit Protection, Over-Temperature Protection, Under-Voltage Protection and Over-Voltage Protection
- WLCSP 2.48X3.17-48B package

## APPLICATIONS

- Mobile phones
- Tablets
- Portable Audio Devices

## DESCRIPTION

The AW82194 is an I$^2$S/TDM input, high efficiency digital Smart K audio amplifier with an integrated 10.25V smart boost converter and SKTune algorithms. Due to its 12uV noise floor and ultra-low distortion, clean listening is guaranteed. It can deliver 5.3W output power into an 8Ω speaker at 1% THD+N.

The AW82194 integrates SKTune algorithm that maximizes speaker performance while maintaining safe speaker conditions. It also increases loudness and enhances the quality of audio signal.

The AW82194 integrates a high-efficiency smart boost converter as the Class-D amplifier supply rail. The output voltage of boost converter can be adjusted smartly according to the input amplitude, which extremely improves the efficiency without clipping distortion.

The AW82194 features high RF suppression and eliminates TDD noise completely benefited from the digital audio input interface. General settings are communicated via an I$^2$C-bus interface, and the device address is configurable.

The AW82194 offers Short Circuit Protection, Over-Temperature Protection, Under-Voltage Protection and Over-Voltage Protection to protect the device.

AW82194 is available in a WLCSP 2.48X3.17-48B package.
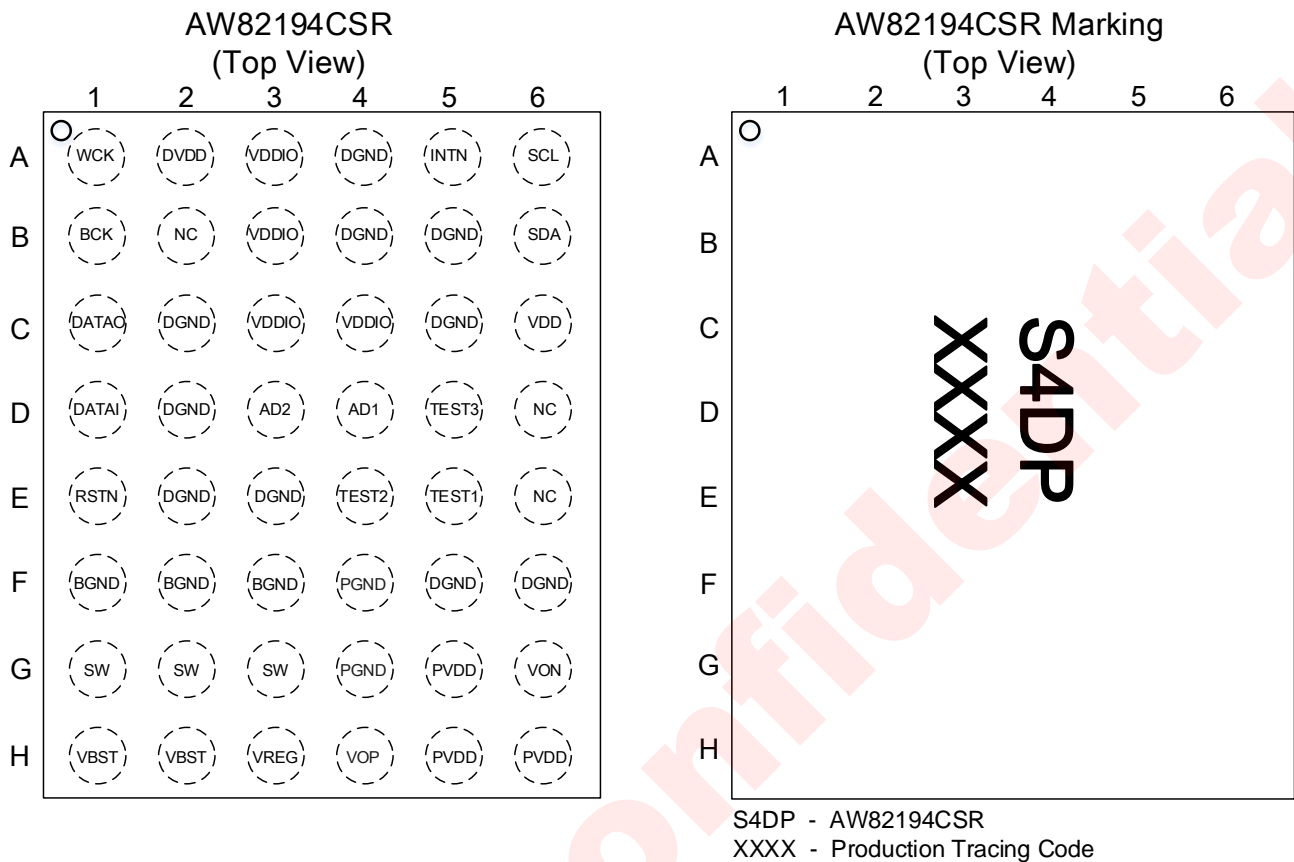
## PIN CONFIGURATION AND TOP MARK

AW82194CSR
(Top View)



AW82194CSR Marking
(Top View)

S4DP - AW82194CSR
XXXX - Production Tracing Code

**Figure 1    AW82194CSR pin diagram top view and device marking**

## PIN DESCRIPTION

| Pin No | Pin Name | Description |
|--------|----------|-------------|
| A1 | WCK | I$^2$S word select input / TDM frame sync signal |
| A2 | DVDD | Digital power supply |
| A3,B3,C3,C4 | VDDIO | Digital IO power supply |
| A4,B4,B5,C2,C5, D2,E2,E3,F5,F6 | DGND | Digital GND |
| A5 | INTN | Interrupt output |
| A6 | SCL | I$^2$C clock input |
| B1 | BCK | I$^2$S/TDM bit clock input |
| B2,D6,E6 | NC | Not connected |
| B6 | SDA | I$^2$C data I/O |
| C1 | DATAO | I$^2$S/TDM data out |
| C6 | VDD | Battery power supply |

| Pin No | Pin Name | Description |
|--------|----------|-------------|
| D1 | DATAI | I$^2$S/TDM data input |
| D3 | AD2 | I$^2$C address select input 2 |
| D4 | AD1 | I$^2$C address select input 1 |
| D5 | TEST3 | Test signal input 3, connected to ground |
| E1 | RSTN | Active low hardware reset |
| E4 | TEST2 | Test signal input 2, connected to ground |
| E5 | TEST1 | Test signal input 1, connected to ground |
| F1,F2,F3 | BGND | Boost GND |
| F4,G4 | PGND | Power GND |
| G1,G2,G3 | SW | Boost switch pin |
| G5,H5,H6 | PVDD | Class-D power supply |
| G6 | VON | Inverting Class-D output |
| H1,H2 | VBST | Boost output |
| H3 | VREG | Voltage output of regulator |
| H4 | VOP | Non-inverting Class-D output |

# FUNCTIONAL BLOCK DIAGRAM
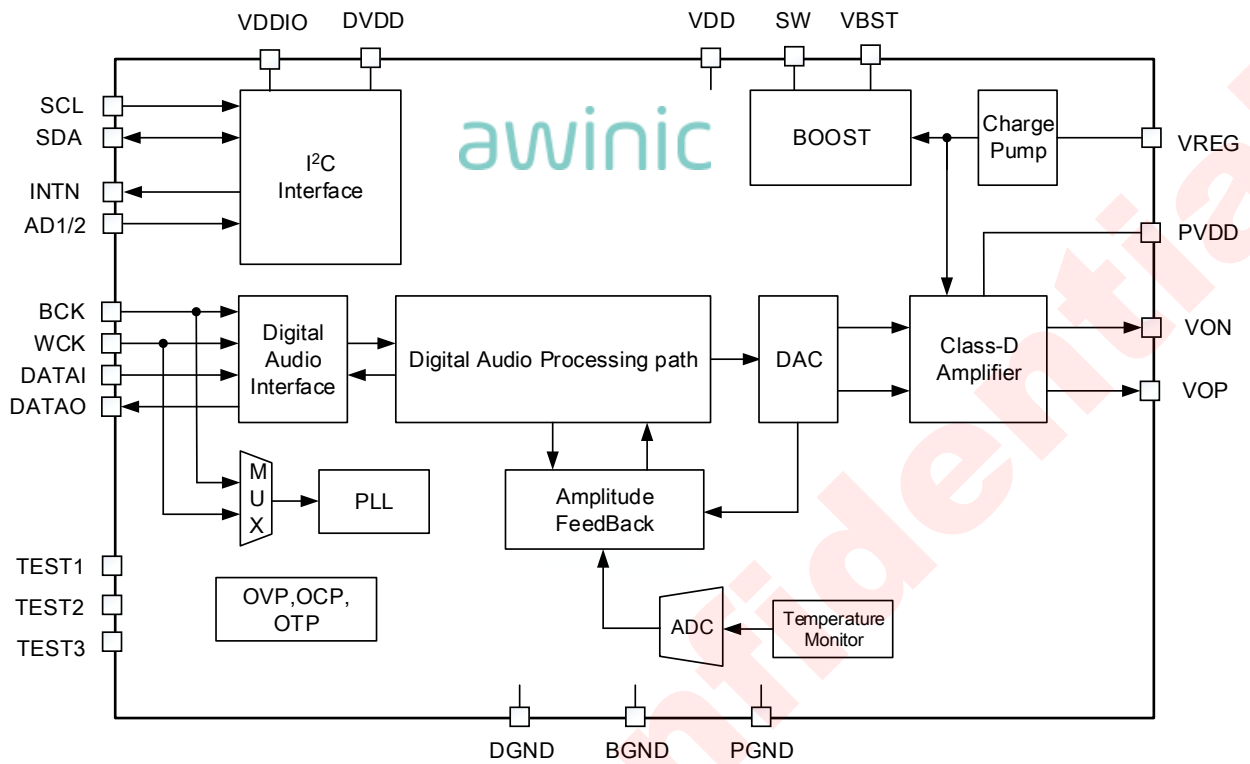


**Figure 2  FUNCTIONAL BLOCK DIAGRAM**
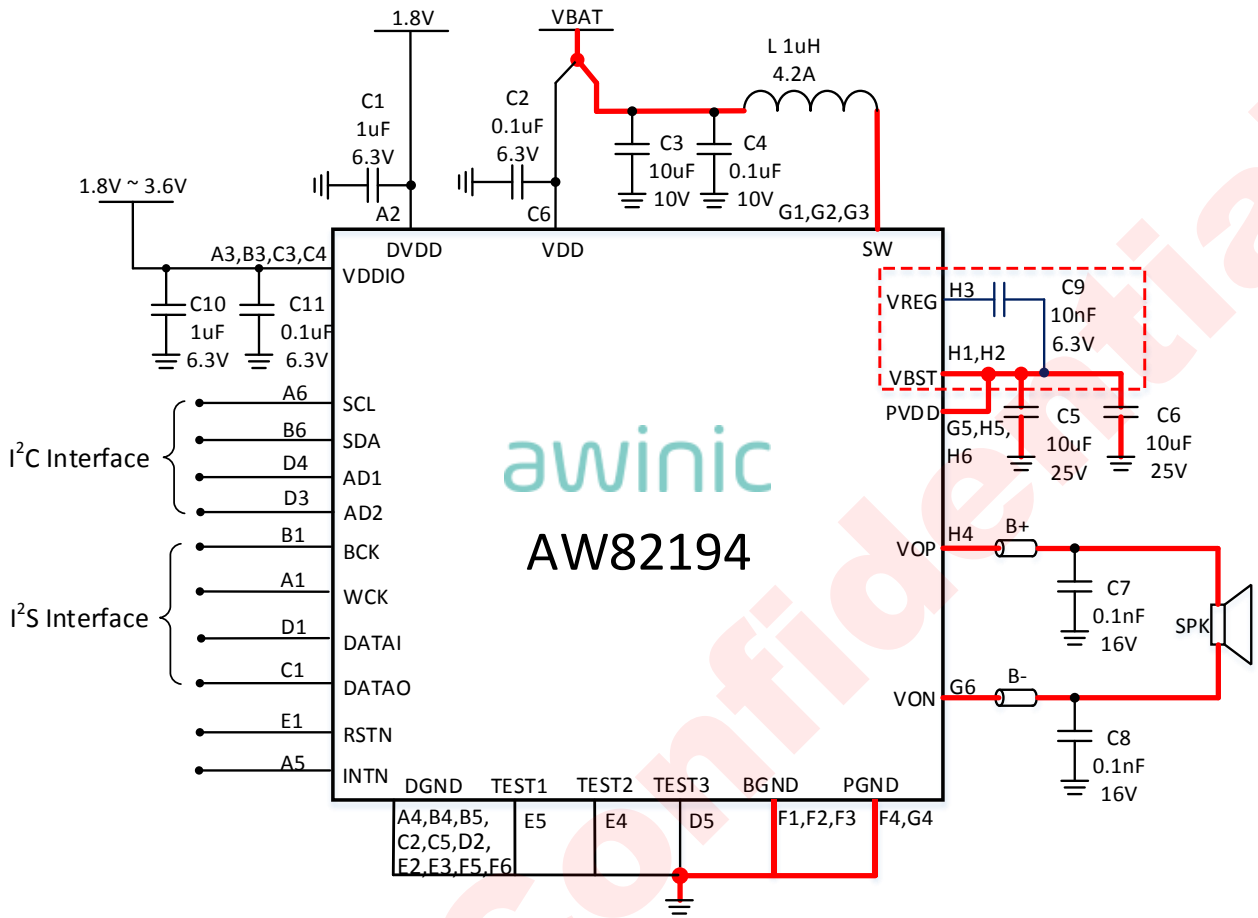
## APPLICATION DIAGRAM



**Figure 3  AW82194 Application Circuit**

Note: Traces carry high current are marked in red in the above figure

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## ORDERING INFORMATION

| Product Type | Temperature | Package | Device Marking | Moisture Sensitivity Level | Environmental Information | Delivery Form |
|---|---|---|---|---|---|---|
| AW82194CSR | -40℃～85℃ | WLCSP 2.48X3.17-48B | S4DP | MSL1 | RoHS+HF | 6000 units/ Tape and Reel |

## ABSOLUTE MAXIMUM RATING(NOTE1)

| Parameter | Range |
|---|---|
| Battery Supply Voltage $V_{DD}$ | -0.3V to 6V |
| Digital Supply Voltage $V_{DVDD}$ | -0.3V to 2V |
| Digital IO Supply Voltage $V_{DDIO}$ | -0.3V to 4.6V |
| Boost output voltage $V_{PVDD}$ | -0.3 to 13V |
| Boost SW pin voltage | -0.3 to $V_{PVDD}$+2V |
| VREG pin voltage | -0.3 to $V_{PVDD}$+5V |
| Minimum load resistance $R_L$ | 5Ω |
| Package Thermal Resistance $\theta_{JA}$ | 60°C/W |
| Ambient Temperature Range | -40°C to 85°C |
| Maximum Junction Temperature $T_{JMAX}$ | 165°C |
| Storage Temperature Range $T_{STG}$ | -65°C to 150°C |
| Lead Temperature（Soldering 10 Seconds） | 260°C |
| ESD Rating [Note 2,3] | |
| HBM（Human Body Model） | ±2000V |
| CDM(Charge Device Model) | ±1000V |
| Latch-up | |
| Test Condition：JEDEC STANDARD NO.78E SEPTEMBER 2016 | +IT：450mA<br>-IT：-450mA |

*Note 1*：*Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.*

*Note 2*：*The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: MIL-STD-883J Method 3015.9*

*Note 3*：*Test method: JEDEC EIA/JESD22-C101F*

# ELECTRICAL CHARACTERISTICS

## CHARACTERISTICS

Test condition : $T_A$=25°C , VDD=3.6V , DVDD=1.8V , VDDIO=1.8V , PVDD=10.25V , $R_L$=8Ω+33μH , f=1kHz(unless otherwise noted)

| Symbol | Description | Test Conditions | Min | Typ. | Max | Units |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Battery supply voltage | On pin VDD | 3 | | 5.5 | V |
| $V_{DVDD}$ | Digital supply voltage | On pin DVDD | 1.65 | 1.8 | 1.95 | V |
| $V_{DDIO}$ | Digital IO supply voltage | On pin VDDIO | 1.65 | | 3.6 | V |
| $I_{VDD}$ | Battery supply current | Operating mode | | 5.5 | | mA |
| | | Power down mode | | 0.3 | 2 | μA |
| $I_{DVDD}$ | Digital supply current | Operating mode, SKTune Speaker Protection Algorithm bypassed | | 4.5 | | mA |
| | | Operating mode, SKTune Speaker Protection Algorithm activated | | 10 | | mA |
| | | Power down mode | | 5 | | μA |
| **Boost** | | | | | | |
| $V_{PVDD}$ | Boost output voltage | | | 10.25 (Note1) | | V |
| $V_{OVP}$ | Over-voltage threshold | | | $V_{PVDD}$+ 0.5 | | V |
| | OVP hysteresis voltage | | | 500 | | mV |
| $I_{L\_PEAK}$ | Inductor peak current limit | | | 3.5 | | A |
| $F_{BST}$ | Operating Frequency | fs = 48KHz | | 1.6 | | MHz |
| $D_{MAX}$ | The maximum duty cycle | | | 90 | | % |
| $\eta_{BST}$ | Boost converter efficiency | VDD=4.2V, $P_O$ = 2.5W | | 88 | | % |
| **Class-D** | | | | | | |
| $R_{dson}$ | Drain-Source on-state resistance | High side MOS + Low side MOS | | 350 | | mΩ |
| Po | Speaker Output Power | THD+N=1%, $R_L$=8Ω+33μH, $V_{DD}$=4.2V, PVDD=10.25V | | 5.3 | | W |
| | | THD+N=10%, $R_L$=8Ω+33μH, $V_{DD}$=4.2V, PVDD=10.25V | | 6.4 | | W |
| | | THD+N=1%, $R_L$=6Ω+33μH, $V_{DD}$=4.2V, PVDD=10.25V | | 5.4 | | W |
| | | THD+N=10%, $R_L$=6Ω+33μH, $V_{DD}$=4.2V, PVDD=10.25V | | 6.5 | | W |

| Symbol | Description | Test Conditions | | Min | Typ. | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{OS}$ | Output offset voltage | I²S signal input 0 | | -30 | 0 | 30 | mV |
| η | Total efficiency (Class-D) | $V_{DD}$=4.2V, Po=0.25W, $R_L$=8Ω+33μH | | | 88 | | % |
| | Total efficiency (Boost+Class-D) | $V_{DD}$=4.2V, Po=1.5W, $R_L$=8Ω+33μH | | | 82 | | % |
| THD+N | Total harmonic distortion plus noise | $V_{DD}$=4.2V, Po=1W, $R_L$=8Ω+33μH, f=1kHz , PVDD=10.25V | | | 0.02 | | % |
| $E_N$ | Speaker Mode Output noise | A-weighting | | | 22 | | μV |
| | Receiver Mode Output noise | A-weighting | | | 12 | | μV |
| SNR | Signal-to-noise ratio | $V_{DD}$=4.2V, PVDD=10.25V, Po=5.3W, $R_L$=8Ω+33μH, A-weighting | | | 108 | | dB |
| PSRR | Power supply rejection ratio | Receiver Mode , $V_{DD}$=4.2V, $V_{p-p\_sin}$=200mV | 217Hz | | -85 | | dB |
| | | | 1kHz | | -80 | | dB |
| **Digital Logical Interface** | | | | | | | |
| $V_{IL}$ | Logic input low level | BCK, WCK, DATAI Pin | | | | 0.3 x $V_{DDIO}$ | V |
| $V_{IH}$ | Logic input high level | | | 0.7 x $V_{DDIO}$ | | $V_{DDIO}$ | V |
| $V_{IL}$ | Logic input low level | RSTN, SCL, SDA, AD1, AD2 Pin | | | | 0.3 x $V_{DVDD}$ | V |
| $V_{IH}$ | Logic input high level | | | 0.7 x $V_{DVDD}$ | | 3.6 | V |
| $V_{OL}$ | Logic output low level | $I_{OUT}$=2mA | | | | 0.45 | V |
| $V_{OH}$ | Logic output high level | $I_{OUT}$=-2mA | | $V_{DDIO}$ - 0.45 | | $V_{DDIO}$ | V |
| **Protection** | | | | | | | |
| $T_{SD}$ | Over temperature protection threshold | | | | 160 | | °C |
| $T_{SDR}$ | Over temperature protection recovery threshold | | | | 130 | | °C |
| UVP | Under-voltage protection voltage | | | | 2.6 | | V |
| | Under-voltage protection hysteresis voltage | | | | 100 | | mV |

*Note 1*：*Registers are adjustable; Refer to the list of registers.*

## I²C INTERFACE TIMING

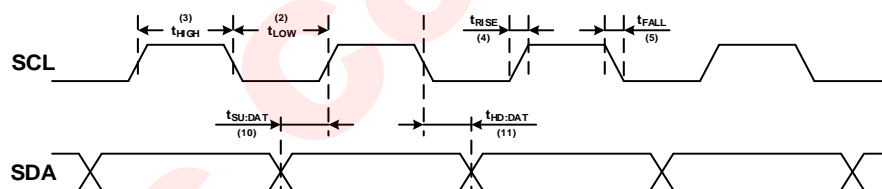| No. | Sym | Name | MIN | TYP | MAX | UNIT |
|-----|-----|------|-----|-----|-----|------|
| | | **Parameter** | | | | |
| 1 | $f_{SCL}$ | SCL Clock frequency | | | 400 | kHz |
| 2 | $t_{LOW}$ | SCL Low level Duration | 1.3 | | | µs |
| 3 | $t_{HIGH}$ | SCL High level Duration | 0.6 | | | µs |
| 4 | $t_{RISE}$ | SCL, SDA rise time | | | 0.3 | µs |
| 5 | $t_{FALL}$ | SCL, SDA fall time | | | 0.3 | µs |
| 6 | $t_{SU:STA}$ | Setup time SCL to START state | 0.6 | | | µs |
| 7 | $t_{HD:STA}$ | (Repeat-start) Start condition hold time | 0.6 | | | µs |
| 8 | $t_{SU:STO}$ | Stop condition setup time | 0.6 | | | µs |
| 9 | $t_{BUF}$ | the Bus idle time START state to STOP state | 1.3 | | | µs |
| 10 | $t_{SU:DAT}$ | SDA setup time | 0.1 | | | µs |
| 11 | $t_{HD:DAT}$ | SDA hold time | 10 | | | ns |



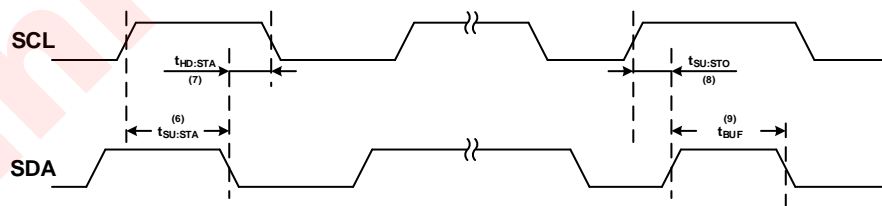**Figure 4  SCL and SDA timing relationships in the data transmission process**



**Figure 5  The timing relationship between START and STOP state**

## DIGITAL AUDIO INTERFACE TIMING

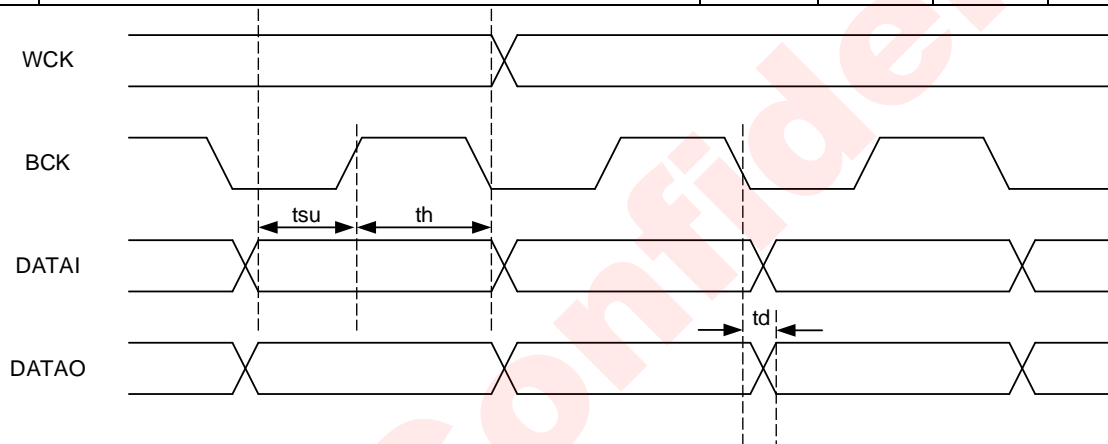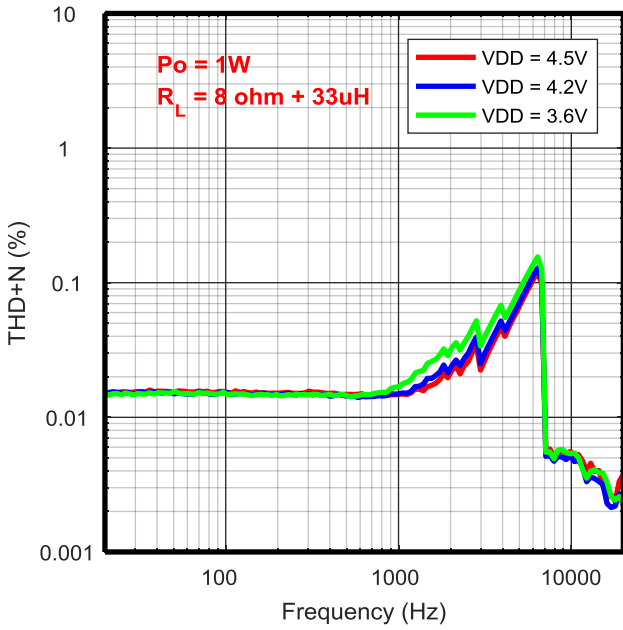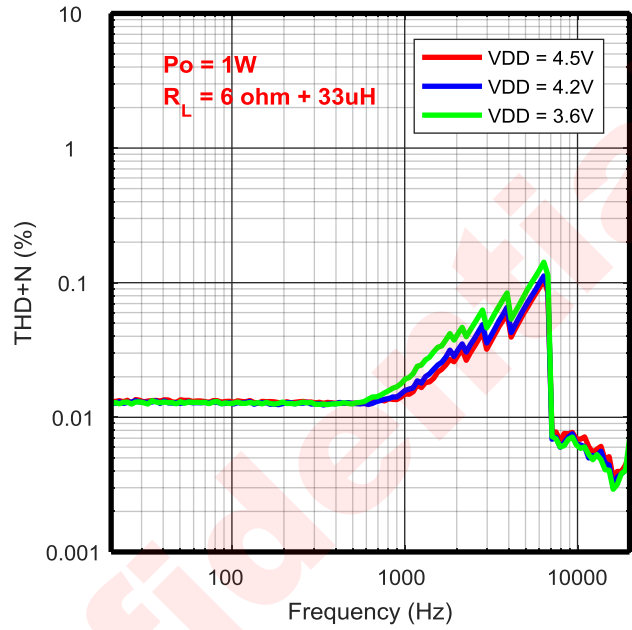| Parameter Name | | Min | Typ. | Max | Units |
|---|---|---|---|---|---|
| $f_s$ | sampling frequency, on pin WCK | 8 | | 96 | kHz |
| $f_{bck}$ | Bit clock frequency, on pin BCK | 32*fs | | 64*fs | Hz |
| $t_{su}$ | WCK, DATAI Setup time to BCK | 10 | | | ns |
| $t_h$ | WCK, DATAI hold time to BCK | 10 | | | ns |
| $t_d$ | DATAO output delay time to BCK | | | 50 | ns |

**Figure 6  Digital Audio Interface Timing**

## TYPICAL CHARACTERISTIC CURVES

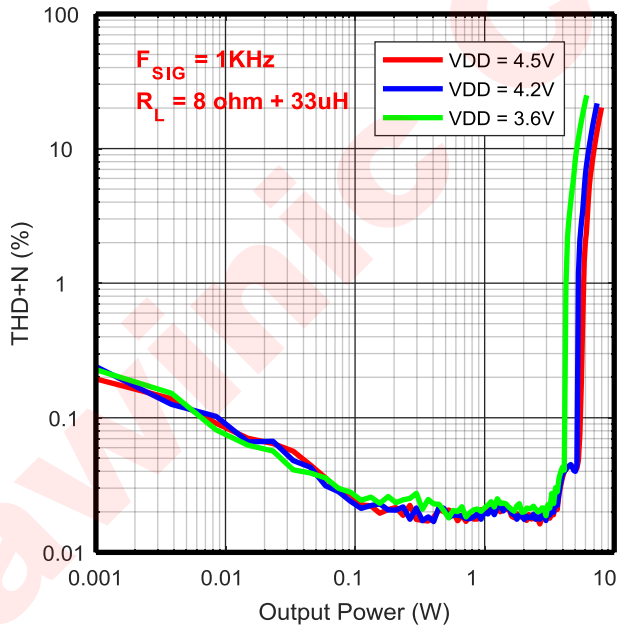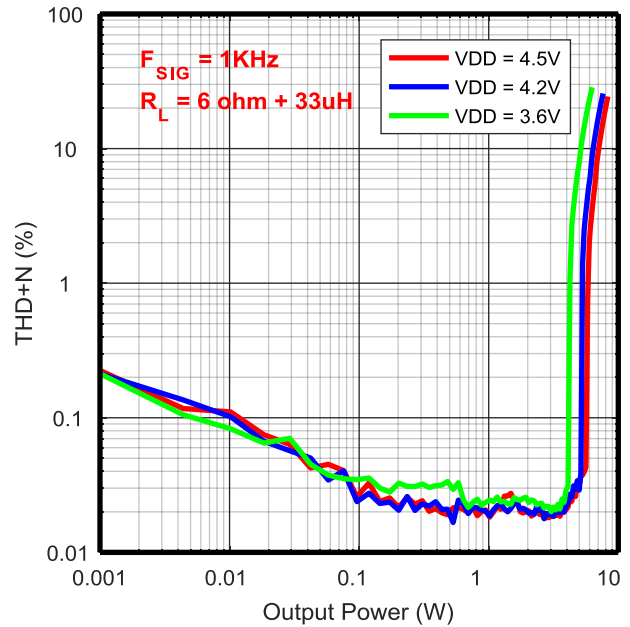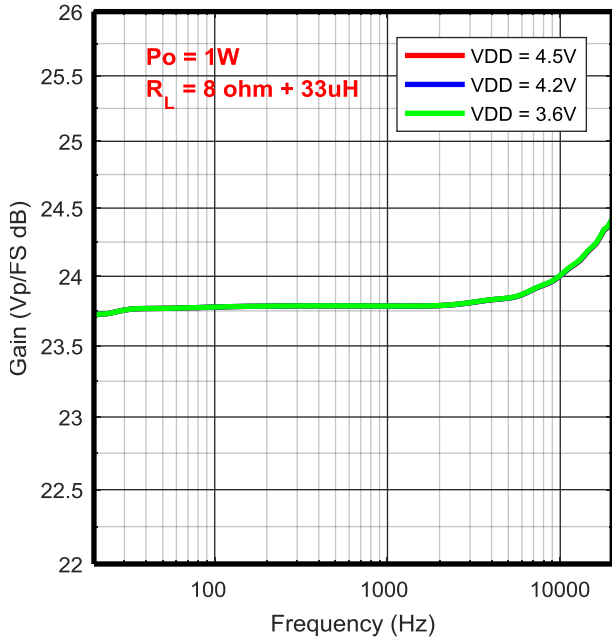### THD+N VS. FREQUENCY



### THD+N VS. FREQUENCY
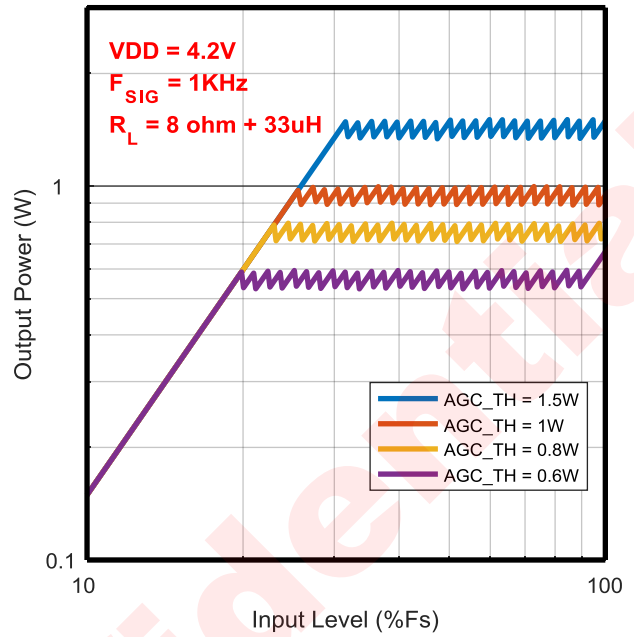


### THD+N VS. OUTPUT POWER
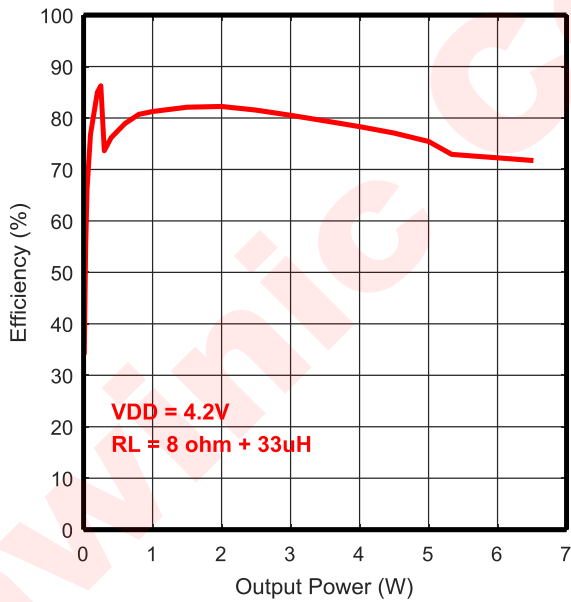


### THD+N VS. OUTPUT POWER
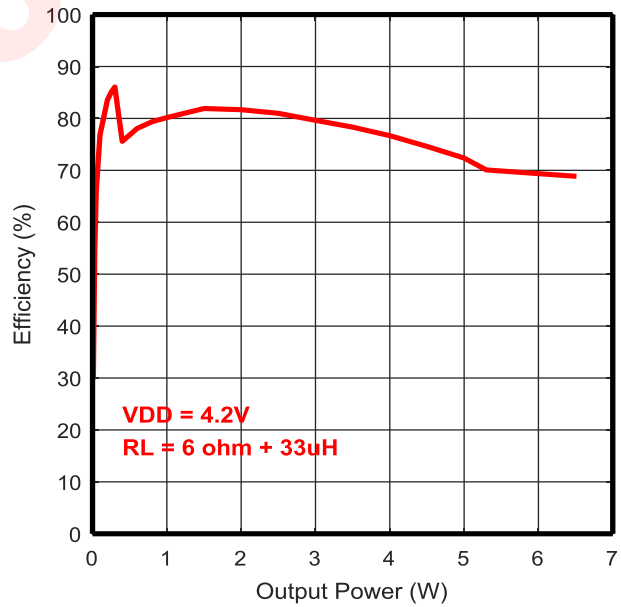
## GAIN VS. FREQUENCY
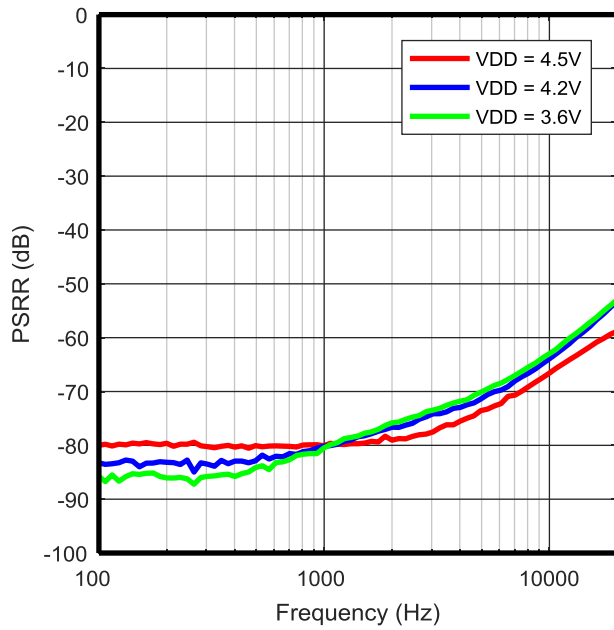


## OUTPUT POWER VS. Din



## EFFICIENCY VS. OUTPUT POWER



## EFFICIENCY VS. OUTPUT POWER

### RECEIVER PSRR VS. FREQUENCY

# DETAIL FUNCTIONAL DESCRIPTION

## POWER ON RESET

The device provides a power-on reset feature that is controlled by VDD and DVDD supply voltage. When the VDD supply voltage raises from 0V to 2.1V, or DVDD supply voltage raises from 0V to 1.1V. The reset signal will be generated to perform a power-on reset operation, which will reset all circuits and configuration registers.

## OPERATION MODE

The device supports 4 operation modes.

**Table 1   Operating Mode**

| Mode | Condition | Description |
|---|---|---|
| **Power-Down** | $V_{DD}$ < 2.1V<br><br>$V_{DVDD}$ < 1.1V | Power supply is not ready, chipset is power down. |
| **Stand-By** | $V_{DD}$ > 3V<br><br>$V_{DVDD}$ > 1.65V | Power supply is ready, most parts of the device are power down for low power consumption except I²C interface |
| **Configuring** | PWDN = 0 | Device is biased while boost and class-D output is floating.<br><br>System configuration carried out in this mode |
| **Operating** | AMPPD = 0 | Amplifier is fully operating |
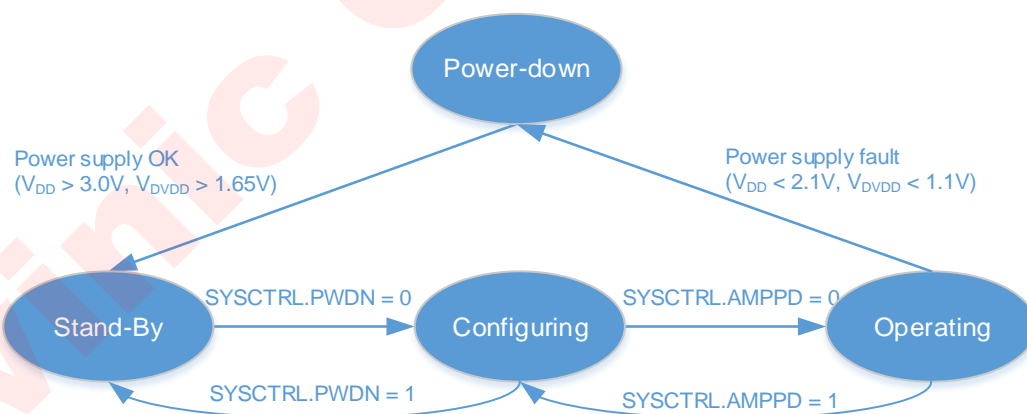


**Figure 7   Device operating modes transition**

### *POWER-DOWN MODE*

The device switches to power-down mode when any of the following events occurred:

■   $V_{DVDD}$ < 1.1 V

■ $V_{DD}$ < 2.1 V
■ RSTN pin goes LOW

In this mode, all circuits inside this device will be shut down except the power-on-reset circuit. I²C interface isn't accessible in this mode, and all of the internal configurable registers are cleared.

The device will jump out of the power-down mode automatically when all of the supply voltages are OK:

$V_{DVDD}$ > 1.65 V and $V_{DD}$ > 3 V

And RSTN goes HIGH.

### *STAND-BY MODE*

The device switches stand-by mode when the power supply voltages are OK and RSTN pin is HIGH. In this mode I²C interface is accessible, other modules are still powered down. Customer can set device to mode when the device is no needed to work.

### *CONFIG MODE*

The device switches to OFF mode when:
■ SYSCTRL.PWDN = 0;
■ SYSCTRL.AMPPD = 1;

In this mode the internal bias, OSC, PLL will start to work

### *OPERATING MODE*

The device is fully operational in this mode. Boost, amplifier loop and power stage circuits will start to work. Customer can set SYSCTRL.AMPPD = 0 to make device in this mode.Power Up Sequence

This device power up sequence is illustrated in the following figure:
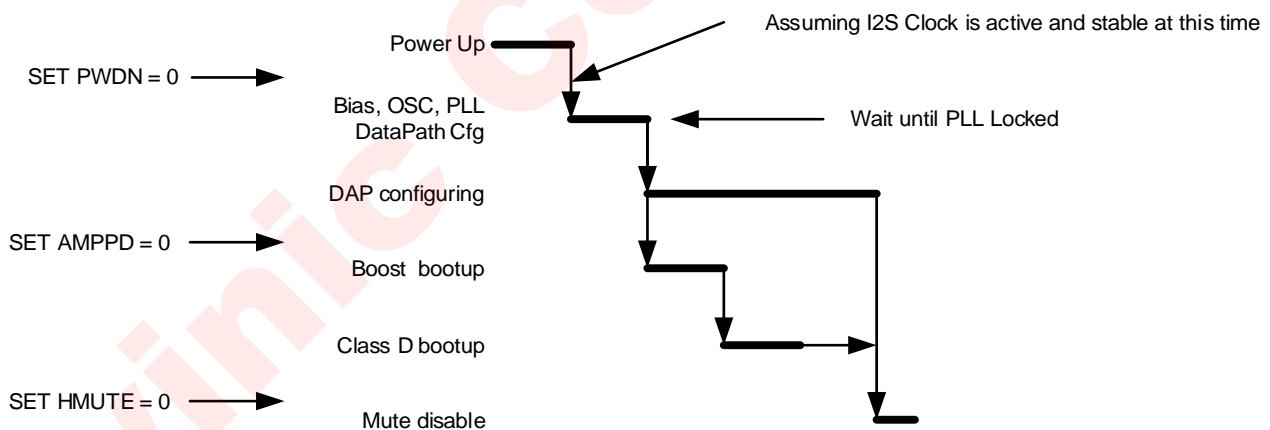


**Figure 8  Power up sequence**

Detail description for each step is listed in the following table.

**Table 2　Detail Description of Power up sequence**

| Index | description | Mode |
|---|---|---|
| 1 | Wait for VDD、DVDD supply power up | Power-Down |
| 2 | I²S + Data Path Configuration | Stand-By |
| 3.1 | Enable system (SYSCTRL.PWDN = 0) | Configuring |
| 3.2 | Bias, OSC, PLL active | |
| 3.3 | Waiting for PLL locked | |
| 4.1 | Enable Boost and amplifier (SYSCTRL.AMPPD =0) Boost and Amplifier boot up | Operating |
| 4.2 | wait SYSST.SWS =1 | |
| 5 | Release Hard-Mute Data Path active | |

Power up sequence considering I2S, I2C timing shows as below:
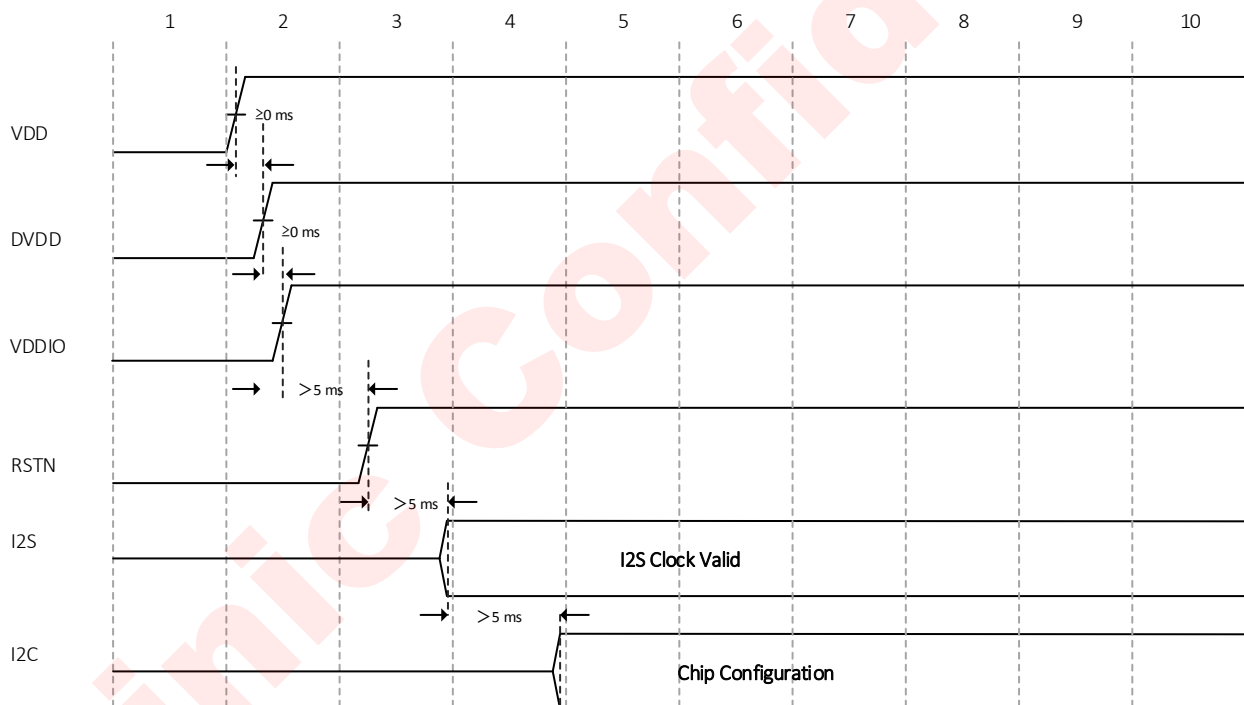


Power down sequence considering I2S, I2C timing shows as below:
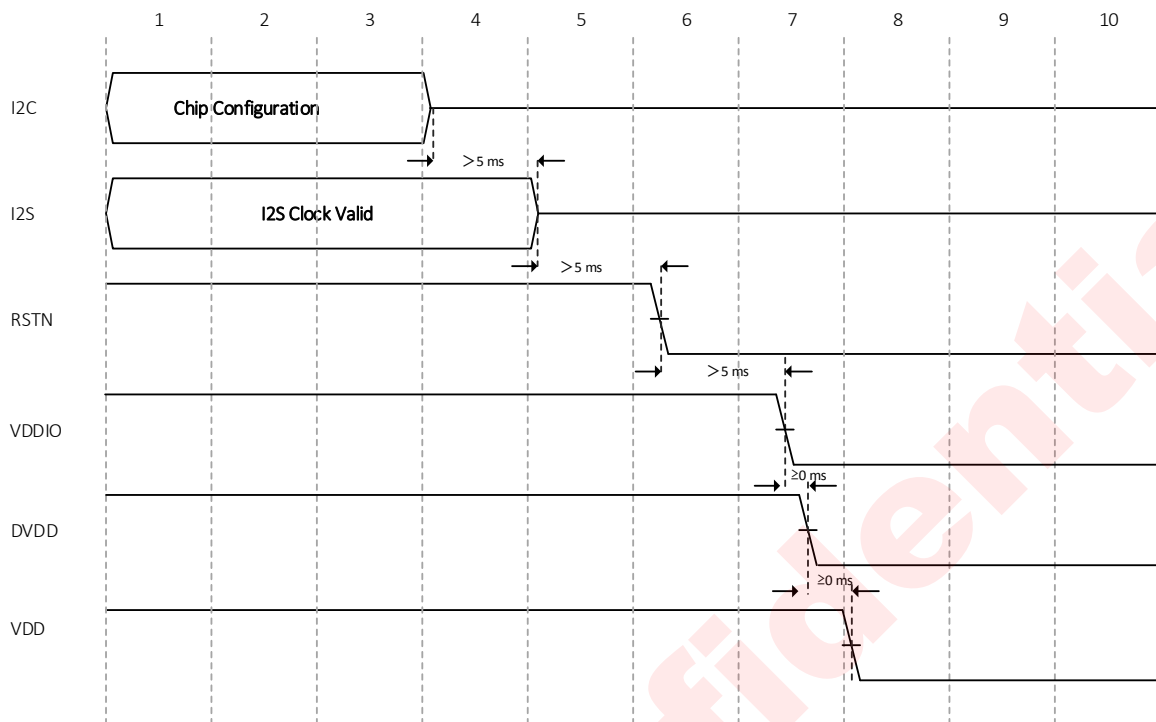
## SOFTWARE RESET

Writing 0x55AA to register ID (0x00) via I$^2$C interface will reset the device internal circuits and all configuration registers.

## DIGITAL AUDIO INTERFACE

Audio data is transferred between the host processor and the device via the Digital Audio Interface. The digital audio interface is in full-duplex via 4 dedicated pins:

- BCK
- WCK
- DATAI
- DATAO

Two-slot I$^2$S and 4-slot TDM are supported in this device. The digital audio Interface on this device is slave only and flexible with data width options, including 16, 20, 24, or 32 bits by configurable registers.

Three modes of I$^2$S are supported, including standard I$^2$S mode, left-justified mode and right-justified data mode, which can be configured via I2SCTRL.I2SMD. These modes are all MSB-first, with data width programmable via I2SCTRL.I2SFS.

The word clock WCK is used to define the beginning of a frame. The frequency of this clock corresponds to the sampling frequency. The device supports the following sample rates (fs): 8 kHz, 11.025 kHz, 12 kHz, 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, 48 kHz and 96 kHz. It is selected via configurable register I2SCTRL.I2SSR.

The bit clock BCK is used to sample the digital audio data across the digital audio interface. The number of bit-clock pulses in a frame is defined as slot length. Three kind of slot length are supported (16/24/32) via configurable register I2SCTRL.I2SBCK. The frequency of BCK can be calculated according to the following equation:

*BCK frequency = SampleRate * SlotLength * SlotNumber*

SampleRate: Sample rate for this digital audio interface;

SlotLength: The length of one audio slot in unit of BCK clock;

SlotNumber: How many slots supported in this audio interface. For example: 2-slot supported in I2S mode, 4-slot supported in TDM mode.

The word select and bit clock signals of the I$^2$S input are the reference signals for the digital audio interface and Phased Locked Loop (PLL).

The input audio data can be attenuated -6dB in this module, by setting bit I2SCTRL.INPLEV. The audio source can be from left channel, right channel or the average of the left and right channel, which is controlled by I2SCTRL.CHSEL.

**Table 3  Supported I2S interface parameters**

| Interface format(MSB first) | Data width | BCK frequency |
|---|---|---|
| Standard I$^2$S | 16b | 32fs/48fs /64fs |
| | 20b/24b/32b | 48fs /64fs |
| left-justified | 16b | 32fs/48fs /64fs |
| | 20b/24b/32b | 48fs /64fs |
| right-justified | 16b | 32fs /48fs /64fs |
| | 20b/24b/32b | 48fs /64fs |

The output port DATAO, can be enabled or disabled via bit I2SCFG1.I2STXEN. The unused slots can be set to Hi-z or zero, which is controlled by I2SCFG1.DOHZ.

### STANDARD I$^2$S MODE
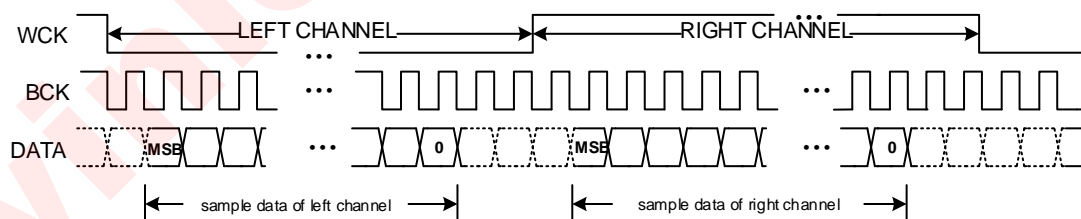


**Figure 9  I$^2$S Timing for Standard I$^2$S Mode**

● When WCK=0 indicating the left channel data, and WCK=1 indicating the right channel data.

● The MSB of the left channel is valid on the second rising edge of the bit clock after the falling edge of the word clock. Similarly the MSB of the right channel is valid on the second rising edge of the bit clock after the rising edge of the word clock.

*LEFT-JUSTIFIED MODE*
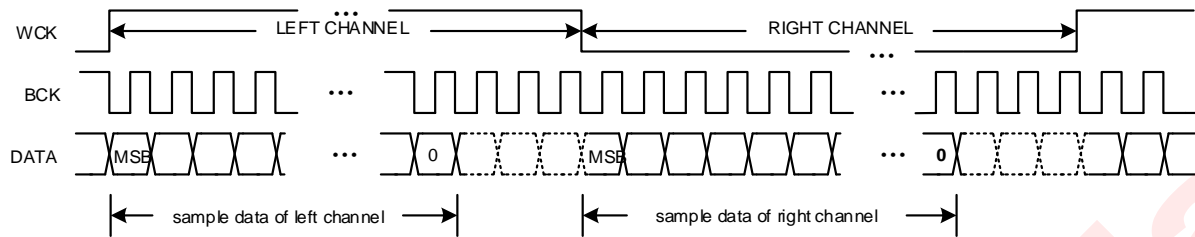


**Figure 10    I²S Timing for Left-Justified Mode**

● When WCK=1 indicating the left channel data, and WCK=0 indicating the right channel data.

● The MSB of the left channel is valid on the first rising edge of the bit clock after the rising edge of the word clock. Similarly the MSB of the right channel is valid on the first rising edge of the bit clock after the falling edge of the word clock.

*RIGHT-JUSTIFIED MODE*
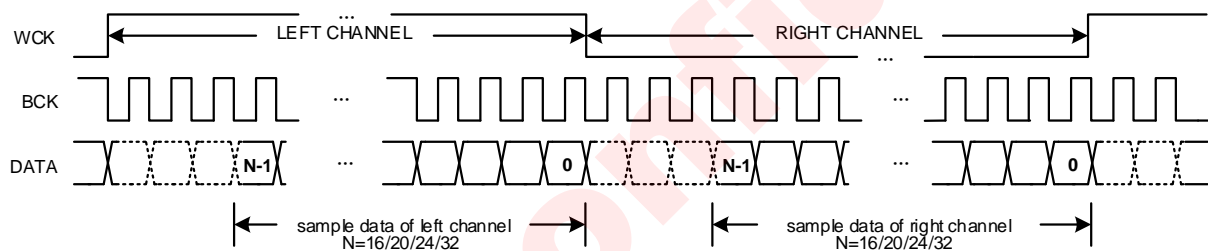


**Figure 11  I²S Timing for Right-Justified Mode**

● When WCK is high indicating the left channel data, and WCK=0 indicating the right channel data.

● The LSB (bit 0) of the left channel is valid on the rising edge of the bit clock preceding the falling edge of the word clock. Similarly, the LSB (bit 0) of the right channel is valid on the rising edge of the bit clock preceding the rising edge of the word clock.

*TDM MODE*

All of the three kind of bit synchronization modes (standard, left-justified, right-justified) are also supported in TDM mode. The difference between TDM and I²S is the slot number supported. 4-slot is supported in TDM mode, while 2-slot is supported in I²S mode
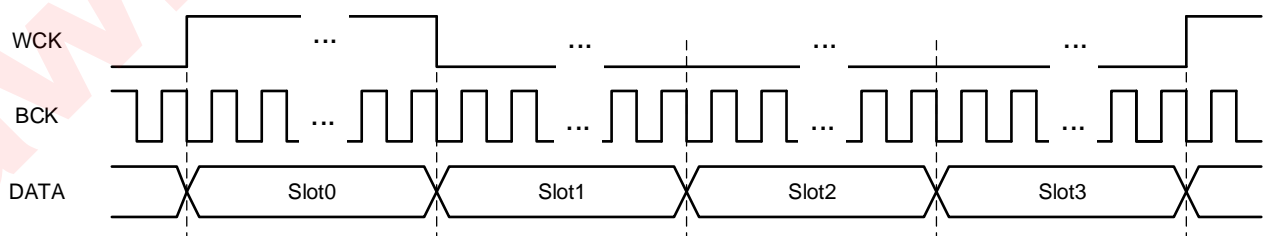


**Figure 12  TDM Timing**

Note: The high level pulse width of WCK signal can be one slot time or one period of BCK.

## DIGITAL AUDIO PROCESSING

This device provides algorithm supporting for audio signal processing. The following functions are processed in this module.

- DCC
- Hardware AGC
- Volume control
- Mute

The signal processing flow in the DAP(Digital Audio Processor) is illustrated in the following figure.
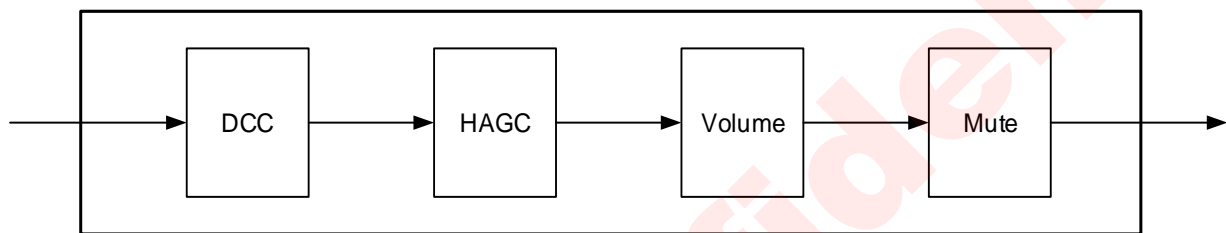


**Figure 13    Block Diagram of DAP**

### *DCC*

This module performs DC canceling for the input audio stream. It blocks DC components into analog class D loop.

### *HAGC*

In the actual audio application, system output power tends to be more than rated power of speaker, such as in the 10.25V power supply, as for 8ohms speaker, the maximum undistorted power is about 5.3W, but many speakers' rated power is about 1W, if there is no output power control, the overload signal can cause damage to the speaker. The audio power amplifier with HAGC can protect the speaker effectively, When the output power is not exceeds the setting threshold, the HAGC module will not attenuate the internal gain. Once the output power exceeds the setting threshold, the HAGC module will reduce the internal gain of amplifier and restricts the output power under the setting threshold.

### *VOLUME CONTROL*

The volume control function attenuates the audio signal at the end of digital audio processing. The range of volume setting is from 0db to -96db with 0.5db/step

### *MUTE*

This module perform mute control for the audio stream

## SKTUNE ALOGRITHM

This device provides algorithm supporting for audio signal processing. The following functions are processed in this module.

- Parametric Audio Path Equalizer(EQ)

- Multi-Band Dynamic Range Compressor (MBDRC)

- Programmable Power Control (PPC)

- Anti-clip Voltage Limiter

The signal processing flow in the DAP(Digital Audio Processor) is illustrated in the following figure:
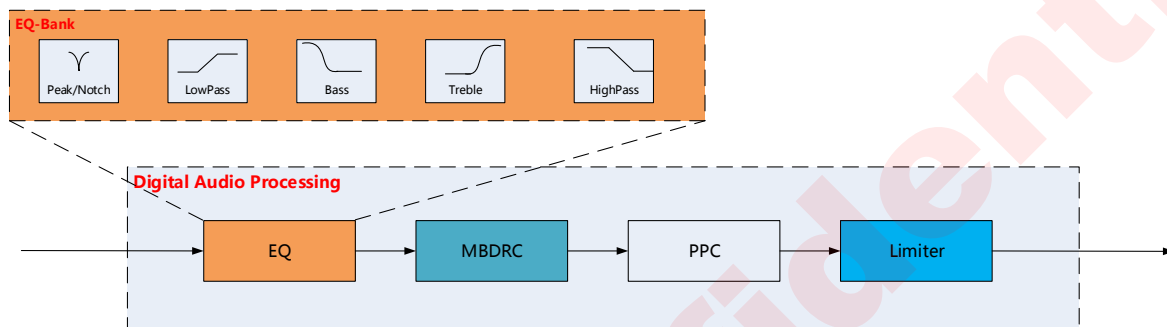


### *PARAMETRIC AUDIO PATH EQUALIZER*

Eight Parametric Audio Path Equalizers(EQ) are available and each of the equalizer can be fully programmable. It's possible to be implemented as any type of filter (high-pass, low-pass, peak, notch, bass, treble etc.) with different design methodologies to achieve the required frequency response.

### *MUTI-BAND DYNAMIC RANGE CONTROL*

A highly configurable and scalable DRC is available to improve audio performance. A block diagram of the DRC is illustrated in the following figure:
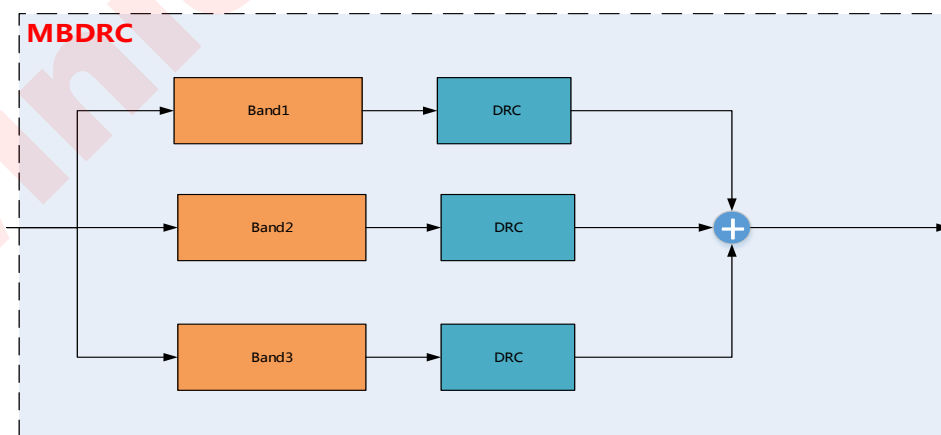


The audio input can be processed as a cascade of individually configurable band-limited DRCs. Three sub-bands DRC are supported.

*PROGRAMMABLE POWER CONTROL*

The power of output signal will be attenuated and limited below the programmable threshold in given attack time, when the amplitude of input signal is above the threshold.

While the attenuation will be released in given release time when the amplitude of input signal is below the threshold.

*ANTI-CLIP VOLTAGE LIMITER*

The anti-clip voltage limiter is used to protect the output from exceeding the amplifier clip level. When signal is over the amplifier clip level it will be attenuated automatically and limited below the threshold without clipping.

# DC-DC CONVERTER

This device using smart boost converter generates the amplifier supply rail, working in 1.6MHz. The DC-DC converter can work in different mode via BSTCTRL2.BST_MODE:

● **Pass-through mode**: the voltage of VDD is transparently passed to output of converter PVDD

● **Force boost mode**: the output voltage is boosted to the programmed output voltage

● **Smart boost 1 mode**: the output voltage can be switch between VDD and programmed output voltage according to the input audio level.

● **Smart boost 2 mode**: the output voltage can be dynamically adjusted according to the amplifier output's signal swing requirements in order to maximize efficiency.

**Pass-through mode**

The internal boost circuit is not working; the voltage of VDD is passed to PVDD directly.

**Force boost mode**

The boost circuit is always working and converts the voltage of VDD to the programmed output voltage. The output voltage is configured via BSTCTRL3.BSTVOUT

**Smart boost 1 mode**

Smart boost 1 mode can dynamically turn off the boost according to the amplifier output's signal swing requirements in order to maximize efficiency.

**Smart boost 2 mode**

The boost circuits working dynamically according to the input audio level. When the level of input audio signal is below the setting threshold, the boost circuit will be deactivated. Till the level of input audio signal raised up and above the threshold, the boost circuit starts to work and boost the amplifier supply rail to the voltage fit the requirement of output signal before the audio stream arriving at amplifier power stage.
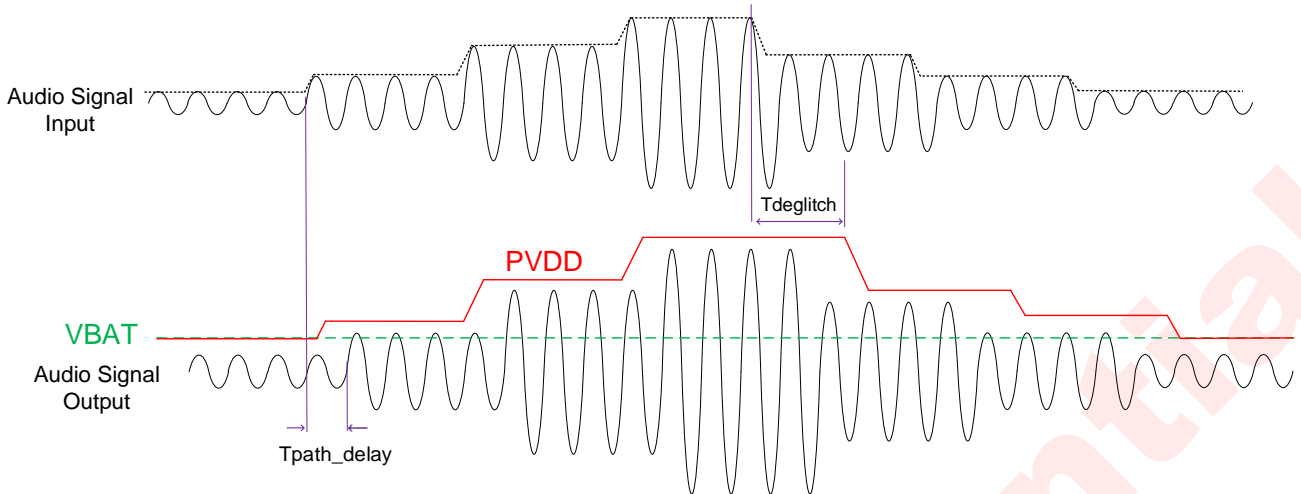
**Figure 14 Boost Circuit Behavior in Smart Boost 2 Mode**

## PROTECTION MECHANISMS

### Over Voltage Protection (OVP)

The boost circuit has integrated the over voltage protection control loop. When the output voltage PVDD is above the threshold, the boost circuits will stop working, until the voltage of PVDD going down and under the normal fixed working voltage.

### Over Temperature Protection (OTP)

The device has automatic temperature protection mechanism which prevents heat damage to the chip. It is triggered when the junction temperature is larger than the preset temperature high threshold (default = 160°C). When it happens, the output stages will be disabled. When the junction temperature drops below the preset temperature low threshold (less than 130°C), the output stages will start to operate normally again

### Over Current (short) Protection (OCP)

The short circuit protection function is triggered when VOP/VON is short to PVDD/GND or VOP is short to VON, the output stages will be shut down to prevent damage to itself. When the fault condition is disappeared, the output stages of device will restart.

### Under Voltage Detection (UVL)

The interrupt bit SYSINT.UVLI will be set to 1 when under voltage occurs, which will be cleared by a read operation of SYSINT register. Usually the SYSINT.UVLI bit can be used to check whether an unexpected under-voltage event has taken place.

## BATTERY VOLTAGE MONITORING

The device monitors the voltage on the VDD pin, which is most commonly the battery for the system. The battery voltage level is available via bits VBAT_DET in the Battery Supply Voltage register VBAT. Status bits BAT_DET can be used to calculate the battery voltage. The battery voltage level $V_{BAT}$ is:

$$V_{BAT} = \frac{VBAT\_DET}{2^{10} - 1} \times 6.025V$$

For example, if VBAT_DET = 101010011, the battery voltage level $V_{BAT}$ is equal to 3.6V.

## DIE TEMPERATURE MONITORING

The device monitors the die temperature and the result is available via bits TEMP_DET in the Temperature register TEMP. The TEMP_DET is a two's complement value. For example, if TEMP_DET = 00011001, the die temperature is 25℃.

## AMPLIFIER TRANSFER FUNCTION

The transfer function from the input to the amplifier PWM output (when no gain and attenuation is applied in digital signal domain) is:

$$V_o = AMP\_NORM\_V \times D_{in}$$

$D_{in}$: the level of input signal with a range from -1 to +1
AMP_NORM_V: the equivalent amplifier output voltage when $D_{in}$ is 1. In receiver mode the AMP_NORM_V is 5V, in speaker mode it's 16V.

## RECEIVER MODE

The device built-in Receiver mode is easy to realize the Speaker and Receiver combo applications, it saves the system cost and board space. If the receiver magnification is one times, the noise floor will be 12μV. Speaker and Receiver combo applications can be realized without changing any hardware.

When the device is set to receiver mode, the power supply of Class D driver stage is from VDD directly without boost.

# I²C INTERFACE

This device supports the I²C serial bus and data transmission protocol in fast mode at 400 kHz. This device operates as a slave on the I²C bus. Connections to the bus are made via the open-drain I/O pins SCL and SDA. The pull-up resistor can be selected in the range of 1k~10kΩ and the typical value is 4.7kΩ. This device can support different high level (1.8V~3.3V) of this I²C interface.

## *DEVICE ADDRESS*

The I²C device address (7-bit) can be set using the AD pin according to the following table: The AD1, AD2 pin configures the two LSB bits of the following 7-bit binary address A6-A0 of 01101xx. The permitted I²C addresses are 0x34(7-bit) through 0x37(7-bit).

**Table 4   Address Selection**

| AD2 | AD1 | Address(7-bit) |
|-----|-----|----------------|
| 0   | 0   | 0x34           |
| 0   | 1   | 0x35           |
| 1   | 0   | 0x36           |
| 1   | 1   | 0x37           |

## *DATA VALIDATION*

When SCL is high level, SDA level must be constant. SDA can be changed only when SCL is low level.
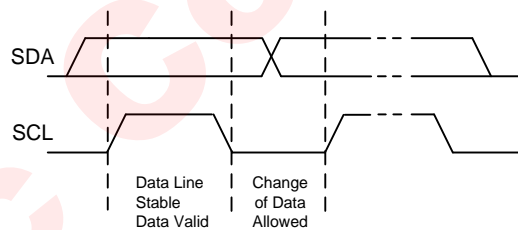


**Figure 15   Data Validation Diagram**

## *I²C START/STOP*

I²C start: SDA changes form high level to low level when SCL is high level.

I²C stop: SDA changes form low level to high level when SCL is high level.

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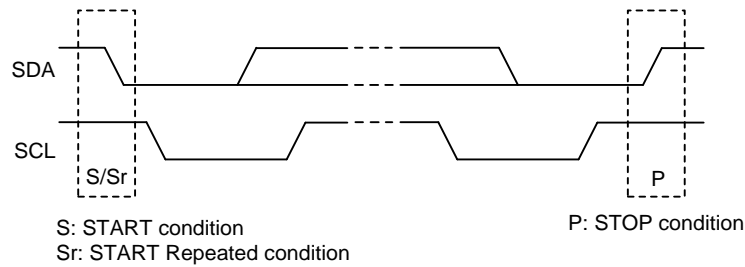
**Figure 16    I²C Start/Stop Condition Timing**

### ACK (ACKNOWLEDGEMENT)

ACK means the successful transfer of I²C bus data. After master sends 8bits data, SDA must be released; SDA is pulled to GND by slave device when slave acknowledges.

When master reads, slave device sends 8bit data, releases the SDA and waits for ACK from master. If ACK is send and I²C stop is not send by master, slave device sends the next data. If ACK is not send by master, slave device stops to send data and waits for I²C stop.
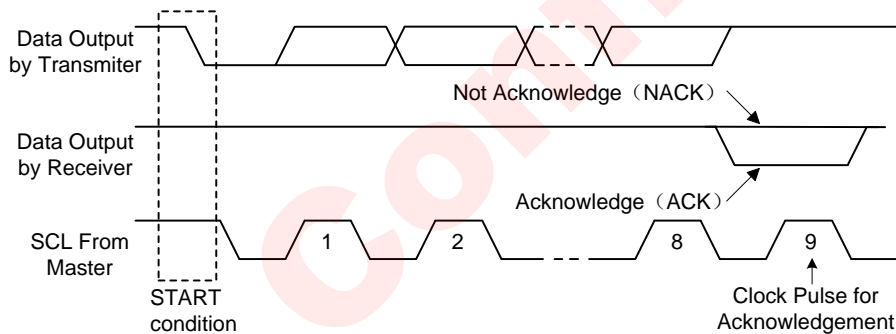


**Figure 17    I²C ACK Timing**

### WRITE CYCLE

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol allows a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a Start Condition, a number of byte transfers (set by the software) and a Stop Condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow.

In a write process, the following steps should be followed:

a)  Master device generates START condition. The "START" signal is generated by lowering the SDA signal while the SCL signal is high.

b)  Master device sends slave address (7-bit) and the data direction bit (r/w = 0).

c)  Slave device sends acknowledge signal if the slave address is correct.

d)  Master sends control register address (8-bit)

e)  Slave sends acknowledge signal

f)  Master sends high data byte of 16-bit data to be written to the addressed register

g)  Slave sends acknowledge signal

h)  Master sends low data byte of 16-bit data to be written to the addressed register

i)  Slave sends acknowledge signal

j)  If master will send further 16-bit data bytes the control register address will be incremented by one after acknowledge signal of step g (repeat step f to g)

k)  Master generates STOP condition to indicate write cycle end
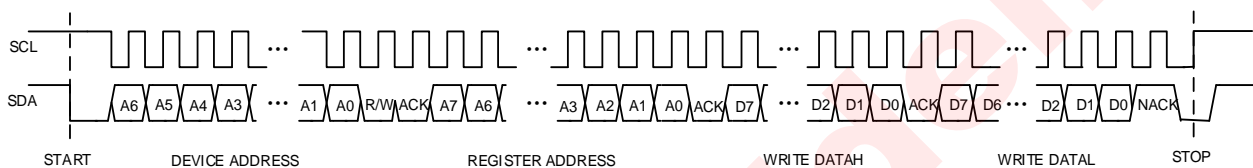


**Figure 18   I$^2$C Write Byte Cycle**

*READ CYCLE*

In a read cycle, the following steps should be followed:

a)  Master device generates START condition

b)  Master device sends slave address (7-bit) and the data direction bit (r/w = 0).

c)  Slave device sends acknowledge signal if the slave address is correct.

d)  Master sends control register address (8-bit)

e)  Slave sends acknowledge signal

f)  Master generates STOP condition followed with START condition or REPEAT START condition

g)  Master device sends slave address (7-bit) and the data direction bit (r/w = 1).

h)  Slave device sends acknowledge signal if the slave address is correct.

i)  Slave sends read high data byte of 16-bit data from addressed register.

j)  Master sends acknowledge signal.

k)  Slave sends read low data byte of 16-bit data from addressed register.

l)  If the master device sends acknowledge signal, the slave device will increase the control register address by one, then send the next 16-bit data from the new addressed register.

m)  If the master device generates STOP condition, the read cycle is ended.
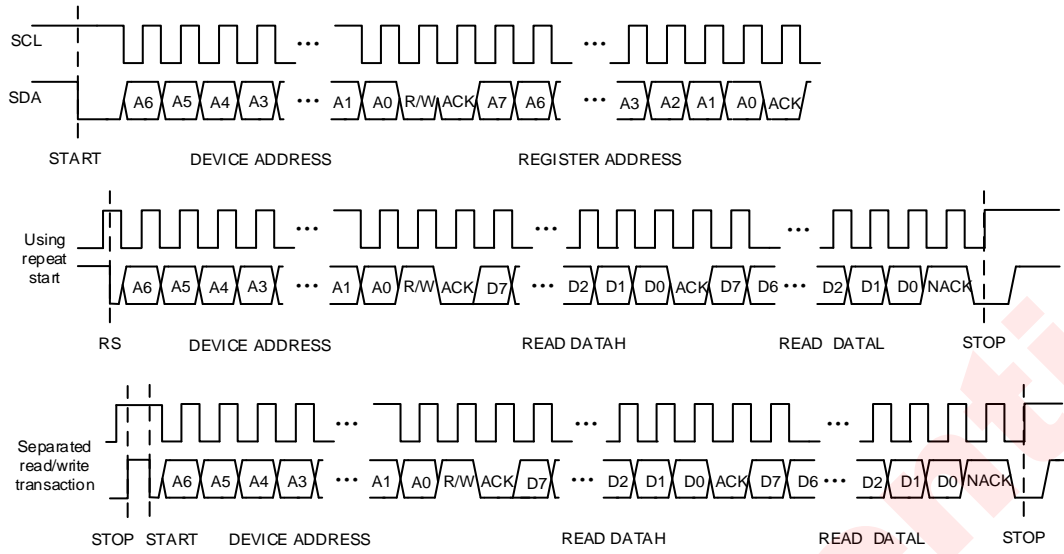
**Figure 19   I²C Read Byte Cycle**

# REGISTER MAP

## REGISTER DESCRIPTION

### REGISTER LIST

| ADDR | NAME | BIT | | | | | | | | | | | | | | | |
|------|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0x00 | ID | IDCODE | | | | | | | | | | | | | | | |
| 0x01 | SYSST | | UVLS | ADPS | DSPS | BSTOCS | OVPS | BSTS | SWS | CLIPS | WDS | NOCLKS | CLKS | OCDS | CLIP_PRES | OTHS | PLLS |
| 0x02 | SYSINT | | UVLI | ADPI | DSPI | BSTOCI | OVPI | BSTI | SWI | CLIPI | WDI | NOCLKI | CLKI | OCDI | CLIP_PREI | OTHI | PLLI |
| 0x03 | SYSINTM | | UVLM | ADPM | DSPM | BSTOCM | OVPM | BSTM | SWM | CLIPM | WDM | NOCLKM | CLKM | OCDM | CLIP_PREM | OTHM | PLLM |
| 0x04 | SYSCTRL | | SPK_GAIN | | | RCV_GAIN | | INTMODE | | RCV_MODE | I2SEN | WSINV | BCKINV | IPLL | DSPBY | AMPPD | PWDN |
| 0x05 | I2SCTRL | | | INPLEV | | CHSEL | | I2SMD | | I2SFS | | I2SBCK | | I2SSR | | | |
| 0x06 | I2SCFG1 | SYNC_TYPE | SLOT_NUM | I2S_TX_SLOTVLD | | I2S_RX_SLOTVLD | | | | CFSEL | | DRVSTREN | DOHZ | | | I2SCHS | I2STXEN |
| 0x08 | PWMCTRL | | | | | | | | | | | | | | | HDCCE | HMUTE |
| 0x09 | HAGCCFG1 | RVTH | | | | | | | | AVTH | | | | | | | |
| 0x0a | HAGCCFG2 | ATTH | | | | | | | | | | | | | | | |
| 0x0b | HAGCCFG3 | RTTH | | | | | | | | | | | | | | | |
| 0x0c | HAGCCFG4 | | | | | | | | HOLDTH | | | | | | | | |
| 0x0d | HAGCCFG5 | | | | | HAGCE | | | | | | | | | | | |
| 0x0f | HAGCCFG6 | VOL | | | | | | | | | | | | | | | |
| 0x10 | HAGCCFG7 | | | | | | | | | | | | BSTVOUT_ST | | | | |
| 0x11 | SYSCTRL2 | | | | | | | | | | | | | BST_IPEAK | | | |
| 0x21 | I2SCFG2 | | | | | | | | | | | | | | | | I2SRXEN |
| 0x60 | BSTCTRL1 | BST_RTH | | | | | | | | BST_ATH | | | | | | | |
| 0x61 | BSTCTRL2 | | | | | | | | BST_MODE | | | | BST_TDEG | | | | |
| 0x62 | BSTCTRL3 | | | | | | | | | | BST_VOUT | | | | | | |
| 0x6d | VBAT | | | | | | | VBAT_DET | | | | | | | | | |
| 0x6e | TEMP | | | | | | | TEMP_DET | | | | | | | | | |

*DETAILED REGISTER DESCRIPTION*

**ID: Chip ID Register (Address 00h)**

| Bit | Symbol | R/W | Description | Default |
|---|---|---|---|---|
| 15:0 | IDCODE | R | Chip ID (1806h) will be returned after read. All configuration registers will be reset to default value after 0x55aa is written to this address | 0x1806 |

**SYSST: System Status Register (Address 01h)**

| Bit | Symbol | R/W | Description | Default |
|---|---|---|---|---|
| 15 | Reserved | - | Reserved | |
| 14 | UVLS | R | VDD under voltage indicator 1: VDD < 2.6V, 0: VDD > 2.7V | |
| 13 | ADPS | R | Smart Boost status. 0:transparent; 1: boost | |
| 12 | DSPS | R | Set when DSP acknowledge request flag is set | |
| 11 | BSTOCS | R | Boost over current indicator | |
| 10 | OVPS | R | Boost OVP status indicator | |
| 9 | BSTS | R | Boost start up finished. 1: finished; 0: not finished | |
| 8 | SWS | R | Amplifier switching status. 1: switching; 0: not switching | |
| 7 | CLIPS | R | Amplifier clipping status. 1: clipping; 0: not clipping | |
| 6 | WDS | R | DSP watchdog is triggered, device will be restarted | |
| 5 | NOCLKS | R | The reference clock of PLL is not available | |
| 4 | CLKS | R | All internal clocks are stable | |
| 3 | OCDS | R | Over current status in amplifier | |
| 2 | CLIP_PRES | R | Ampifier clipping pre status. | |
| 1 | OTHS | R | Die Temperature is higher than 160℃ | |
| 0 | PLLS | R | PLL locked status. 1: locked; 0: unlocked | |

**SYSINT: System Interrupt Register (Address 02h)**

| Bit | Symbol | R/W | Description | Default |
|---|---|---|---|---|
| 15 | Reserved | - | Reserved | |
| 14 | UVLI | RC | Interrupt indicator for Power On and UVLS | |
| 13 | ADPI | RC | Interrupt indicator for ADPS | |
| 12 | DSPI | RC | Interrupt indicator for DSPS. | |
| 11 | BSTOCI | RC | Interrupt indicator for BSTOCS. | |
| 10 | OVPI | RC | Interrupt indicator for OVPS. | |
| 9 | BSTI | RC | Interrupt indicator for BSTS. | |
| 8 | SWI | RC | Interrupt indicator for SWS. | |
| 7 | CLIPI | RC | Interrupt indicator for CLIPS. | |
| 6 | WDI | RC | Interrupt indicator for WDS | |
| 5 | NOCLKI | RC | Interrupt indicator for NOCLKS. | |
| 4 | CLKI | RC | Interrupt indicator for CLKS. | |
| 3 | OCDI | RC | Interrupt indicator for OCDS | |
| 2 | CLIP_PREI | RC | Interrupt indicator for CLIP_PRES | |
| 1 | OTHI | RC | Interrupt indicator for OTHS. | |
| 0 | PLLI | RC | Interrupt indicator for PLLS. | |
| Note: It will be set to '1' once corresponding interrupt bit changed | | | | |

**SYSINTM: System Interrupt mask Register (Address 03h)**

| Bit | Symbol | R/W | Description | Default |
|-----|--------|-----|-------------|---------|
| 15 | Reserved | - | Reserved | 0x1 |
| 14 | UVLM | RW | Interrupt mask for UVLI. | 0x1 |
| 13 | ADPM | RW | Interrupt mask for ADPI. | 0x1 |
| 12 | DSPM | RW | Interrupt mask for DSPI. | 0x1 |
| 11 | BSTOCM | RW | Interrupt mask for BSTOCI. | 0x1 |
| 10 | OVPM | RW | Interrupt mask for OVPI. | 0x1 |
| 9 | BSTM | RW | Interrupt mask for BSTI. | 0x1 |
| 8 | SWM | RW | Interrupt mask for SWI. | 0x1 |
| 7 | CLIPM | RW | Interrupt mask for CLIPI. | 0x1 |
| 6 | WDM | RW | Interrupt mask for WDI. | 0x1 |
| 5 | NOCLKM | RW | Interrupt mask for NOCLKI. | 0x1 |
| 4 | CLKM | RW | Interrupt mask for CLKI. | 0x1 |
| 3 | OCDM | RW | Interrupt mask for OCDI. | 0x1 |
| 2 | CLIP_PREM | RW | Interrupt mask for CLIP_PREI. | 0x1 |
| 1 | OTHM | RW | Interrupt mask for OTHI. | 0x1 |
| 0 | PLLM | RW | Interrupt mask for PLLI. | 0x1 |
| Note: | Corresponding interrupt will be masked when the mask bit is set to '1' | | | |

**SYSCTRL: System Control Register (Address 04h)**

| Bit | Symbol | R/W | Description | Default |
|-----|--------|-----|-------------|---------|
| 15 | Reserved | - | Reserved | |
| 14:12 | SPK_GAIN | RW | Speaker mode AMP_NORM_V configuration<br>0: AMP_NORM_V=7<br>1: AMP_NORM_V=8<br>2: AMP_NORM_V=10<br>3: AMP_NORM_V=12<br>4: AMP_NORM_V=14<br>6: AMP_NORM_V=16<br>Others: Reserved | 0x6 |
| 11:10 | RCV_GAIN | RW | Receiver mode AMP_NORM_V configuration<br>0: AMP_NORM_V=4.5<br>1: AMP_NORM_V=5<br>2: AMP_NORM_V=5.5<br>3: AMP_NORM_V=5.5 | 0x0 |
| 9:8 | INTMODE | RW | Interrupt mode<br>[0]: INTN pin source selection. 0: SYSINT; 1: SYSST<br>[1]: INTN output mode selection. 0: Open-drain, 1:push&pull | 0x0 |
| 7 | RCV_MODE | RW | Receiver mode<br>0: Speaker mode<br>1: Receiver mode | 0x0 |
| 6 | I2SEN | RW | Enable/Disable whole I2S interface module<br>0: disable<br>1: enable | 0x0 |
| 5 | WSINV | RW | I2S Left/Right channel switch<br>0: No switch<br>1: Left/Right switch | 0x0 |

| 4 | BCKINV | RW | I2S bit clock invert control<br>0: not invert<br>1: inverted | 0x0 |
|---|--------|----|----------------------------------------------------------------|-----|
| 3 | IPLL | RW | PLL reference clock selection<br>0: bit clock<br>1: word selection signal | 0x0 |
| 2 | Reserved | - | Reserved | 0x1 |
| 1 | AMPPD | RW | Amplifier power down control bit<br>0: Amplifier active<br>1: Amplifier power down | 0x1 |
| 0 | PWDN | RW | System power down control bit<br>0: Active<br>1: All circuits will enter power down mode | 0x1 |

**I2SCTRL: I2S interface Control Register (Address 05h)**

| Bit | Symbol | R/W | Description | Default |
|-----|--------|-----|-------------|---------|
| 15:14 | Reserved | - | Reserved | 0x0 |
| 13 | INPLEV | RW | Input level selection<br>0: All input signal will not be attenuated at first<br>1: All input signal will be attenuated by -6dB at first | 0x0 |
| 12 | Reserved | - | Reserved | 0x0 |
| 11:10 | CHSEL | RW | Left/right channel selection for I2S input<br>0: Reserved<br>1: Left<br>2: Right<br>3: Mono, (L+R)/2 | 0x1 |
| 9:8 | I2SMD | RW | I2S interface mode<br>0: Philip standard I2S (default)<br>1: MSB justified<br>2: LSB justified<br>3: Reserved | 0x0 |
| 7:6 | I2SFS | RW | I2S data width<br>0: 16 bits<br>1: 20 bits<br>2: 24 bits<br>3: 32 bits | 0x3 |
| 5:4 | I2SBCK | RW | I2S BCK mode<br>0: 32*fs(16*2)<br>1: 48*fs(24*2)<br>2: 64*fs(32*2)<br>3: Reserved | 0x2 |

| 3:0 | I2SSR | RW | I2S interface sample rate configuration<br>0: 8 kHz<br>1: 11.025 kHz<br>2: 12 kHz<br>3: 16 kHz<br>4: 22.05 kHz<br>5: 24 kHz<br>6: 32 kHz<br>7: 44.1 kHz<br>8: 48 kHz<br>9: 96 kHz<br>10~15: Reserved | 0x8 |

**I2SCFG1: I2S Configuration Register 1 (Address 06h)**

| Bit | Symbol | R/W | Description | Default |
|---|---|---|---|---|
| 15 | FSYNC_TYPE | RW | Audio Frame synchronization signal(WCK) pulse width configuration<br>0: one slot width<br>1: one BCK clock cycle | 0x0 |
| 14 | SLOT_NUM | RW | 0: 2 slots (Compatible with I2S)<br>1: 4 slots (TDM mode, max 4 slots support) | 0x0 |
| 13:12 | TX_SLOT_VLD | RW | TX slot select<br>0: Data send on slot 0<br>1: Data send on slot 1<br>2: Data send on slot 2<br>3: Data send on slot 3 | 0x3 |
| 11:8 | RX_SLOT_VLD | RW | RX slot select<br>3: RX slot 0,1<br>5: RX slot 0,2<br>6: RX slot 1,2<br>9: RX slot 0,3<br>10: RX slot 1,3<br>12: RX slot 2,3<br>Others: RX slot 0,1 | 0x3 |
| 7:6 | Reserved | - | Reserved | 0x0 |
| 5 | DRVSTREN | RW | DATAO driving strength setting<br>0: 2 mA<br>1: 8 mA | 0x0 |
| 4 | DOHZ | RW | Unused channel data mode<br>0: 0<br>1: Hi-Z | 0x0 |
| 3:1 | Reserved | - | Reserved | 0x0 |
| 0 | I2STXEN | RW | Enable/Disable I2S transmitter module<br>0: Disable<br>1: Enable | 0x0 |

## PWMCTRL: PWM Control Register (Address 08h)

| Bit | Symbol | R/W | Description | Default |
|---|---|---|---|---|
| 15:2 | Reserved | - | Reserved | 0x2803 |
| 1 | HDCCE | RW | Hardware DC Canceling control<br>0: Hardware DC cancel disable;<br>1: Hardware DC cancel enable. | 0x1 |
| 0 | HMUTE | RW | Hardware mute control<br>0: Hardware mute disable;<br>1: Hardware mute enable. | 0x1 |

## HAGCCFG1: Hardware AGC Configuration Register 1 (Address 09h)

| Bit | Symbol | R/W | Description | Default |
|---|---|---|---|---|
| 15:8 | RVTH | RW | Release Amplitude threshold, in percent of signal full scale | 0x39 |
| 7:0 | AVTH | RW | Attack Amplitude threshold, in percent of signal full scale | 0x40 |

## HAGCCFG2: Hardware AGC Configuration Register 2 (Address 0ah)

| Bit | Symbol | R/W | Description | Default |
|---|---|---|---|---|
| 15:0 | ATTH | RW | Attack time threshold in unit of 20.8µs<br>0: Reserved<br>n: Gain decreased 0.5db per n*20.8µs | 0x30 |

## HAGCCFG3: Hardware AGC Configuration Register 3 (Address 0bh)

| Bit | Symbol | R/W | Description | Default |
|---|---|---|---|---|
| 15:0 | RTTH | RW | Release time threshold in unit of 20.8µs<br>0: Reserved<br>n: Gain decreased 0.5db per n*20.8µs | 0x1E0 |

## HAGCCFG4: Hardware AGC Configuration Register 4 (Address 0ch)

| Bit | Symbol | R/W | Description | Default |
|---|---|---|---|---|
| 15:8 | Reserved | - | Reserved | 0x7A |
| 7:0 | HOLDTH | RW | Attack time threshold in unit of about 166µs<br>0: Reserved<br>n: Attack counter holding at least n*166µs | 0x64 |

## HAGCCFG5: Hardware AGC Configuration Register 5 (Address 0dh)

| Bit | Symbol | R/W | Description | Default |
|---|---|---|---|---|
| 15:9 | Reserved | - | Reserved | |
| 8 | HAGCE | RW | Hardware AGC enable<br>0: Disable<br>1: Enable | 0x0 |
| 7:0 | Reserved | - | Reserved | 0x1B |

**HAGCCFG6: Hardware AGC Configuration Register 6 (Address 0fh)**

| Bit | Symbol | R/W | Description | Default |
|------|--------|-----|-------------|---------|
| 15:8 | VOL | RW | Volume control, from 0 to -96dB<br>[3:0] : in unit of -0.5dB<br>[7:4] : in unit of -6dB | 0x0 |
| 7:0 | Reserved | - | Reserved | |

**HAGCCFG7: Hardware AGC Configuration Register 7 (Address 10h)**

| Bit | Symbol | R/W | Description | Default |
|------|--------|-----|-------------|---------|
| 15:4 | Reserved | - | Reserved | |
| 3:0 | BSTVOUT_ST | R | Actual setting of boost output voltage<br>0: 6.5 V<br>1: 6.75 V<br>2: 7 V<br>3: 7.25 V<br>4: 7.5 V<br>5: 7.75 V<br>6: 8 V<br>7: 8.25 V<br>8: 8.5 V<br>9: 8.75 V<br>10: 9 V<br>11: 9.25 V<br>12: 9.5 V<br>13: 9.75V<br>14: 10V<br>15: 10.25V | |

**SYSCTRL2: System Control Register 2 (Address 11h)**

| Bit | Symbol | R/W | Description | Default |
|------|--------|-----|-------------|---------|
| 15:3 | Reserved | - | Reserved | |
| 2:0 | BST_IPEAK | RW | Boost peak current limiter threshold<br>0: 2.5A<br>1: 2.75A<br>2: 3.0A<br>3: 3.25A<br>4: 3.5A<br>5: 3.75A<br>6: 4.0A<br>7: Reserved | 0x4 |

**I2SCFG2: I2S Configuration Register 2 (Address 21h)**

| Bit | Symbol | R/W | Description | Default |
|------|--------|-----|-------------|---------|
| 15:1 | Reserved | - | Reserved | 0x108 |
| 0 | I2SRXEN | RW | Enable/Disable I2S receiver module<br>0: Disable<br>1: Enable | 0x1 |

### BSTCTRL1: Boost Control Register 1 (Address 60h)

| Bit | Symbol | R/W | Description | Default |
|---|---|---|---|---|
| 15:14 | Reserved | - | Reserved | 0x0 |
| 13:8 | BST_RTH | RW | Smart boost release threshold setting. When signal is below the threshold, the voltage of VBST will not be raised up higher than VDD in smart boost mode Release threshold = BST_RTH * 1/64 FullScale | 0x4 |
| 7:6 | Reserved | - | Reserved | 0x0 |
| 5:0 | BST_ATH | RW | Smart boost attack threshold setting. When signal is above over the threshold, the voltage of VBST will be raised up higher than VDD in smart boost mode Attack threshold = BST_ATH * 1/64 FullScale | 0x2 |

### BSTCTRL2: Boost Control Register 2 (Address 61h)

| Bit | Symbol | R/W | Description | Default |
|---|---|---|---|---|
| 15:7 | Reserved | - | Reserved | 0x0 |
| 6:4 | BST_MODE | RW | BOOST mode selection<br>0: Transparent Mode<br>1: Force Boost Mode<br>5: Smart Boost 1 Mode<br>6: Smart Boost 2 Mode<br>Others: reserved | 0x2 |
| 3 | Reserved | - | Reserved | |
| 2:0 | BST_TDEG | RW | Smart Boost small signal level detection deglitch time<br>0: 1.33 ms<br>1: 2.66 ms<br>2: 5.32 ms<br>3: 21.30 ms<br>4: 85.20 ms<br>5: 340.79 ms<br>6: 1.363 s<br>7: 2.73 s | 0x6 |

### BSTCTRL3: Boost Control Register 3 (Address 62h)

| Bit | Symbol | R/W | Description | Default |
|---|---|---|---|---|
| 15:4 | Reserved | - | Reserved | 0x0 |
| 3:0 | BSTVOUT | RW | Boost max output voltage configuration<br>0: 6.5 V<br>1: 6.75 V<br>2: 7 V<br>3: 7.25 V<br>4: 7.5 V<br>5: 7.75 V<br>6: 8 V<br>7: 8.25 V<br>8: 8.5 V<br>9: 8.75 V<br>10: 9 V<br>11: 9.25 V<br>12: 9.5 V<br>13: 9.75V<br>14: 10V<br>15: 10.25V | 0x8 |

**VBAT: Battery Supply Voltage Register (Address 6dh)**

| Bit | Symbol | R/W | Description | Default |
|---|---|---|---|---|
| 15:10 | Reserved | - | Reserved | 0x0 |
| 9:0 | VBAT_DET | R | Detected voltage of battery, and the full range is 6.025V<br>$V_{BAT} = VBAT\_DET/1023 \times 6.025$ | 0x263 |

**TEMP: Temperature Register (Address 6eh)**

| Bit | Symbol | R/W | Description | Default |
|---|---|---|---|---|
| 15:10 | Reserved | - | Reserved | 0x0 |
| 9:0 | TEMP_DET | R | Detected die temperature (Two's Complement), typical values are as follows<br>0x3D8 : -40degree<br>…<br>0x00 : 0 degree<br>0x01 : 1 degree<br>…<br>0x19 : 25 degree<br>…<br>0x37 : 55 degree<br>… | 0x19 |

# APPLICATION INFORMATION

## EXTERNAL COMPONENTS

### *BOOST INDUCTOR SELECTION*

Selecting inductor needs to consider Inductance, size, magnetic shielding, saturation current and temperature current.

a) Inductance

Inductance value is limited by the boost converter's internal loop compensation. In order to ensure phase margin sufficient under all operating conditions, recommended 1µH inductor.

b) Size

For a certain value of inductor, the smaller the size, the greater the parasitic series resistance of the inductor DCR, the higher the loss, corresponds to the lower efficiency.

c) Magnetic shielding

Magnetic shielding can effectively prevent the inductance of the electromagnetic radiation interference. It is much better to choose inductance with magnetic shielding in the application of EMI sensitive environment.

d) Saturation current and temperature rise of current

Inductor saturation current and temperature rise current value are important basis for selecting the inductor. As the inductor current increases, on the one hand, since the magnetic core begins to saturate, inductance value will decline; on the other hand, the inductor's parasitic resistance inductance and magnetic core loss can lead to temperature rise. In general, the current value is defined as the saturation current $I_{SAT}$ when the inductance value drops to 70%; the current value is defined as temperature rise current $I_{RMS}$ when inductance temperature rise 40°C.

For particular applications, need to calculate the maximum $I_{L\_PEAK}$ and $I_{L\_RMS}$, which is a basis of selecting the inductor. When VDD = 4.2V, PVDD=9.5V, $R_L$ = 8Ω, amplifier $R_{DSON}$ = 350mΩ, when THD = 1% (the maximum power without distortion), the output power is calculated as follows:

$$P_{out} = \frac{\left(V_{out} \times \frac{R_L}{R_L + R_{DSON}}\right)^2}{2 \times R_L} = \frac{\left(9.5 \times \frac{8}{8 + 0.35}\right)^2}{2 \times 8} = 5.16W$$

In such a large output power, the overall efficiency of the power amplifier is typically 70%, in order to calculate the maximum average current $I_{MAX\_AVG\_VDD}$ and maximum peak current $I_{MAX\_PEAK\_VDD}$ drawn from VDD:

$$I_{MAX\_AVG\_VDD} = \frac{P_{out}}{V_{in} \times \eta} = \frac{5.16}{4.2 \times 0.7} = 1.75A$$

$$I_{MAX\_PEAK\_VDD} = 2 \times I_{MAX\_AVG\_VDD} = 2 \times 1.75A = 3.5A$$

If inductor DCR is 50mΩ, the inductor power loss at this time is:

$$P_{DCR\_LOSS} = 1.5 \times I_{MAX\_AVG\_VDD}^2 \times DCR = 1.5 \times 1.75^2 \times 0.05W = 230mW$$

Wherein the coefficient 1.5 is the square of the ratio of the sine wave current RMS value and average value (there is no consideration of the impact of the inductor ripple, the actual DCR loss will be even greater). If the loss which is resulting from DCR is less than 1% at maximum efficiency ($P_{OUT}$ = 2.5W, η = 80%), then:

$$I_{AVG\_VDD} = \frac{P_{out}}{V_{in} \times \eta} = \frac{2.5}{4.2 \times 0.8} = 0.75A$$

$$DCR = \frac{P_{DCR\_LOSS}}{1.5 \times I_{MAX\_AVG\_VDD}^2} \leq 1\% \times \frac{P_{out}}{1.5 \times I_{AVG\_VDD}^2 \times \eta} = \frac{0.01 \times 2.5}{1.5 \times 0.75^2 \times 0.8}\Omega = 37m\Omega$$

According to the working principle of the Boost, we can calculate the size of the inductor current ripple $\Delta_{IL}$:

$$\Delta I_L = \frac{V_{in} \times (V_{out} - V_{in})}{V_{out} \times f \times L} = \frac{4.2 \times (9.5 - 4.2)}{9.5 \times 1.6 \times 10^6 \times 1 \times 10^{-6}} = 1.46A$$

Thus, the maximum peak inductor current $I_{L\_PEAK}$ and maximum effective inductor current $I_{L\_RMS}$ is:

$$I_{L\_PEAK} = I_{MAX\_PEAK\_VDD} + \frac{\Delta I_L}{2} = 3.5 + \frac{1.46}{2}A = 4.23A$$

$$I_{L\_RMS} = \sqrt{I_{MAX\_PEAK\_VDD}^2 + \frac{\Delta I_L^2}{12}} = \sqrt{3.5^2 + \frac{1.46^2}{12}}A = 3.52A$$

From the above calculation results:
1) For typical DCR about 50mΩ inductance, the efficiency loss caused by around1.5%;
2) In practice, the maximum output power of the amplifier is likely to reach 5.6W in an instant, so the selected inductor saturation current $I_{SAT}$ requires more than the maximum inductor peak current $I_{L\_PEAK}$;
3) In some cases, if the $I_{L\_PEAK}$ calculated according to the above method is greater than the set of input inductor current limit value $I_{PEAK}$, shows the power amplifier is restricted by inductance input current limit, the actual maximum output power is less than the calculated value, the measured value shall prevail, and $I_{SAT}$ need greater than the set current limiting value $I_{PEAK}$, and cannot be less than 3.5A;
4) Take PVDD = 9.5V for example, under different conditions, the typical method of selecting $I_{SAT}$ in the following table:

| $V_{DD}$ (V) | PVDD (V) | $R_L$ (Ω) | $I_{PEAK}$ (A) | Efficiency(η) (%) | $P_O$ (W) | $I_{L\_PEAK}$ (A) | Inductor saturation current ISAT minimum value (A) |
|---|---|---|---|---|---|---|---|
| 4.2 | 9.5 | 8 | 4.25 | 74 | 5.2 | 4.15 | 4.2 |
| 4.2 | 9.5 | 6 | 4.25 | 69 | 5.4 | 4.5 | 4.2 |

5) As the result of the action of AGC，amplifier will not work long hours at maximum power without distortion, the actual average inductor current is far less than the maximum inductor current effective $I_{L\_RMS}$, so when selecting the inductor, the inductor temperature rise current is not usually a limiting factor;
6) Inductor Selection example: the inductor package size is 252012, inductance value is 1μH, DCR Typical value is 48mΩ, the typical saturation current $I_{SAT}$ is 4.2A, the typical temperature rise current $I_{RMS}$ is 3.4A, suitable for VDD=3.6V, PVDD=9.5V, speaker impedance $R_L$=8Ω, inductor input current limit $I_{PEAK}$= 4.25A. If you choose $I_{SAT}$ or $I_{RMS}$ of the inductance is too small, it is possible to cause the chip don't work properly, or the temperature of the inductance is too high.

| Inductance value | size | DCR（Ω） | $I_{SAT}$（A） | $I_{RMS}$（A） |
|---|---|---|---|---|
| 1μH | 2.5×2.0×1.2mm | 0.054 | 4.2 | 3.4 |

*BOOST CAPACITOR SELECTION*

Boost output capacitor is usually within the range 0.1μF~47μF. It needs to use Class II type (EIA) multilayer ceramic capacitors (MLCC). Its internal dielectric is ferroelectric material (typically $BaTiO_3$), a high the dielectric constant in order to achieve smaller size, but at the same Class II type (EIA) multilayer ceramic capacitors has poor temperature stability and voltage stability as compared to the Class I type (EIA) capacitance. Capacitor is selected based on the requirements of temperature stability and voltage stability, considering the capacitance material, capacitor voltage, and capacitor size and capacitance values.

A)  temperature stability

Class II capacitance have different temperature stability in different materials, usually choose X5R type in order to ensure enough temperature stability, and X7R type capacitance has better properties, the price is relatively more expensive; X5R capacitance change within ± 15% in temperature range of 55°C to 85°C, X7R capacitance change within ±15% in temperature range of -55°C~125°C. The Boost output capacitance of DEVICE recommends X5R ceramic capacitors.

B) Voltage Stability

Class II type capacitor has poor voltage stability Capacitance values falling fast along with the DC bias voltage applied across the capacitor increasing. The rate of decline is related to capacitance material, capacitors rated voltage, capacitance volume. Take TDK C series X5R for example, its pressure voltage value is 16V or 25V; the package size is 0805, 1206 or 0603, the capacitance value is 10μF. The capacitor's voltage stability of different types of capacitor is as shown below:
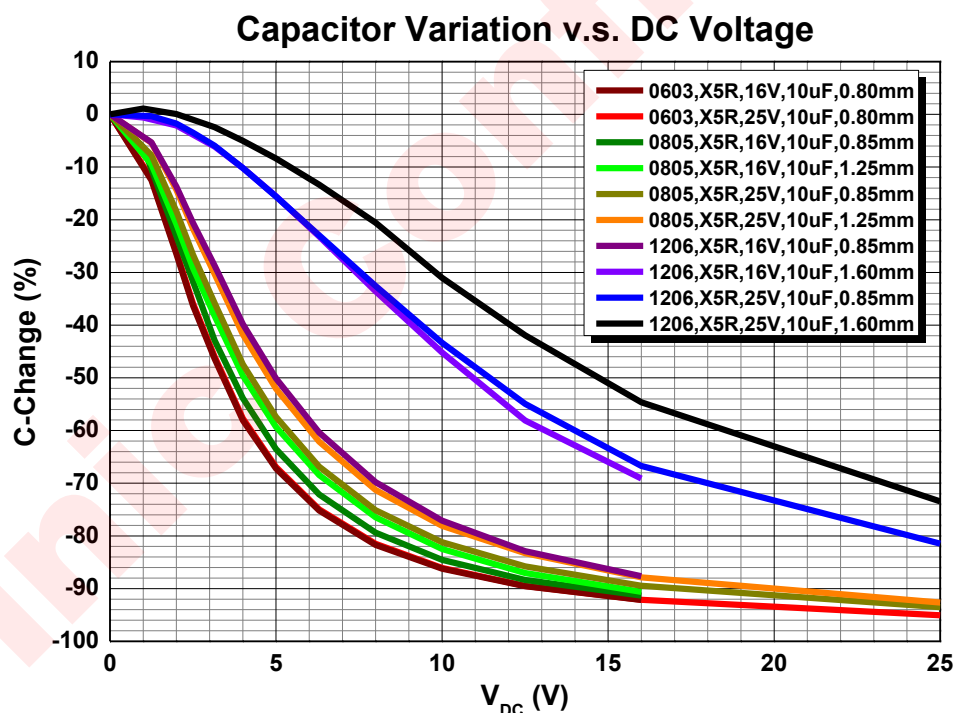


**Figure 20   Different types of capacitive voltage stability**

It can be found that the rate of capacitance capacity value descent becomes slow along with "large capacitor size, capacitance pressure voltage rise". The larger the package size, the better voltage stability. The higher the height, the better voltage stability with the same length and width of the capacitance. Voltage stability of smaller package size (0603) capacitor change affected by the pressure value is very small.

In typical applications, it is necessary to ensure the residual capacitance should **≥4μF** when PVDD=10.25V.

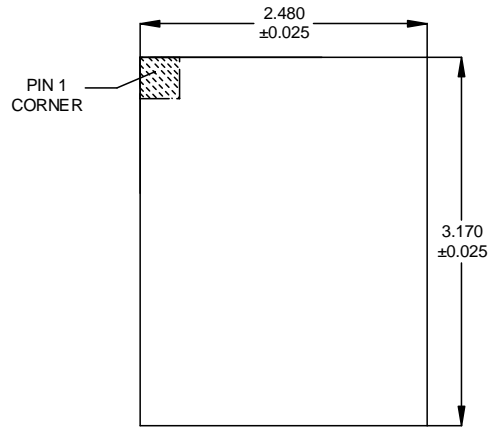Take the following capacitances as the Boost of the output capacitor for example:

| value | material | size (mm$^3$) | rated voltage (V) | quantity | value@10.25V |
|-------|----------|---------------|-------------------|----------|--------------|
| 10µF | X5R | 1.60×0.80×0.80 (0603) | 16 | 3 | 4.5µF |
| 10µF | X5R | 2.00×1.25×1.25 (0805) | 25 | 2 | 4.2µF |

As for the different manufacturers' capacitors, it's important to determine the type and quantity of the capacitors through the capacitor voltage stability data provided by the manufacturer.
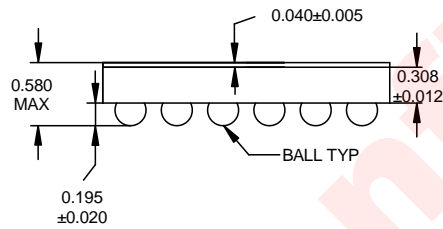
### *SUPPLY DECOUPLING CAPACITOR*

The device is a high-performance audio amplifier that requires adequate power supply decoupling. Place a low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1µF. This choice of capacitor and placement helps with higher frequency transients, spikes, or digital hash on the line. Additionally, placing this decoupling capacitor close to the DEVICE is important, as any parasitic resistance or inductance between the device and the capacitor causes efficiency loss. In addition to the 0.1µF ceramic capacitor, place a 10µF capacitor on the VBAT supply trace. This larger capacitor acts as a charge reservoir, providing energy faster than the board supply, thus helping to prevent any droop in the supply voltage.
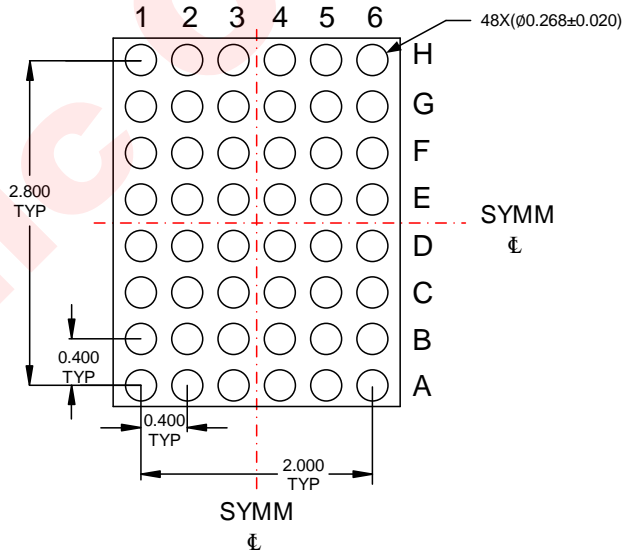
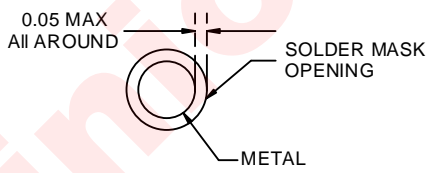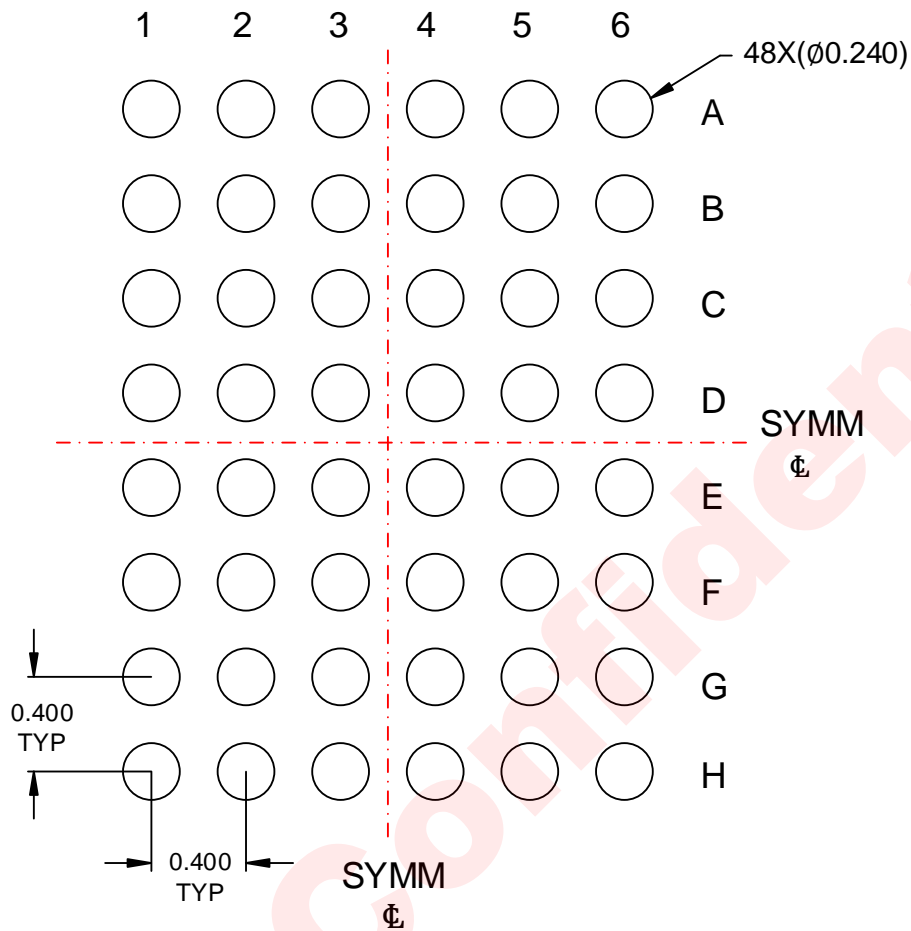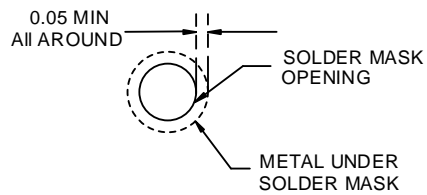## PACKAGE DESCRIPTION
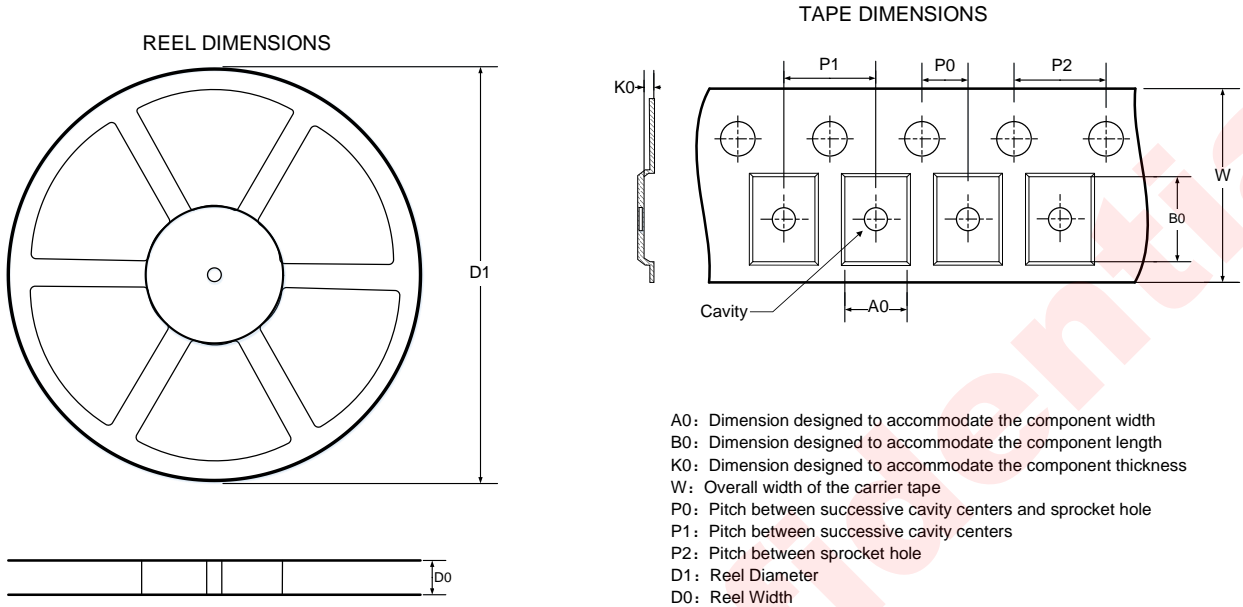


Top View

Side View

Bottom View

Unit：mm

## LAND PATTERN DATA



48X(∅0.240)

0.400 TYP

0.400 TYP

SYMM ₵

SYMM ₵

0.05 MAX All AROUND

SOLDER MASK OPENING

METAL

**NON-SOLDER MASK DEFINED**

0.05 MIN All AROUND

SOLDER MASK OPENING

METAL UNDER SOLDER MASK

**SOLDER MASK DEFINED**

Unit: mm

# TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

Pin 1

Sprocket Holes

User Direction of Feed

Pocket Quadrants
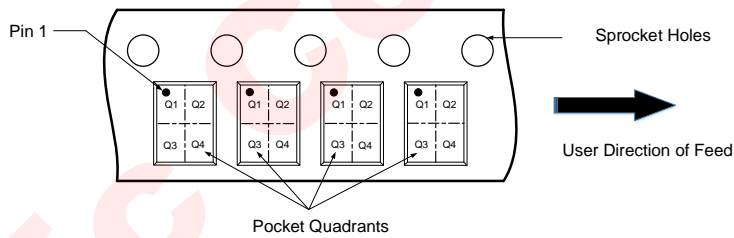
**All Dimensions are nominal**

| D1 (mm) | D0 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P0 (mm) | P1 (mm) | P2 (mm) | W (mm) | Pin1 Quadrant |
|---------|---------|---------|---------|---------|---------|---------|---------|--------|---------------|
| 330.00 | 12.40 | 2.62 | 3.30 | 0.81 | 2.00 | 8.00 | 4.00 | 12.00 | Q1 |

## REVISION HISTORY

| Version | Date | Change Record |
|---------|------|---------------|
| V1.0 | Jul. 2019 | Officially Released |

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