Low Noise Amplifier with Bypass Switch for LTE High Band

FEATURES

- Operating frequency 2300MHz to 2690MHz
- Noise figure(NF) =1.0dB
- High power gain =13.4dB
- Insertion Loss in bypass mode =4dB
- Gain mode IIP3ib =+5dBm
- Gain mode input 1dB-compression point=-2dBm
- Bypass mode input 1dB-compression point= +8dBm
- Supply voltage: 1.5V to 3.3V
- Gain mode current 9mA
- Bypass mode current <1uA
- Input and output DC decoupled
- Requires only one input matching inductor
- Integrated matching for the output
- FCDFN 1.1mmX0.7mmX0.37mm -6L package
- 2kV HBM ESD protection (including RFIN and RFOUT pin)

GENERAL DESCRIPTION

- The AW15208HFDR is a Low Noise Amplifier with bypass designed for LTE receiver applications. The AW15208HFDR requires only one external input matching inductor, reduces assembly complexity and the PCB area, enabling a cost-effective solution.
- The AW15208HFDR achieves low noise figure, high linearity, high gain, over a wide range of supply voltages from 1.5V up to 3.3V. All these features make AW15208HFDR an excellent choice for LTE LNA as it improves sensitivity with low noise figure and high gain, provides better immunity against jammer signals with high linearity, reduces filtering requirement of preceding stage and hence reduces the overall cost.
- The AW15208HFDR is available in a small lead-free, RoHS-Compliant, FCDFN 1.1mmX0.7mmX0.37 mm -6L package.

APPLICATIONS

- Cell phones
- Tablets
- Other RF front-end modules

TYPICAL APPLICATION CIRCUIT

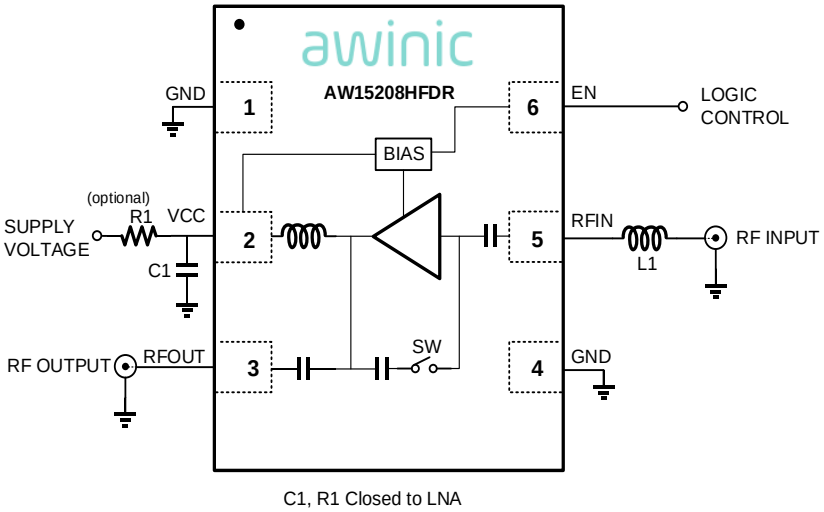


Figure 1 Typical Application Circuit of AW15208HFDR

PIN CONFIGURATION AND TOP MARK

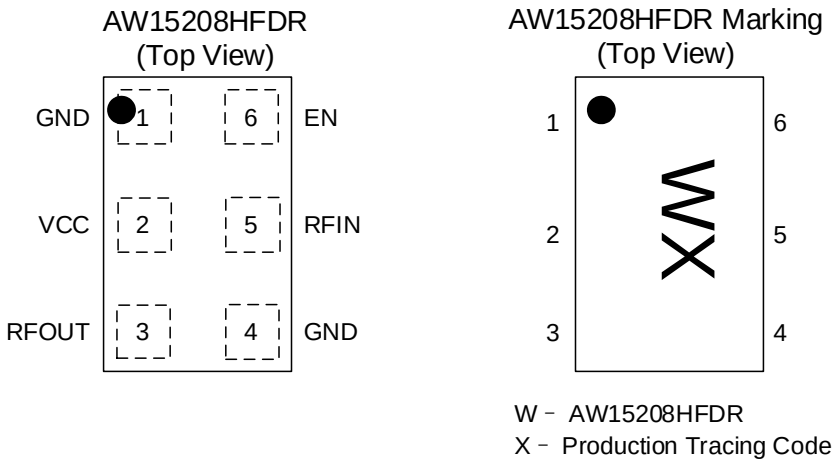


Figure 2 Pin Configuration and Top Mark

PIN DEFINITION

No.	NAME	DESCRIPTION
1	GND	Ground
2	VCC	Supply connection
3	RFOUT	RF output
4	GND	Ground
5	RFIN	RF input
6	EN	EN (high level) supports 1.8V/2.8V IO with internal 150Kohm pull-down resistor

FUNCTIONAL BLOCK DIAGRAM

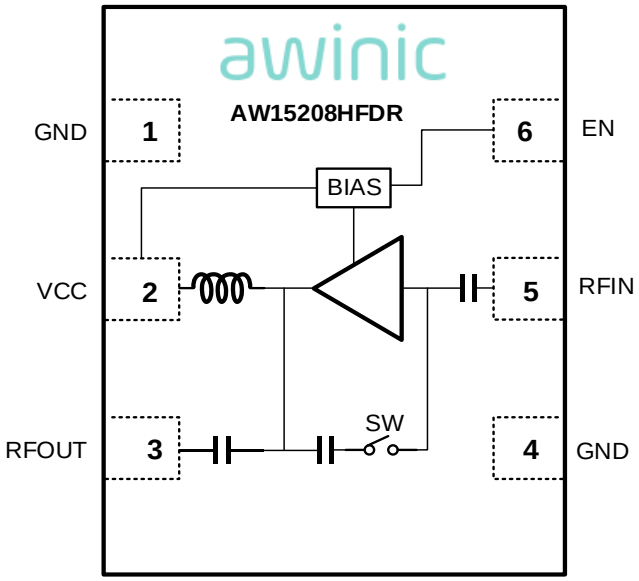


Figure 3 Functional Block Diagram

ORDERING INFORMATION

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW15208HFDR	-40℃～85℃	FCDFN 1.1mmX 0.7mm -6L	W	MSL1	ROHS+HF	3000 units/Tape & Reel

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETERS	RANGE
Supply voltage VCC	-0.3V to 3.6V
EN pin voltage	-0.3V to 3.6V
Supply maximum current ICC	30mA
RF input power Pin	25dBm
Maximum Junction temperature T_{JMAX}	150℃
Storage temperature T_{STG}	-65℃ to 150℃
Operating free-air temperature range	-40℃ to 85℃
Lead temperature (Soldering 10 Seconds)	260℃
ESD[2]	
HBM	±2kV
CDM	±1kV
Latch-up	
Standard: JEDEC STANDARD NO.78D NOVEMBER 2011	+IT: +200mA -IT: -200mA

[1] Conditions out of those ranges listed in “absolute maximum ratings” may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in “recommended operating conditions”. Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

[2] The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: MIL-STD-883J Method 3015.9. The CDM test method: JEDEC EIA/JESD22-C101F.

ELECTRICAL CHARACTERISTICS

TA=+25°C , V_{CC}=2.8V, EN=1.8V/2.8V, frequency=2300MHz to 2690MHz. Input matched to 50Ω using a 3.3nH[3] inductor in series. (unless otherwise noted).

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
DC Electrical Characteristic						
VCC	Supply Voltage		1.5	-	3.3	V
VEN	Digital Input-Logic High		0.8		3.3	V
	Digital Input-Logic Low				0.45	V
Gain Mode						
ICC	Supply Current			9	12.5	mA
Gp	Power Gain	2300MHz-2400MHz	12	13.6	14.5	dB
		2400MHz-2496MHZ	12	13.2	14.5	
		2496MHz-2690MHz	12	12.8	14.5	
		f=2350MHz [4]	12	13.7	14.5	
		f=2655MHz [5]	12	13.0	14.5	
RLin	Input Return Loss	f=2350MHz [4]	6	7		dB
		f=2655MHz [5]	6	9		
RLout	Output Return Loss	f=2350MHz [4]	6	8		dB
		f=2655MHz [5]	6	7		
ISL	Reverse Isolation	f=2350MHz [4]	18	26		dB
		f=2655MHz [5]	18	26		
NF	Noise Figure	f=2350MHz [4][6]		1.0	1.4	dB
		f=2655MHz [5][6]		1.3	1.4	
IP1dB	In-band input 1dB-compression point	f=2350MHz [4]	-6	-3		dBm
		f=2655MHz [5]	-6	-1		
IIP3ib	In-band input 3rd-order intercept point	f=2350MHz [4]	-0.5	5		dBm
		f=2655MHz [5]	-0.5	7.5		
ton	turn-on time	time from V_{EN} ON to 90% of the gain		2	4	μs
toff	turn-off time	time from V_{EN} OFF to 10% of the gain		1	2	μs
Bypass Mode						
ICC	Supply Current	VEN<0.45V			1	uA
Gp	Power Gain	2300MHz-2400MHz	-4.5	-3.8		dB
		2400MHz-2496MHz	-4.5	-3.5		
		2496MHz-2690MHz	-4.5	-3.5		
		f=2350MHz [4]	-4.5	-3.8		
		f=2655MHz [5]	-4.5	-3.5		
RLin	Input Return Loss	f=2350MHz [4]	6	9		dB
		f=2655MHz [5]	6	9		
RLout	Output Return Loss	f=2350MHz [4]	6	8.5		dB

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
		f=2655MHz [5]	6	7.5		
IP1dB	In-band input 1dB-compression point	f=2350MHz [4]	2	7		dBm
		f=2655MHz [5]	2	8		
IIP3ib	In-band input 3rd-order intercept point	f=2350MHz [4]	6	8		dBm
		f=2655MHz [5]	6	8		

[3] High quality-factor 3.3nH inductor.
[4] E-UTRA operating band40(2300MHz to 2400MHz) , input power is-25dBm.
[5] E-UTRA operating band 7(2620MHz to 2690MHz) , input power is -25dBm.
[6] PCB losses are subtracted.

TA=+25°C , V_{CC}=1.8V, EN=1.8V, frequency=2300MHz to 2690MHz. Input matched to 50Ω using a 3.3nH[3] inductor in series. (unless otherwise noted).

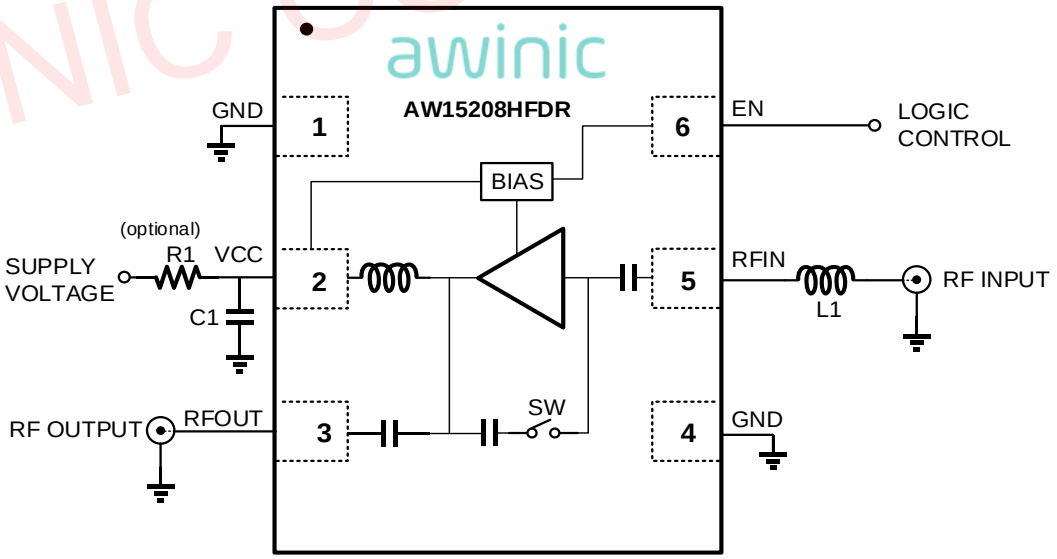
Symbol	Parameter	Test Condition	Min	Typ	Max	Units
DC Electrical Characteristic						
VCC	Supply Voltage		1.5	-	3.3	V
VEN	Digital Input-Logic High		0.8		3.3	V
	Digital Input-Logic Low				0.45	V
Gain Mode						
ICC	Supply Current			8.0	10	mA
Gp	Power Gain	2300MHz-2400MHz	11.4	13.2	14	dB
		2400MHz-2496MHz	11.4	12.8	14	
		2496MHz-2690MHz	11.4	12.5	14	
		f=2350MHz [4]	11.4	13.2	14	
		f=2655MHz [5]	11.4	12.5	14	
RLin	Input Return Loss	f=2350MHz [4]	6	7		dB
		f=2655MHz [5]	6	9		
RLout	Output Return Loss	f=2350MHz [4]	6	8		dB
		f=2655MHz [5]	6	7		
ISL	Reverse Isolation	f=2350MHz [4]	18	26		dB
		f=2655MHz [5]	18	26		
NF	Noise Figure	f=2350MHz [4][6]		1.0	1.4	dB
		f=2655MHz [5][6]		1.3	1.4	
IP1dB	In-band input 1dB-compression point	f=2350MHz [4]	-6	-5.2		dBm
		f=2655MHz [5]	-6	-3.7		
IIP3ib	In-band input 3rd-order intercept point	f=2350MHz [4]	-0.5	3		dBm
		f=2655MHz [5]	-0.5	5		
ton	turn-on time	time from VEN ON to 90% of the gain		2	4	μs
toff	turn-off time	time from V_{EN} OFF to 10% of the gain		1	2	μs
Bypass Mode						
ICC	Supply Current	VEN<0.45V			1	uA
Gp	Power Gain	2300MHz-2400MHz	-4.8	-4		dB

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
		2400MHz-2496MHz	-4.8	-3.8		
		2496MHz-2690MHz	-4.8	-3.8		
		f=2350MHz [4]	-4.8	-4		
		f=2655MHz [5]	-4.8	-3.8		
RLin	Input Return Loss	f=2350MHz [4]	6	8.5		dB
		f=2655MHz [5]	6	7.5		
RLout	Output Return Loss	f=2350MHz [4]	6	8.5		dB
		f=2655MHz [5]	6	7.5		
IP1dB	In-band input 1dB-compression point	f=2350MHz [4]	2	5		dBm
		f=2655MHz [5]	2	5.5		
IIP3ib	In-band input 3rd-order intercept point	f=2350MHz [4]	5	7		dBm
		f=2655MHz [5]	5	7		

[3] High quality-factor 3.3nH inductor.
[4] E-UTRA operating band40(2300MHz to 2400MHz) , input power is -25dBm..
[5] E-UTRA operating band 7(2620MHz to 2690MHz) , input power is -25dBm.
[6] PCB losses are subtracted.

MEASUREMENT DIAGRAM

Test DC Characteristics(Current & Power Consumption)



C1, R1 Closed to LNA

Figure 4 AW15208HFDR DC Test Diagram

Test S-Parameter

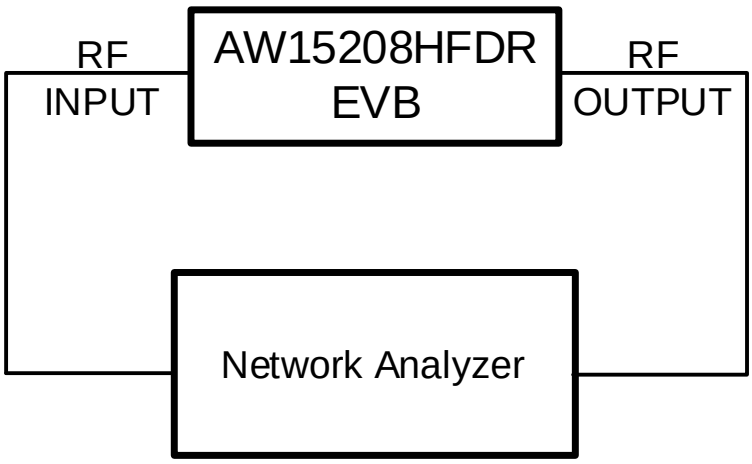


Figure 5 AW15208HFDR S-parameter Measurement Diagram

Test Noise Figure

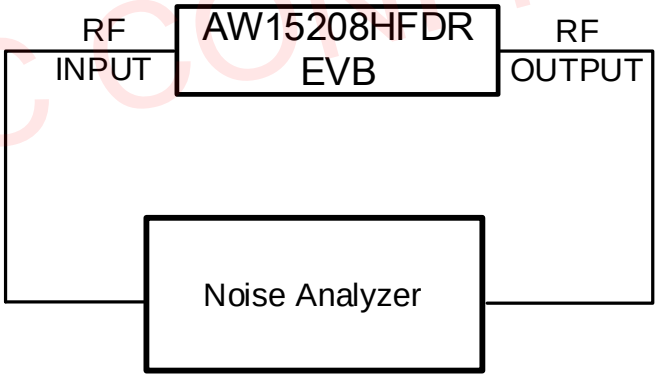


Figure 6 AW15208HFDR Noise Figure Measurement Diagram

Test IIP3

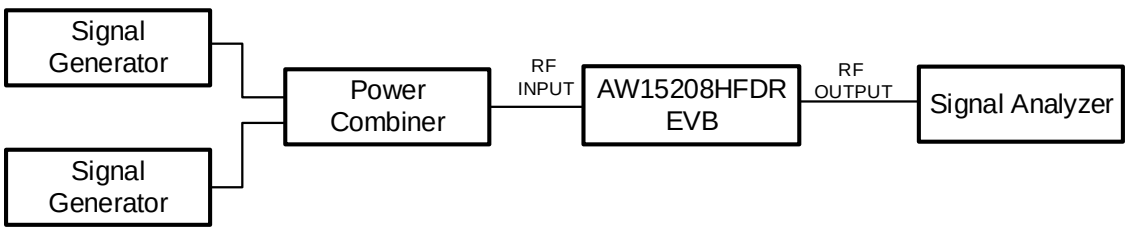


Figure 7 AW15208HFDR IIP3 Measurement Diagram

APPLICATION INFORMATION

Choice of components

- The AW15208HFDR requires only one external inductor for input matching. If the device/phone manufacturers implement very good power supply filtering on their boards, the bypass capacitor mentioned in this application circuit may be optional. With the power supply decoupling capacitor, better performance would be received, like a little higher gain, etc. The value is optimized for the key performance, such as higher power gain, lower noise figure, and better return loss. Typical value of inductor is 3.3nH with high quality factor, and capacitor is 1nF. The typical application circuit can refer to Figure1.
- The output of AW15208HFDR is internally matched to 50 ohm and a DC blocking capacitor is integrated on-chip, thus no external component is required at the output.
- The AW15208HFDR should be placed close to the diversity antenna with the input-matching inductor. Use 50 ohm micro-strip lines to connect RF INPUT and RF OUTPUT. Bypass capacitor need be located close to the device. For long V_{CC} lines, it may be necessary to add more decoupling capacitors. Proper grounding of the GND pins is very important.

Following tables show recommended inductor and capacitor values.

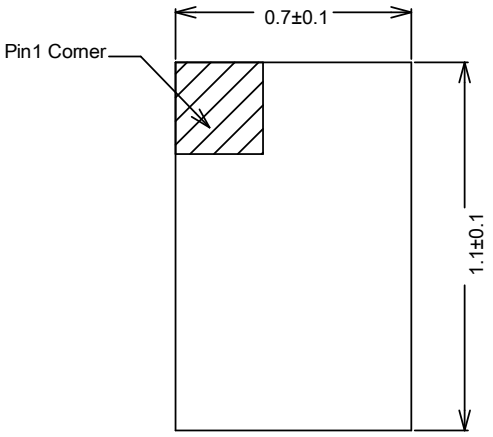
Inductor Selection Table

Component	Part	Typical(nH)	Q(min)	Frequency(MHz)	MFR	Size
L1	LQW15A	3.3	25	250	Murata	0402

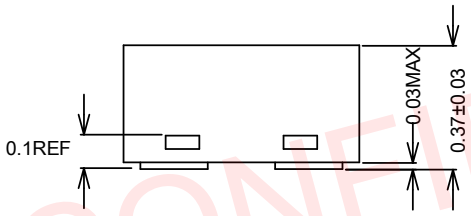
Capacitor Selection Table

Component	Part	Typical(pF)	Voltage(V)	MFR	Size
C1	GRM155	1000	50	Murata	0402

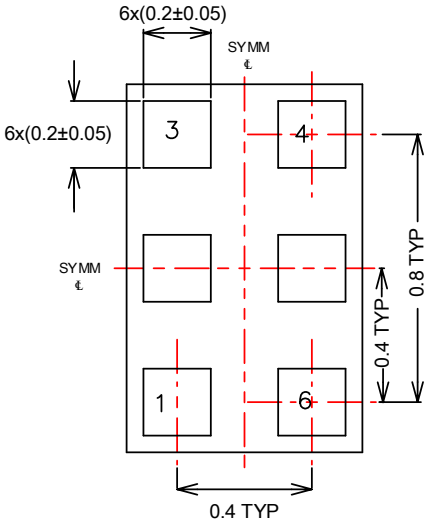
PACKAGE DESCRIPTION



TOP VIEW



SIDE VIEW



BOTTOM VIEW

Unit：mm

Figure 8 Package Outline

LAND PATTERN

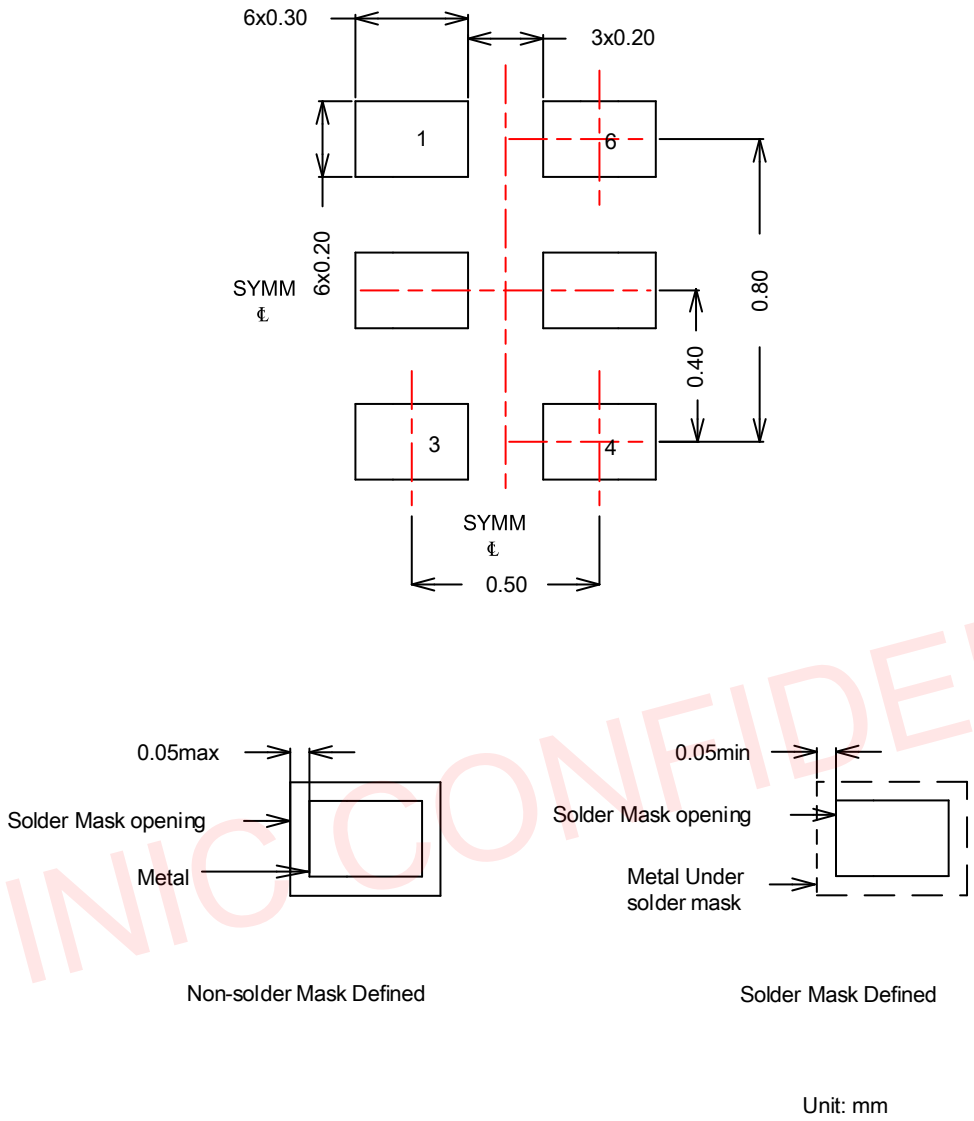
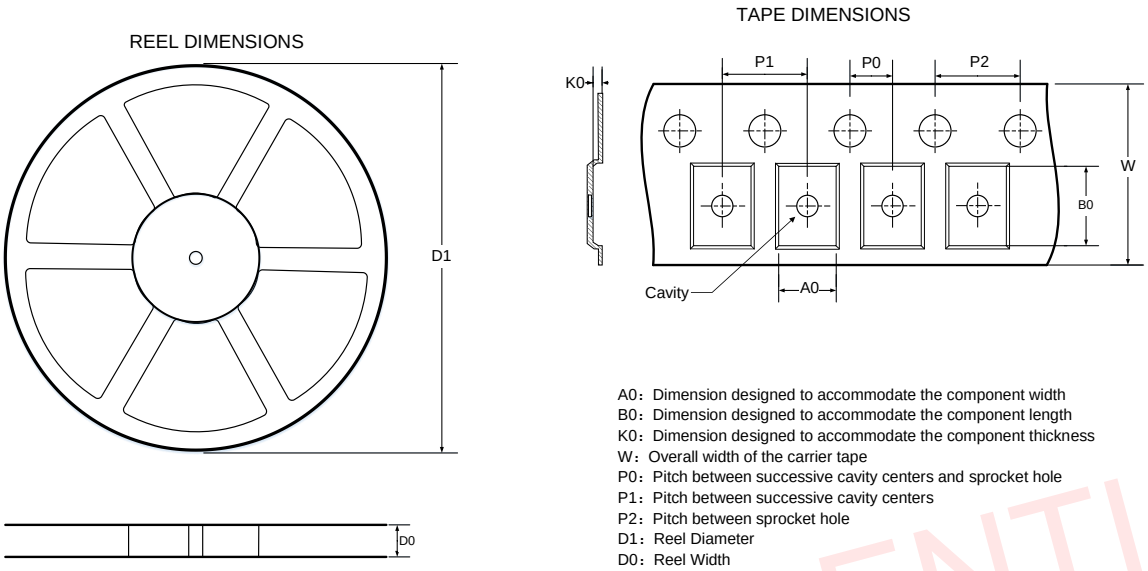
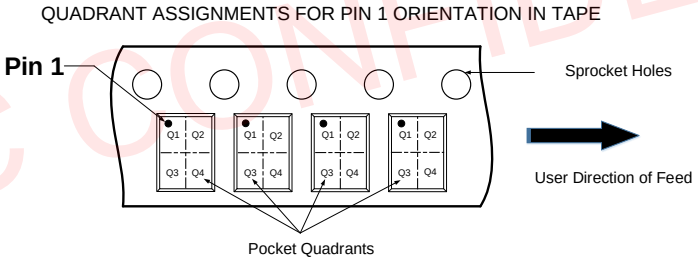


Figure 9 Land Pattern

TAPE & REEL DESCRIPTION



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width



DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.4	0.8	1.2	0.55	2	2	4	8	Q1

All dimensions are nominal

Figure 10 Tape & Reel Description

REVISION HISTORY

Version	Date	Change Record
V1.0	Mar.2019	Officially Released
V1.1	Oct.2019	Update electrical characteristics
V1.2	Oct.2019	Update electrical characteristics
V1.3	Nov.2019	Update electrical characteristics

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