H-Bridge DC Motor Driver

Features

- Drives a DC Motor or Other Loads
- Rdson HS + LS: 340mΩ
- 1.9-A Maximum Drive Current
- VDD: 1.8V to 12V Supply Voltage Range
- VCC: 1.8V to 5.5V Supply Voltage Range
- Low-Power Sleep Mode With 120-nA Maximum Sleep Current
- DFN 2mm X2mm X0.75mm-8L package
- Short-Circuit Protection
- Over-Temperature Protection
- Under-Voltage Protection

Applications

- Cameras
- DSLR Lenses
- Consumer Products
- Toys
- Robotics
- Medical Devices

General Description

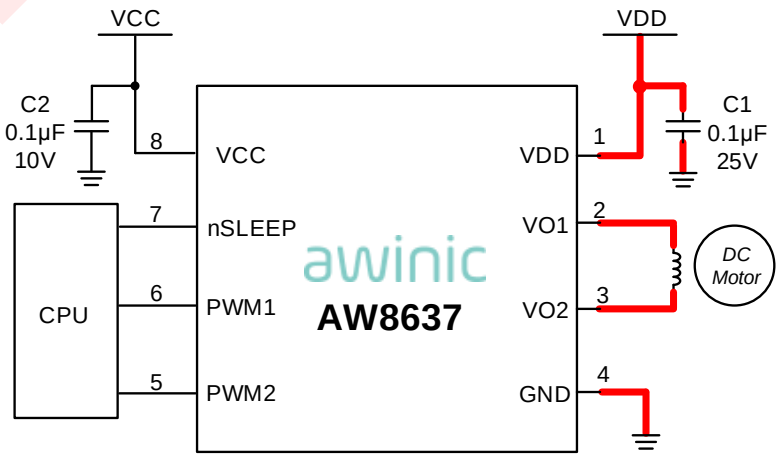
The AW8637 provides an integrated motor driver solution for cameras, consumer products, toys, and other low-voltage or battery-powered motion control applications. The device can drive one dc motor or other devices like solenoids. The output driver block consists of N-channel power MOSFETs configured as an H-bridge to drive the motor winding. An internal charge pump generates needed gate drive voltages.

The AW8637 can supply up to 1.9A of output current. It operates on a motor power supply voltage from 1.8V to 12V, and a device power supply voltage of 1.8V to 5.5V.

The AW8637 has a PWM (PWM1-PWM2) input interface, witch is compatible with industry standard devices.

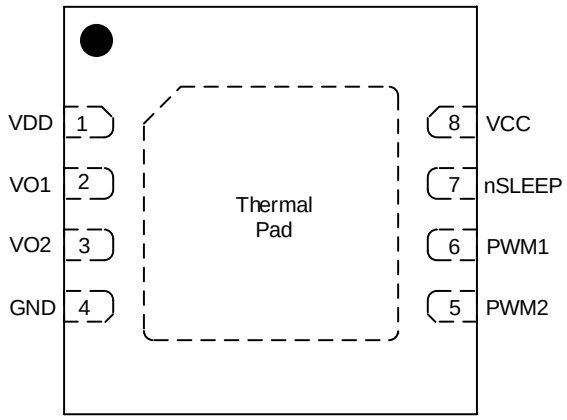
Internal shutdown functions are provided for Over-current protection, Short-circuit protection, Under-voltage lockout, and Over-temperature protection.

Typical Application Circuit

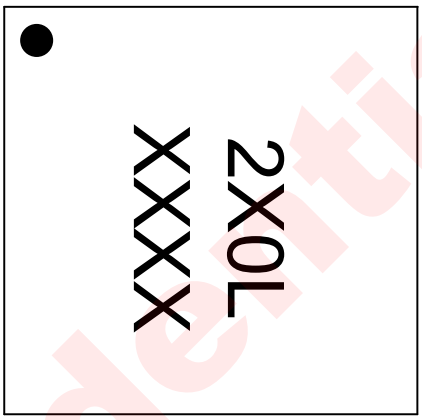


Pin Configuration And Top Mark

AW8637DNR
(Top View)



AW8637DNR Marking
(Top View)



2X0L - AW8637DNR
XXXX - Production Tracing Code

Figure 1 Pin Configuration And Top Mark

Pin Definition

No.	NAME	DESCRIPTION
1	VDD	Motor power supply. Bypass this pin to the GND pin with a 0.1-μF ceramic capacitor rated for VDD.
2	VO1	Motor output. Connect these pins to the motor winding.
3	VO2	
4	GND	Device ground. This pin must be connected to ground.
5	PWM2	PWM2 input
6	PWM1	PWM1 input
7	nSLEEP	Sleep mode input. When this pin is in logic low, the device enters low-power sleep mode. The device operates normally when this pin is logic high. Internal pulldown
8	VCC	Logic power supply. Bypass this pin to the GND pin with a 0.1-μF ceramic capacitor rated for VCC.
9	Thermal pad	Beneath the IC for heat dissipation. Always solder to the PCB ground for high-current power converter

Functional Block Diagram

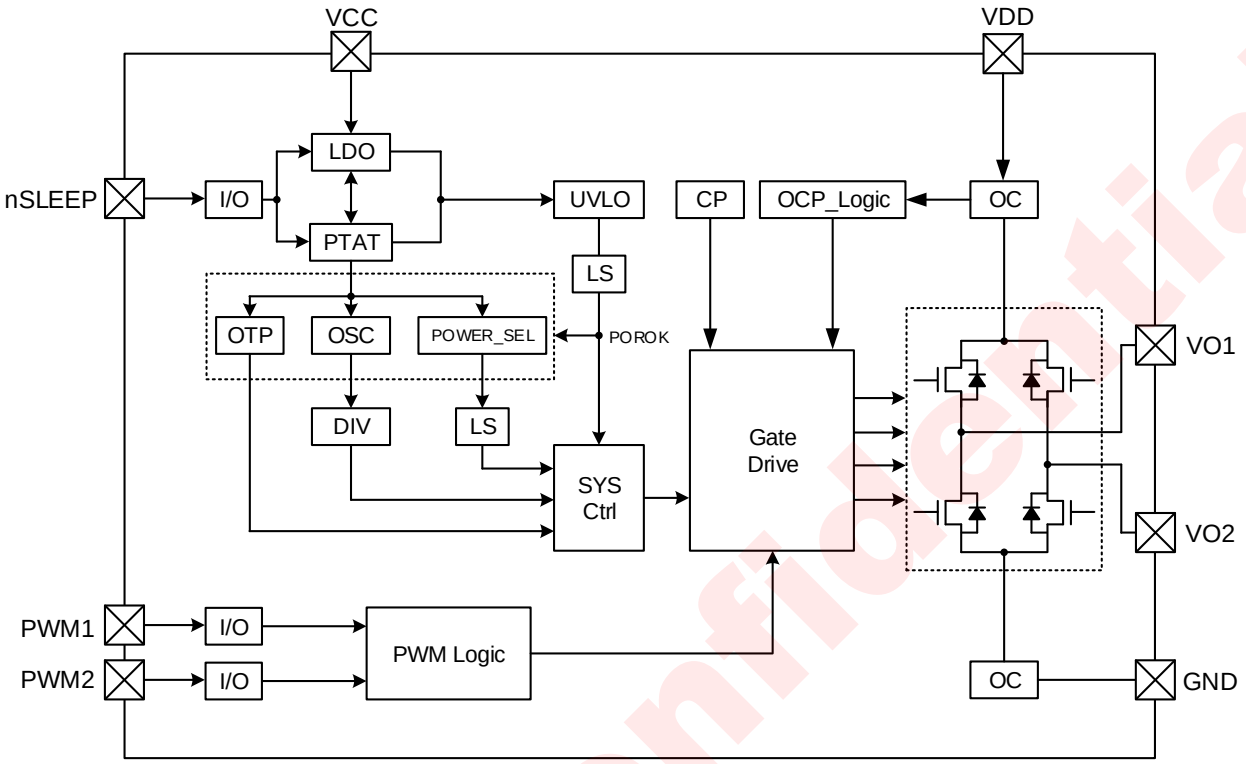


Figure 2 Functional Block Diagram

Typical Application Circuits

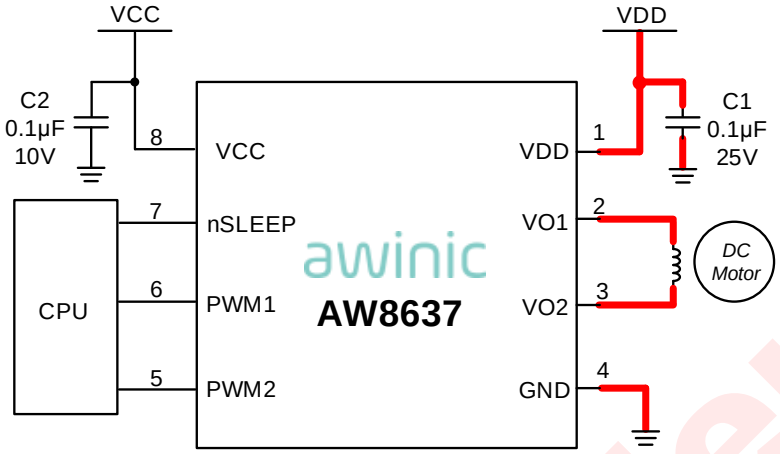


Figure 3 Typical Application Circuit of AW8637

Notice for Typical Application Circuits:

1：Please place C1，C2 as close to the chip as possible. The capacitors should be placed in the same layer with the AW8637 chip.

2：For the sake of driving capability, the power lines and output lines should be short and wide as possible.

3：The power path marked in red as shown in the figures above, please traces according to 2A power line alignment rules.

4：**Table 1** lists the recommended external components for the device.

Table 1 External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C_1	VDD	GND	25V, 0.1μF ceramic capacitor rated for VDD
C_2	VCC	GND	10V, 0.1μF ceramic capacitor rated for VCC

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW8637 DNR	-40℃~85℃	DFN 2mmX2mm-8L	2X0L	MSL1	ROHS+HF	3000 units/Tape and Reel

Absolute Maximum Ratings(NOTE1)

PARAMETERS	RANGE
Motor power-supply voltage (VDD)	-0.3V to 13V
Logic power-supply voltage (VCC)	-0.3V to 5.5V
Control pin voltage (PWM1, PWM2, nSLEEP)	-0.5V to 5.5V
Peak drive current (VO1, VO2)	Internally limited
Junction-to-ambient thermal resistance θ_{JA}	97.7°C /W
Operating free-air temperature range	-40°C to 85°C
Maximum operating junction temperature T_{JMAX}	160°C
Storage temperature TSTG	-65°C to 150°C
Lead temperature (soldering 10 seconds)	260°C
ESD(Including CDM HBM MM)(NOTE 2)	
HBM(Human Body Model)	±3kV
CDM(Charge Device Model)	±1.5kV
Latch-Up	
Test Condition: JEDEC STANDARD NO.78E	+IT：200mA -IT：-200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ANSI/ESDA/JEDEC JS-001

Electrical Characteristics

T_A=25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (VDD, VCC)						
VDD	VDD operating voltage		0		12	V
I_{VDD}	VDD operating supply current	VDD=5V; VCC=3V; No PWM;No load		40	100	μA
		VDD=5V; VCC=3V; 50kHz PWM; No load		0.8	1.5	mA
I_{VDDQ}	VDD sleep mode supply current	VDD=5V; VCC=3V; nSLEEP=0		30	95	nA
VCC	VCC operating voltage		1.8		5.5	V
I_{VCC}	VCC operating supply current	VDD=5V; VCC=3V; No PWM; No load		300	500	μA
		VDD=5V; VCC=3V; 50kHz PWM; No load		0.7	1.5	mA
I_{VCCQ}	VCC sleep mode supply current	VDD=5V; VCC=3V; nSLEEP=0		5	25	nA
CONTROL INPUTS (PWM1, PWM2, nSLEEP)						
V_{IL}	Input logic-low voltage	VCC=1.8V			0.38 × VCC	V
		VCC=5.5V			0.19 × VCC	V
V_{IH}	Input logic-high voltage	VCC=1.8V	0.55 × VCC			V
		VCC=5.5V	0.41 × VCC			V
V_{HYS}	Input logic hysteresis	VCC=1.8V		0.09 × VCC		V
		VCC=5.5V		0.17 × VCC		V
I_{IL}	Input logic low current	VIN=0V	–5		5	μA
I_{IH}	Input logic high current	VIN=3.3V		33	50	μA
R_{PD}	Pulldown resistance			100		kΩ
MOTOR DRIVER OUTPUTS (VO1, VO2)						
$r_{DS(on)}$	HS + LS FET on-resistance	VDD=5V; VCC=3V; I_O= 800mA; T_J=25°C		340	380	mΩ
I_{OFF}	Off-state leakage current	V_{OUT}=0V	–200		200	nA
PROTECTION CIRCUITS						
V_{UVLO}	VCC undervoltage lockout	VCC falling			1.7	V
		VCC rising			1.8	V
I_{OCP}	Overcurrent protection trip level		1.9		3.5	A
t_{DEG}	Overcurrent deglitch time			1		μs
t_{RETRY}	Overcurrent retry time			1		ms
T_{TSD}	Thermal shutdown temperature	Die temperature T_J	150	160	180	°C

Timing Requirements

T_A=25°C, VDD=5V, VCC=3V

NO.	DESCRIPTION		TYP	UNIT
1	t_1	Output enable time	850	ns
2	t_2	Output disable time	30	ns
3	t_3	Delay time, PWMx high to VOx high	850	ns
4	t_4	Delay time, PWMx low to VOx low	30	ns
5	t_5	Output rise time	450	ns
6	t_6	Output fall time	450	ns
7	t_{wake}	Wake time, nSLEEP rising edge to part active	15	μs

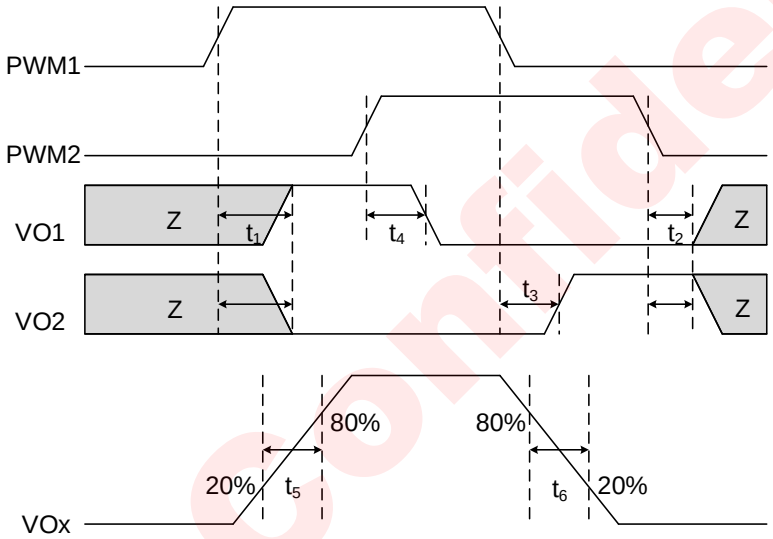


Figure 4 Input and Output Timing for AW8637

Detailed Functional Description

OVERVIEW

The AW8637 is an H-bridge driver that can drive one dc motor or other devices like solenoids. The outputs are controlled using a PWM interface (PWM1 and PWM2) on the AW8637 device. A low-power sleep mode is included, which can be enabled using the nSLEEP pin.

The device greatly reduce the component count of motor driver systems by integrating the necessary driver FETs and FET control circuitry into a single device. In addition, the AW8637 adds protection features beyond traditional discrete implementations: under-voltage lockout, overcurrent protection, and thermal shutdown.

FEATURE DESCRIPTION

BRIDGE CONTROL

The AW8637 is controlled using a PWM input interface. Each output is controlled by a corresponding input pin. **Table 2** shows the logic for the AW8637 device.

Table 2 AW8637 Device Logic

nSLEEP	PWM1	PWM2	VO1	VO2	FUNCTION (DC MOTOR)
0	X	X	Z	Z	Coast
1	0	0	Z	Z	Coast
1	0	1	L	H	Reverse
1	1	0	H	L	Forward
1	1	1	L	L	Brake

SLEEP MODE

If the nSLEEP pin is brought to a logic-low state, the AW8637 enters a low-power sleep mode. In this state, all unnecessary internal circuitry is powered down.

POWER SUPPLIES AND INPUT PINS

The input pins can be driven within the recommended operating conditions with or without the VCC, VDD, or both power supplies present. No leakage current path will exist to the supply. Each input pin has a weak pulldown resistor (approximately 100 kΩ) to ground.

The VCC and VDD supplies can be applied and removed in any order. When the VCC supply is removed, the device enters a low-power state and draws very little current from the VDD supply. The VCC and VDD pins can be connected together if the supply voltage is between 1.8V and 5.5V.

The VDD voltage supply does not have any under-voltage lockout protection (UVLO) so as long as VCC>1.8V; the internal device logic remains active, which means that the VDD pin voltage can drop to 0V. However, the load cannot be sufficiently driven at low VDD voltages.

VCC UNDERVOLTAGE LOCKOUT

If at any time the voltage on the VCC pin falls below the under-voltage lockout threshold voltage, all FETs in the H-bridge are disabled. Operation resumes when the VCC pin voltage rises above the UVLO threshold.

OVERCURRENT PROTECTION

An analog current-limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than t_{DEG}, all FETs in the H-bridge are disabled. Operation resumes automatically after t_{RETRY} has elapsed. Overcurrent conditions are detected on both the high-side and low side FETs. A short to the VDD pin, GND, or from the VO1 pin to the VO2 pin results in an overcurrent condition.

THERMAL SHUTDOWN

If the die temperature exceeds safe limits, all FETs in the H-bridge are disabled. After the die temperature falls to a safe level, operation automatically resumes.

Table 3 Fault Behavior

FAULT	CONDITION	H-BRIDGE	RECOVERY
VCC under-voltage (UVLO)	VCC<1.7V	Disabled	VCC>1.8V
Overcurrent (OCP)	I_{OUT}>1.9A (MIN)	Disabled	t_{RETRY} elapses
Thermal Shutdown (TSD)	T_J>160°C (MIN)	Disabled	T_J<130°C

DEVICE FUNCTIONAL MODES

The AW8637 is active unless the nSLEEP pin is brought logic low. In sleep mode, the H-bridge FETs are disabled Hi-Z. The AW8637 is brought out of sleep mode automatically if nSLEEP is brought logic high. The H-bridge outputs are disabled during under-voltage lockout, overcurrent, and over-temperature fault conditions.

Application Information

The AW8637 is used to drive one dc motor or other devices like solenoids. The following design procedure can be used to configure the AW8637 device.

DESIGN REQUIREMENTS

Table 4 lists the required parameters for a typical usage case.

Table 4 System Design Requirements

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Motor supply voltage	VDD	9V
Logic supply voltage	VCC	3.3V
Target rms current	I_{OUT}	0.8A
Externally applied PWM frequency	f_{PWM}	0 to 200kHz

MOTOR VOLTAGE

The appropriate motor voltage depends on the ratings of the motor selected and the desired RPM. A higher voltage spins a brushed dc motor faster with the same PWM duty cycle applied to the power FETs. A higher voltage also increases the rate of current change through the inductive motor windings.

LOW-POWER OPERATION

When entering sleep mode, recommends setting all inputs as a logic low to minimize system power.

APPLICATION CURVES

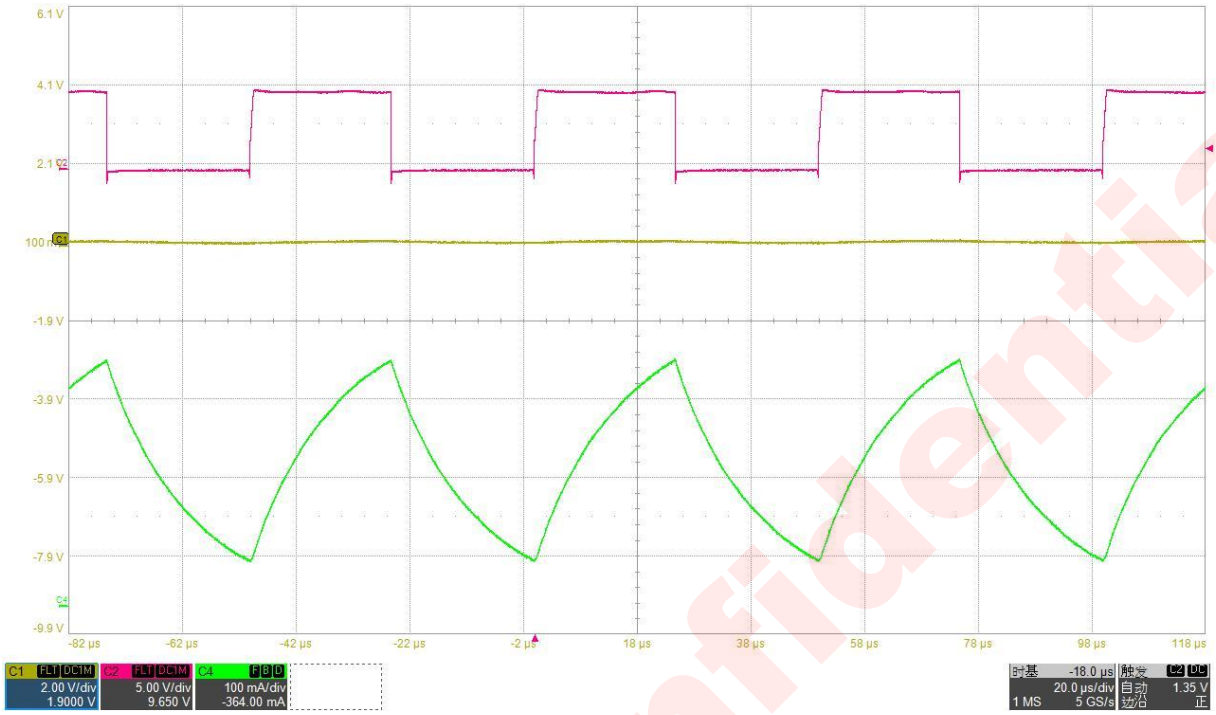


Figure 5 50% Duty Cycle Reverse Direction

Figure 6 20% Duty Cycle Reverse Direction

POWER SUPPLY RECOMMENDATIONS

BULK CAPACITANCE

Having appropriate local bulk capacitance is an important factor in motor-drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The power-supply capacitance and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed dc, brushless dc, stepper)
- The motor braking method

The inductance between the power supply and motor drive system limits the rate at which current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The datasheet generally provides a recommended value, but system-level testing is required to determine the appropriate size of bulk capacitor.

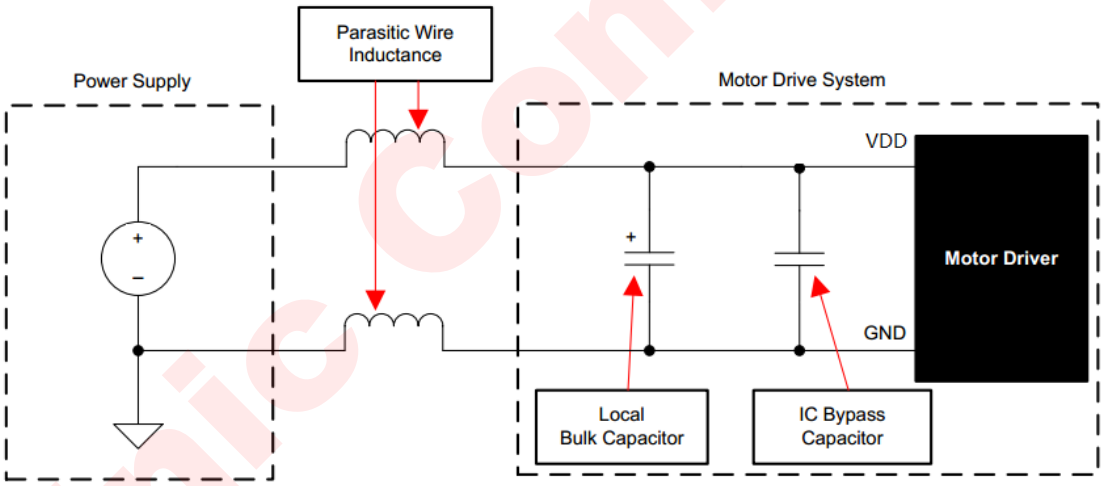


Figure 7 Example Setup of Motor Drive System With External Power Supply

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

PCB Layout Consideration

EXTERNAL COMPONENTS PLACEMENT

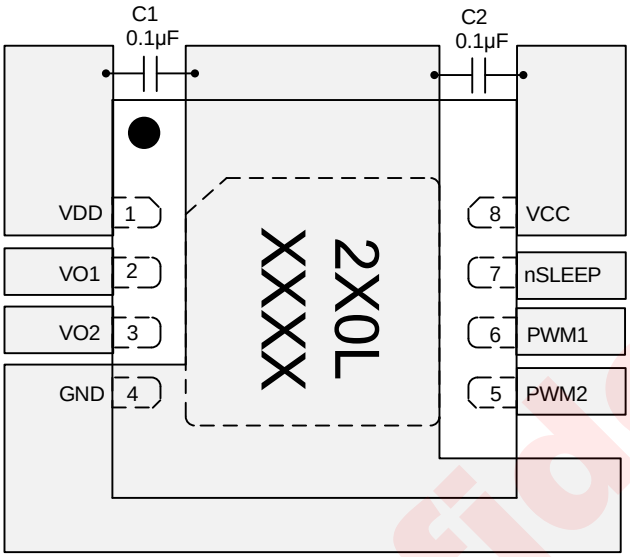


Figure 8 AW8637 External Components Placement

LAYOUT CONSIDERATIONS

This device is a high voltage driver chip. To obtain the optimal performance, PCB layout should be considered carefully. The suggested Layout is illustrated in the following diagram:

1. All of the external components close to IC in top layer PCB;
2. Create solid GND plane near and around the IC;
3. No via in traces from IC pin VDD/VCC through C1/C2 to IC pin GND, keep the trace as short as possible;
4. Try to provide a separate short and thick power line to the device, the copper width is recommended to be larger than 0.75mm. The decoupling capacitors should be placed as close as possible to boost power supply pin;
5. The output line from the device to load should be as short and thick as possible. The width is recommended to be larger than 0.5mm;

POWER DISSIPATION

Power dissipation in the AW8637 is dominated by the power dissipated in the output FET resistance, or $r_{DS(on)}$. Use Equation to estimate the average power dissipation when running a stepper motor.

$$P_{TOT} = r_{DS(on)} \times (I_{OUT(rms)})^2$$

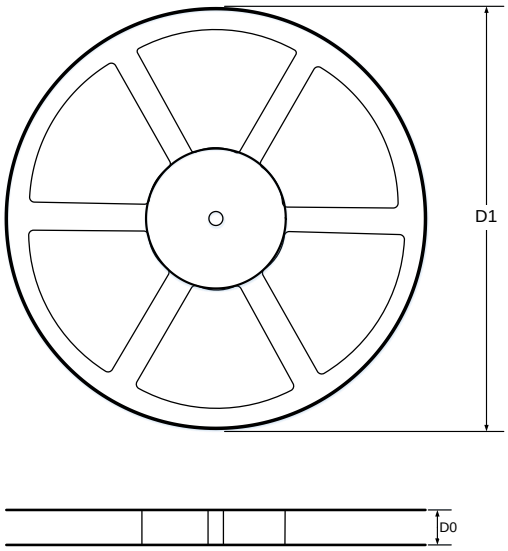
Where

- P_{TOT} is the total power dissipation
- $r_{DS(on)}$ is the resistance of the HS plus LS FETs
- $I_{OUT(rms)}$ is the rms or dc output current being supplied to the load

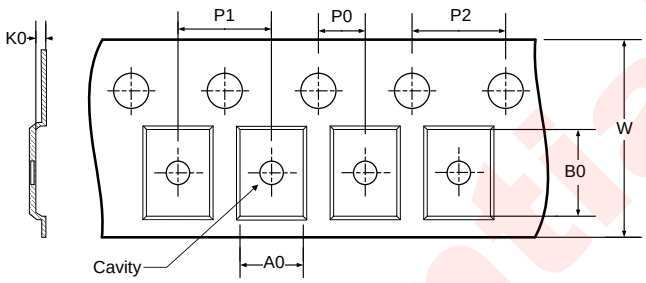
The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

Tape And Reel Information

REEL DIMENSIONS

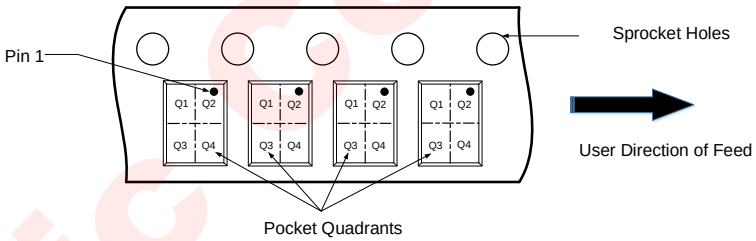


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

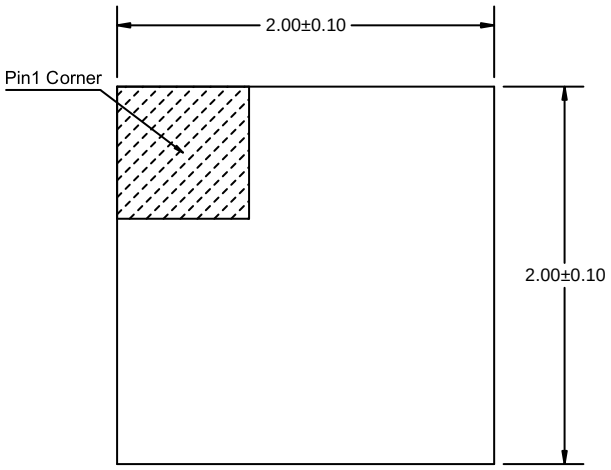
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



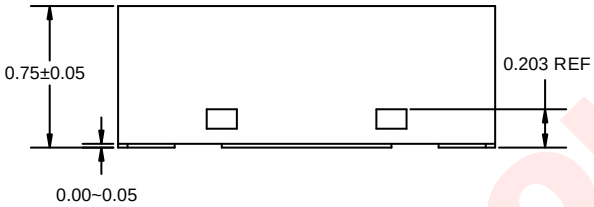
All Dimensions are nominal

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.4	2.3	2.3	1.0	2.0	4.0	4.0	8.0	Q2

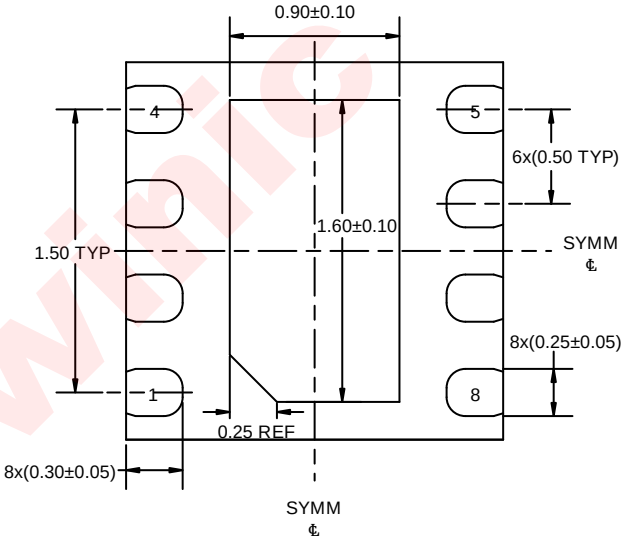
Package Description



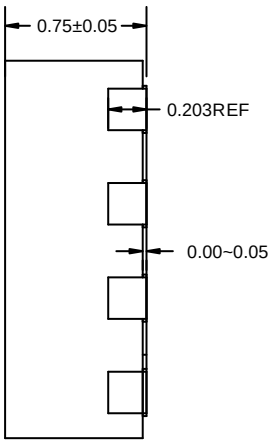
Top View



Side View



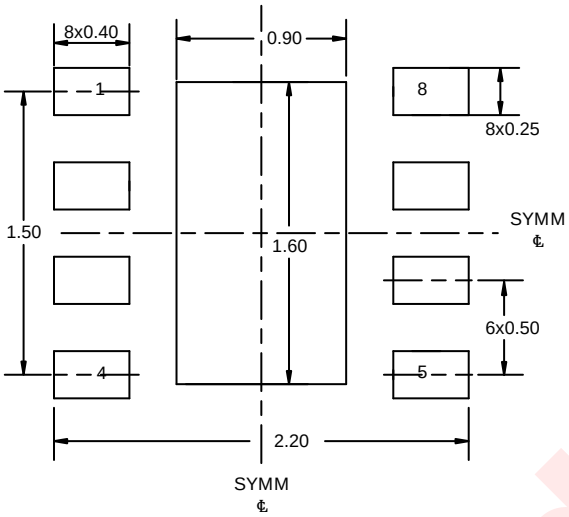
Bottom View

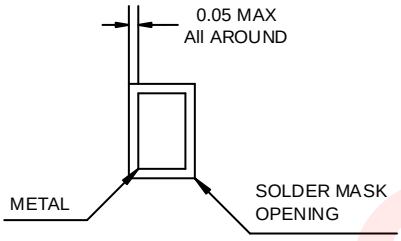


Side View

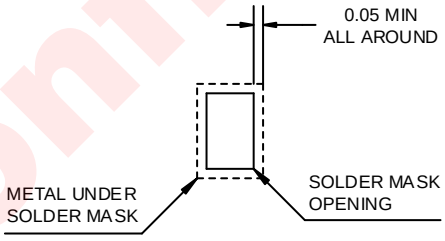
Unit: mm

Land Pattern Data





NON-SOLDER MASK DEFINED



SOLDER MASK DEFINED

Unit: mm

Revision History

Version	Date	Change Record
V1.0	June 2019	Officially released
V1.1	June 2019	Change the SPEC for some parameter

Disclaimer

All trademarks are the property of their respective owners. Information in this document is believed to be accurate and reliable. However, Shanghai AWINIC Technology Co., Ltd (AWINIC Technology) does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

AWINIC Technology reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. Customers shall obtain the latest relevant information before placing orders and shall verify that such information is current and complete. This document supersedes and replaces all information supplied prior to the publication hereof.

AWINIC Technology products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an AWINIC Technology product can reasonably be expected to result in personal injury, death or severe property or environmental damage. AWINIC Technology accepts no liability for inclusion and/or use of AWINIC Technology products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications that are described herein for any of these products are for illustrative purposes only. AWINIC Technology makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

All products are sold subject to the general terms and conditions of commercial sale supplied at the time of order acknowledgement.

Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Reproduction of AWINIC information in AWINIC data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. AWINIC is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of AWINIC components or services with statements different from or beyond the parameters stated by AWINIC for that component or service voids all express and any implied warranties for the associated AWINIC component or service and is an unfair and deceptive business practice. AWINIC is not responsible or liable for any such statements.

单击下面可查看定价，库存，交付和生命周期等信息

>>AWINIC(艾为)