0.06-4.2GHz SP2T Switch for 3G/4G/5G N78 TRX

FEATURES

- Broadband frequency range: 0.06 to 4.2 GHz
- Low insertion loss: 0.4dB typical @ 2.7 GHz
- High isolation: >23dB @ 2.7 GHz
- Integrated logic
- Small DFN (6-pin, 1.1mm x 0.7 mm x 0.55 mm) package (MSL1, 260 °C per JEDEC J-STD-020)

APPLICATIONS

- Cellular 3G/4G/5G N78 TRX
- Cellular modems , tablets and USB Devices
- Other RF front-end modules

GENERAL DESCRIPTION

The AW13412 is a SP2T switch with low insertion loss and high Isolation. It can be used to support band switching and mode switching for cellular 3G/4G, data cards and tablets.

The symmetrical design of internal ports makes it convenient for PCB routing and adjustment of receiving and transmitting signals. The band/mode switching is realized by the GPIO pins as referenced in the chip block diagram and the control logic.

The AW13412 is provided in a compact DFN 1.1mm x 0.7mm x 0.55mm-6L package.

TYPICAL APPLICATION CIRCUIT

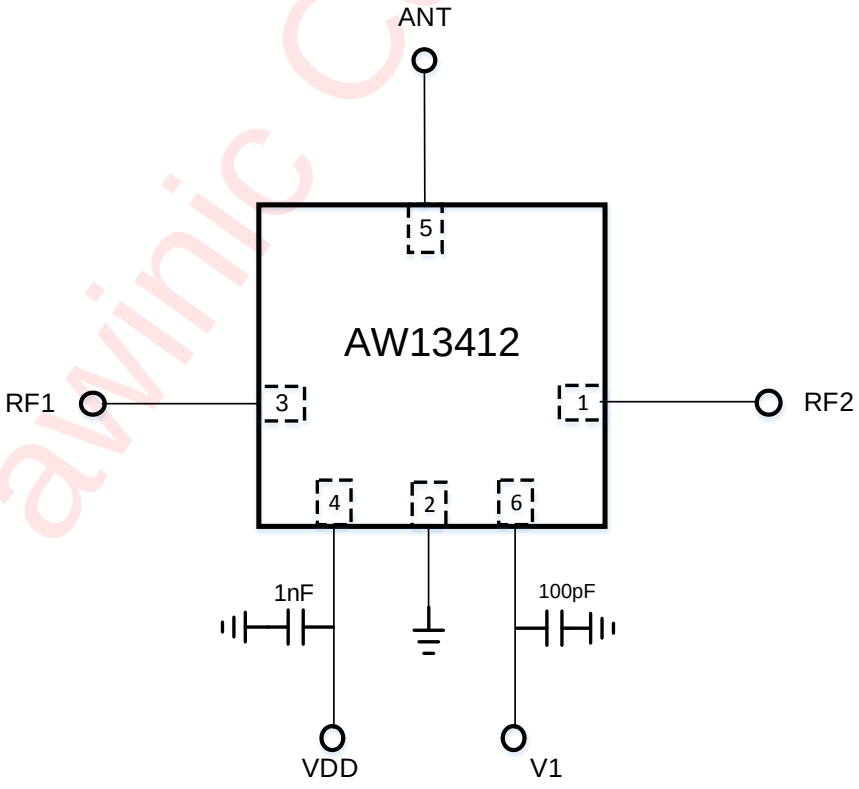


Figure 1 Typical Application Circuit of AW13412

PIN CONFIGURATION AND TOP MARK

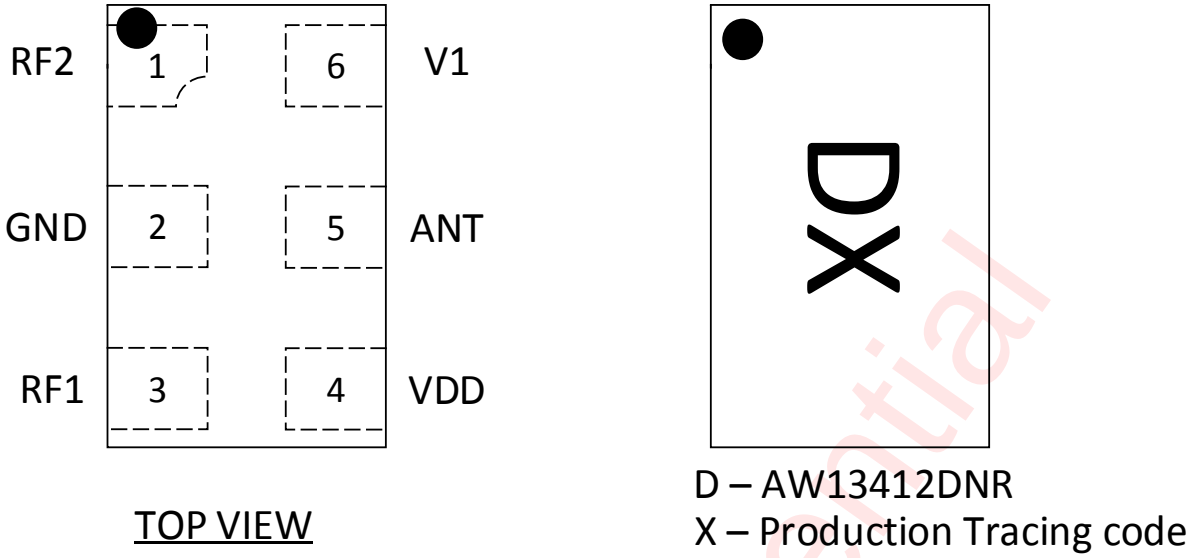


Figure 2 Pin Configuration and Top Mark

PIN DEFINITION

No.	NAME	DESCRIPTION
1	RF2	RF I/O path 2
2	GND	Ground
3	RF1	RF I/O path 1
4	VDD	DC power supply
5	ANT	Antenna port
6	V1	DC control voltage 1

FUNCTIONAL BLOCK DIAGRAM

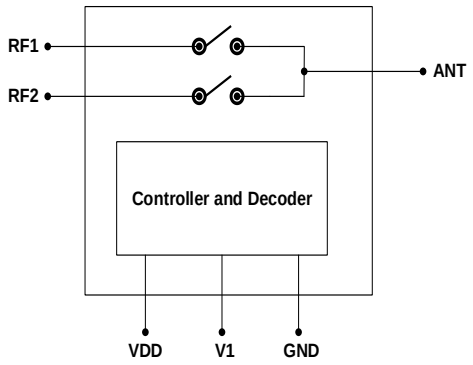


Figure 3 FUNCTIONAL BLOCK DIAGRAM

ORDERING INFORMATION

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW13412DNR	-40°C～85°C	DFN 1.1mmX0.7mm -6L	D	MSL1	ROHS+HF	3000 units/ Tape and Reel

AW13412□□□
Shipping
R:Tape & Reel
Package Type
DN:DFN

ABSOLUTE MAXIMUM RATINGS(NOTE1)

PARAMETERS		RANGE
Supply Voltage Range VDD		1.8V to 3.3V
Control Voltage Range	V1	0V to 3.3V
RF input power(RF1/RF2)		34dBm
Operating Free-air Temperature Range		-40°C to 85°C
Storage Temperature T_{STG}		-65°C to 150°C
Lead Temperature (Soldering 10 Seconds)		260°C
Reflow times		⩾3
ESD (NOTE 2)		
HBM (ANSI/ESDA/JEDEC JS-001-2017)		±1000V
CDM (JEDEC EIA/JESD22-C101F)		±500V
Latch up (JEDEC STANDARD NO.78E SEPTEMBER 2016)		100mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001

ELECTRICAL CHARACTERISTICS

VDD=2.8V, V1=0/1.8V, PIN=0dBm, TOP=+25℃, Z_0=50Ω. (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
DC Specifications						
VDD	Supply Voltage		1.8	2.8	3.1	V
IDD	Supply Current			24		μA
VCTL_H VCTL_L	Control Voltage High Low		1.35 0	1.8	3.3 0.45	V
ICTL	Control Current	VCTL = 1.8V	-1	-0.1		μA
tPUP	Power Up Setting Time	50% of VDD voltage to 90% of final RF power, switching between RF1/2			10	μS
tON	Turn-on Switching Time	50% of final control voltage to 90% of final RF power, switching between RF1/2		0.5	1.2	μS
RF Specifications						

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
IL	Insertion loss(ANT pin to RF1/RF2)	0.06-0.1G 0.1-1.0G 1.0-2.0G 2.0-2.7G 2.7-4.2G		0.24 0.26 0.28 0.35 0.65	0.3 0.4 0.45 0.50	dB dB dB dB dB
ISO	Isolation (ANT pin to RF1/RF2)	0.06-0.1G 0.1-1.0G 1.0-2.0G 2.0-2.7G 2.7-4.2G	37 33 27 23	39 35 31 26 19		dB dB dB dB dB
RL	Input return loss (ANT pin to RF1/RF2)	0.06-0.1G 0.1-1.0G 1.0-2.0G 2.0-2.7G 2.7-4.2G	30 23 20 18	32 27 22 20 11		dB dB dB dB dB
2fo	Second harmonics (ANT pin to RF1/RF2)	PIN=+26dBm, 0.06-4.2GHz		85		dBc
3fo	Third harmonics (ANT pin to RF1/RF2)	PIN=+26dBm, 0.06-4.2GHz		88		dBc
$P_{0.1dB}$	0.1dB Compression Point (ANT pin to RF1/RF2)	0.06GHz–4.2GHz		33		dBm
IIP3	3rd Order Input Intercept Point	@ 2.0GHz, PIN=+26dBm, Δf=1MHz		57		dBm

TIMING DIAGRAM (POWER ON AND OFF SEQUENCE)

It is very important that the user adheres to the correct power-on/off sequence in order to avoid damaging the device. The control signal V1 should be set to 0V unless VDD is set in the operating voltage range.

Power ON:

1) Apply voltage supply --- VDD
2) Set Controls---V1
3) Apply RF input

Change switch position from one RF port to another:

1) Remove RF input
2) Change control voltages V1 to set the switch to desired RF port
3) Apply RF input

Power OFF:

1) Remove RF input
2) Remove control voltages-V1
3) Remove VDD input

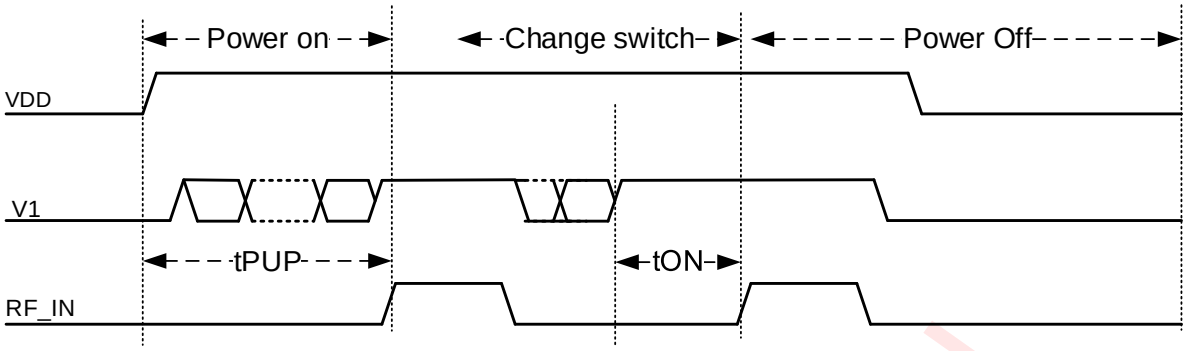


Figure 6 **Power on/Change switch/Power off sequence**

AW13412 CONTROL LOGIC

State	Active Path	V1
0	ANT to RF1	0
1	ANT to RF2	1

APPLICATION CIRCUITS

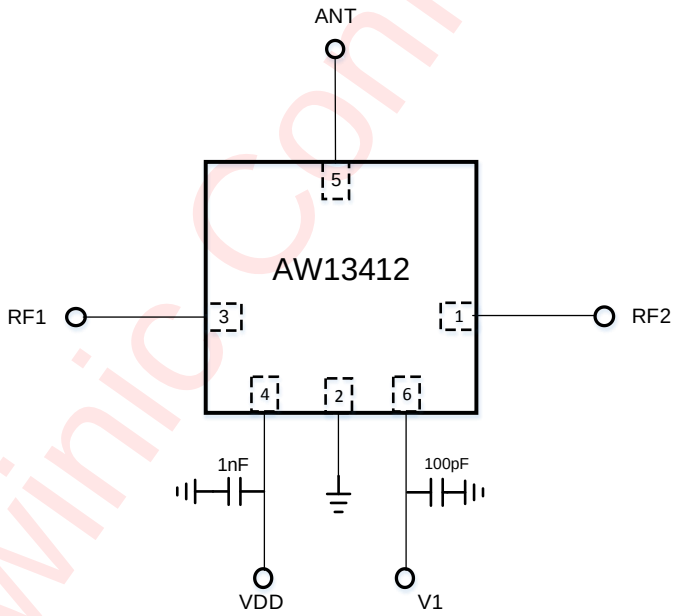


Figure 6 **AW13412 EVB Schematic**

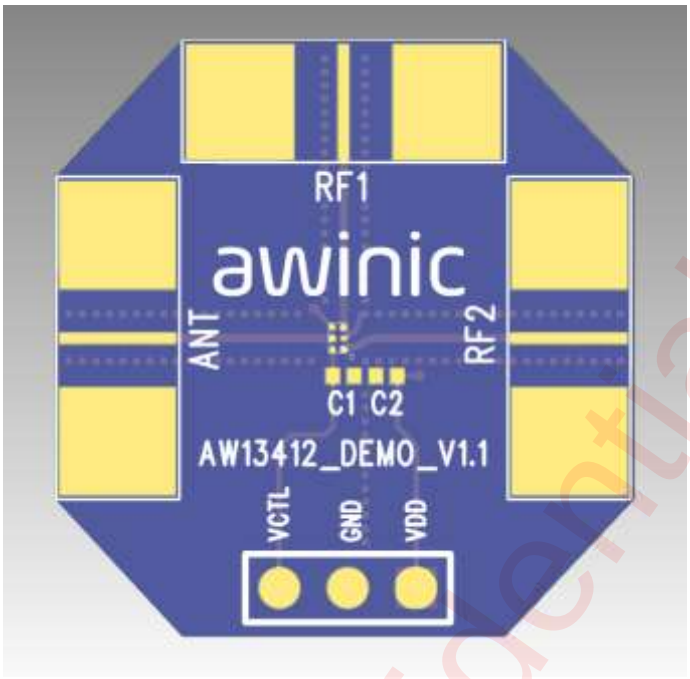
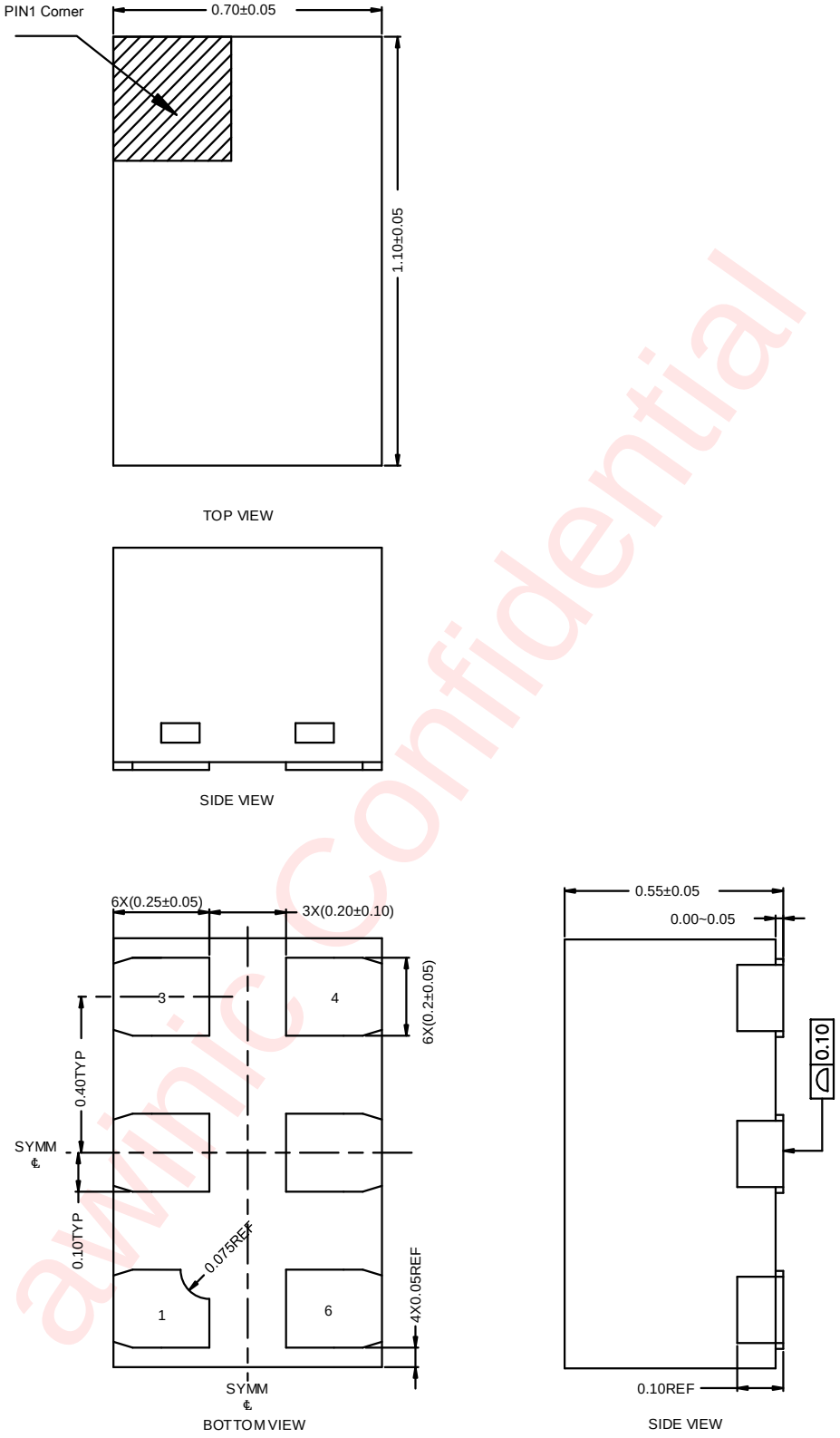


Figure 6 AW13412 EVB

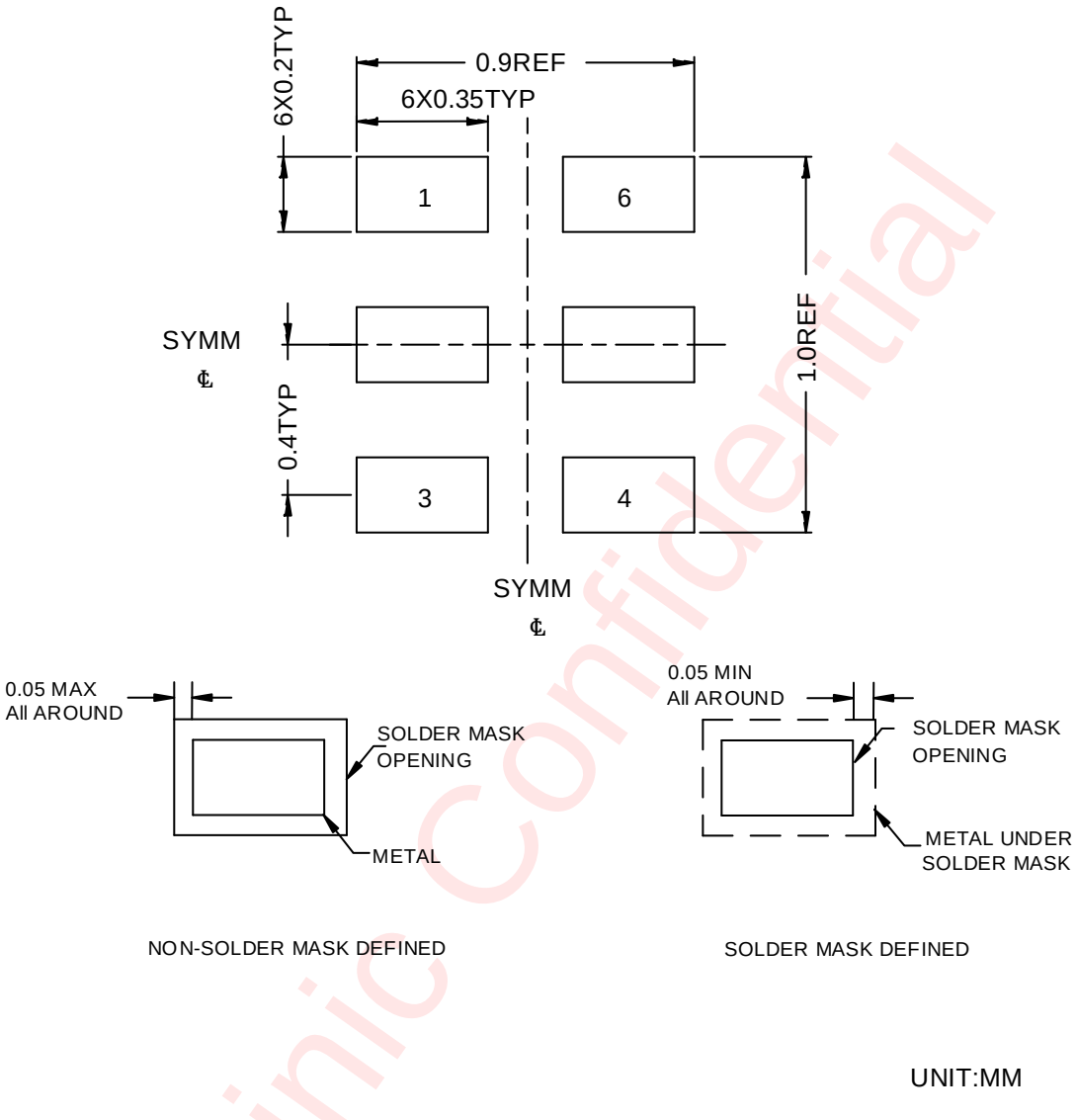
PACKAGE OUTLINE DIMENSIONS



UNIT:MM

Figure 7 Package Outline

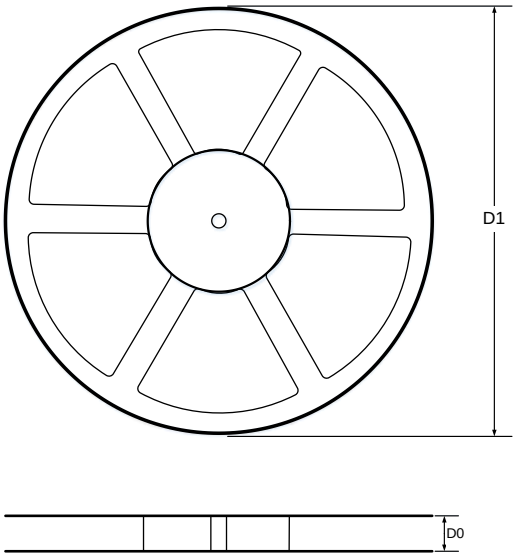
LAND PATTERN DATA



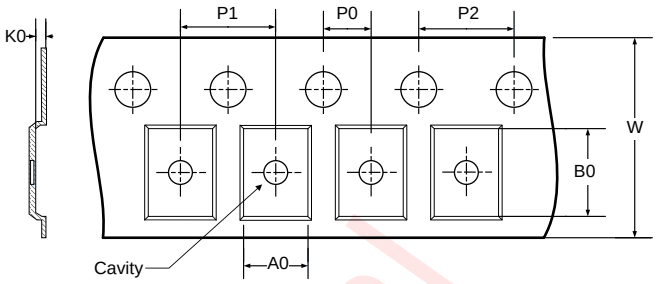
UNIT:MM

TAPE AND REEL INFORMATION

REEL DIMENSIONS

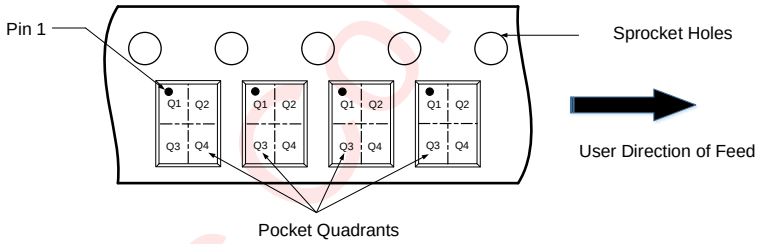


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

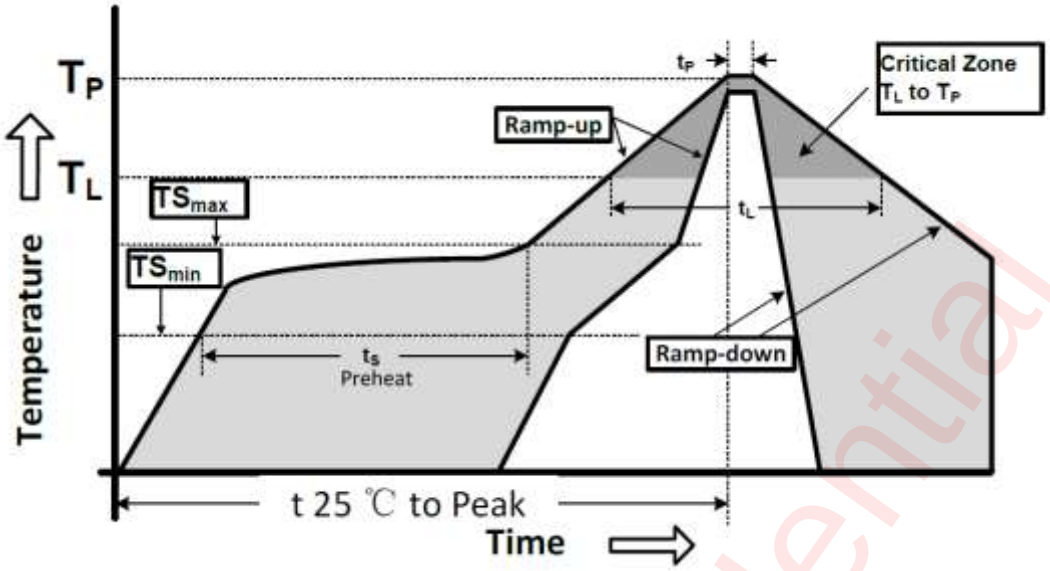


All dimensions are nominal

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.4	0.82	1.22	0.66	2	2	4	8	Q1

Figure 8-1 Tape and Reel

REFLOW



Reflow Note	Spec
Ramp-up rate（TSmax to Tp）	3℃/second max.
Preheat temperature（Tsmin to Tsmax）	150℃ to 200℃
Preheat time（ts）	60 – 180 seconds
Time above TL , 217℃（tL）	60 – 150 seconds
Peak temperature（Tp）	260℃
Time within 5℃ of peak temperature(tp)	20 – 40 seconds
Ramp-down rate	6℃/second max.
Time 25℃ to peak temperature	8 minutes max.

REVISION HISTORY

Vision	Date	Change Record
V1.0	Aug 2017	Officially Released
V1.1	Nov 2017	Change datasheet template
V1.2	Oct 2018	Change: 1. Pin1 marker 2. POD 3. Tape and reel information 4. Typical Application Circuit 5. T_{STG} 6. Latch up
V1.3	Mar 2019	Change the spec IL
V1.4	Mar 2019	1. Change the spec IL and features of IL 2. Change maximum VDD to 3.3 V
V1.5	Jun 2019	1. Change the spec IL and features of IL 2. Change the spec ISO and features of ISO
V1.6	Mar 2020	1. Update 4GHz specification 2. Change the tON and IDD、ICTL specification
V1.7	Jun 2020	1. Change the spec VDD 2. Update the time of application
V1.8	Jun 2020	1. Change the spec VDD
V1.9	Jul 2020	1. Update 60MHz to 100MHz specification 2. Change the spec $P_{0.1dB}$
V2.0	Mar 2021	1. Update to 4.2GHz specification

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