30W, 4.5V to 26V, High efficiency Stereo Class D Audio Amplifier with Low Idle Power Dissipation

Features

- Wide Voltage Range: 4.5V - 26V
- Output Power:
  - BTL mode: 2×30W@8Ω, 24V,THD+N<1%
  - PBTL mode: 1×60W@4Ω, 24V,THD+N<1%
- Low THD+N: 0.03% at 1W, 1kHz input, 8Ω
- 17mA Idle Current in Low-Loss Mode
- Overall efficiency up to 94%
- Multiple switching frequencies
  - AM avoidance
  - Master/Slave synchronization
  - Up to 1.2MHz switching frequency
- Programmable Power Limit
- Support Spread Spectrum to Enhance EMI Performance
- Support parallel BTL Mode and MONO Mode
- Integrated self-protection：over-voltage, under-voltage, over-temperature, DC-detect and short-circuit protection
- ETSSOP 11mm×8.1mm -32L Package

Applications

- Speaker bar、After-market automotive、CRT TV and Consumer Audio Applications

General Description

AW83118 is a stereo efficient, Class-D audio power amplifier for driving speakers up to 60W/4Ω in PBTL mode. It can run 2×30W/8Ω without heat sink on a dual layer PCB. In Low-Loss mode, it consumes a low idle current, allowing for longer audio play and improved thermal performance in Speaker bar and Consumer Audio applications.

The AW83118 advanced oscillator/PLL circuit employs a multiple switching frequency option to avoid AM interferences; this is achieved together with an option of Master/Slave mode, making it possible to synchronize multiple devices.

The AW83118 built-in over-voltage, under-voltage protection, DC protection, thermal protection and short-circuit protection, effectively prevent it from being damaged.

AW83118 is available in ETSSOP 11mm×8.1mm-32L package.

Typical Application Circuit

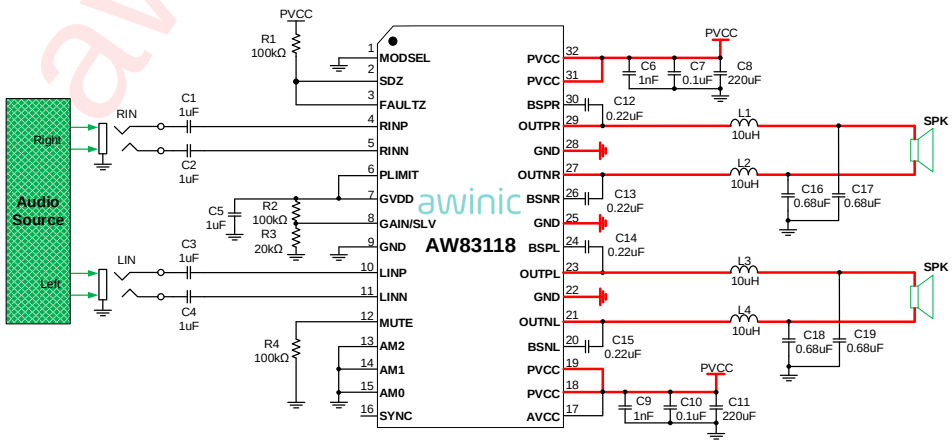
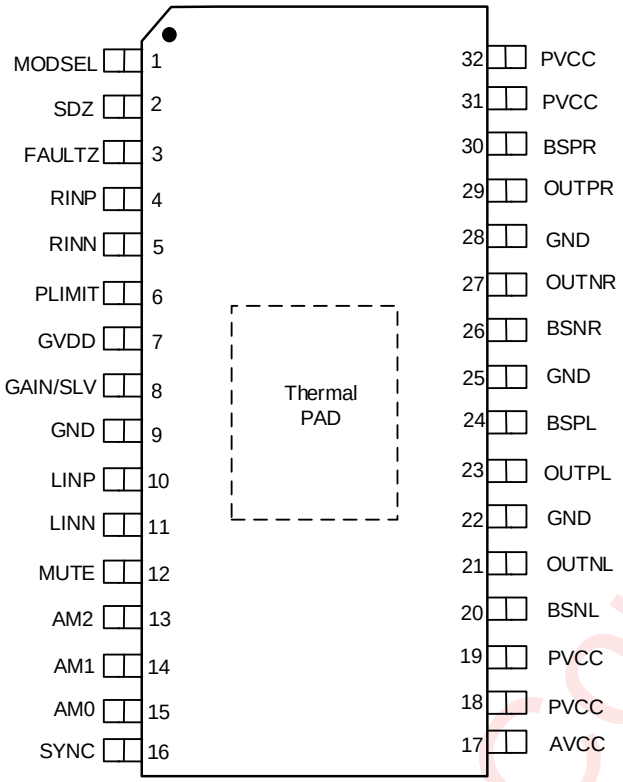


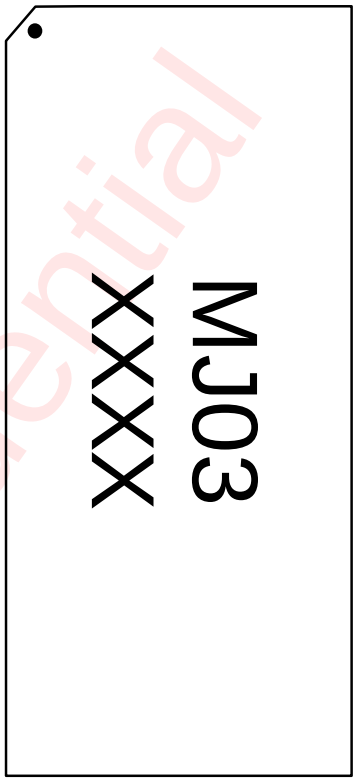
Figure 1 Typical Application Circuit of AW83118

Pin Configuration And Top Mark

AW83118TSR PIN Configuration
(Top View)



AW83118TSR MARKING
(Top View)



MJ03 - AW83118TSR
XXXX - Production Tracing Code

Figure 2 Pin Configuration and Top Mark

Pin Definition

No.	NAME	DESCRIPTION
1	MODSEL	Mode selection logic input (LOW = BD mode, HIGH = Low-Loss mode). TTL logic levels with compliance to PVCC.
2	SDZ	Shutdown logic input for audio amp (LOW = outputs Hi-Z, HIGH = outputs enabled). TTL logic levels with compliance to PVCC.
3	FAULTZ	General fault reporting including Over-temp, DC Detect. Open drain. FAULTZ = High, normal operation, FAULTZ = LOW, fault condition.
4	RINP	Positive audio input for right channel. Biased at 2.75V. Connect to GND for MONO mode.
5	RINN	Negative audio input for right channel. Biased at 2.75V. Connect to GND for MONO mode.
6	PLIMIT	Power limit level control. Connect a resistor divider from GVDD to GND to set power limit. Connect directly to GVDD for no power limit.

7	GVDD	Internally generated FET gate drive supply. Nominal voltage is 5.75V.
8	GAIN/SLV	Selects Gain and selects between Master and Slave mode depending on pin voltage divider.
9	GND	Ground
10	LINP	Positive audio input for left channel. Biased at 2.75V. Connect to GND for PBTL mode.
11	LINN	Negative audio input for left channel. Biased at 2.75V. Connect to GND for PBTL mode.
12	MUTE	Mute signal for fast disable/enable of outputs (HIGH = outputs Hi-Z, LOW = outputs enabled). TTL logic levels with compliance to AVCC.
13	AM2	AM Avoidance Frequency Selection Pin2.
14	AM1	AM Avoidance Frequency Selection Pin1.
15	AM0	AM Avoidance Frequency Selection Pin0.
16	SYNC	Clock input/output for synchronizing multiple class-D devices. Not connect for Master mode.
17	AVCC	Analog supply.
18,19	PVCC	Power supply.
20	BSNL	Bootstrap supply (BST) for left channel output, negative high-side FET.
21	OUTNL	Class-D H-bridge negative output for left channel.
22	GND	Power Ground.
23	OUTPL	Class-D H-bridge positive output for left channel.
24	BSPL	Bootstrap supply (BST) for left channel output, positive high-side FET.
25	GND	Power Ground.
26	BSNR	Bootstrap supply (BST) for right channel output, negative high-side FET.
27	OUTNR	Class-D H-bridge negative output for right channel.
28	GND	Power Ground.
29	OUTPR	Class-D H-bridge positive output for right channel.
30	BSPR	Bootstrap supply (BST) for right channel output, positive high-side FET.
31,32	PVCC	Power supply

Functional Block Diagram

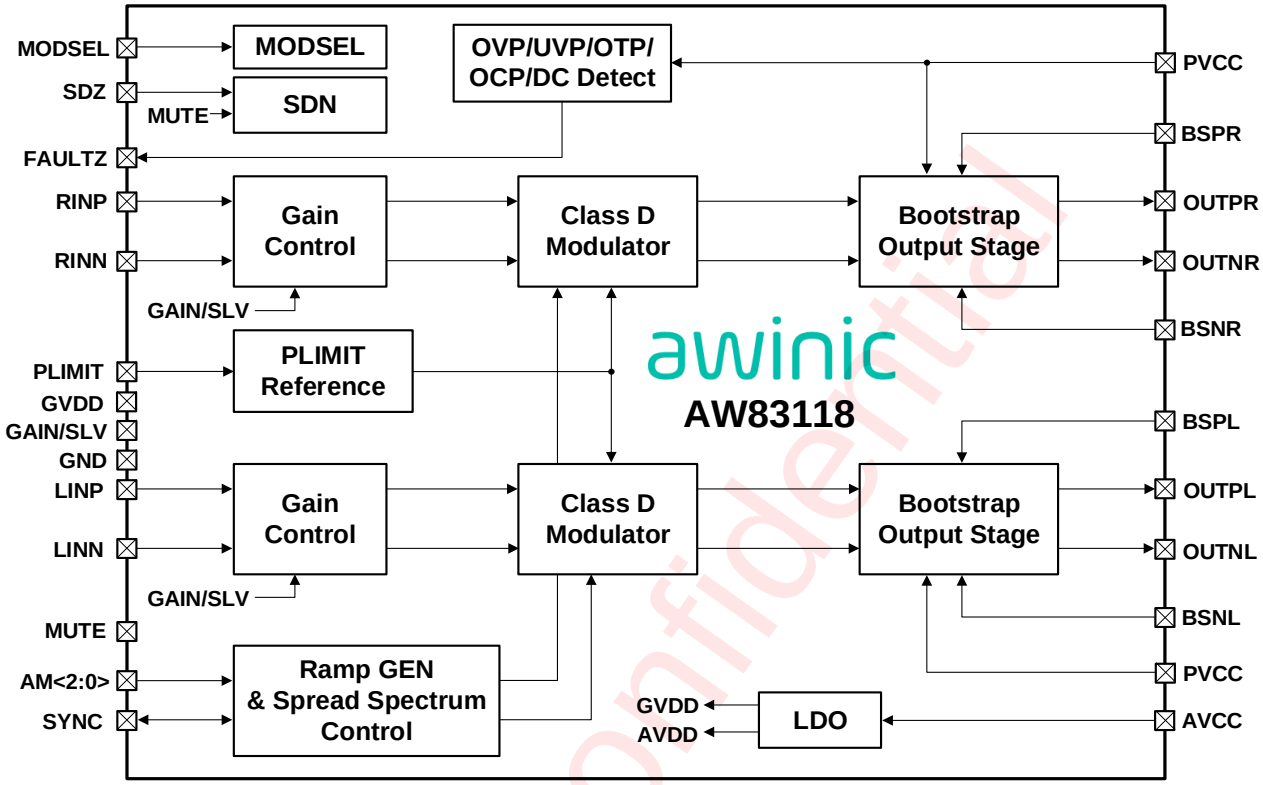


Figure 3 AW83118 Functional Diagram

Typical Application Circuits

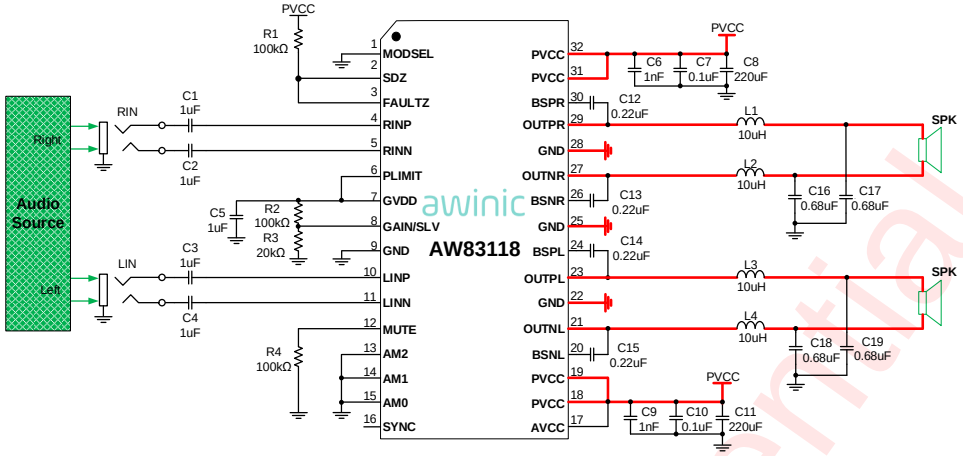


Figure 4 AW83118 Typical Application Diagram

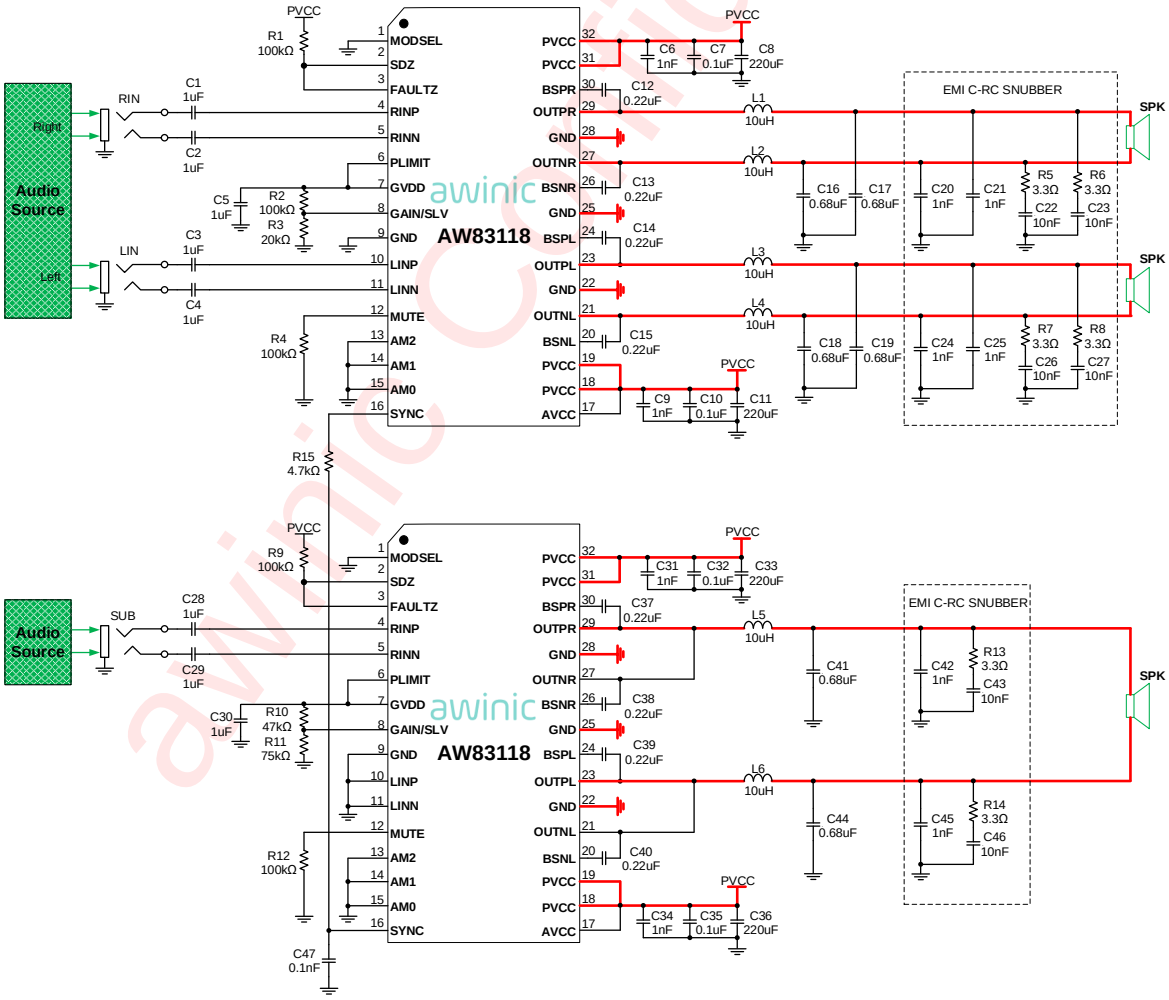


Figure 5 AW83118 2.1 Master and Slave Application Diagram

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW83118TSR	-40°C～85°C	ETSSOP 11mmX8.1mm -32L	MJ03	MSL3	ROHS+HF	2500 units/ Tape and Reel

Absolute Maximum Ratings(NOTE1)

PARAMETERS		RANGE
Supply voltage range	PVCC, AVCC	-0.3V to 30V
Input voltage range	RINP, RINN, LINP, LINN	-0.3V to 6V
	PLIMIT, GAIN/SLV, SYNC	-0.3V to GVDD+0.3V
	AM0, AM1, AM2, MUTE, SDZ, MODSEL	-0.3V to PVCC+0.3V
Output voltage range	FAULTZ	-0.3V to PVCC+0.3V
	GVDD, OUTNL, OUTPL, OUTNR, OUTPR	-0.3V to PVCC+0.3V
Junction-to-ambient thermal resistance θ_{JA}		20.34°C /W
Junction-to-board characterization parameter θ_{JB}		8.23°C /W
Junction-to-top characterization parameter θ_{JC}		10.76°C /W
Operating free-air temperature range		-40°C to 85°C
Maximum operating junction temperature T_{JMAX}		165°C
Storage temperature T_{STG}		-65°C to 150°C
Lead temperature (soldering 10 seconds)		260°C
ESD(Including CDM HBM MM)(NOTE 2)		
PVCC PIN HBM		±2kV
Other PIN HBM		±2kV
CDM		±1.5kV
Latch-up		
Test condition: JESD78E		+IT：200mA -IT：-200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001

Electrical Characteristics

AVCC=PVCC=12V to 24V, RL=4Ω, T_A=25°C for general test condition (unless otherwise noted)

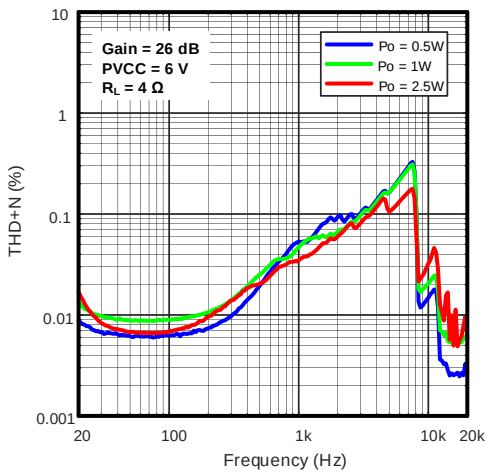
PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage	PVCC, AVCC	4.5		26	V
V_{IH}	High-level input voltage	AM0,AM1,AM2,MUTE,SDZ,MODSEL,SYNC	2			V
V_{IL}	Low-level input voltage	AM0,AM1,AM2,MUTE,SDZ,MODSEL,SYNC			0.8	V
V_{OL}	Low-level output voltage	FAULTZ, $R_{PULL-UP}$=100kΩ, PVCC=26V			0.8	V
I_{IH}	High-level input current	AM0, AM1, AM2, MUTE, SDZ,MODSEL(V_I=2V, PVCC=18V)			5	μA
R_L(BTL)	Minimum load impedance	Output filter: L=10μH, C=680nF	3.2	4		Ω
R_L(PBTL)		Output filter: L=10μH, C=1μF	1.6	2		Ω
L_O	Output-filter inductance	Minimum output filter inductance under short-circuit condition	2			μH
DC						
|V_{OS}|	Class-D output offset voltage (measured differentially)	VI=0V, Gain=35dB			30	mV
I_{CC}	Quiescent supply current	SDZ=2V, No load or filter, PVCC=12V		17		mA
		SDZ=2V, No load or filter, PVCC=24V		23		
$I_{CC(SD)}$	Quiescent supply current in shutdown mode	SDZ=0.8V, No load or filter, PVCC=12V		20		μA
		SDZ=0.8V, No load or filter, PVCC=24V		30		
$r_{DS(on)}$	Drain-source on-state resistance, measured pin to pin	PVCC=21V, I_{out}=500mA, T_J=25°C		110		mΩ
G	Gain (BTL)	R1=5.6kΩ, R2=Open	18.5	20	21.5	dB
		R1=20kΩ, R2=100kΩ	23.5	25	26.5	
		R1=39kΩ, R2=100kΩ	29.5	31	32.5	
		R1=47kΩ, R2=75kΩ	33.5	35	36.5	
	Gain (SLV)	R1=51kΩ, R2=51kΩ	18.5	20	21.5	
		R1=75kΩ, R2=47kΩ	23.5	25	26.5	
		R1=100kΩ, R2=39kΩ	29.5	31	32.5	
		R1=100kΩ, R2=16kΩ	33.5	35	36.5	
t_{on}	Turn-on time	SDZ=2V		40		ms

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
t_{off}	Turn-off time	SDZ=0.8V		2		μs
GVDD	Gate drive supply	I_{GVDD}<200μA	5.4	5.75	6.6	V
V_O	Output voltage maximum under PLIMIT control	V_{PLIMIT}=2V, V_I=1Vrms	8.5	10	11.5	V
AC						
PSRR	Power supply ripple rejection	200mVpp ripple at 1kHz，Gain=20dB，Inputs AC-coupled to GND		70		dB
P_O (BTL)	Continuous output power	THD+N=10%, f=1kHz, PVCC=15V, R_L =4Ω		25.5		W
		THD+N=10%, f=1kHz, PVCC=21V, R_L =4Ω		53.5		
P_O(PBTL)	Continuous output power(note1)	THD+N=1%, f=1kHz, PVCC=24V, R_L =2Ω		112		W
THD+N	Total harmonic distortion + noise	VCC=21V, f=1kHz, PO=25W		0.05%		
Vn	Output integrated noise	20-20kHz, A-weighted filter, Gain=20dB		65		μV
				-84		dBV
	Crosstalk	V_O=1Vrms, Gain=20dB, f=1kHz		-100		dB
SNR	Signal-to-noise ratio	THD+N<1%, f=1kHz, Gain=20dB, A-weighted		102		dB
f_{OSC}	Oscillator frequency	AM2=0, AM1=0, AM0=0		400		kHz
		AM2=0, AM1=0, AM0=1		500		
		AM2=0, AM1=1, AM0=0		600		
		AM2=0, AM1=1, AM0=1		1000		
		AM2=1, AM1=0, AM0=0		1200		
		AM2=1, AM1=0, AM0=1		300		
		AM2=1, AM1=1, AM0=0, Spread Spectrum Range=12%, Central Modulation Frequency		500		
		AM2=1, AM1=1, AM0=1	Reserved			
T_{OT}	Thermal trip point			160		°C
$T_{OT, hys}$	Thermal hysteresis			25		°C
I_{OC}	Over current trip point			9.5		A

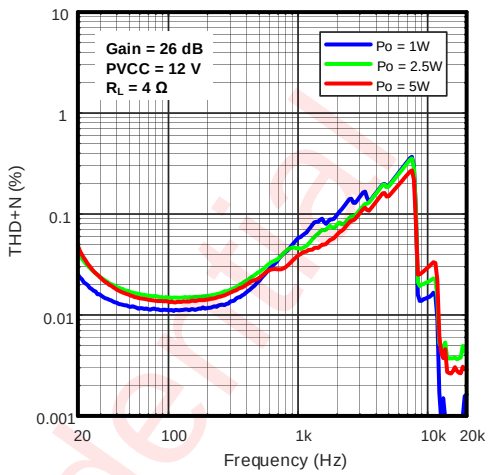
Note1: Heat dissipation treatment is required to test without OT

Typical Characteristics

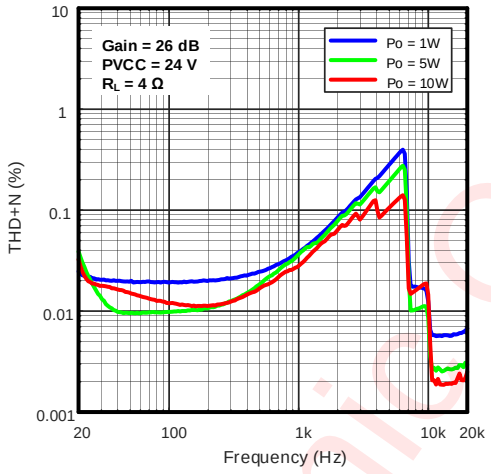
fosc=400kHz, BD Mode, T_A=25°C (unless otherwise noted).



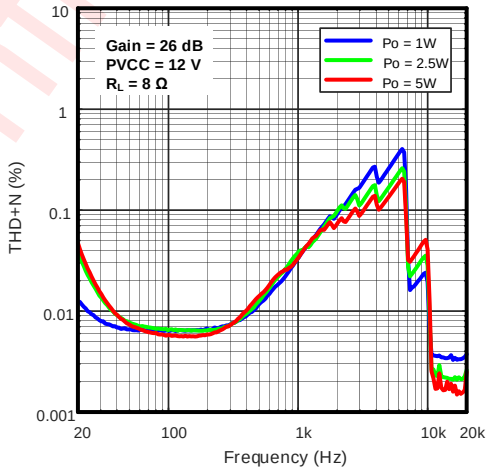
THD+N (BTL) vs Frequency



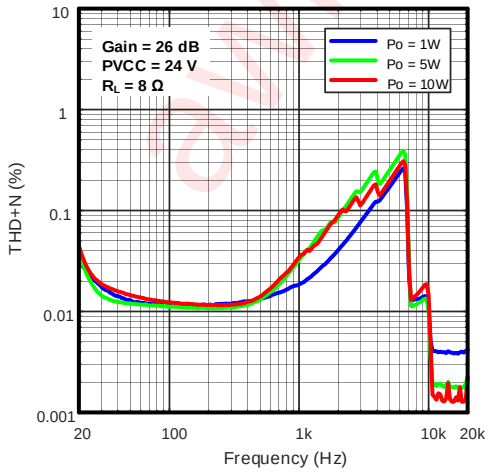
THD+N (BTL) vs Frequency



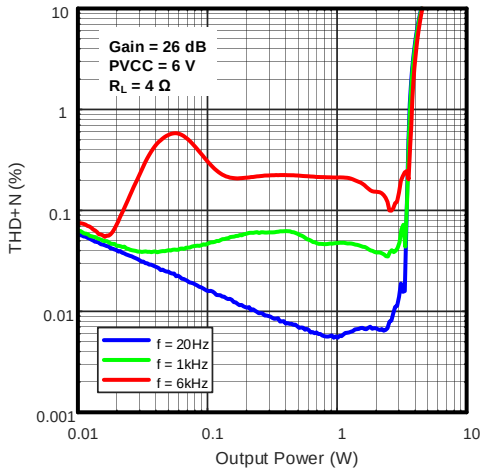
THD+N (BTL) vs Frequency



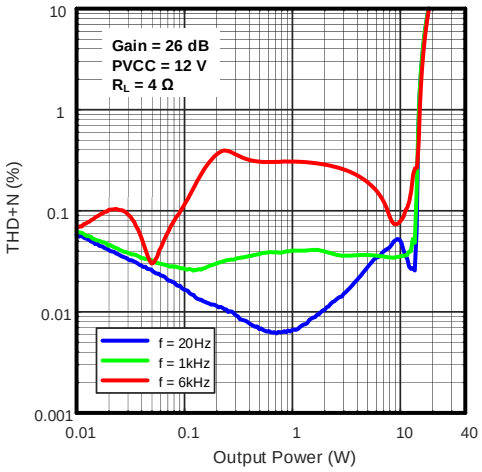
THD+N (BTL) vs Frequency



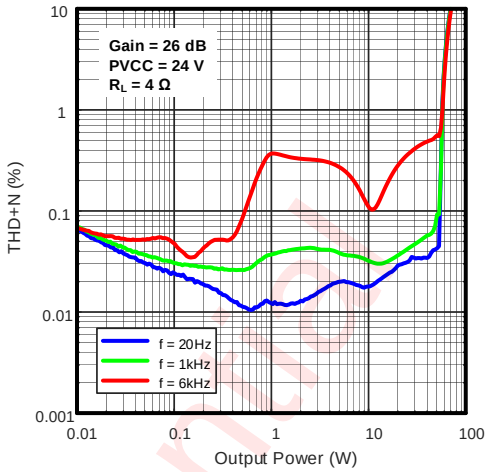
THD+N (BTL) vs Frequency



THD+N (BTL) vs Po



THD+N (BTL) vs Po



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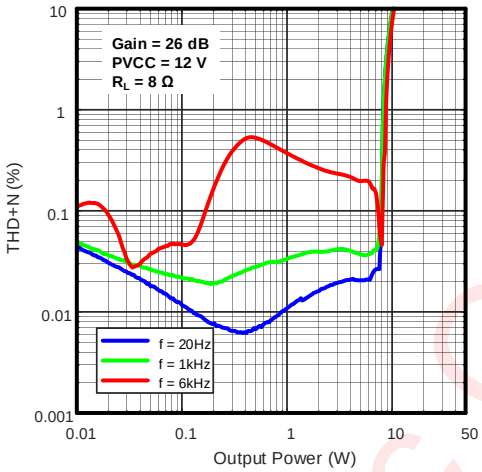

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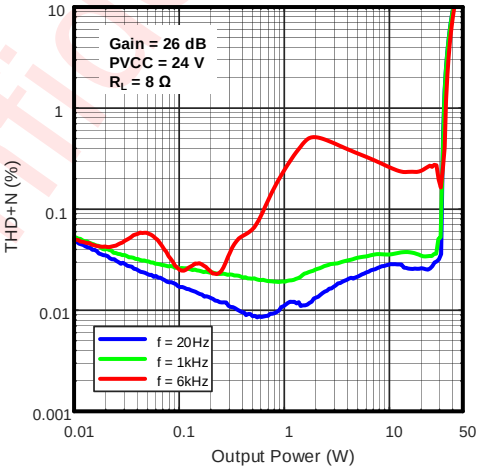
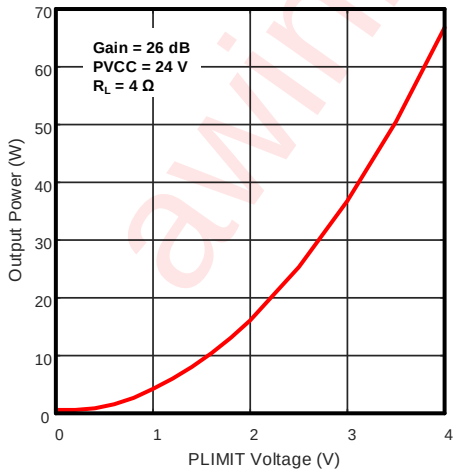
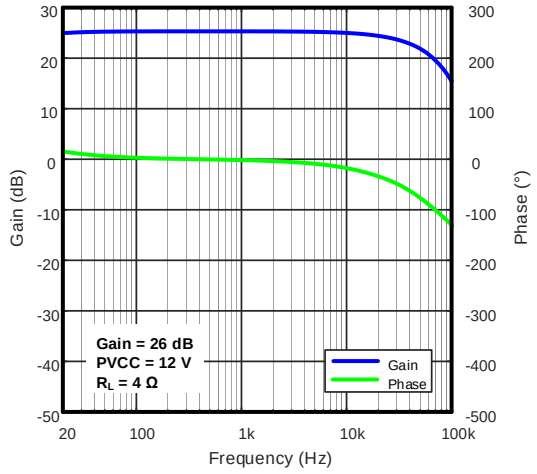


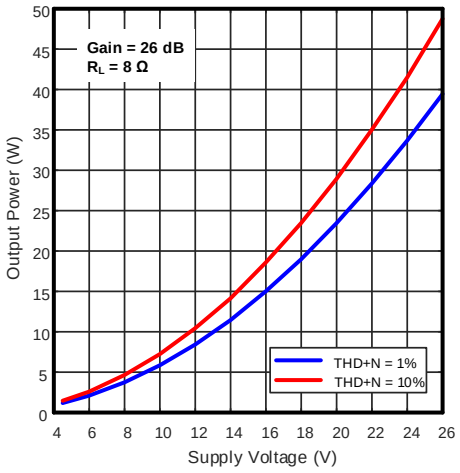
THD+N (BTL) vs Po



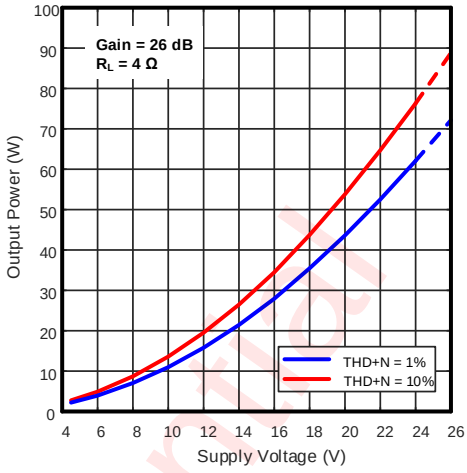
Po (BTL) vs PLIMIT Voltage



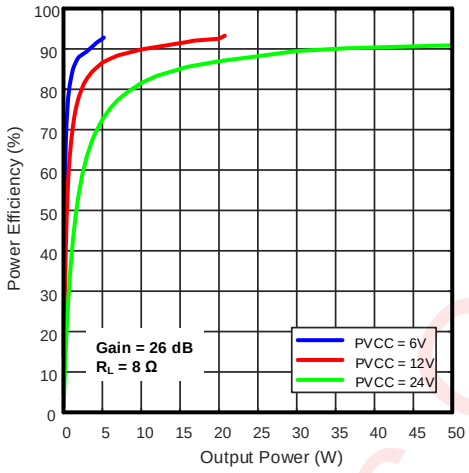
Gain/Phase (BTL) vs Frequency



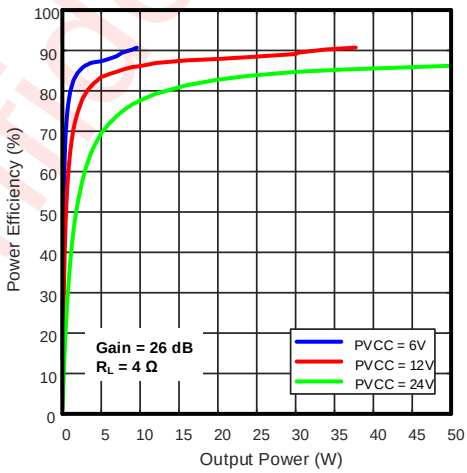
Po (BTL) vs Supply Voltage



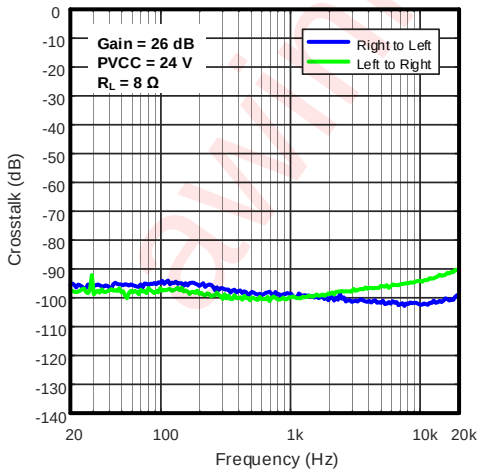
Po (BTL) vs Supply Voltage



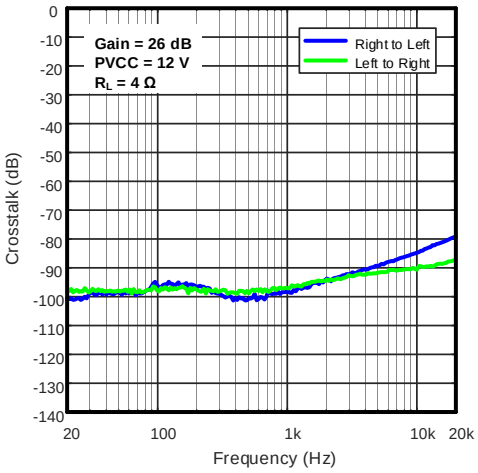
Efficiency (BTL) vs Po



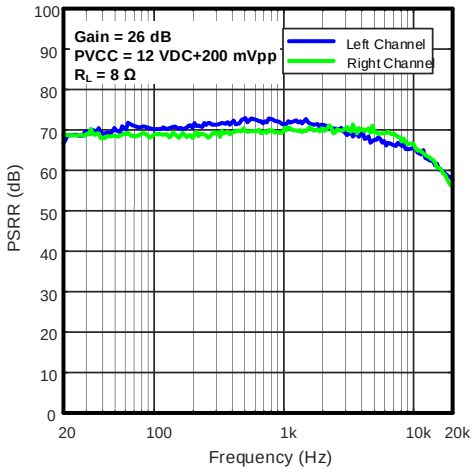
Efficiency (BTL) vs Po



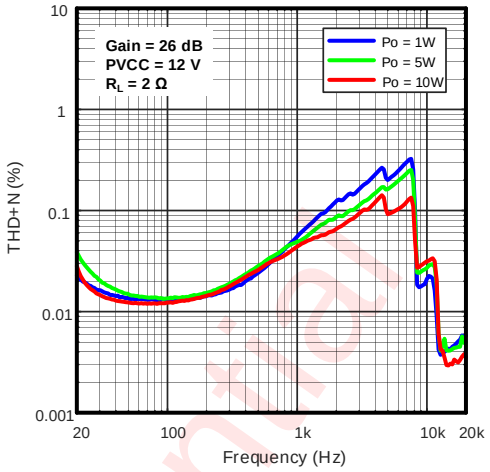
Crosstalk (BTL) vs Frequency



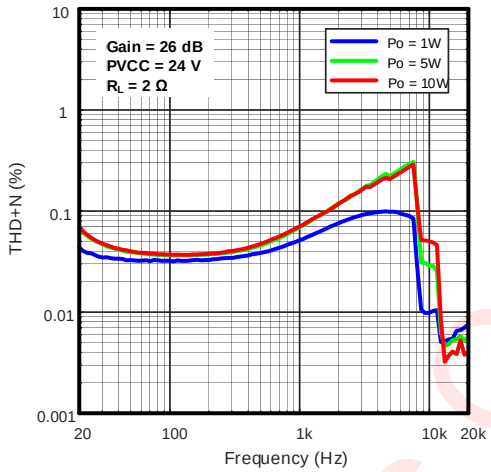
Crosstalk (BTL) vs Frequency



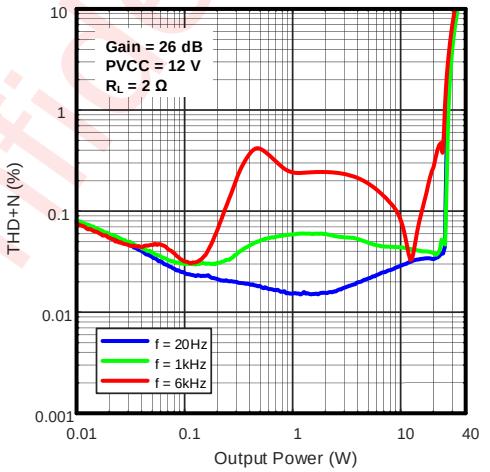
PSRR (BTL) vs Frequency



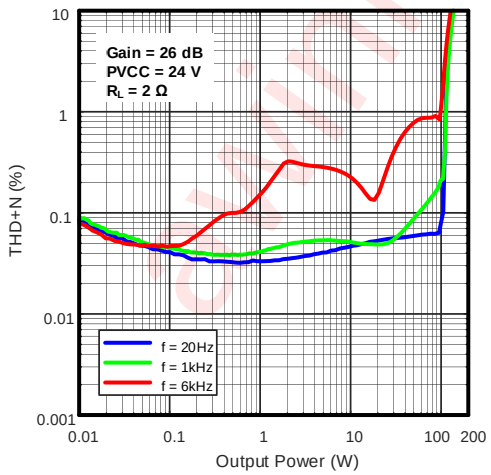
THD+N (PBTL) vs Frequency



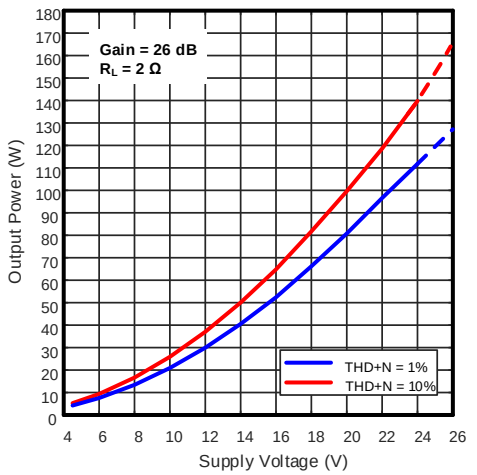
THD+N (PBTL) vs Frequency



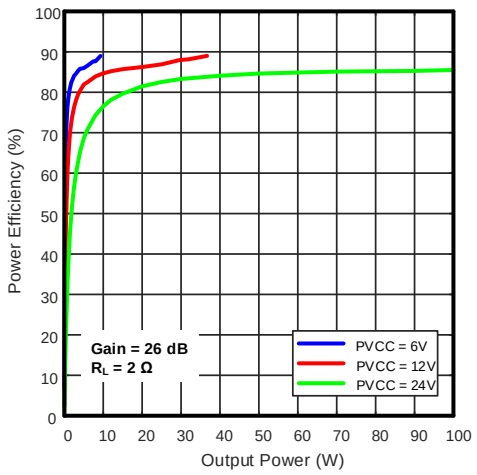
THD+N (PBTL) vs Po



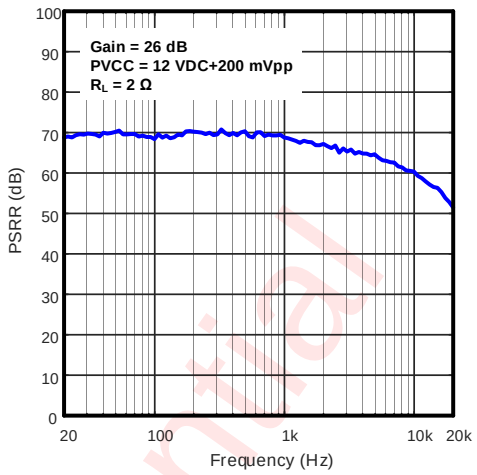
THD+N (PBTL) vs Po



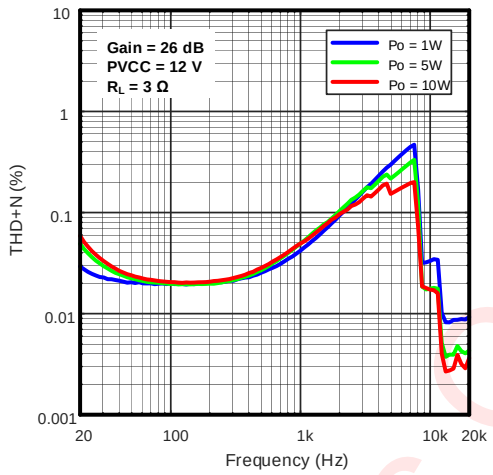
Po (PBTL) vs Supply Voltage



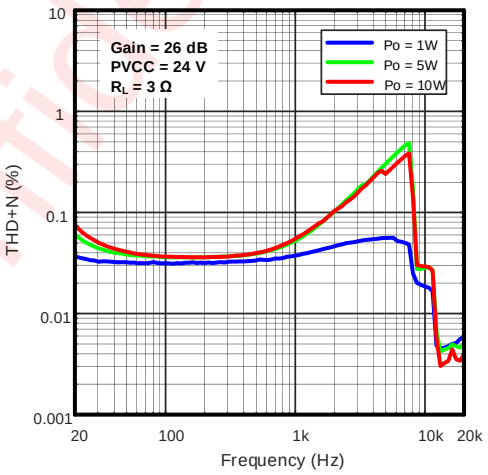
Efficiency (PBTL) vs Po



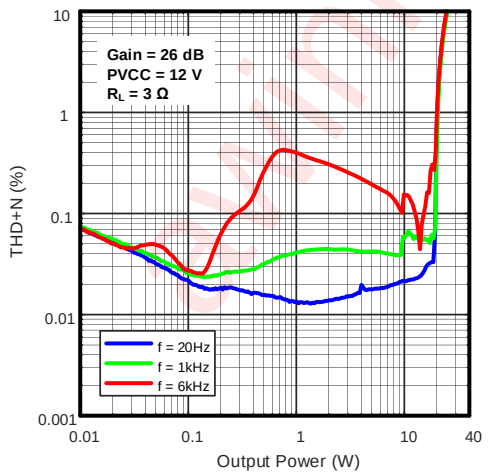
PSRR (PBTL) vs Frequency



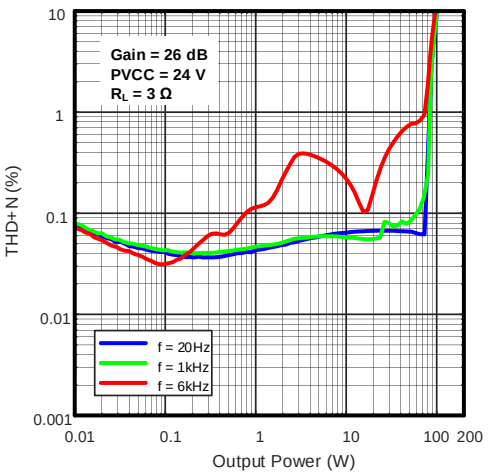
THD+N (PBTL) vs Frequency



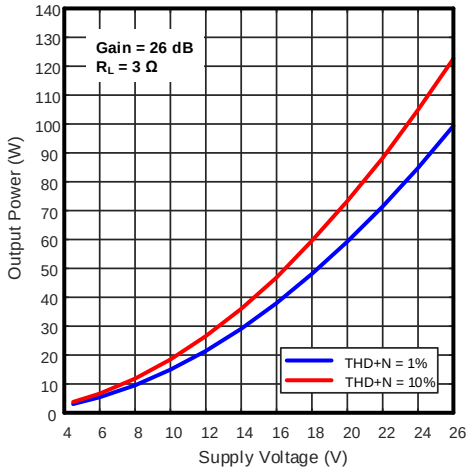
THD+N (PBTL) vs Frequency



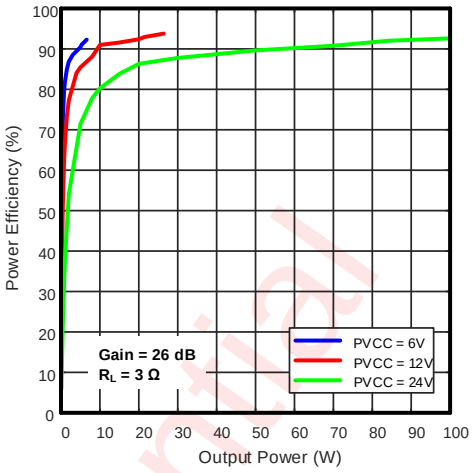
THD+N (PBTL) vs Po



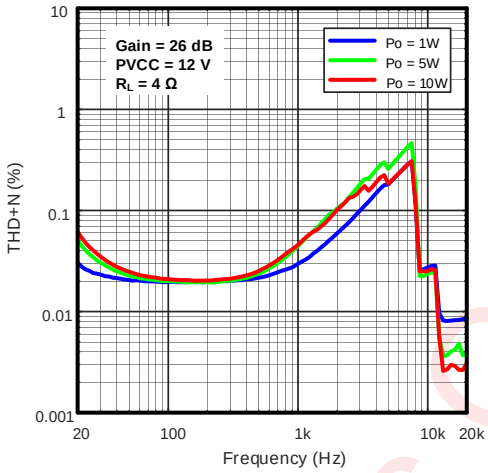
THD+N (PBTL) vs Po



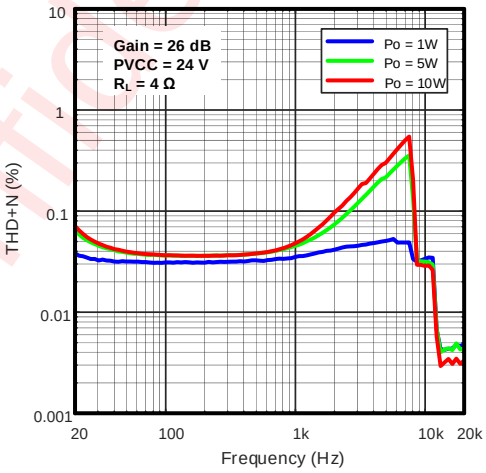
Po (PBTL) vs Supply Voltage



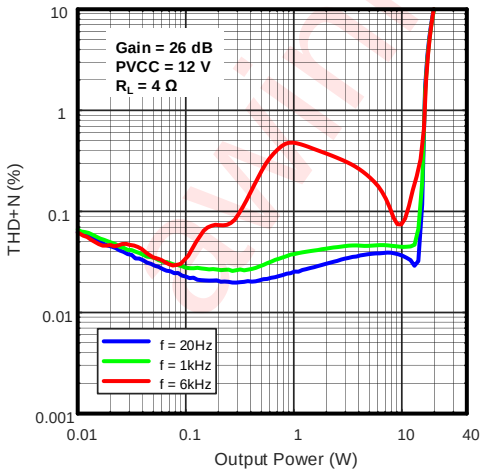
Efficiency (PBTL) vs Po



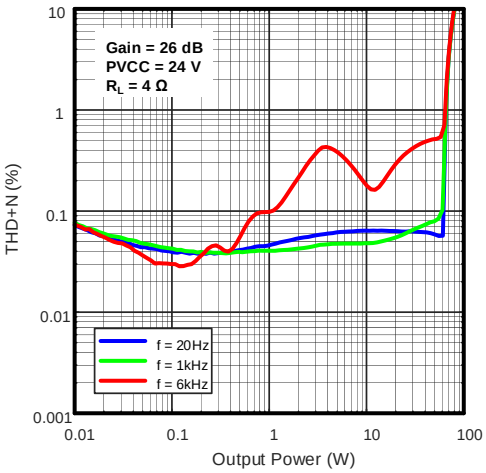
THD+N (PBTL) vs Frequency



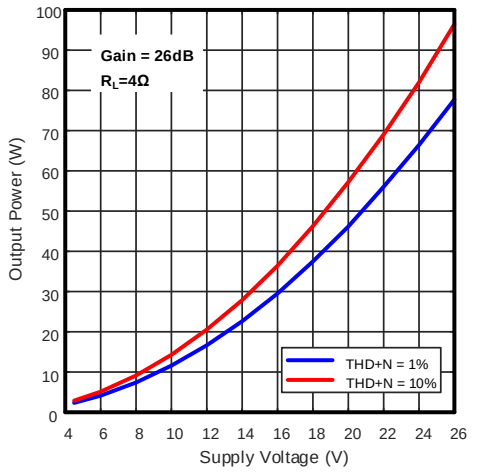
THD+N (PBTL) vs Frequency



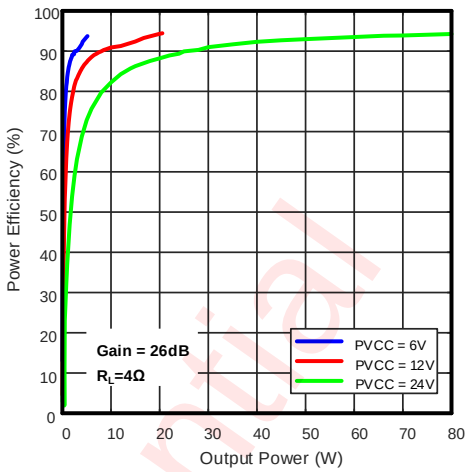
THD+N (PBTL) vs Po



THD+N (PBTL) vs Po



Po (PBTL) vs Supply Voltage



Efficiency (PBTL) vs Po

Note: Dashed lines represent thermally limited region for the continuous output power.

Detailed Functional Description

The AW83118 device is a highly efficient and highly integrated Class D audio amplifier. The amplifier is designed for driving 60W/4Ω speakers in PBTL mode, and driving 2×30W/8Ω speakers in dual channel BTL mode under 4.5~26V PVCC supply voltage.

Gain Setting and Master/Slave Mode

The gain of the AW83118 is set by the voltage divider connected to the GAIN/SLV control pin. Master or Slave mode is also controlled by the same pin. An internal ADC is used to detect the 8 input states. The first four stages sets the GAIN in Master mode in gains of 20, 25, 31, 35 dB respectively, while the next four stages sets the GAIN in Slave mode in gains of 20, 25, 31, 35 dB respectively. The gain setting is latched during power-up and cannot be changed while device is powered. Table 1 lists the recommended resistor values and the state and gain:

Table 1 Gain and Master/Slave

MASTER / SLAVE MODE	GAIN	R1(to GND)(1)	R2(to GVDD)(1)	INPUT IMPEDANCE
Master	20 dB	5.6 kΩ	OPEN	60 kΩ
Master	25 dB	20 kΩ	100 kΩ	30 kΩ
Master	31 dB	39 kΩ	100 kΩ	15 kΩ
Master	35 dB	47 kΩ	75 kΩ	9 kΩ
Slave	20 dB	51 kΩ	51 kΩ	60 kΩ
Slave	25 dB	75 kΩ	47 kΩ	30 kΩ
Slave	31 dB	100 kΩ	39 kΩ	15 kΩ
Slave	35 dB	100 kΩ	16 kΩ	9 kΩ

(1) Resistor tolerance should be 5% or better.

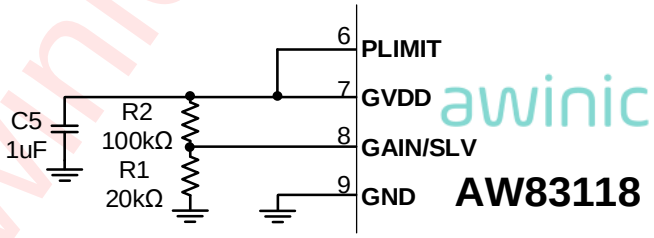


Figure 6 Gain, Master/Slave

In Master mode, SYNC terminal is an output, in Slave mode, SYNC terminal is an input for a clock input. TTL logic levels with compliance to GVDD. If SYNC terminal is provided by an external platform as a clock input in Slave mode, it must be given before SDZ goes high level voltage.

Startup and Shutdown Operation

The AW83118 employs a shutdown mode of operation designed to reduce supply current (Icc) to the absolute minimum level during periods of nonuse for power conservation. The SDZ input terminal should be held high during normal operation when the amplifier is in use. Pulling SDZ low will put the outputs to mute and the amplifier to enter a low-current state. It is not recommended to leave SDZ unconnected, because amplifier operation would be unpredictable.

For the best power-off pop performance, place the amplifier in the shutdown mode prior to removing the power supply. The gain setting is selected at the end of the start-up cycle. At the end of the start-up cycle, the gain is selected and cannot be changed until the next power-up.

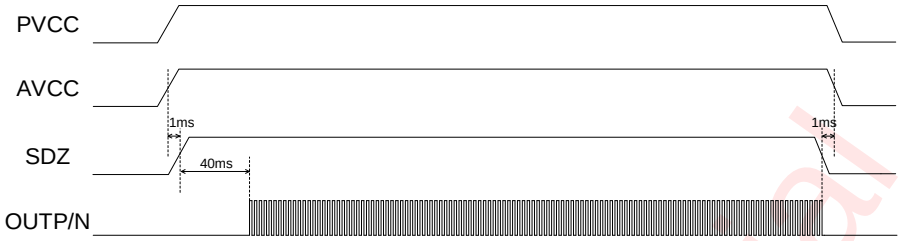


Figure 7 Startup and shutdown Sequence

Differential Inputs

The differential input stage of the amplifier cancels any noise that appears on both input lines of the channel. To use the AW83118 with a differential source, connect the positive lead of the audio source to the RINP or LINP input and the negative lead from the audio source to the RINN or LINN input. To use the AW83118 with a single-ended source, ac ground the negative input through a capacitor equal in value to the input capacitor on positive and apply the audio source to either input. In a single-ended input application, the unused input should be ac grounded at the audio source instead of at the device input for best noise performance. For good transient performance, the impedance seen at each of the two differential inputs should be the same.

The impedance seen at the inputs should be limited to an RC time constant of 1 ms or less if possible. This is to allow the input dc blocking capacitors to become completely charged during the 10 ms power-up time. If the input capacitors are not allowed to completely charge, there will be some additional sensitivity to component matching which can result in pop if the input components are not well matched.

Device Protection System

The AW83118 contains a complete set of protection circuits carefully designed to make system design efficient as well as to protect the device against any kind of permanent failures due to short circuits, overload, over temperature, and under-voltage. The FAULTZ pin will signal if an error is detected according to Table 2:

Table 2 Fault Reporting

FAULT	TRIGGERING CONDITION (typical value)	FAULTZ	ACTION	SELF-CLEARING/ LATCHED
Under Voltage on PVCC	PVCC < 4.1V	-	Output high impedance	Self-clearing
Over Voltage on PVCC	PVCC > 29V	-	Output high impedance	Self-clearing
Over Current	Output short or short to PVCC or GND	Low	Output high impedance	Latched
Over Temperature	T_j> 160℃	Low	Output high impedance	Latched
Too High DC Offset	DC output voltage	Low	Output high impedance	Latched

Short-Circuit Protection and Automatic Recovery Feature

The AW83118 has protection from over current conditions caused by a short circuit on the output stage. The short circuit protection fault is reported on the FAULTZ pin as a low state. The amplifier outputs are switched to a high impedance state when the short circuit protection latch is engaged. The latch can be cleared by cycling the SDZ pin through the low state.

If automatic recovery from the short circuit protection latch is desired, connected the FAULTZ pin directly to the SDZ pin. This allows the FAULTZ pin function to automatically drive the SDZ pin low which clears the short circuit protection latch.

In systems where a possibility of a permanent short from the output to PVCC or to a high voltage battery like a car battery can occur, pull the MUTE pin low with the FAULTZ signal with a inverting transistor to ensure a high-Z restart, like shown in the figure below.

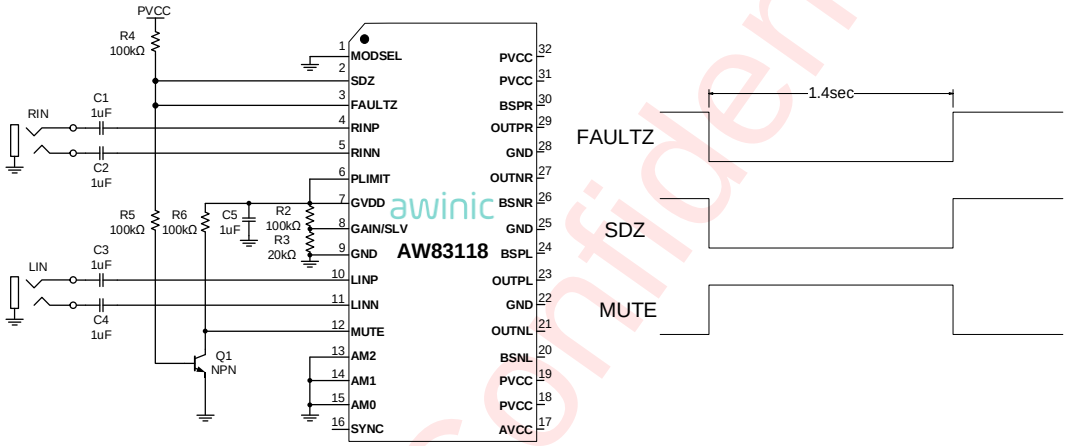


Figure 8 MUTE Driven by Inverted FAULTZ and Timing Requirement for SDZ

Thermal Protection

Thermal protection on the AW83118 prevents damage to the device when the internal die temperature exceeds 160°C. There is a ±15°C tolerance on this trip point from device to device. Once the die temperature exceeds the thermal trip point, the device enters into the shutdown state and the outputs are disabled. This is a latched fault.

Thermal protection faults are reported on the FAULTZ terminal as a low state.

If automatic recovery from the thermal protection latch is desired, connect the FAULTZ pin directly to the SDZ pin. This allows the FAULTZ pin function to automatically drive the SDZ pin low which clears the thermal protection latch.

DC Detect Protection

The AW83118 has circuitry which will protect the speakers from DC current which might occur due to defective capacitors on the input or shorts on the printed circuit board at the inputs. A DC detect fault will be reported on the FAULT pin as a low state. The DC Detect fault will also cause the amplifier to shutdown by changing the state of the outputs to Hi-Z.

If automatic recovery from the DC Detect protection latch is desired, connect the FAULTZ pin directly to the SDZ pin. This allows the FAULTZ pin function to automatically drive the SDZ pin low which clears the DC Detect protection latch.

A DC Detect Fault is issued when the output differential duty-cycle of either channel exceeds 63% for more than 625 msec at the same polarity. Table 3 below shows some examples of the typical DC Detect Protection

threshold for several values of the supply voltage. This feature protects the speaker from large DC currents or AC currents less than 2Hz. To avoid nuisance faults due to the DC detect circuit, hold the SDZ pin low at power up until the signals at the inputs are stable. Also, take care to match the impedance seen at the positive and negative inputs to avoid nuisance DC detect faults.

Table 3 lists the minimum output offset voltage required to trigger the DC detect. The outputs must remain at or above the voltage listed in the table for more than 625 msec to trigger the DC detect.

Table 3 DC Detect Threshold

PVCC(V)	VOS-OUTPUT OFFSET VOLTAGE（V）
4.5	1.17
6	1.56
12	3.12
18	4.68

PLIMIT Operation

The AW83118 has a built-in voltage limiter that can be used to limit the output voltage level below the supply rail, the amplifier simply operates as if it was powered by a lower supply voltage, and thereby limits the output power. Add a resistor divider from GVDD to ground to set the voltage at the PLIMIT pin. An external reference may also be used if tighter tolerance is required. Add a 1μF capacitor from pin PLIMIT to ground to ensure stability.

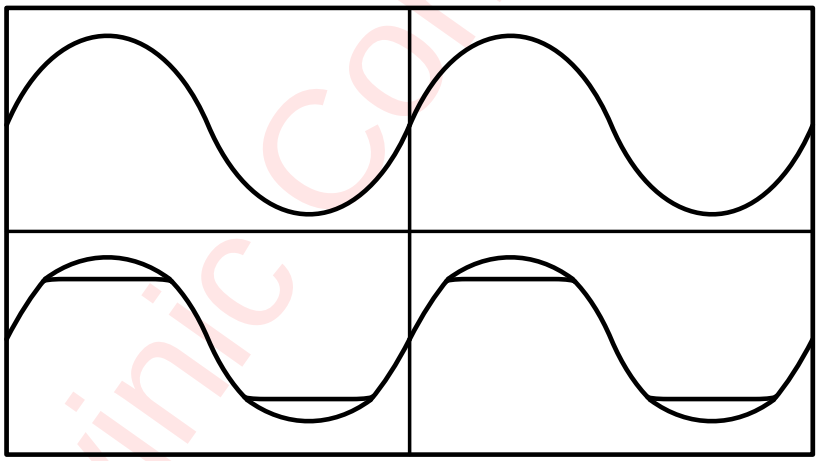


Figure 9 Power Limit Example

The PLIMIT circuit sets a limit on the output peak-to-peak voltage. The limiting is done by limiting the duty cycle to a fixed maximum value. This limit can be thought of as a “virtual” voltage rail which is lower than the supply connected to PVCC. This “virtual” rail is approximately 5 times the voltage at the PLIMIT pin. This output voltage can be used to calculate the maximum output power for a given maximum input voltage and speaker impedance.

$$P_{OUT}\ (unclipped\ ) = \frac{((\frac{R_L}{R_L + 2 * R_S}) * V_P)^2}{2 * R_L}$$

where

R_L is the load resistance.

R_S is the total series resistance including $R_{DS(on)}$, and output filter resistance.

V_P is the peak amplitude, V_P = 5 × PLIMIT voltage.

Table 4 Power Limit Voltage

PVCC (V)	PLIMIT VOLTAGE (V)(1)	R to GND	R to GVDD	OUTPUT VOLTAGE (V_{rms})
12	1.2	18 kΩ	68 kΩ	5.79
12	1.84	24 kΩ	51 kΩ	8.62
12	GVDD	Open	Short	10.31
24	2	24 kΩ	45 kΩ	8.83
24	2.7	45 kΩ	51 kΩ	11.75
24	GVDD	Open	Short	17.36

(1) PLIMIT measurements taken with EVM gain set to 25dB and input voltage set to $1V_{rms}$.

Device Modulation Scheme

The AW83118 has the option of running in either BD modulation or Low-Loss modulation; this is set by the MODSEL pin.

MODSEL=0: BD modulation

This is a modulation scheme that allows operation without the classic LC reconstruction filter when the amp is driving an inductive load with short speaker wires. Each output is switching from 0V to the supply voltage. The OUTP and OUTN are in phase with each other with no input so that there is little or no current in the speaker. The duty cycle of OUTP is greater than 50% and OUTN is less than 50% for positive output voltages. The duty cycle of OUTP is less than 50% and OUTN is greater than 50% for negative output voltages. The voltage across the load sits at 0V throughout most of the switch period, reducing the switching current, which reduces any I^2R losses in the load.

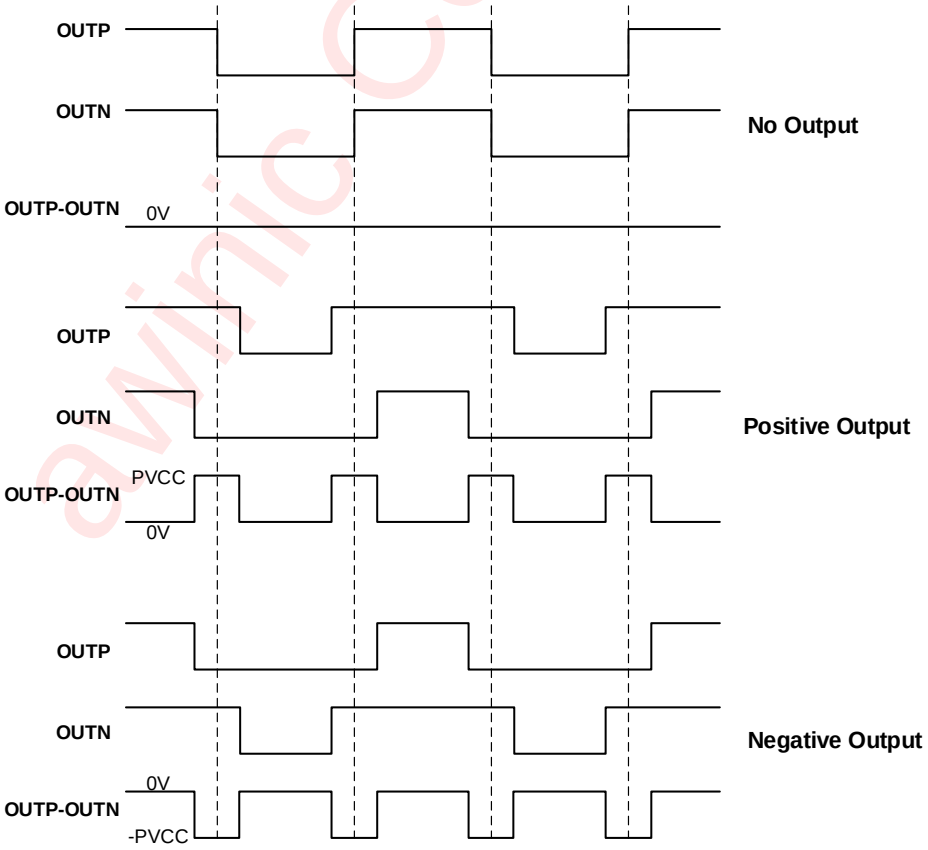


Figure 10 BD Mode Modulation

MODSEL=1: Low-Loss modulation

The Low-Loss mode alters the normal modulation scheme in order to achieve higher efficiency with a slight penalty in THD degradation and more attention required in the output filter selection. In Low-Loss mode the outputs operate at 20% modulation during idle conditions. When an audio signal is applied one output will decrease and one will increase. The decreasing output signal will quickly rail to GND at which point all the audio modulation takes place through the rising output. The result is that only one output is switching during a majority of the audio cycle. Efficiency is improved in this mode due to the reduction of switching losses. The THD penalty in Low-Loss mode is minimized by the high performance feedback loop. The resulting audio signal at each half output has a discontinuity each time the output rails to GND. This can cause ringing in the audio reconstruction filter unless care is taken in the selection of the filter components and type of filter used.

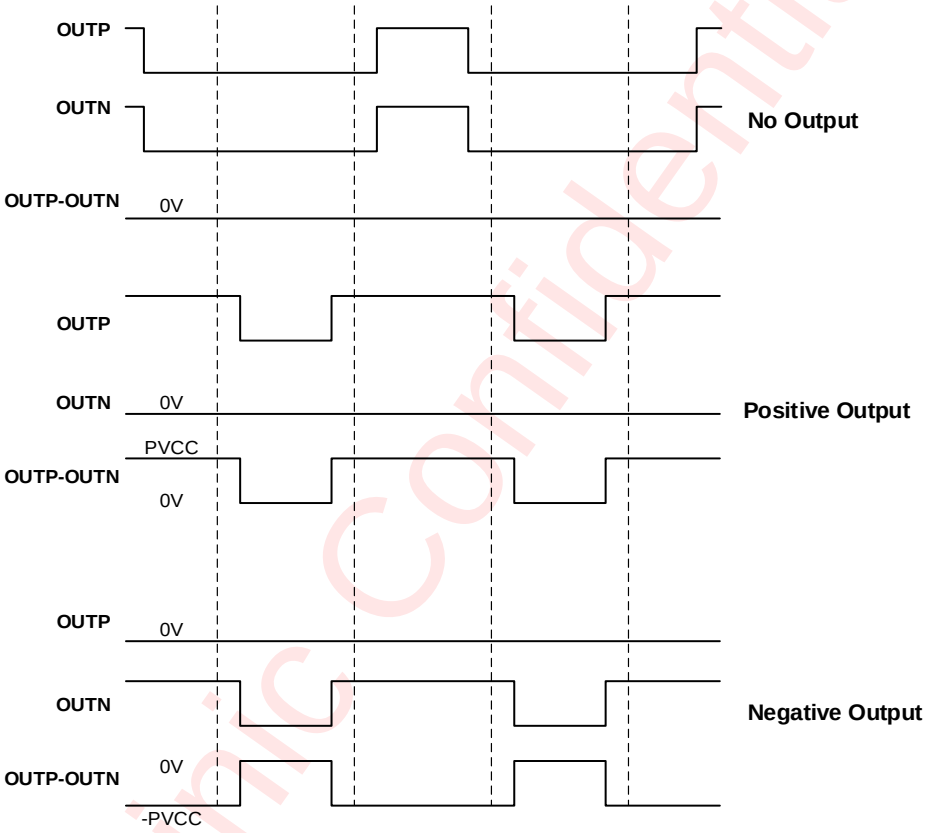


Figure 11 Low-Loss Mode Modulation

AM Avoidance EMI Reduction

To reduce interference in the AM radio band, the AW83118 has the ability to change the modulation frequency via AM<2:0> pins. The recommended frequencies are listed in Table 5. The fundamental frequency and its second harmonic straddle the AM radio band listed. This eliminates the tones that can be present due to the modulation frequency being demodulated by the AM radio.

Table 5 AM Frequencies

US	EUROPEAN	Modulation Frequency(kHz)	AM2	AM1	AM0
AM Frequency(kHz)	AM Frequency(kHz)				
	522-540	300	1	0	1
540-917	540-914	1200	1	0	0
917-1125	914-1122	600	0	1	0

US	EUROPEAN	Modulation Frequency(kHz)	AM2	AM1	AM0
AM Frequency(kHz)	AM Frequency(kHz)				
1125-1375	1122-1373	1000	0	1	1
1375-1547	1373-1548	1000	0	1	1
1547-1700	1548-1701	1000	0	1	1

Spread Spectrum

The recommended frequencies are listed in Table 6. AM<2:0>=000~101, the modulation frequency is 300~1200kHz. AM<2:0>=110, the AW83118 supports spread spectrum(1) control of the modulation frequency to improve EMI performance, the central modulation frequency is 500kHz, spread spectrum range is 12%; AM<2:0>=111, it is reserved.

Table 6 Modulation Frequencies

AM2	AM1	AM0	Modulation Frequency(kHz)
0	0	0	400
0	0	1	500
0	1	0	600
0	1	1	1000
1	0	0	1200
1	0	1	300
1	1	0	500±12%(1)
1	1	1	Reserved

(1) It is noted that Slave Mode does not supported spread spectrum control the modulation frequency.

Output spectrums of the AW83118 is different whether or enable spread spectrum by configure AM<2:0>. Figure 12 is output spectrum of AM<2:0>=001(fsw=500kHz), and Figure 13 is output spectrum when AM<2:0>=110, fsw=500kHz±12%.

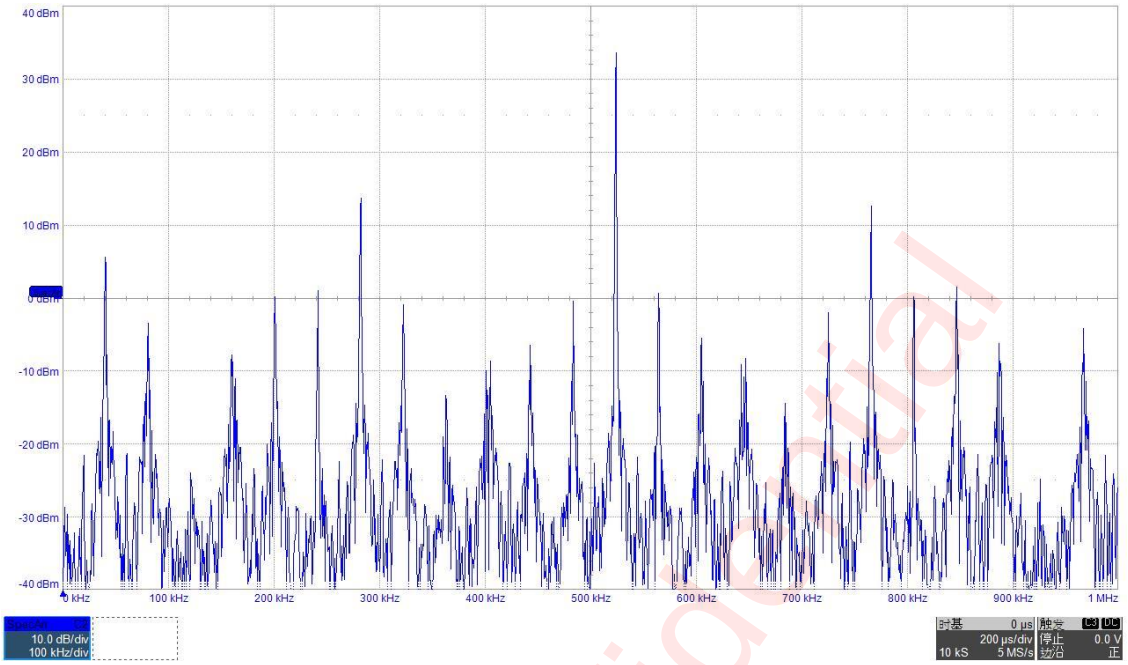


Figure 12 AM<2:0>=001, fsw=500kHz, Output spectrum of the AW83118

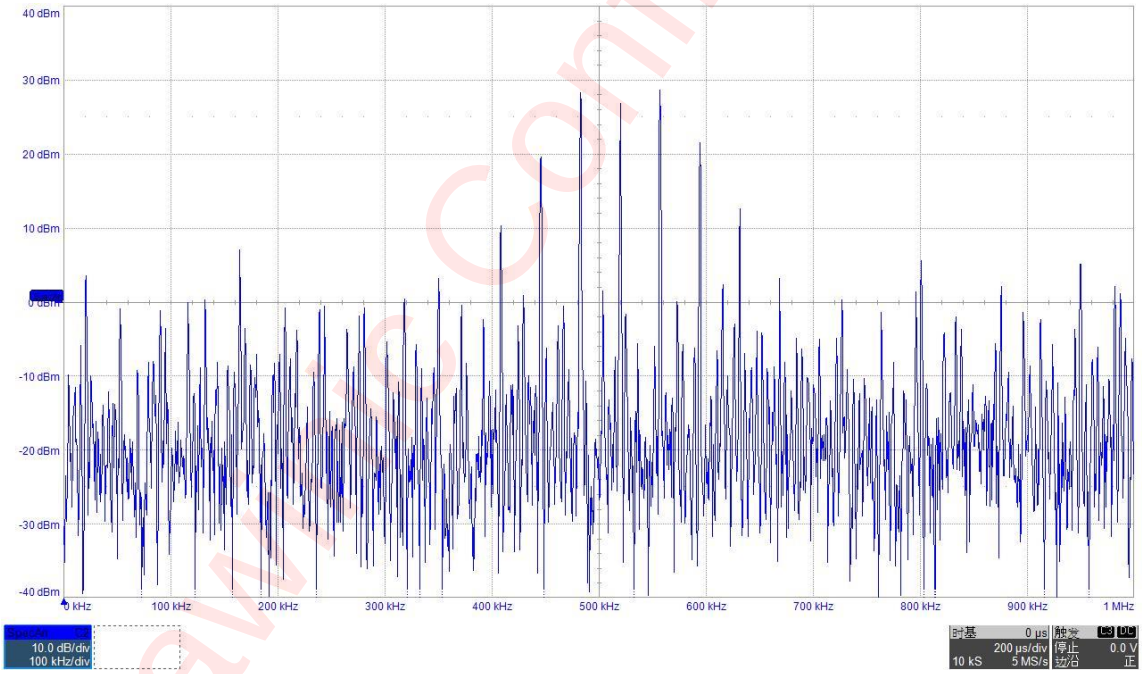


Figure 13 AM<2:0>=110, fsw=500kHz±12%, Output spectrum of the AW83118

(1) It is noted that Slave Mode does not supported spread spectrum control the modulation frequency.

PBTL Mode

The AW83118 can be connected in PBTL mode enabling up to 100W output power. This is done by:

1) Connect INPL and INNL directly to Ground (without capacitors) this sets the device in PBTL mode during power up.

2) Analog input signal is applied to INPR and INNR.

3) Connect OUTPR and OUTNR together for the positive speaker terminal and OUTNL and OUTPL together for negative pin.

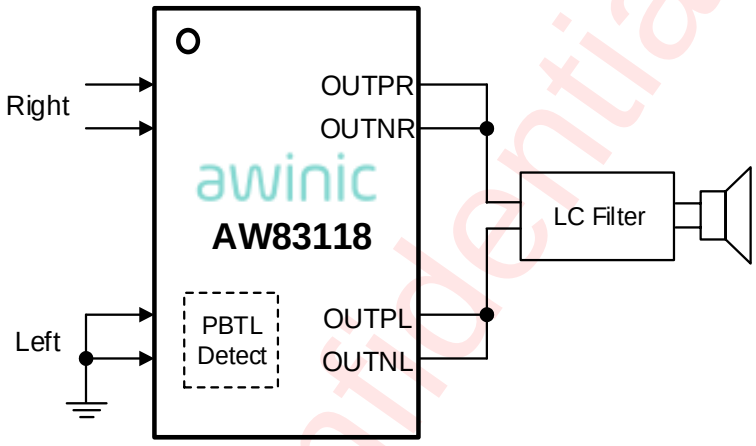


Figure 14 PBTL Mode

MONO Mode

The AW83118 can be connected in MONO mode to cut the idle power-loss nearly by half. This is done by:

1) Connect INPR and INNR directly to Ground (without capacitors) this sets the device in MONO mode during power up.

2) Analog input signal is applied to INPL and INNL.

3) Connect OUTPL and OUTNL to speaker just like normal BTL mode.

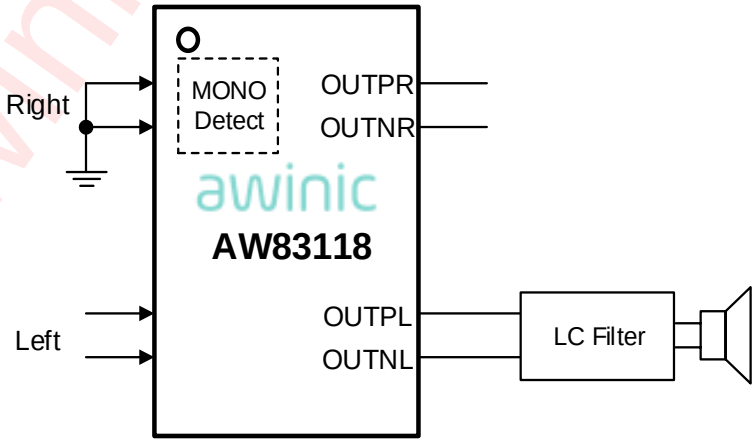


Figure 15 MONO Mode

Application Information

Capacitors Selection

Input Capacitor (input high-pass cutoff frequency)

The AW83118 input stage is a fully differential input stage and the input impedance changes with the gain setting from 9 kΩ at 35 dB gain to 60 kΩ at 20 dB gain. Table 7 lists the values from min to max gain. The tolerance of the input resistor value is ±20% so the minimum value will be higher than 7.2 kΩ. The inputs need to be AC-coupled to minimize the output dc-offset and ensure correct ramping of the output voltages during power-ON and power-OFF. The input ac-coupling capacitor together with the input impedance forms a high-pass filter with the following cur-off frequency:

$$f = \frac{1}{2\pi Z_i C_i}$$

If a flat bass response is required down to 20 Hz the recommended cut-off frequency is a tenth of that, 2 Hz. Table 7 lists the recommended ac-couplings capacitors for each gain step. If a -3 dB is accepted at 20 Hz 10 times lower capacitors can used.

Table 7 Recommended Input AC-Coupling Capacitors

GAIN	INPUT IMPEDANCE	INPUT CAPACITANCE	HIGH-PASS FILTER
20 dB	60 kΩ	1.5 μF	1.8 Hz
25 dB	30 kΩ	3.3 μF	1.6 Hz
31 dB	15 kΩ	5.6 μF	1.9 Hz
35 dB	9 kΩ	10 μF	1.8 Hz

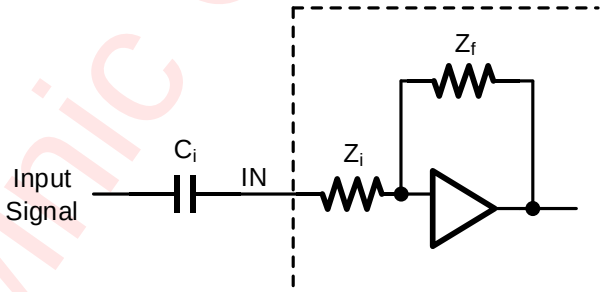


Figure 16 Input Capacitor and Impedance

The input capacitors used should be a type with low leakage, like quality electrolytic, tantalum or ceramic. If a polarized type is used the positive connection should face the input pins which are biased to 3 Vdc.

GVDD Decoupling Capacitor

The GVDD supply is used to power the gates of the output full bridge transistors. It can also be used to supply the PLIMIT and GAIN/SLV voltage dividers. AW83118 advises to decouple GVDD with a X5R ceramic 1μF capacitor to GND. The GVDD supply is not intended to be used for external supply. It is recommended to limit the current consumption by using resistor voltage dividers for GAIN/SLV and PLIMIT of 100 kΩ or more.

Supply Decoupling Capacitor

Good quality decoupling capacitors can improve the efficiency and the best performance of the power amplifier. At the same time, in order to get good high frequency transient performance in a high-speed switching application, the ESR value of the capacitor should be as small as possible. In AW83118 applications, low ESR (equivalent-series-resistance) X5R or better ratings ceramic capacitors are recommended. Consider temperature, ripple current, and voltage overshoots when selecting decoupling capacitors. Also, these decoupling capacitors should be located near the PVCC and GND connections to the device in order to minimize series inductances. Select the bulk capacitors at the PVCC for proper voltage margin and adequate capacitance to support the requirements. In practice, with a well-designed power supply, two 220μF, 50V capacitors should be sufficient. One capacitor should be placed near the PVCC at each side of the device.

Bootstrap Capacitor

The full H-bridge output stages use only NMOS transistors. Therefore, they require bootstrap capacitors for the high side of each output to turn on correctly. A 220nF, 25V ceramic capacitor of quality X5R or better, must be connected from each output to its corresponding bootstrap input. The bootstrap capacitors connected between the BSxx pins and corresponding output function as a floating power supply for the high-side N-channel power MOSFET gate drive circuitry. During each high-side switching cycle, the bootstrap capacitors hold the gate-to-source voltage high enough to keep the high-side MOSFETs turned on.

LC Filter Selection

The main reason that the traditional class-D amplifier-based on AD modulation needs an output filter is that the switching waveform results in maximum current flow. This causes more loss in the load, which causes lower efficiency. The ripple current is large for the traditional modulation scheme, because the ripple current is proportional to voltage multiplied by the time at that voltage. The differential voltage swing is 2×PVCC, and the time at each voltage is half the period for the traditional modulation scheme. An ideal LC filter is needed to store the ripple current from each half cycle for the next half cycle, while any resistance causes power dissipation. The speaker is both resistive and reactive, whereas an LC filter is almost purely reactive.

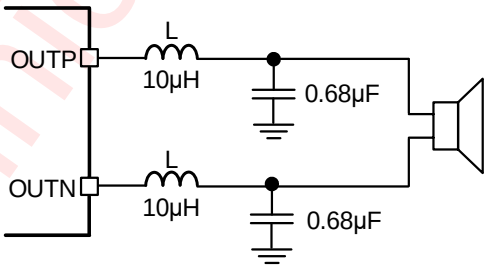


Figure 17 Output LC Filters

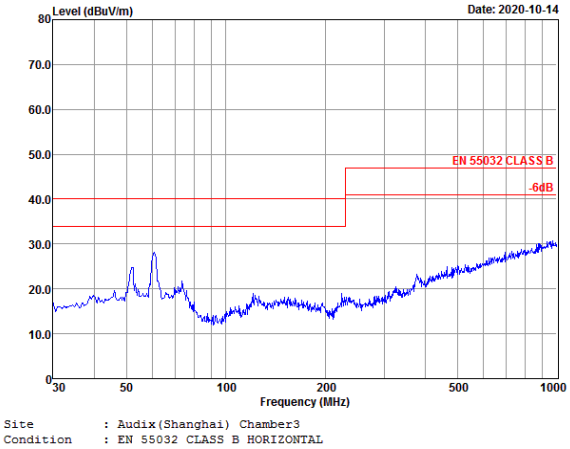
An LC filter with a cutoff frequency less than the class-D switching frequency allows the switching current to flow through the filter instead of the load. The filter has less resistance but higher impedance at the switching frequency than the speaker, which results in less power dissipation, therefore increasing efficiency.

Additional EMC improvements may be obtained by adding snubber networks from each of the class-D outputs to ground. Suggested values for a simple RC series snubber network would be 10Ω in series with a 220pF capacitor although design of the snubber network is specific to every application and must be designed taking into account the parasitic reactance of the printed circuit board as well as the audio amplifier. Take care to evaluate the stress on the component in the snubber network especially if the amplifier is running at high PVCC. Also, make sure the layout of the snubber network is tight and returns directly to the GND pins on the IC.

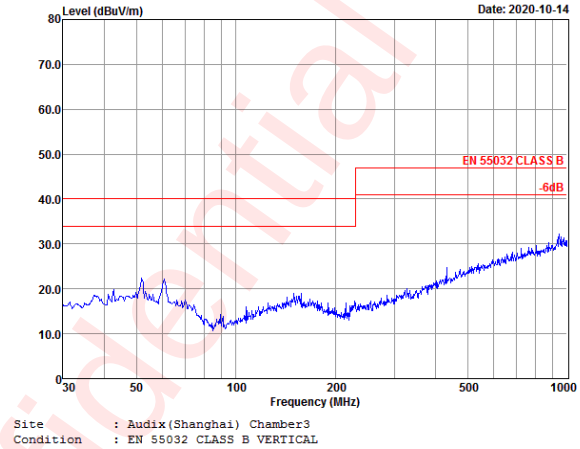
Application Performance Curves

EN55022 Radiated Emissions Results

AW83118 DEMO, PVCC=12V, 8Ω speakers, speaker cable length is 1m, AM<2:0>=110, Spread Spectrum range is 12%, Po=1W.



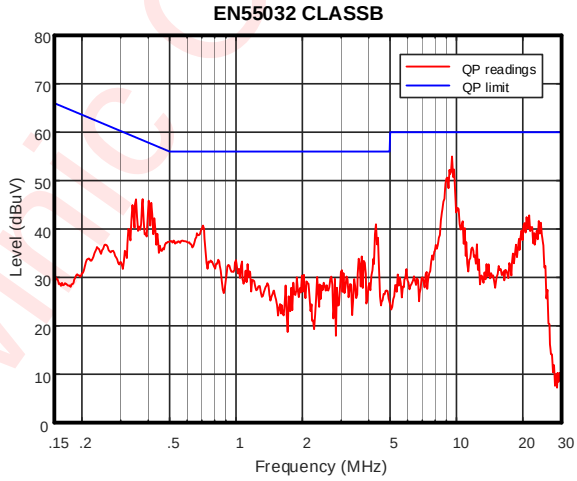
Radiated Emission - Horizontal



Radiated Emission - Vertical

EN55032 Conducted Emissions Results

AW83118 DEMO, PVCC=12V, 8Ω speakers, speaker cable length is 1m, AM<2:0>=110, Spread Spectrum range is 12%, Po=4W.



Conducted Emission - Line

PCB Layout Consideration

AW83118 is a high efficiency, stereo class-D audio amplifier with wide voltage range, to obtain the optimal performance, PCB layout should be considered carefully. Here are some guidelines:

1. The high-frequency decoupling capacitors should be placed as close to the PVCC and AVCC terminals as possible. Large (220μF or greater) bulk power supply decoupling capacitors should be placed near the AW83118 on the PVCC supplies. Local, high-frequency bypass capacitors should be placed as close to the PVCC pins as possible. These caps can be connected to the IC GND pad directly for an excellent ground connection. Consider adding a small, good quality low ESR ceramic capacitor between 220pF and 1nF and a large mid-frequency cap of value between 100nF and 1μF also of good quality to the PVCC connections at each end of the chip.
2. The PVCC decoupling capacitors should connect to GND. All ground should be connected at the IC GND, which should be used as a central ground connection or star ground for the AW83118.
3. The LC filter should be placed as close to the outputs. The capacitors used in both the ferrite and LC filters should be grounded.
4. Place the AW83118 device away from the edge of the PCB when possible to ensure that the heat can travel away from the device on all four sides.
5. Because the ground pins are the best conductors of heat in the package, maintain a contiguous ground plane from the ground pins to the PCB area surrounding the device for as many of the ground pins as possible.
6. Ensure the vias do not cut off power current flow from the power supply through the planes on internal layers. If needed, remove some vias that are farthest from the AW83118 to open up the current path to and from the device.

Layout Example

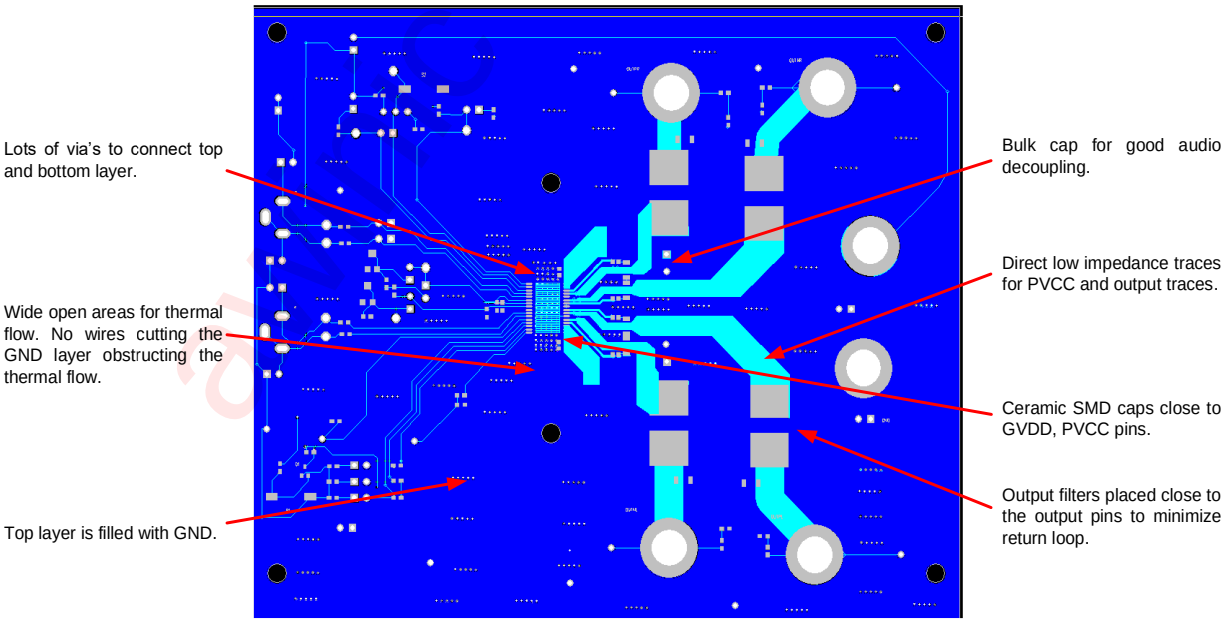


Figure 18 Layout Example Top

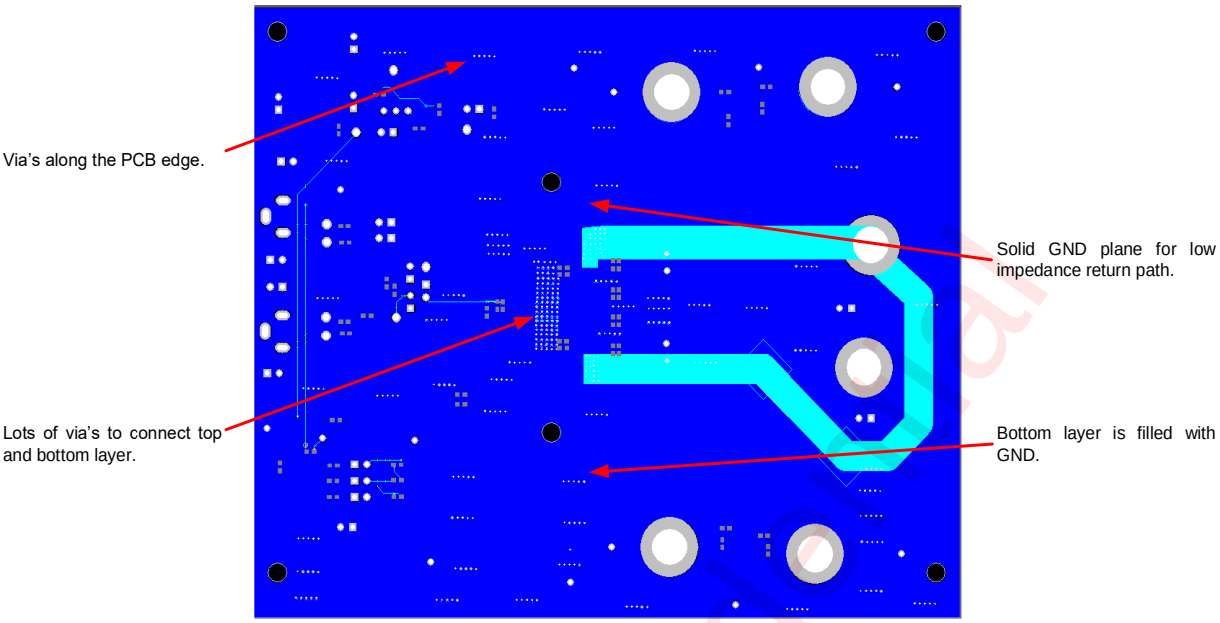
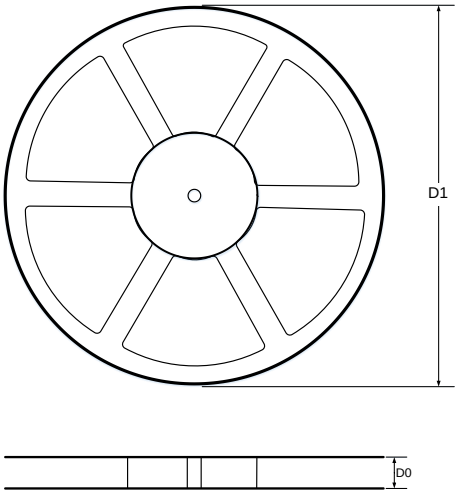


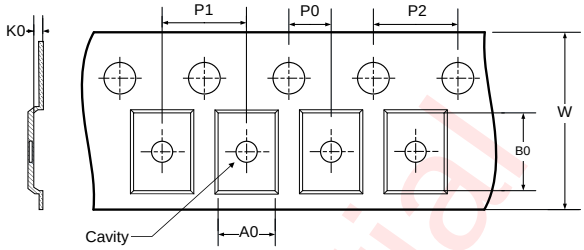
Figure 19 Layout Example Bottom

Tape And Reel Information

REEL DIMENSIONS

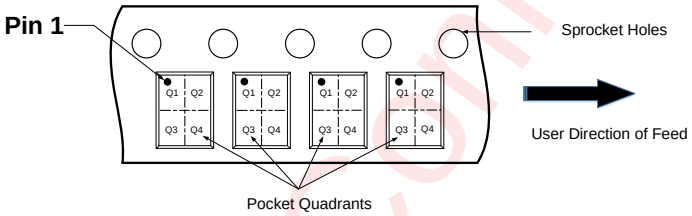


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



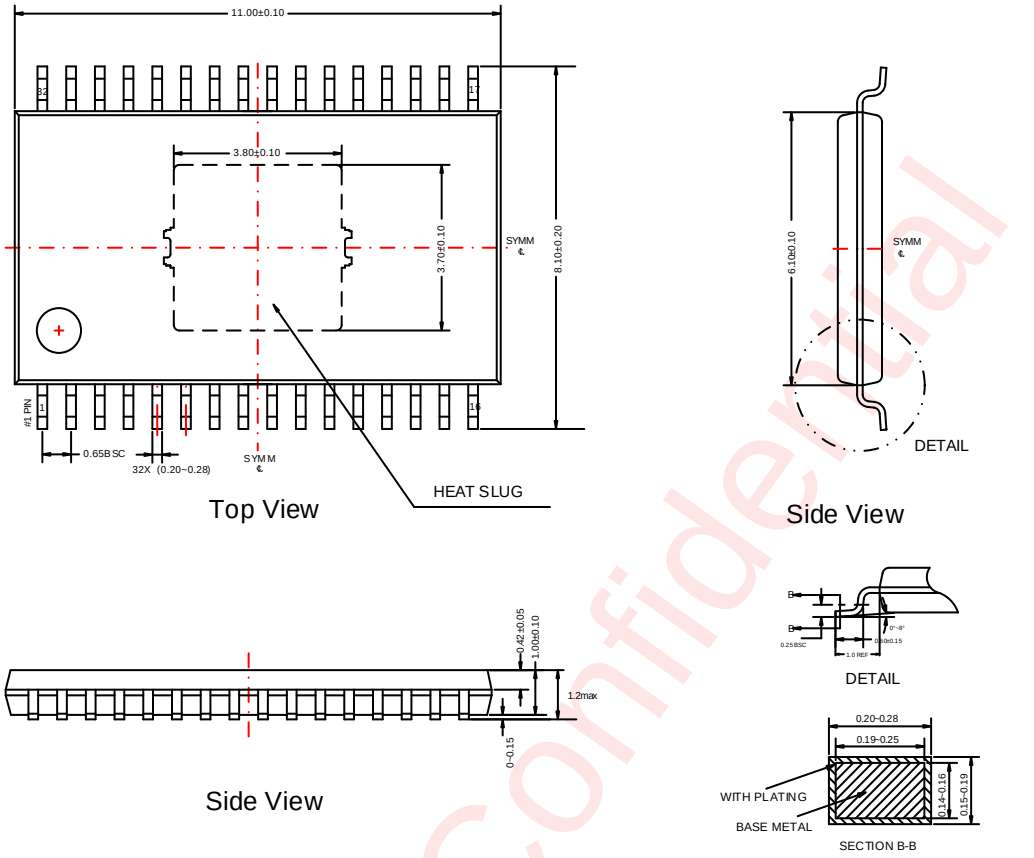
Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330	24.4	8.6	11.5	1.6	2	12	4	24	Q1

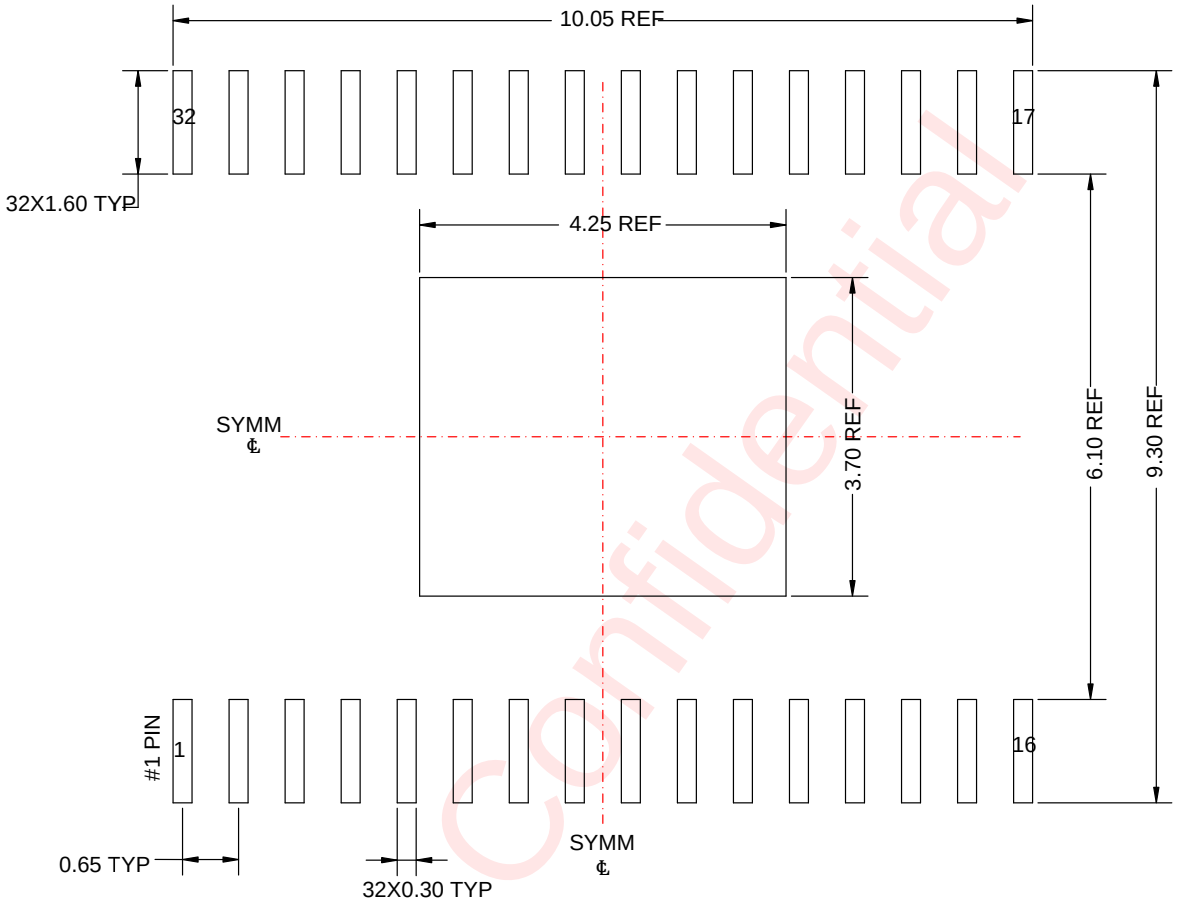
All dimensions are nominal

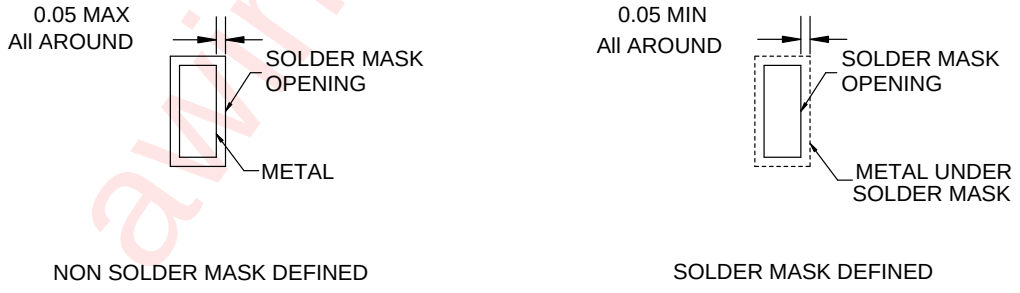
Package Description



UNIT:mm

Land Pattern Data





Unit：mm

Version Information

Version	Date	Description
V1.0	2020-10-22	AW83118TSR datasheet V1.0
V1.1	2020-12-02	Update PSRR data and curve.
V1.2	2021-10-22	Add the output power at 2Ω load.
V1.3	2021-10-31	Update Land Pattern Data
V1.4	2021-11-02	Update Land Pattern Data
V1.5	2021-12-09	Update temperature and table4 Power Limit Voltage
V1.6	2022-02-18	Update Absolute Maximum Ratings and Pin Definition
V1.7	2022-03-17	Update the Gain value , Add the value of θ_{JB} and θ_{JC}
V1.8	2022-07-22	Update Figure 8

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