

## Over-Voltage Protection Load Switch

### FEATURES

- Highly reliable 1.2mm × 1.2mm FCQFN-9 package
- Integrated low  $R_{dson}$  nFET switch: typical 30mΩ
- 5A continuous current capability
- Default Over-Voltage Protection (OVP) threshold
  - AW33901: 5.95V
  - AW33902: 6.2V
  - AW33905: 6.8V
  - AW33909: 9.98V
  - AW33910: 10.5V
- OVP threshold adjustable range: 4V to 20V
- Input maximum voltage rating: 32V<sub>DC</sub>
- Fast turn-off response: typical 50ns
- Over-Temperature Protection (OTP)
- Under-Voltage Lockout (UVLO)

### APPLICATIONS

- Smartphones
- Tablets
- Charging Ports

### GENERAL DESCRIPTION

The AW339XX features an ultra-low 30mΩ (typ.)  $R_{dson}$  nFET load switch. When input voltage exceeds the OVP threshold, the switch is turned off very fast to prevent damage to the protected downstream devices. The IN pin is capable of withstanding fault voltages up to 32V<sub>DC</sub>.

The default OVP threshold is 5.95V (AW33901), 6.2V (AW33902), 6.8V (AW33905), 9.98V (AW33909) and 10.5V (AW33910). The OVP threshold can be adjusted from 4V to 20V through external OVLO pin.

The device features an open-drain output  $\overline{ACOK}$ , when  $V_{IN\_UVLO} < V_{IN} < V_{IN\_OVLO}$  and the switch is on,  $\overline{ACOK}$  will be driven low to indicate a good power input, otherwise it is in high impedance mode (HiZ).

The device features over-temperature protection that prevents itself from thermal damaging.

The AW339XX is available in a RoHS compliant 1.2mm × 1.2mm FCQFN-9 package.

### TYPICAL APPLICATION CIRCUIT

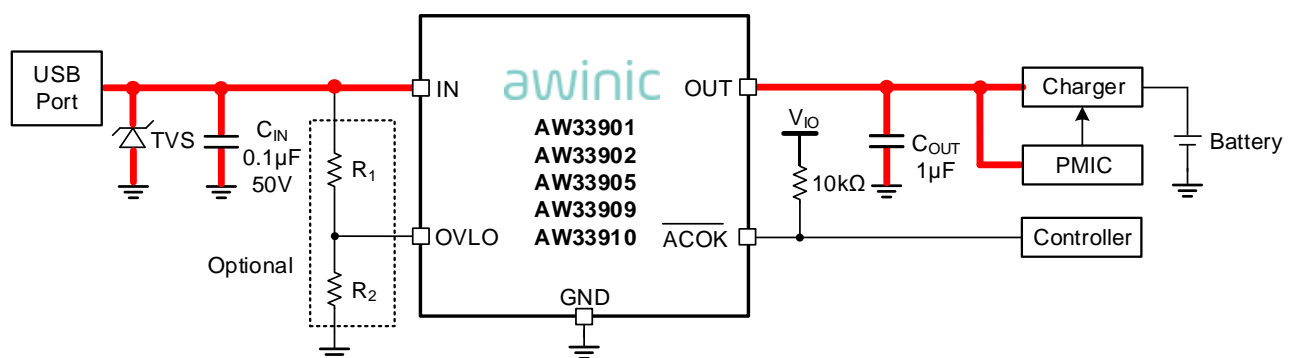


Figure 1 AW339XX typical application circuit

Note: when using default OVP threshold,  $R_1$  and  $R_2$  are not required, and connect OVLO pin to ground.

All the trademarks mentioned in the document are the property of their owners.

## DEVICE COMPARISON TABLE

Device	$V_{IN\_OVLO}(V)$				$V_{IN\_OVLO}$ Hysteresis(mV)
	Condition	Min.	Typ.	Max.	
AW33901	$V_{IN}$ rising	5.83	5.95	6.07	130
AW33902	$V_{IN}$ rising	6.08	6.20	6.32	130
AW33905	$V_{IN}$ rising	6.66	6.80	6.94	140
AW33909	$V_{IN}$ rising	9.78	9.98	10.18	210
AW33910	$V_{IN}$ rising	10.29	10.50	10.71	210

## PIN CONFIGURATION AND TOP MARK

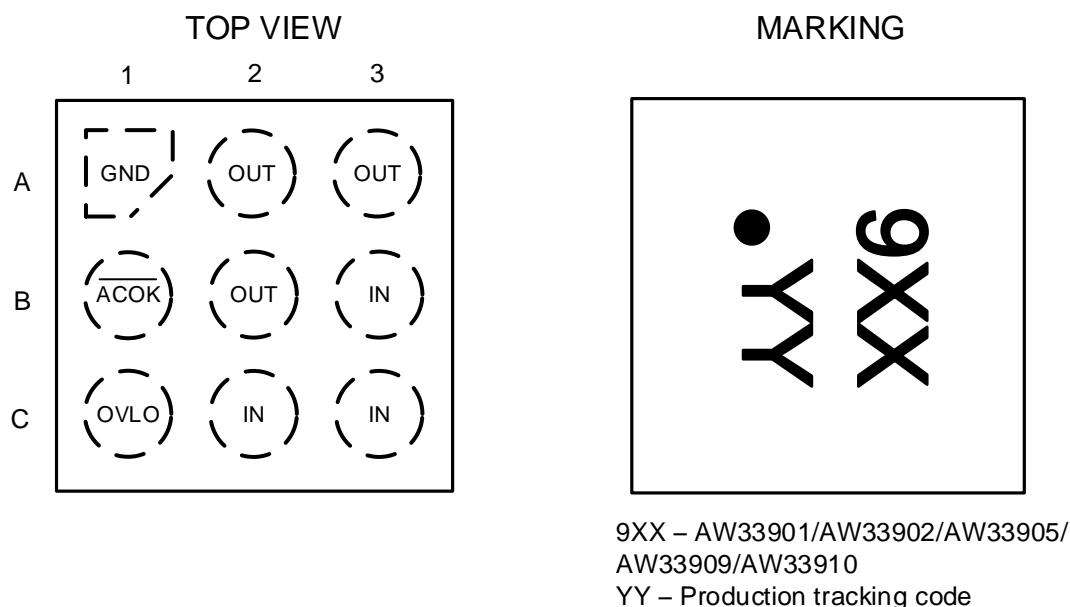


Figure 2 Pin Configuration and Top Mark

## PIN DEFINITION

Pin	Name	Description
B3,C2,C3	IN	Switch input and device power supply
A1	GND	Device ground
C1	OVLO	OVP threshold adjustment pin
A2,A3,B2	OUT	Switch output
B1	$\overline{ACOK}$	Power good flag, active-low, open-drain

FUNCTIONAL BLOCK DIAGRAM

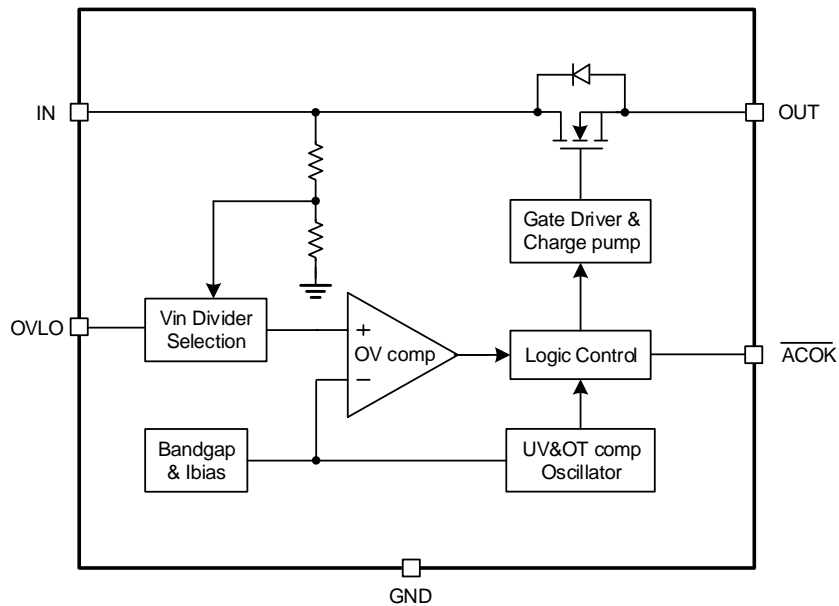


Figure 3 Functional Block Diagram

TYPICAL APPLICATION CIRCUITS

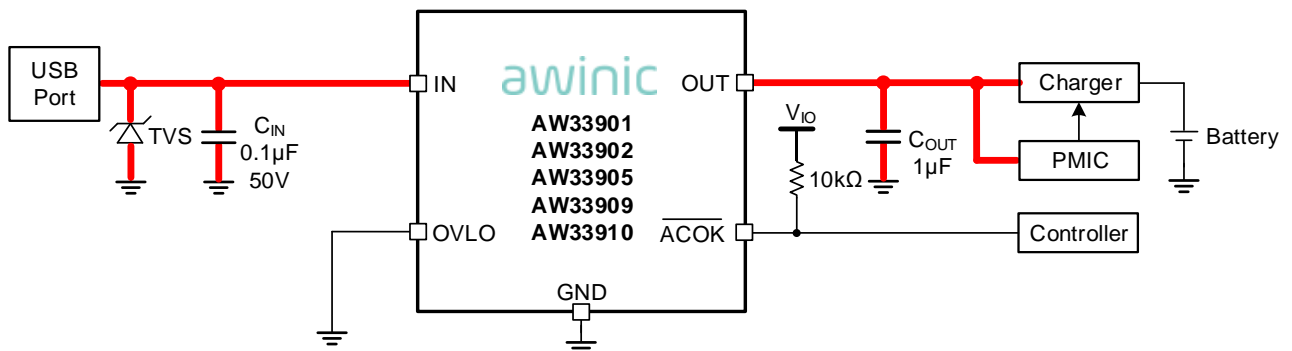


Figure 4 AW339XX typical application circuit(using default OVP threshold)

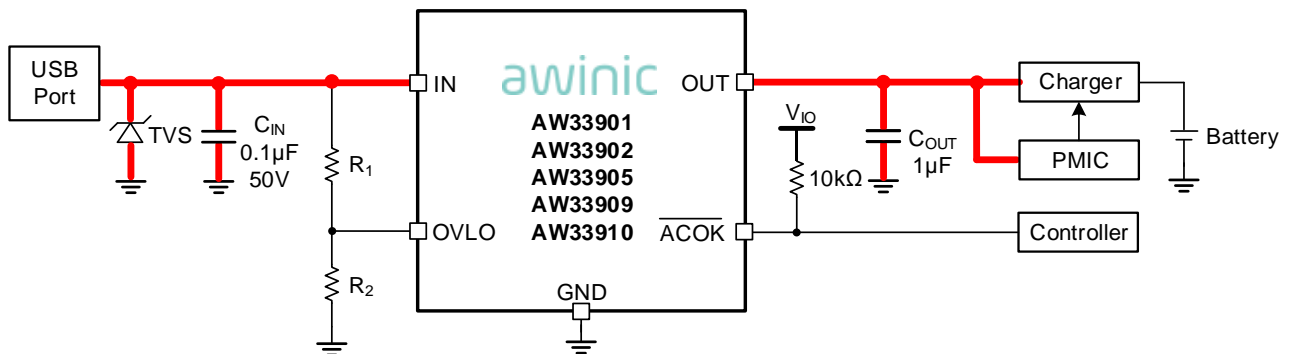


Figure 5 AW339XX typical application circuit(using external OVP threshold)

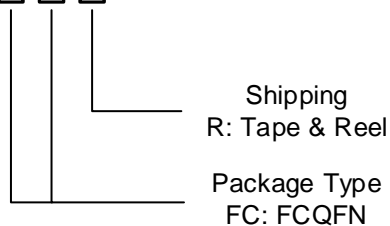
**Notice for Typical Application Circuits:**

1. When the default OVP threshold is used, connect OVLO pin to GND directly or through a  $0\Omega$  resistor. OVLO pin cannot be left floating.
2. If  $R_1$  and  $R_2$  are used to adjust the OVP threshold, it is better to use 1% precision resistors to improve the OVP threshold precision.
3.  $C_{IN} = 0.1\mu F$  is recommended for typical application, larger  $C_{IN}$  is also acceptable. The rated voltage of  $C_{IN}$  should be larger than the TVS maximum clamping voltage, if no TVS is applied and only AW339XX is used, the rated voltage of  $C_{IN}$  should be 50V.
4.  $C_{OUT} = 1\mu F$  is recommended for typical application, larger  $C_{OUT}$  is also acceptable. The rated voltage of  $C_{OUT}$  should be larger than the OVP threshold. For example, if the OVP threshold is 6.8V, the rated voltage of  $C_{OUT}$  should be 10V or higher.

## ORDERING INFORMATION

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW33901FCR	-40°C – 85°C	1.2mm × 1.2mm × 0.55mm FCQFN-9	901	MSL1	ROHS+HF	Tape and Reel 3000pcs/Reel
AW33902FCR	-40°C – 85°C	1.2mm × 1.2mm × 0.55mm FCQFN-9	902	MSL1	ROHS+HF	Tape and Reel 3000pcs/Reel
AW33905FCR	-40°C – 85°C	1.2mm × 1.2mm × 0.55mm FCQFN-9	905	MSL1	ROHS+HF	Tape and Reel 3000pcs/Reel
AW33909FCR	-40°C – 85°C	1.2mm × 1.2mm × 0.55mm FCQFN-9	909	MSL1	ROHS+HF	Tape and Reel 3000pcs/Reel
AW33910FCR	-40°C – 85°C	1.2mm × 1.2mm × 0.55mm FCQFN-9	910	MSL1	ROHS+HF	Tape and Reel 3000pcs/Reel

AW339XX □ □ □



## ABSOLUTE MAXIMUM RATINGS<sup>(NOTE1)</sup>

Symbol	Parameter	Condition	Min.	Max.	Unit
V <sub>IN</sub>	Input DC voltage		-0.3	32	V
V <sub>IN_PUL</sub>	Input peak pulse voltage	20μs pulse width, repeat 100 times		40	V
V <sub>OUT</sub>	Output voltage		-0.3	See <sup>(NOTE 2)</sup>	V
V <sub>ACOK</sub>	ACOK voltage		-0.3	7	V
V <sub>OVLO</sub>	OVLO voltage		-0.3	7	V
I <sub>SW</sub>	Continuous current of switch IN-OUT <sup>(NOTE 3)</sup>	Continuous current on IN and OUT pin		5	A
I <sub>PEAK</sub>	Peak current	Peak input and output current on IN and OUT pin(10ms)		8	A
I <sub>DIODE</sub>	Continuous diode current	Continuous forward current through the nFET body diode		1.5	A
T <sub>A</sub>	Ambient temperature		-40	85	°C
T <sub>J</sub>	Junction temperature		-40	150	°C
T <sub>STG</sub>	Storage temperature		-65	150	°C
T <sub>LEAD</sub>	Soldering temperature	At leads, 10 seconds		260	°C

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: 29V or V<sub>IN</sub>+0.3V, whichever is smaller.

NOTE3: Limited by thermal design.

## THERMAL INFORMATION

Symbol	Parameter	Condition	Value	Unit
R <sub>θJA</sub>	Thermal resistance from junction to ambient <sup>(NOTE 1)</sup>	In free air	70	°C/W

NOTE1: Thermal resistance from junction to ambient is highly dependent on PCB layout.

## ESD AND LATCH-UP RATINGS

Symbol	Parameter	Condition	Value	Unit
V <sub>ESD</sub>	Human Body Model	All pins, per MIL-STD-883J Method 3015.9	±6.5	kV
	Charged Device Model	All pins, per ESDA/JEDEC JS-002-2014	±2	kV
	Machine Model	All pins, per JESD22-A115C	±450	V
I <sub>Latch-up</sub>	Latch-up	All pins, per JESD78D, I Trigger	±800	mA

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>IN</sub>	Input DC voltage	3		30	V
C <sub>IN</sub>	Input capacitance		0.1		μF
C <sub>OUT</sub>	Output load capacitance		1	100	μF

## ELECTRICAL CHARACTERISTICS

$T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  unless otherwise noted. Typical values are guaranteed for  $V_{IN} = 5\text{V}$ ,  $C_{IN} = 0.1\mu\text{F}$ ,  $I_{IN} \leq 5\text{A}$  and  $T_A = 25^{\circ}\text{C}$ .

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units				
$R_{dson}$	Switch on resistance	$V_{IN} = 5\text{V}$ , $I_{OUT} = 1\text{A}$ , $T_A = 25^{\circ}\text{C}$		30	41	$\text{m}\Omega$				
$I_q$	Input quiescent current	$V_{IN} = 5\text{V}$ , $V_{OVLO}=0\text{V}$ , $I_{OUT} = 0\text{A}$		80	150	$\mu\text{A}$				
$I_{IN\_OVLO}$	Input current at over-voltage condition	$V_{IN} = 5\text{V}$ , $V_{OVLO}=3\text{V}$ , $V_{OUT} = 0\text{V}$		78	150	$\mu\text{A}$				
$V_{OVLO\_TH}$	OVLO set threshold		1.16	1.20	1.24	V				
$V_{OVLO\_RNG}$	OVP threshold adjustable range		4		20	V				
$V_{OVLO\_SEL}$	External OVLO select threshold	OVLO rising	0.19	0.26	0.33	V				
		Hysteresis		0.06		V				
$I_{OVLO}$	OVLO pin leakage current	$V_{OVLO}=V_{OVLO\_TH}$	-0.2		0.2	$\mu\text{A}$				
<b>Protection</b>										
$V_{IN\_OVLO}$	OVP trip level	AW33901	$V_{IN}$ rising	5.83	5.95	6.07	V			
			Hysteresis		0.13					
		AW33902	$V_{IN}$ rising	6.08	6.20	6.32				
			Hysteresis		0.13					
		AW33905	$V_{IN}$ rising	6.66	6.80	6.94				
			Hysteresis		0.14					
		AW33909	$V_{IN}$ rising	9.78	9.98	10.18				
			Hysteresis		0.21					
		AW33910	$V_{IN}$ rising	10.29	10.50	10.71				
			Hysteresis		0.21					
		$V_{IN\_UVLO}$	UVLO trip level	$V_{IN}$ rising				2.9	3.0	V
				Hysteresis				0.1		



## ELECTRICAL CHARACTERISTICS(CONTINUED)

$T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  unless otherwise noted. Typical values are guaranteed for  $V_{IN} = 5\text{V}$ ,  $C_{IN} = 0.1\mu\text{F}$ ,  $I_{IN} \leq 5\text{A}$  and  $T_A = 25^{\circ}\text{C}$ .

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Units
<b>Protection(continued)</b>						
$T_{SDN}$	Shutdown temperature			150		$^{\circ}\text{C}$
$T_{SDN\_HYS}$	Shutdown temperature hysteresis			20		$^{\circ}\text{C}$
$R_{DCHG}$	Output resistance discharge	$V_{OUT}=7\text{V}, V_{OVLO}=3\text{V}$		50		$\Omega$
<b>Digital Logical Interface</b>						
$V_{OL}$	$\overline{\text{ACOK}}$ output low voltage	$I_{SINK}=1\text{mA}$			0.4	V
$I_{LEAK\_ACOK}$	$\overline{\text{ACOK}}$ leakage current	$V_{IO}=5\text{V}, \overline{\text{ACOK}}$ de-asserted	-0.5		0.5	$\mu\text{A}$
<b>Timing Characteristics (Figure 6)</b>						
$t_{DEB}$	Debounce time	From $V_{IN} > V_{IN\_UVLO}$ to 10% $V_{OUT}$		15		ms
$t_{START}$	Start-up time	From $V_{IN} > V_{IN\_UVLO}$ to $\overline{\text{ACOK}}$ low		30		ms
$t_{ON}$	Switch turn-on time	$R_L = 100\Omega, C_L = 22\mu\text{F}, V_{OUT}$ from 10% $V_{IN}$ to 90% $V_{IN}$		2		ms
$t_{OFF}$	Switch turn-off time	$C_L = 0\mu\text{F}, R_L = 100\Omega, V_{IN} > V_{IN\_OVLO}$ to $V_{OUT}$ stop rising, $V_{IN}$ rise at $10\text{V}/\mu\text{s}$		50		ns

## TIMING DIAGRAM

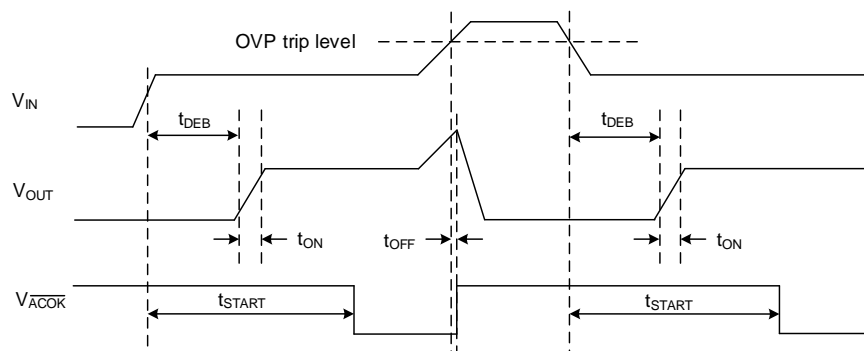


Figure 6 Timing diagram

## TYPICAL CHARACTERISTICS

Table 1 Table of Figures

INDEX	Figure No
$R_{dson}$ vs. Output Current	<b>FIGURE 7</b>
$R_{dson}$ vs. Temp. ( $I_{OUT} = 1A$ )	<b>FIGURE 8</b>
$R_{dson}$ vs. Input Voltage ( $I_{OUT} = 1A$ )	<b>FIGURE 9</b>
Input Supply Current vs. Supply Voltage	<b>FIGURE 10</b>
Normalized Internal OVP Threshold	<b>FIGURE 11</b>
External OVP Threshold	<b>FIGURE 12</b>
Power-up ( $C_{OUT} = 1\mu F$ , 100mA load)	<b>FIGURE 13</b>
Power-up ( $C_{OUT} = 100\mu F$ , 100mA load)	<b>FIGURE 14</b>
OVP Response (AW33905)	<b>FIGURE 15</b>
400V Surge Response (AW33905 with 12V TVS)	<b>FIGURE 16</b>

$V_{IN} = 5V$ ,  $V_{OVLO} = 0V$ ,  $C_{IN} = 0.1\mu F$ ,  $C_{OUT} = 1\mu F$ , and  $T_A = 25^\circ C$  unless otherwise specified.

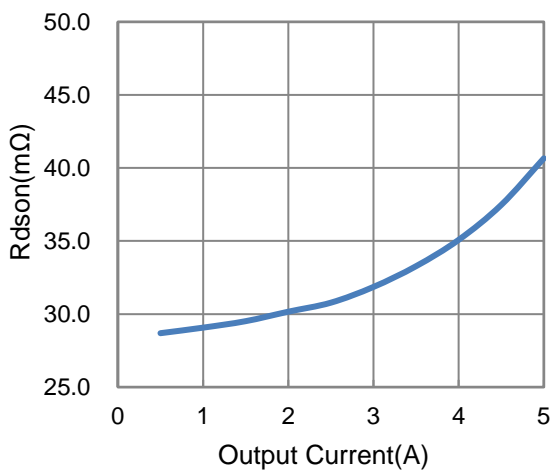


Figure 7  $R_{dson}$  vs. Output Current

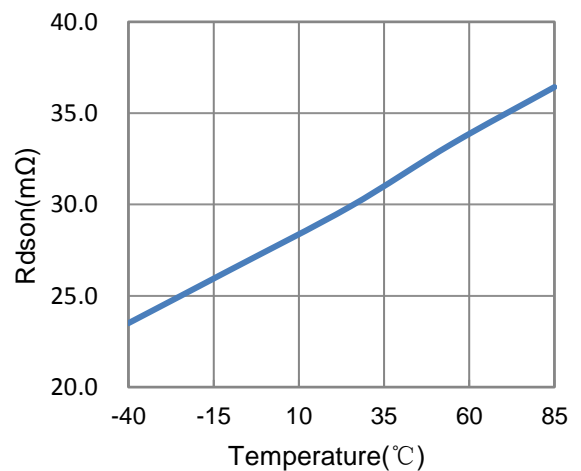


Figure 8  $R_{dson}$  vs. Temp. ( $I_{OUT} = 1A$ )

## TYPICAL CHARACTERISTICS (CONTINUED)

$V_{IN} = 5V$ ,  $V_{OVLO} = 0V$ ,  $C_{IN} = 0.1\mu F$ ,  $C_{OUT} = 1\mu F$ , and  $T_A = 25^\circ C$  unless otherwise specified.

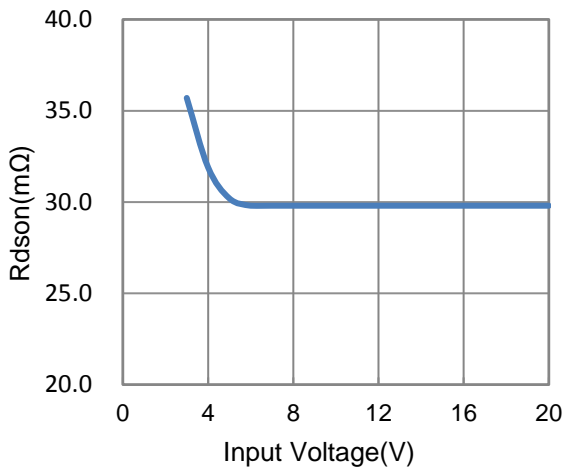


Figure 9  $R_{dson}$  vs. Input Voltage ( $I_{OUT} = 1A$ )

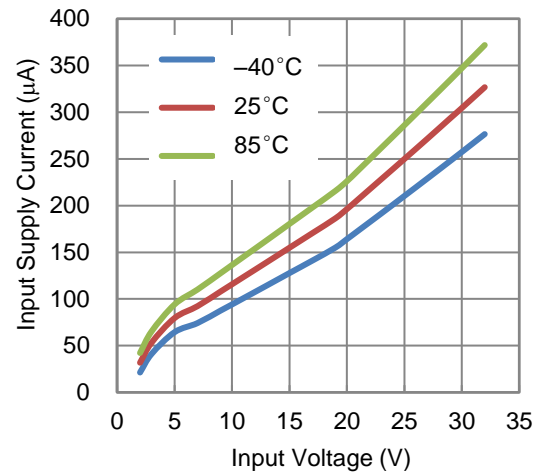


Figure 10 Input Supply Current vs. Supply Voltage

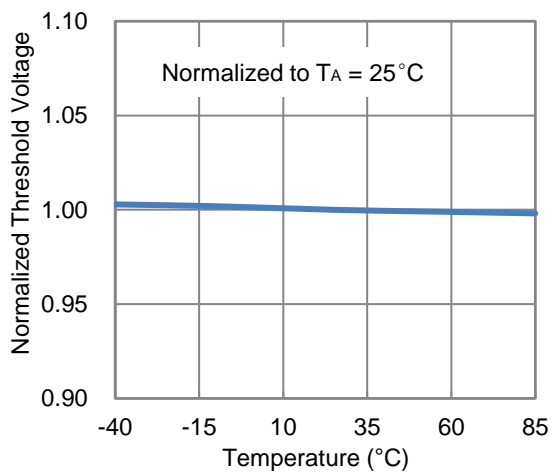


Figure 11 Normalized Internal OVP Threshold

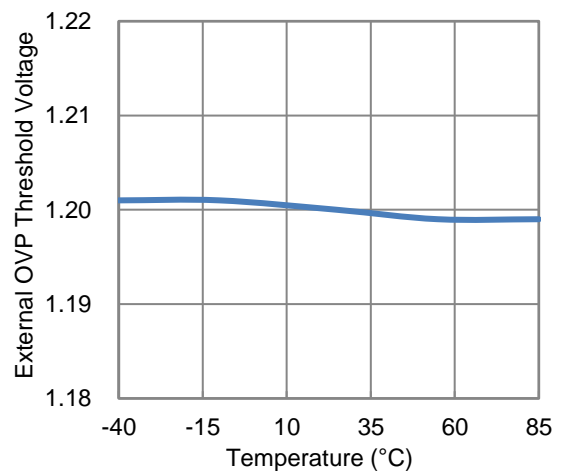


Figure 12 External OVP Threshold

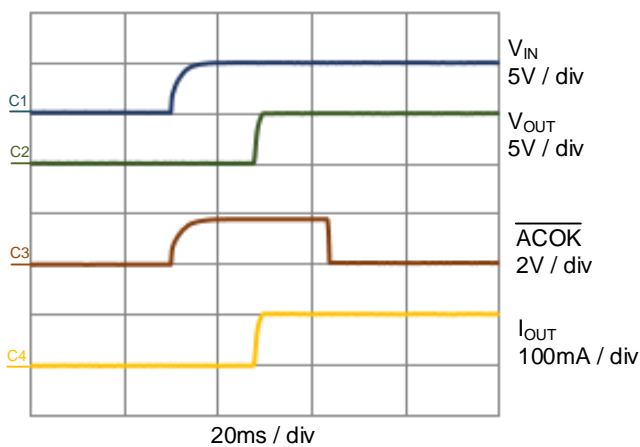


Figure 13 Power-up ( $C_{OUT} = 1\mu F$ , 100mA load).

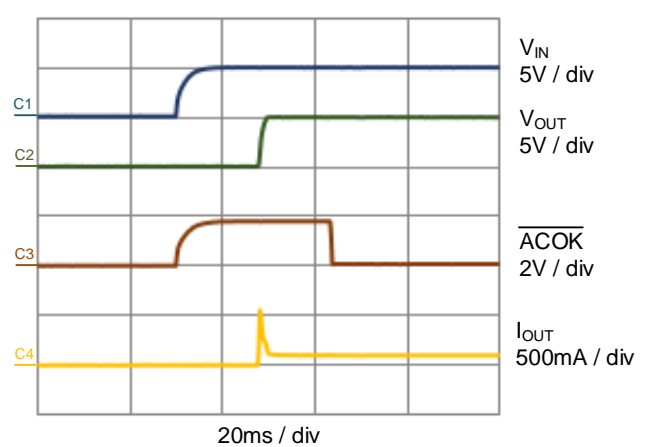


Figure 14 Power-up ( $C_{OUT} = 100\mu F$ , 100mA load)

## TYPICAL CHARACTERISTICS (CONTINUED)

$V_{IN} = 5V$ ,  $V_{OVLO} = 0V$ ,  $C_{IN} = 0.1\mu F$ ,  $C_{OUT} = 1\mu F$ , and  $T_A = 25^\circ C$  unless otherwise specified.

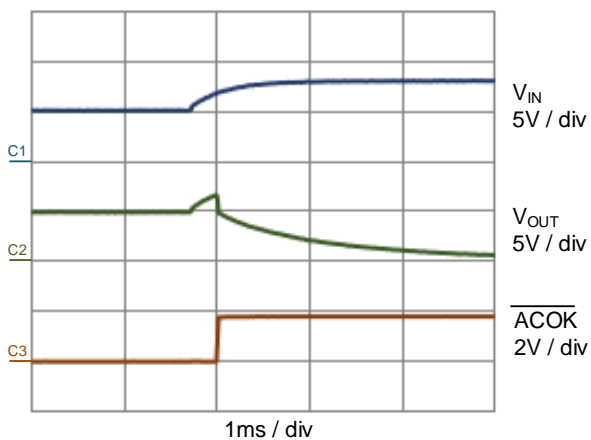


Figure 15 OVP Response (AW33905)

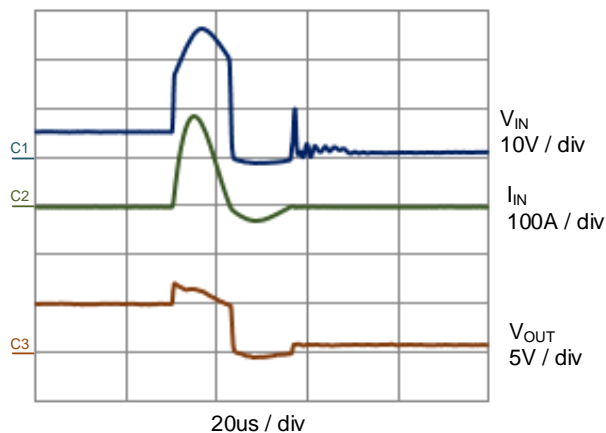


Figure 16 400V Surge Response (AW33905 with 12V TVS)

## DETAILED FUNCTIONAL DESCRIPTION

### Device Operation

If the input voltage is between UVLO and OVP threshold, the internal charge pump begins to work after debounce time, the gate of the nFET switch will be slowly charged high till the switch is fully on.  $\overline{\text{ACOK}}$  will be driven low about 30ms after  $V_{\text{IN}}$  valid, indicating the switch is on with a good power input. If the input voltage exceeds the OVP trip level, the switch will be turned off in about 50ns. If input voltage falls below UVLO threshold, or over-temperature happens, the switch will also be turned off.

### Over-Voltage Protection

If the input voltage exceeds the OVP rising trip level, the switch will be turned off in about 50ns. The switch will remain off until  $V_{\text{IN}}$  falls below the OVP falling trip level.

### OVP Threshold Adjustment

If the default OVP threshold is used, OVLO pin must be grounded. If OVLO pin is not grounded, and by connecting external resistor divider to OVLO pin as shown in the typical application circuit, between IN and GND, the OVP threshold can be adjusted as following:

$$V_{\text{IN\_OVLO}} = \frac{R_1+R_2}{R_2} V_{\text{OVLO\_TH}}$$

The adjustment range is 4V to 20V. When the OVLO pin voltage  $V_{\text{OVLO}}$  exceeds  $V_{\text{OVLO\_SEL}}$  (0.26V typical),  $V_{\text{OVLO}}$  is compared with the reference voltage  $V_{\text{OVLO\_TH}}$  (1.2V typical) to judge whether input supply is over-voltage. It is recommended that the total resistance of R1 and R2 is less than 100k $\Omega$ . For example, if we select  $R_1 = 51\text{k}\Omega$  and  $R_2 = 12.4\text{k}\Omega$ , then the new OVP threshold calculated from the above formula is 6.14V.

### $\overline{\text{ACOK}}$ Output

The device features an open-drain output  $\overline{\text{ACOK}}$ , it should be connected to the system I/O rail through a pull-up resistor. If the device is enabled and  $V_{\text{IN\_UVLO}} < V_{\text{IN}} < V_{\text{IN\_OVLO}}$ ,  $\overline{\text{ACOK}}$  will be driven low indicating the switch is on with a good power input. If OVP, UVLO, or OT occurs, the switch will be turned off and  $\overline{\text{ACOK}}$  will be pulled high. If this function is not needed,  $\overline{\text{ACOK}}$  pin can be floating or grounded.

### USB On-The-Go (OTG) Operation

If  $V_{\text{IN}} = 0\text{V}$  and OUT is supplied by OTG voltage, the body diode of the load switch conducts current from OUT to IN and the voltage drop from OUT to IN is approximately 0.7V. When  $V_{\text{IN}} > V_{\text{IN\_UVLO}}$ , internal charge pump begins to open the load switch after debounce time (15ms typical). After switch is fully on, current is supplied through switch channel and the voltage drop from OUT to IN is minimum.

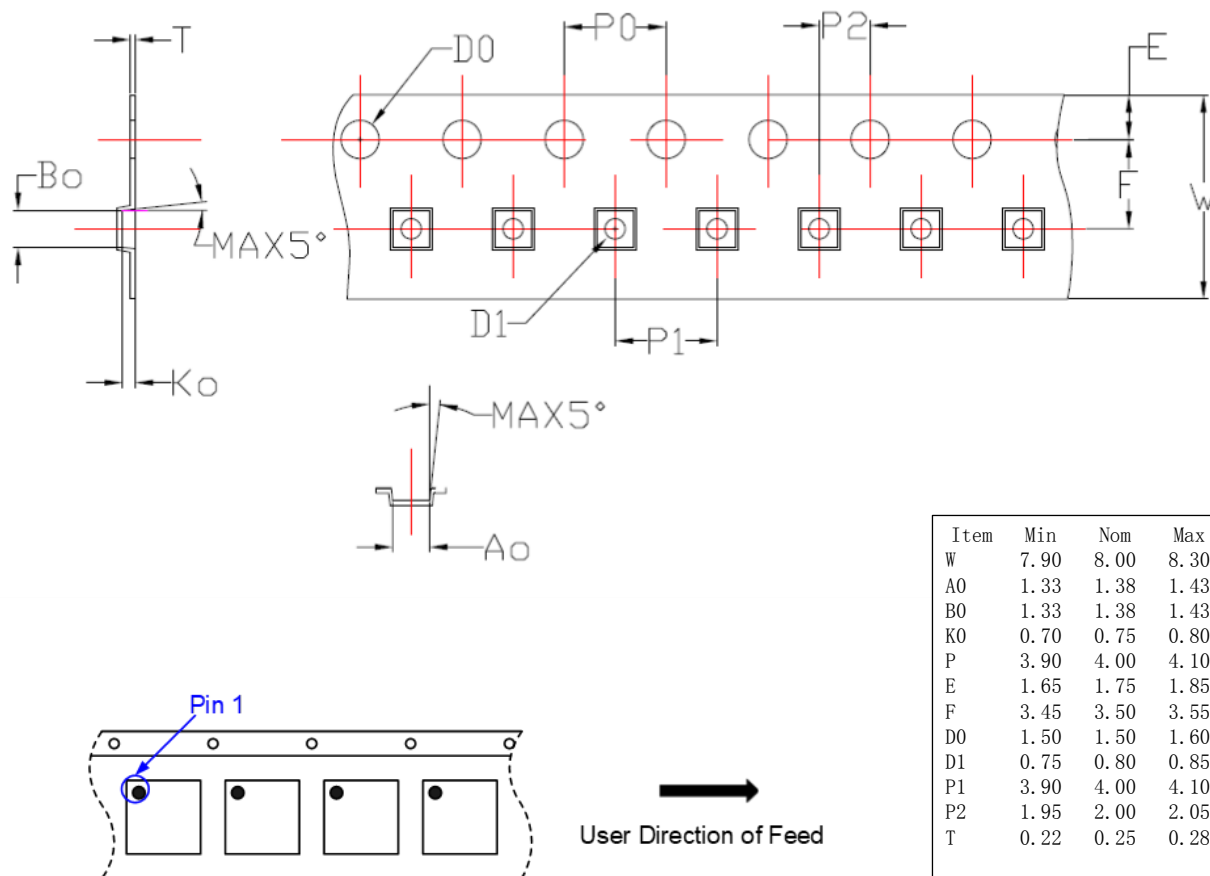
## PCB LAYOUT CONSIDERATION

To make fully use of the performance of AW339XX, the guidelines below should be followed.

1. All the peripherals should be placed as close to the device as possible. Place the input capacitor  $C_{IN}$  on the top layer (same layer as the AW339XX) and close to IN pin, and place the output capacitor  $C_{OUT}$  on the top layer (same layer as the AW339XX) and close to OUT pin.
2. IN pin routing passes through the external TVS firstly, and then connect AW339XX.
3. Red bold paths on figure 4 and 5 are power lines that will flow large current, please route them on PCB as straight, wide and short as possible.
4. If  $R_1$  and  $R_2$  are used, route OVLO line on PCB as short as possible to reduce parasitic capacitance.
5. The power trace from USB connector to AW339XX may suffer from ESD event, keep other traces away from it to minimize possible EMI and ESD coupling.
6. Use rounded corners on the power trace from USB connector to AW339XX to decrease EMI coupling.

## TAPE AND REEL INFORMATION

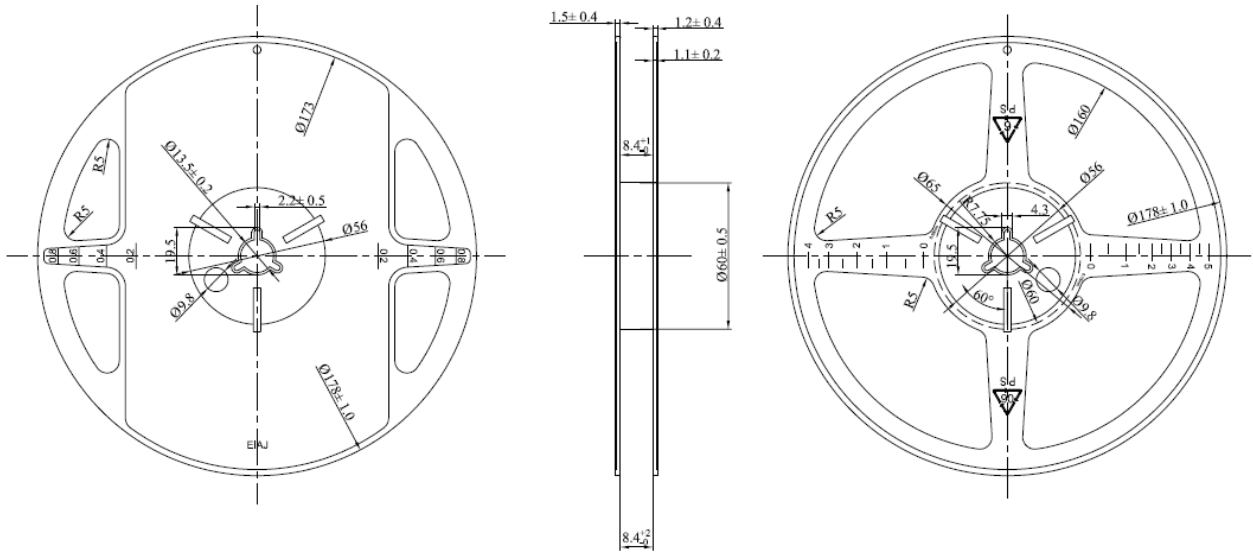
### CARRIER TAPE



#### NOTE:

1. Unit: mm;
2. Material: ABS;
3. Carrier camber not exceed 1mm in 250mm;
4. 10 sprocket hole pitch cumulative tolerance  $\pm 0.2\text{mm}$ ;
5. All tape and sprocket hole dimensioning are as per EIA-481 unless otherwise stated;
6. A0 and B0 measured on a place in the middle of the corner RADII.

REEL



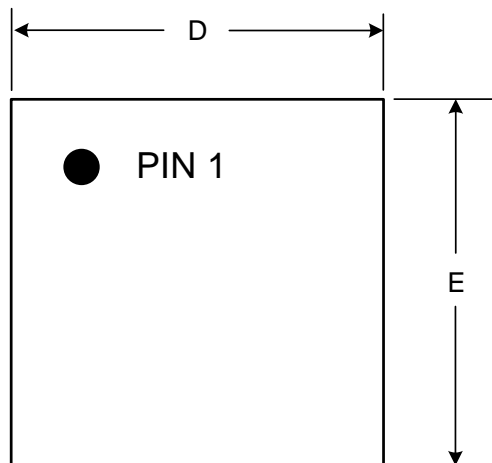
NOTE:

1. Units: mm;
2. Material: polystyrene;
3. Planeness: max 3mm;
4. Surface resistance:  $10^5$  to  $10^{11}$  ohms/sq;
5. All outstanding tolerance:  $\pm 0.25$ mm.

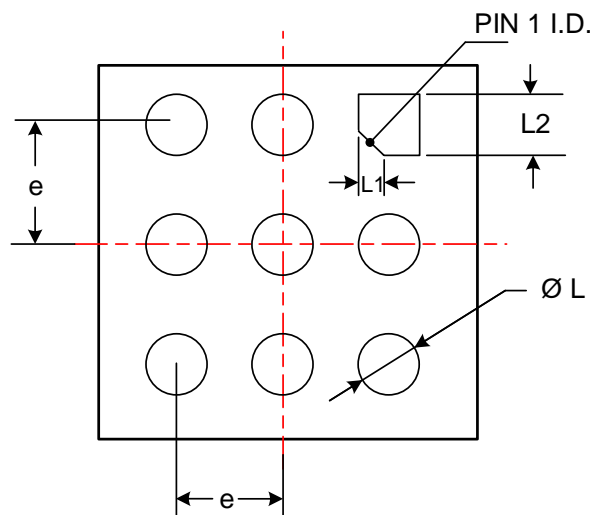


## PACKAGE DESCRIPTION

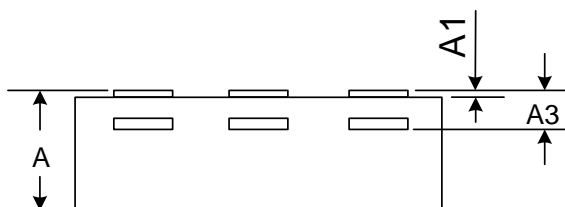
TOP VIEW



BOTTOM VIEW



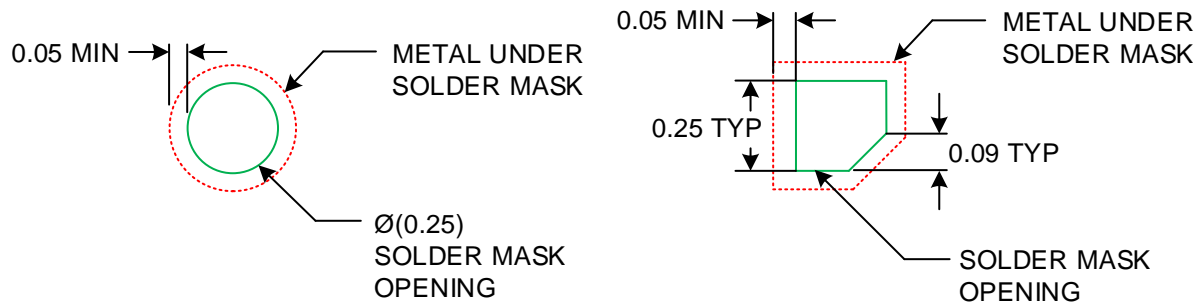
SIDE VIEW



SYMBOL	MIN	NOM	MAX
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
A3	0.152REF.		
D	1.10	1.20	1.30
E	1.10	1.20	1.30
e	0.400REF.		
L	0.18	0.25	0.30
L1	0.090REF.		
L2	0.250REF.		

Unit: mm

## SOLDER MASK DETAILS



SOLDER MASK DETAILS  
NOT TO SCALE

NOTE:

Unit: mm.

## REFLOW

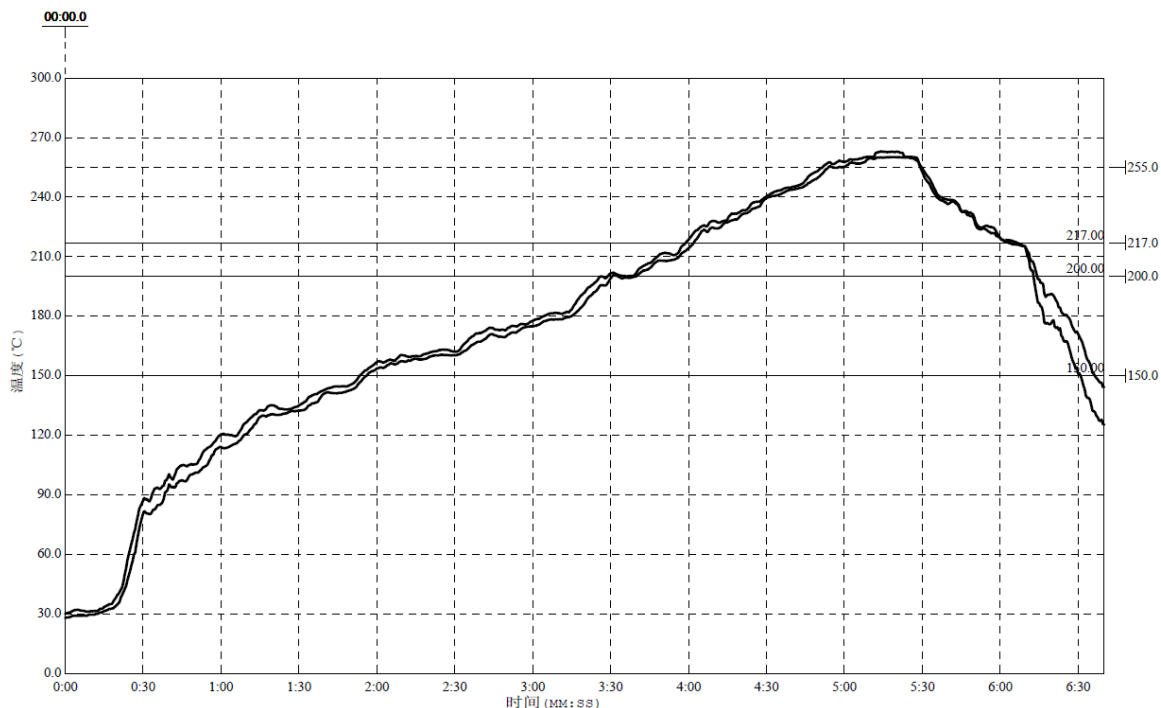


Figure 17 Package Reflow Oven Thermal Profile

Table 1 Package Reflow Standard

Reflow Note	Spec
Average ramp-up rate (217°C to Peak)	Max. 3°C /sec
Time of Preheat temp.(from 150°C to 200°C)	60-120 sec
Time to be maintained above 217°C	60-150 sec
Peak Temperature	>260°C
Time within 5°C of actual peak temp	20-40 sec
Ramp-down rate	Max. 6°C /sec
Time from 25°C to peak temp	Max. 8min

NOTE 1: All data are compared with the package-top temperature, measured on the package surface;

NOTE 2: AW339XX adopted the Pb-Free assembly.

## REVISION HISTORY

Vision	Date	Change Record
V0.9	November 2017	Datasheet V0.9 Released.
V1.0	December,2017	<ol style="list-style-type: none"> <li>1. Added AW33901 part number.</li> <li>2. Added Typical Characteristics.</li> <li>3. Added Tape and Reel information.</li> <li>4. Added Solder Mask Details.</li> </ol>
V1.1	February,2018	<ol style="list-style-type: none"> <li>1. Modified Reel information.</li> <li>2. Modified POD information.</li> <li>3. Modified Solder Mask Details.</li> </ol>
V1.2	September, 2018	Storage Temperature Modified

## DISCLAIMER

Information in this document is believed to be accurate and reliable. However, Shanghai AWINIC Technology Co., Ltd (AWINIC Technology) does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

AWINIC Technology reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. Customers shall obtain the latest relevant information before placing orders and shall verify that such information is current and complete. This document supersedes and replaces all information supplied prior to the publication hereof.

AWINIC Technology products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an AWINIC Technology product can reasonably be expected to result in personal injury, death or severe property or environmental damage. AWINIC Technology accepts no liability for inclusion and/or use of AWINIC Technology products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications that are described herein for any of these products are for illustrative purposes only. AWINIC Technology makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

All products are sold subject to the general terms and conditions of commercial sale supplied at the time of order acknowledgement.

Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Reproduction of AWINIC information in AWINIC data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. AWINIC is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of AWINIC components or services with statements different from or beyond the parameters stated by AWINIC for that component or service voids all express and any implied warranties for the associated AWINIC component or service and is an unfair and deceptive business practice. AWINIC is not responsible or liable for any such statements.

单击下面可查看定价，库存，交付和生命周期等信息

[>>AWINIC\(艾为\)](#)