A Low Power One-key Capacitor Touch Sensor

Features

- Sensitivity adjusted by the capacitance (0~50pF) outside (Refer to the DG_AW93001_Hardware_Design_Guide for details)
- Maximum response time
  - Slow scan mode: 160ms(AW93001STR /BSTR/DNR/BDNR/CDNR/DDNR)
  - Slow scan mode: 64ms(AW93001EDNR /FDNR)
  - Fast scan mode: 48ms(AW93001STR /BSTR/DNR/BDNR/HDNR/GDNR/MDNR /LDNR/CSTR/DSTR/CDNR/DDNR/EDNR /FDNR)
- Push-pull output (AW93001STR/DSTR/DNR /HDNR/MDNR)
  - Active high/low selected by pin AHLB
- Push-pull output, active high(AW93001CDNR /EDNR)
- Open-drain output, active low (AW93001BSTR /CSTR/BDNR/GDNR/LDNR/DDNR/FDNR)
- Toggle output selected by pin TOG
- Low power consumption
  - Slow scan mode (128ms): 1.3μA
  - Slow scan mode (32ms): 3.3μA
  - Fast scan mode (16ms): 5.4μA
- 2.4V~5.5V power supply
- Operation temperature range: -40°C~85°C
- Package
  - SOT23-6L
  - DFN 1.5mmx1.0mmx0.55mm-6L
  - DFN 2.0mmx2.0mmx0.75mm-6L
  - DFN 1.0mmx1.0mmx0.37mm-4L

General Description

AW93001 is a single channel capacitive touch controller with low power consumption and wide operation voltage range.

With the help of signal processing algorithms, the device is able to track slow environmental variations, and maintain high performance operation.

AW93001 is designed for replacing traditional mechanical button. It can be applied in many fields, such as consumer electronics, white goods and appliances, etc.

Applications

Wearable device, White goods and appliances

Replacing traditional mechanical button

Typical Application Circuit

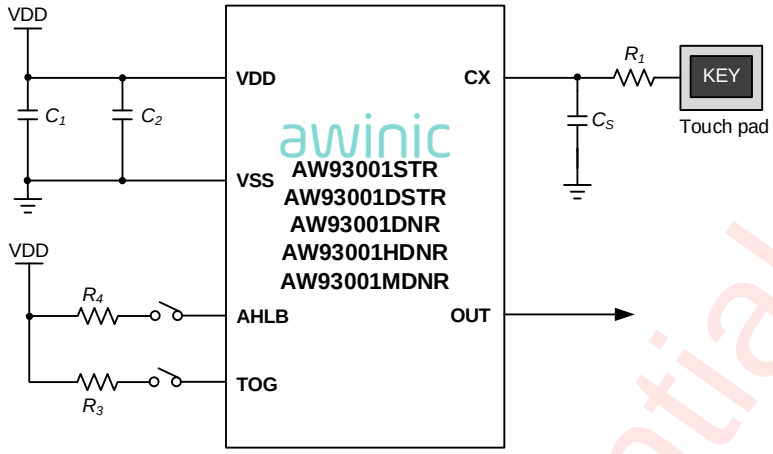


Figure 1 AW93001STR/DSTR/DNR/HDNR/MDNR Typical Application Circuit (push-pull output)

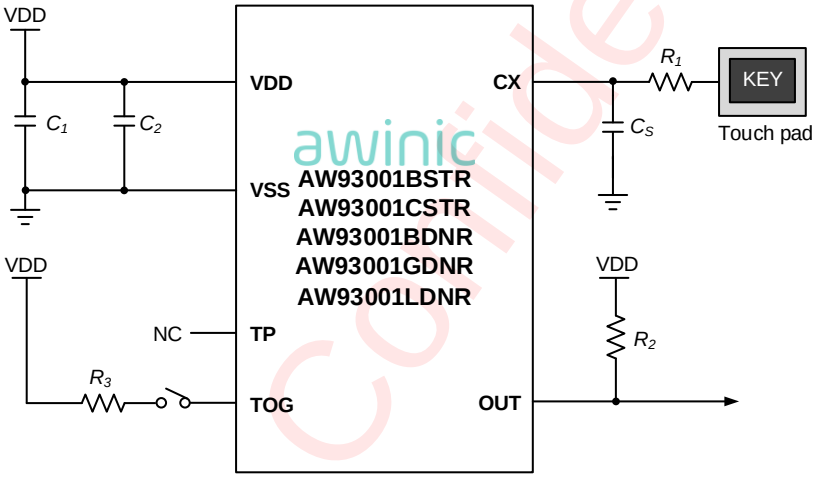


Figure 2 AW93001BSTR/CSTR/BDNR/GDNR/LDNR Typical Application Circuit (open-drain output)

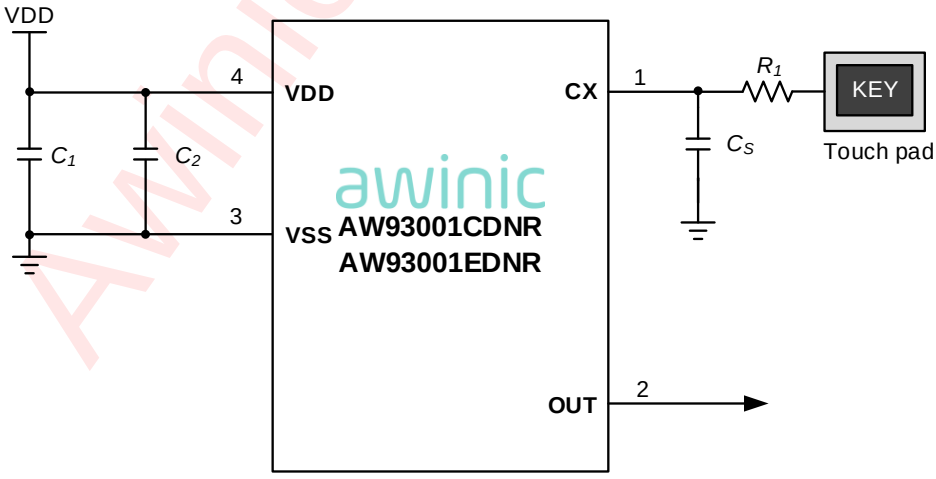


Figure 3 AW93001CDNR/EDNR Typical Application Circuit (push-pull output)

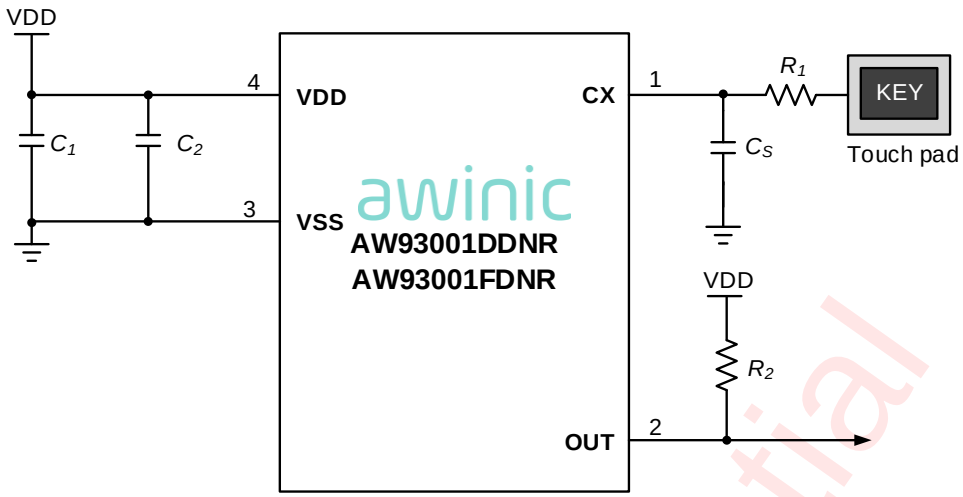
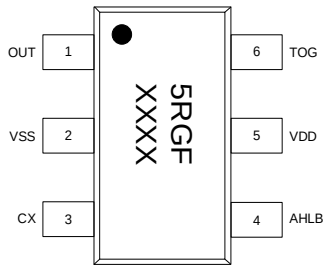


Figure 4 AW93001DDNR/FDNR Typical Application Circuit (open-drain output)

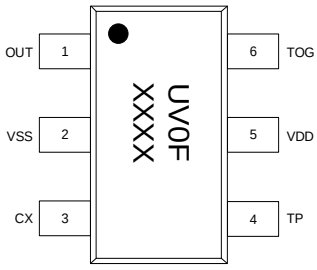
Pin Configuration And Top Mark

AW93001STR Top View



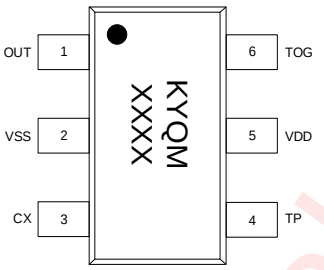
5RGF – AW93001STR
XXXX- Production Tracing Code

AW93001BSTR Top View



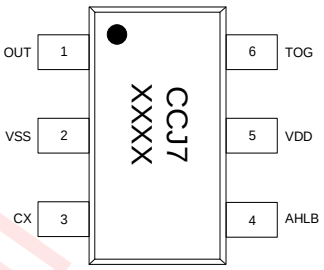
UV0F – AW93001BSTR
XXXX- Production Tracing Code

AW93001CSTR Top View



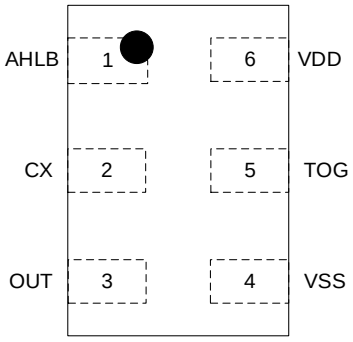
KYQM – AW93001CSTR
XXXX- Production Tracing Code

AW93001DSTR Top View

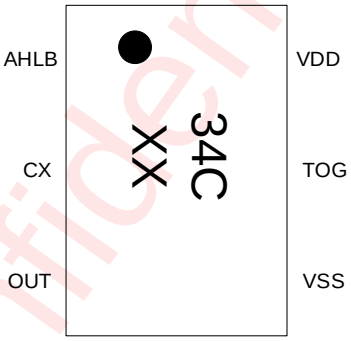


CCJ7 – AW93001DSTR
XXXX- Production Tracing Code

AW93001DNR
(Top View)

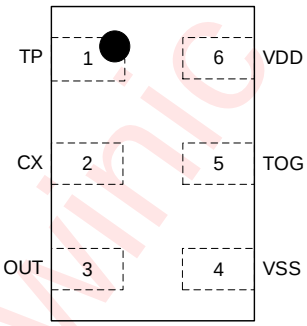


AW93001DNR Marking
(Top View)

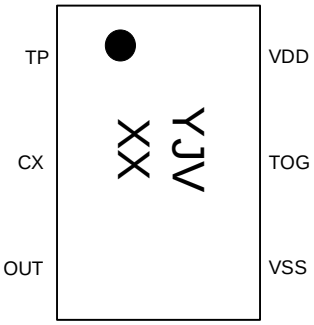


34C - AW93001DNR
XX - Production Tracing Code

AW93001BDNR
(Top View)

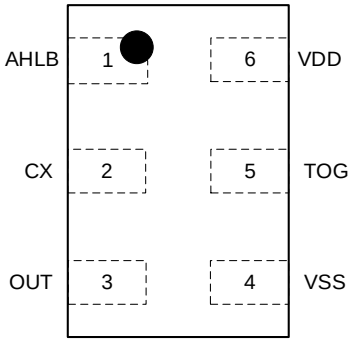


AW93001BDNR Marking
(Top View)

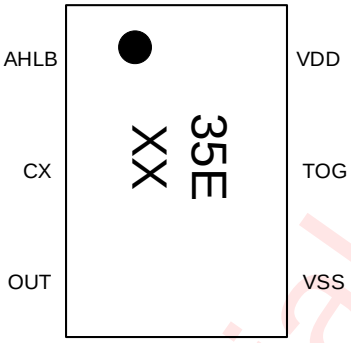


YJV - AW93001BDNR
XX - Production Tracing Code

AW93001HDNR
(Top View)

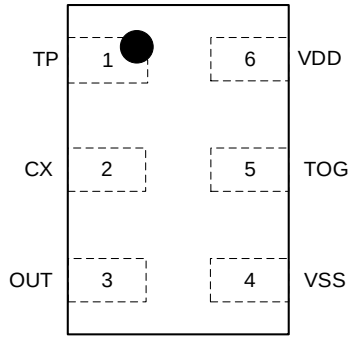


AW93001HDNR Marking
(Top View)

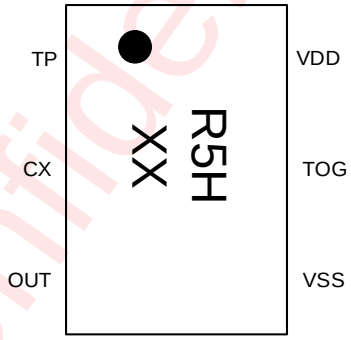


35E - AW93001HDNR
XX - Production Tracing Code

AW93001GDNR
(Top View)

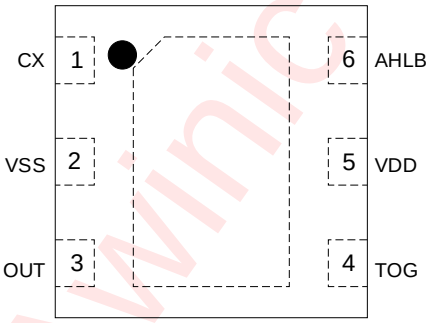


AW93001GDNR Marking
(Top View)

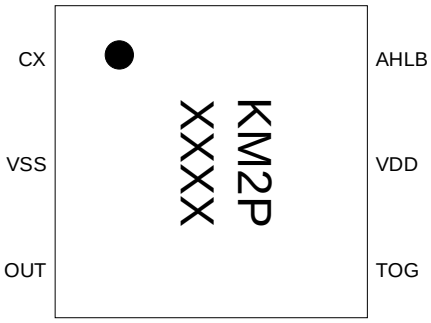


R5H - AW93001GDNR
XX - Production Tracing Code

AW93001MDNR
(Top view)

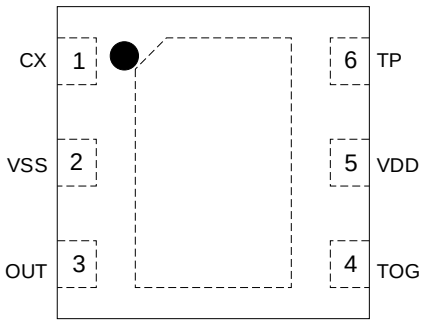


AW93001MDNR
(Top view)

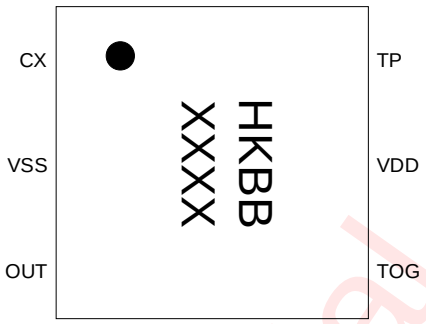


KM2P - AW93001MDNR
XXXX - Production Tracing Code

AW93001LDNR
(Top view)

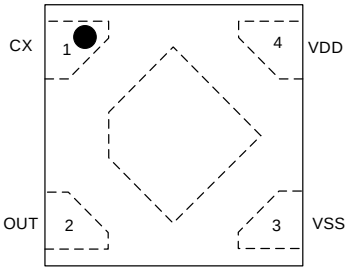


AW93001LDNR
(Top view)

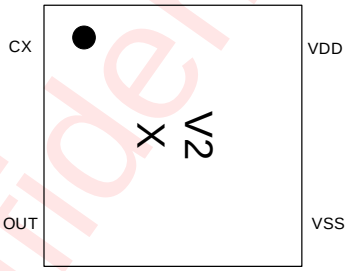


HKBB - AW93001LDNR
XXXX - Production Tracing Code

AW93001CDNR
(Top View)

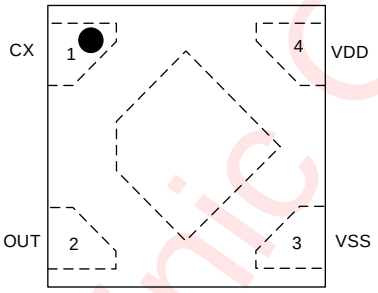


AW93001CDNR Marking
(Top View)

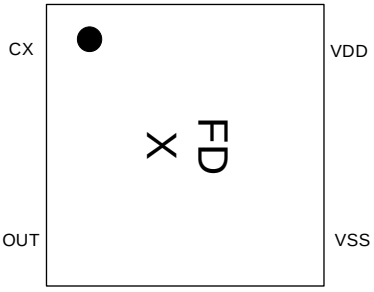


V2 - AW93001CDNR
X - Production Tracing Code

AW93001DDNR
(Top View)

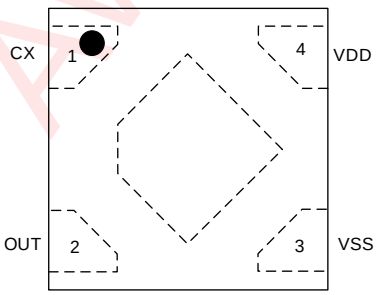


AW93001DDNR Marking
(Top View)

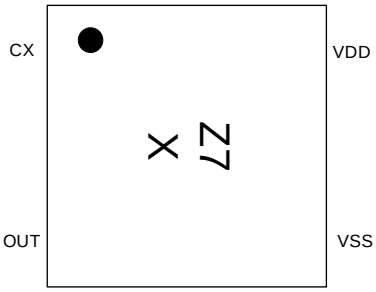


FD - AW93001DDNR
X - Production Tracing Code

AW93001EDNR
(Top View)

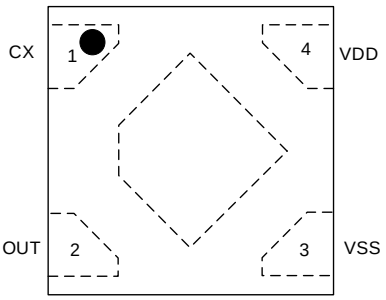


AW93001EDNR Marking
(Top View)

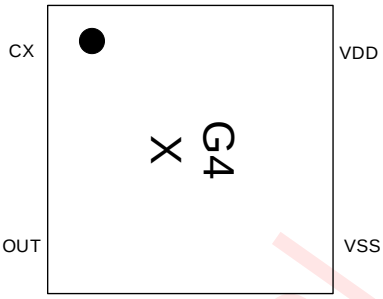


Z7 - AW93001EDNR
X - Production Tracing Code

AW93001FDNR
(Top View)



AW93001FDNR Marking
(Top View)



G4 - AW93001FDNR
X - Production Tracing Code

Pin Definition

Table 1 AW93001STR/DSTR/DNR/HDNR/MDNR Pin Definition

NAME	Pin No.			DESCRIPTION
	AW93001 STR/DSTR	AW93001 DNR/HDNR	AW93001 MDNR	
OUT	1	3	3	Push-pull output
VSS	2	4	2	Ground
CX	3	2	1	Capacitive detector input
AHLB	4	1	6	Output active high or low selection, internal pull-down resistor of 50kΩ Floating : Active high; Tied high: Active low
VDD	5	6	5	Power supply (2.4V~5.5V), requires decoupling capacitor
TOG	6	5	4	Output type option, internal pull-down resistor of 50kΩ Floating : Direct output; Tied high: Toggle output

Table 2 AW93001BSTR/CSTR/BDNR/GDNR/LDNR Pin Definition

NAME	Pin No.			DESCRIPTION
	AW93001 BSTR/CSTR	AW93001 BDNR/GDNR	AW93001 LDNR	
OUT	1	3	3	Open-drain output, requires pull-up resistor
VSS	2	4	2	Ground
CX	3	2	1	Capacitive detector input
TP	4	1	6	Test pin, typically floating
VDD	5	6	5	Power supply (2.4V~5.5V), requires decoupling capacitor
TOG	6	5	4	Output type option, internal pull-down resistor of 50kΩ Floating : Direct output; Tied high: Toggle output

Table 3 AW93001CDNR/DDNR/EDNR/FDNR Pin Definition

NAME	Pin No.	DESCRIPTION
CX	1	Capacitive detector input
OUT	2	Push-pull output (AW93001CDNR/EDNR) Open-drain output (AW93001DDNR/FDNR), require pull-up resistor
VSS	3	Ground
VDD	4	Power supply (2.4V~5.5V), requires decoupling capacitor

Device Comparison

Table 4 Device Comparison

Device	Package	Scan mode		MOT	Output Mode
		Fast scan	Slow scan		
AW93001STR	SOT23-6L	16ms	128ms	16s	Push-pull
AW93001BSTR	SOT23-6L	16ms	128ms		Open-drain
AW93001DNR	DFN1510-6L	16ms	128ms		Push-pull
AW93001BDNR	DFN1510-6L	16ms	128ms		Open-drain
AW93001HDNR	DFN1510-6L	16ms	--		Push-pull
AW93001GDNR	DFN1510-6L	16ms	--		Open-drain
AW93001MDNR	DFN2x2-6L	16ms	--		Push-pull
AW93001LDNR	DFN2x2-6L	16ms	--		Open-drain
AW93001CSTR	SOT23-6L	16ms	--	100s	Open-drain
AW93001DSTR	SOT23-6L	16ms	--		Push-pull
AW93001CDNR	DFN1x1-4L	16ms	128ms	16s	Push-pull
AW93001DDNR	DFN1x1-4L	16ms	128ms		Open-drain
AW93001EDNR	DFN1x1-4L	16ms	32ms		Push-pull
AW93001FDNR	DFN1x1-4L	16ms	32ms		Open-drain

Functional Block Diagram

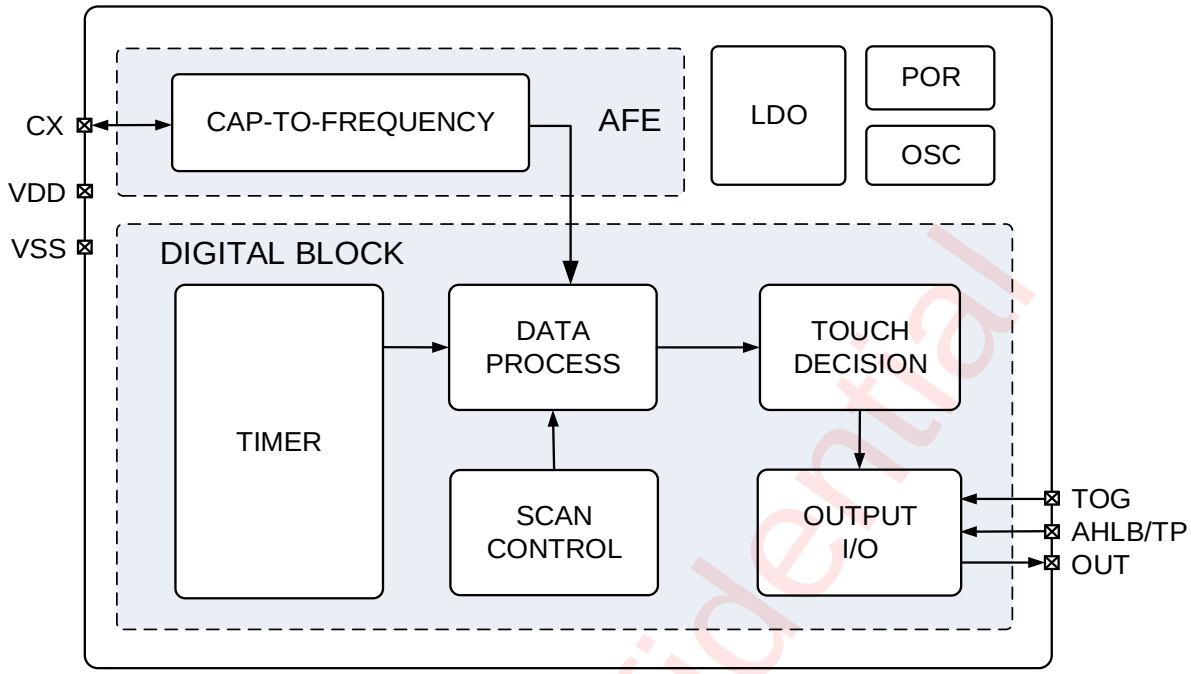


Figure 5 AW93001STR/BSTR/CSTR/DSTR/DNR/BDNR/HDNR/GDNR/MDNR/LDNR Functional Block Diagram

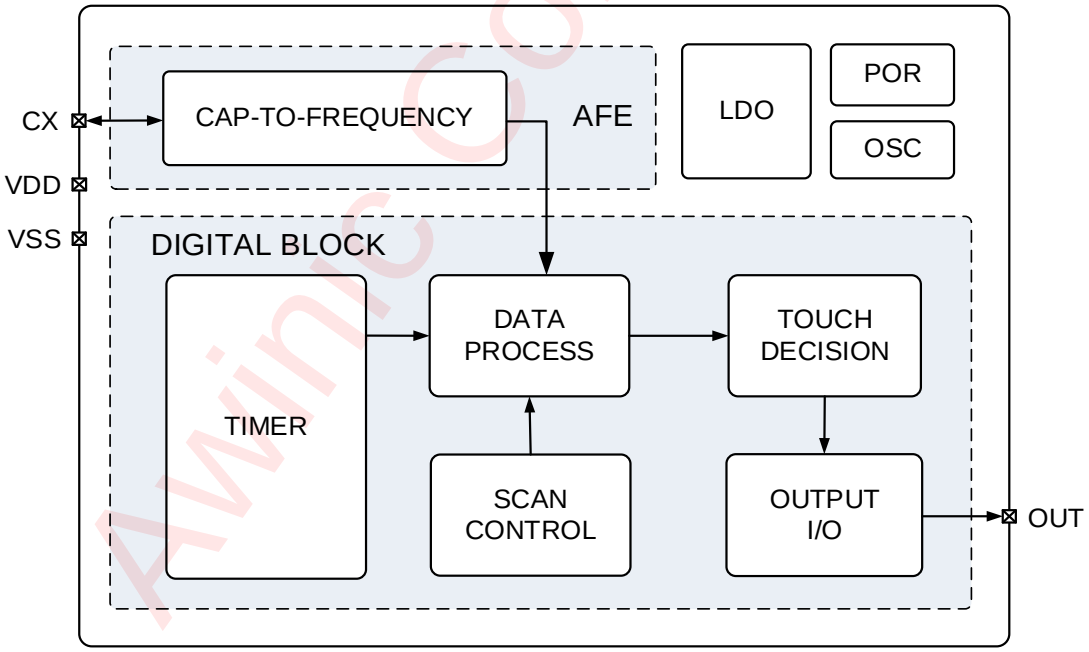


Figure 6 AW93001CDNR/DDNR/EDNR/FDNR Functional Block Diagram

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW93001STR	-40°C~85°C	SOT23-6L	5RGF	MSL3	ROHS+HF	3000 units/ Tape and Reel
AW93001BSTR	-40°C~85°C	SOT23-6L	UV0F	MSL3	ROHS+HF	3000 units/ Tape and Reel
AW93001CSTR	-40°C~85°C	SOT23-6L	KYQM	MSL3	ROHS+HF	3000 units/ Tape and Reel
AW93001DSTR	-40°C~85°C	SOT23-6L	CCJ7	MSL3	ROHS+HF	3000 units/ Tape and Reel
AW93001DNR	-40°C~85°C	DFN 1.5mmx1.0mm-6L	34C	MSL1	ROHS+HF	4500 units/ Tape and Reel
AW93001BDNR	-40°C~85°C	DFN 1.5mmx1.0mm-6L	YJV	MSL1	ROHS+HF	4500 units/ Tape and Reel
AW93001HDNR	-40°C~85°C	DFN 1.5mmx1.0mm-6L	35E	MSL1	ROHS+HF	4500 units/ Tape and Reel
AW93001GDNR	-40°C~85°C	DFN 1.5mmx1.0mm-6L	R5H	MSL1	ROHS+HF	4500 units/ Tape and Reel
AW93001MDNR	-40°C~85°C	DFN 2.0mmx2.0mm-6L	KM2P	MSL1	ROHS+HF	3000 units/ Tape and Reel
AW93001LDNR	-40°C~85°C	DFN 2.0mmx2.0mm-6L	HKBB	MSL1	ROHS+HF	3000 units/ Tape and Reel
AW93001CDNR	-40°C~85°C	DFN 1.0mmx1.0mm-4L	V2	MSL1	ROHS+HF	4500 units/ Tape and Reel
AW93001DDNR	-40°C~85°C	DFN 1.0mmx1.0mm-4L	FD	MSL1	ROHS+HF	4500 units/ Tape and Reel
AW93001EDNR	-40°C~85°C	DFN 1.0mmx1.0mm-4L	Z7	MSL1	ROHS+HF	4500 units/ Tape and Reel
AW93001FDNR	-40°C~85°C	DFN 1.0mmx1.0mm-4L	G4	MSL1	ROHS+HF	4500 units/ Tape and Reel

Absolute Maximum Ratings(NOTE1)

PARAMETERS		RANGE
Supply voltage range VDD		-0.3V to 6.0V
Input voltage range	CX, TP, AHLB, TOG	-0.3V to 6.0V
Output voltage range	OUT	-0.3V to 6.0V
Operating free-air temperature range		-40°C to 85°C
Maximum operating junction temperature T_{JMAX}		150°C
Storage temperature T_{STG}		-65°C to 150°C
Lead temperature (soldering 10 seconds)		260°C
ESD(Including CDM HBM)(NOTE2)		
HBM		±6kV
CDM		±1.5kV
Latch-Up		
Test condition: JESD78E		+IT: 200mA , -IT: -200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2017(HBM) ESDA/JEDEC JS-002-2018(CDM).

Electrical Characteristics

Note: Typical values are given for T_A = +25°C, VDD=3.0V unless otherwise specified.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
VDD	Operation voltage	-	2.4	3.0	5.5	V
I_{SL}	Current in slow scan mode	C_S=20pF, scan period=128ms	-	1.3	-	μA
		C_S=20pF, scan period=32ms	-	3.3	-	μA
I_{FS}	Current in fast scan mode	C_S=20pF, scan period=16ms	-	5.4	-	μA
V_{IH}	Input high level	Pin AHLB, TOG	1.4	-	-	V
V_{IL}	Input low level	Pin AHLB, TOG	-	-	0.4	V
I_{OH}	Output high current	VOH≥VDD-0.4V	-	-	-4	mA
I_{OL}	Output low current	VOL≤0.4V	8	-	-	mA
R_{PD}	Input pin pull-down resistor	Pin TOG, AHLB	-	50	-	kΩ
T_{RESP}	Response time(NOTE3)	Fast scan mode, scan period=16ms	34	-	48	ms
		Slow scan mode, scan period=32ms	34	-	64	ms
		Slow scan mode, scan period=128ms	34	-	160	ms

NOTE3: It has an error of ± 10% according to the mass production test data.

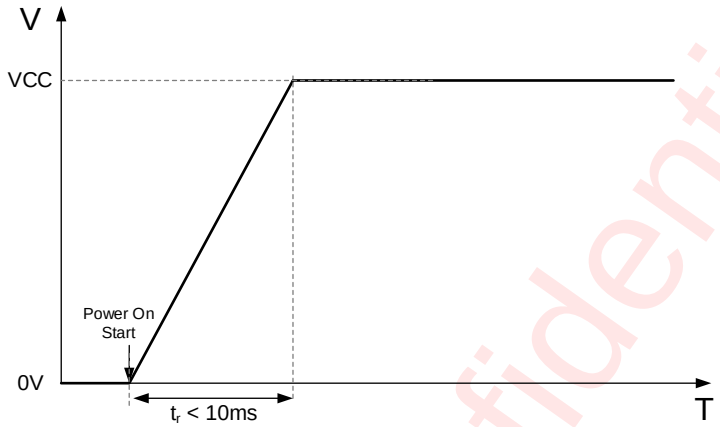
Detailed Functional Description

Power On Timing

To ensure that the internal configuration parameters are correctly loaded during each power-on process of AW93001, the power design of AW93001 needs to follow the following power-on timing limit:

During the process of voltage rise or normal power supply, abnormal voltage fluctuations can not occur in the power supply. The peak to peak value of voltage fluctuation should below 200mV.

As the following timing figure:



Note: Especially during the battery welding process, abnormal voltage fluctuations may occur.

Figure 3 AW93001 Power on Timing

Initialization

After power-on, the chip executes initialization process automatically, it lasts for about 500ms. During initialization, touch decision does not work, and no touch status can be reported.

Scan Mode

The AW93001STR/BSTR/DNR/BDNR/CDNR/DDNR have two scan modes, fast scan mode and slow scan mode, In fast scan mode, the scan period is about 16ms, and the maximum response time is about 48ms. In slow scan mode, the scan period is about 128ms with lower power consumption, and the maximum response time is about 160ms. For power saving, the device automatically switches scan mode between fast and slow mode according to touch detection status. After power-on, the device enters fast scan mode directly. In fast scan mode, if there is no touch detected for 8s continuously, the device switches to slow scan mode. In slow scan mode, if touch is detected, the device returns to fast scan mode at once.

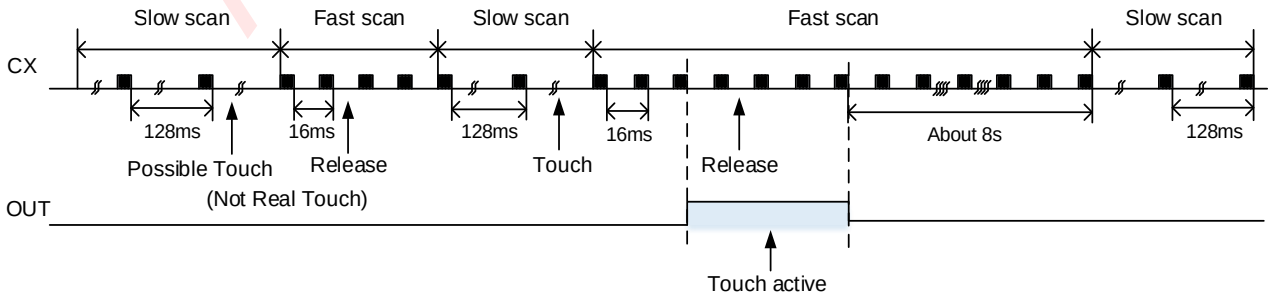


Figure 7 AW93001STR/BSTR/DNR/BDNR/CDNR/DDNR Scan Mode

The AW93001EDNR/FDNR have two scan modes, fast scan mode and slow scan mode, In fast scan mode, the scan period is about 16ms, and the maximum response time is about 48ms. In slow scan mode, the scan period is about 32ms with lower power consumption, and the maximum response time is about 64ms.

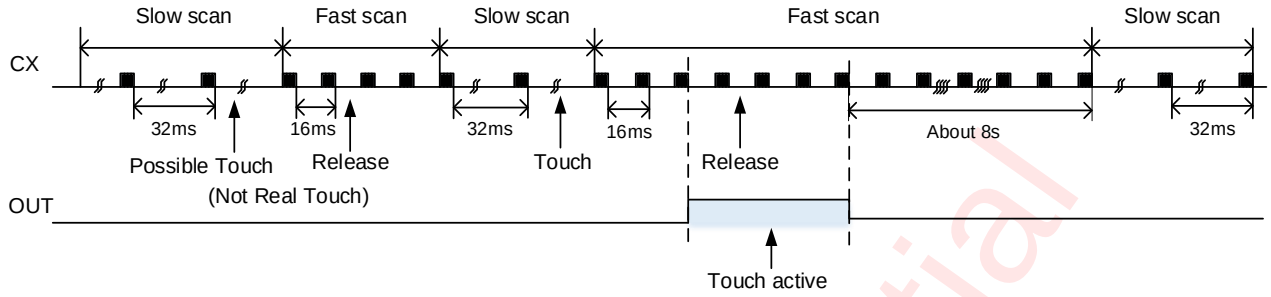


Figure 8 AW93001EDNR/FDNR Scan Mode

The AW93001CSTR/DSTR/HDNR/GDNR/MDNR/LDNR only has fast scan mode. In fast scan mode, the scan period is about 16ms, and the maximum response time is about 48ms. After power-on, the device enters fast scan mode directly and keeps it all the time.

Output Mode

For AW93001STR/DNR/HDNR/MDNR, pin OUT is a push-pull output, and the output mode depends on the initial power-on states of pin AHLB and pin TOG. Pin TOG selects direct output or toggle output, and pin AHLB selects active high or active low.

Table 5 AW93001STR/DSTR/DNR/HDNR/MDNR Output Mode

Pin TOG	Pin AHLB	Pin OUT's output mode
Floating	Floating	Direct output, active high
Floating	Tied high	Direct output, active low
Tied high	Floating	Toggle output, initial state is low
Tied high	Tied high	Toggle output, initial state is high

For AW93001BSTR/CSTR/BDNR/GDNR/LDNR, pin OUT is an open-drain output, and the output mode only depends on the initial power-on state of pin TOG.

Table 6 AW93001BSTR/CSTR/BDNR/GDNR/LDNR Output Mode

Pin TOG	Pin OUT's output mode
Floating	Direct output, active low
Tied high	Toggle output, initial state is high-Z

When pin AHLB or pin TOG is tied high, the internal pull-down function of these pin is closed, so no additional power consumption will be generated.

For AW93001CDNR/EDNR, pin OUT is a push-pull output, and the output is high level active.

For AW93001DDNR/FDNR, pin OUT is an open-drain output, and the output is low level active.

Maximum Key-on Duration Time

In order to prevent the false touch detection caused by objects covering the touch pad, the chip sets maximum key-on duration time. For AW93001STR/BSTR/DNR/BDNR/HDNR/GDNR/MDNR/LDNR/CDNR/DDNR/EDNR /FDNR/CDNR/DDNR/EDNR/FDNR, if the devices' touch status last over 16s, it will be released until a new touch action. For AW93001CSTR/DSTR, if the devices' touch status last over 100s, it will be released until a new touch action.

Application Information

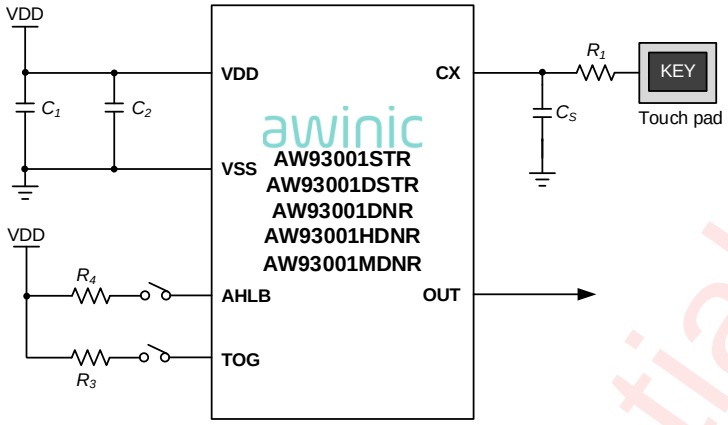


Figure 9 AW93001STR/DSTR/DNR/HDNR/MDNR Typical Application Circuit (push-pull output)

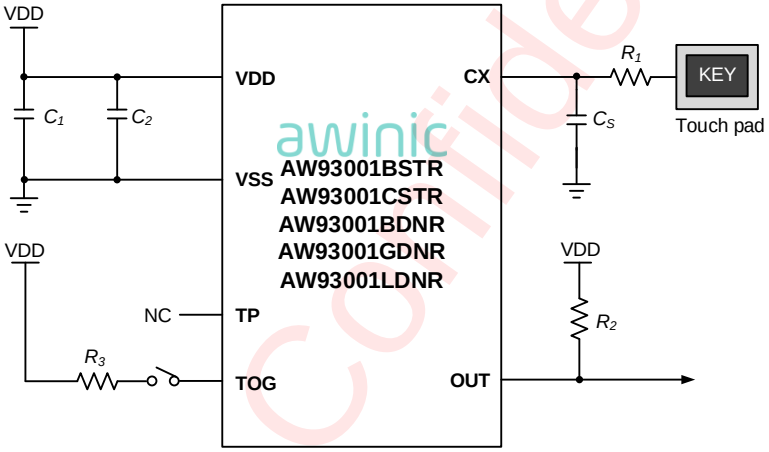


Figure 10 AW93001BSTR/CSTR/BDNR/GDNR/LDNR Typical Application Circuit (open-drain output)

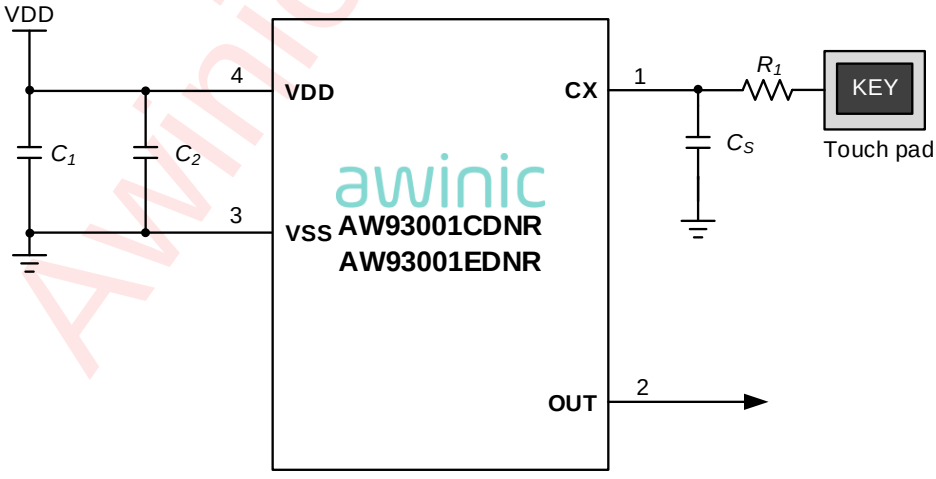


Figure 11 AW93001CDNR/EDNR Typical Application Circuit(push-pull output)

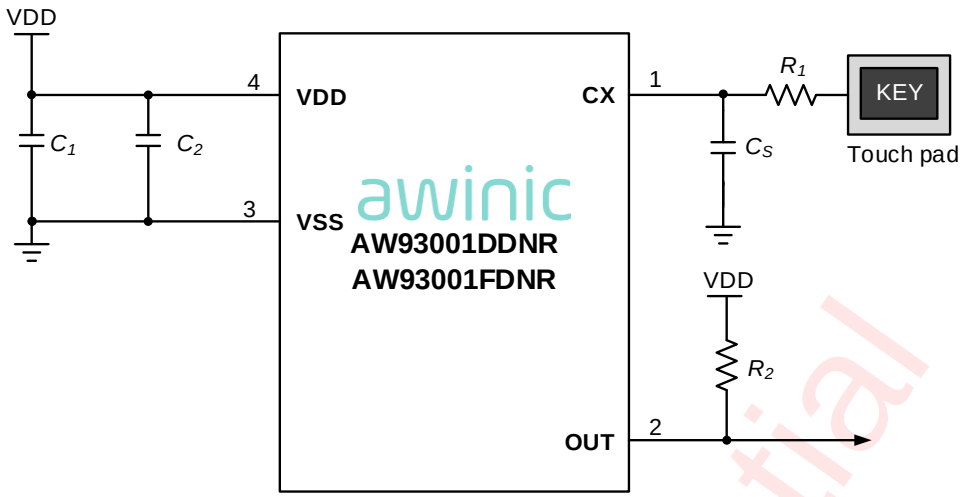


Figure 12 AW93001DDNR/FDNR Typical Application Circuit(open-drain output)

To obtain the optimal performance, the capacitive touch controller's application circuit should be considered carefully. Here are some guidelines:

1. The chip should be supplied by stable power, otherwise it may cause abnormal sensitivity or false detection.
2. Add a resistor R_1 between C_S and Touch pad to improve ESD protection and reduce EMI.
3. Sensitivity can be adjusted by C_S. The smaller the C_S, the higher the sensitivity, the higher the power consumption. It is suggested to use temperature insensitive capacitors to adjust the sensitivity, such as NP0 capacitors.
4. Sensitivity can be adjusted by the electrode size. Using a larger electrode size can increase sensitivity, but the electrode size must be used in the effective scope.
5. Sensitivity can be adjusted by the panel thickness. Using a thinner panel can increase sensitivity, but the panel thickness must be used in the effective scope.

Recommended Components List

Component	Name	Description	Typ.	Unit
C	C_1	-	1	μF
	C_2	-	0.1	μF
	C_S	5% resolution Low temperature coefficient	-	pF
R	R_1	5% resolution	4.7	kΩ
	R_2	5% resolution	100	kΩ
	R_3	5% resolution	4.7	kΩ
	R_4	5% resolution	4.7	kΩ

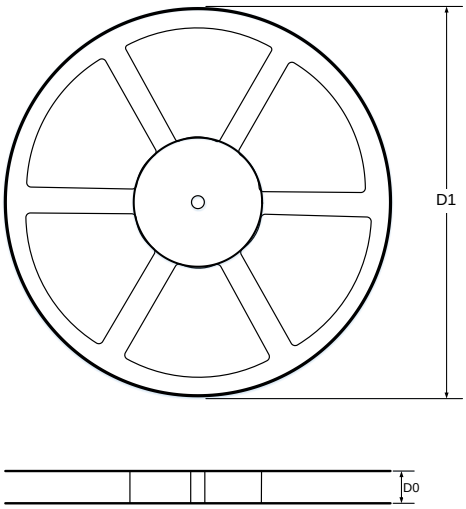
PCB Layout Consideration

To obtain the optimal performance, PCB layout should be considered carefully. Here are some guidelines:

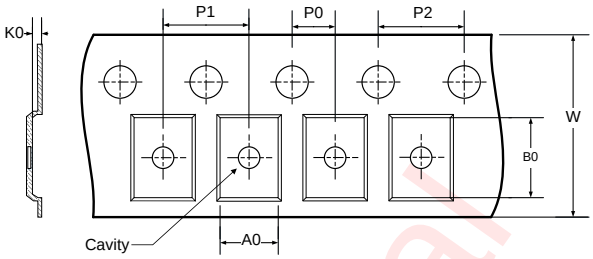
1. The connections between the capacitors (C_1, C_2) and the IC as short as possible, to reduce noise and EMI.
2. The distance from the touch pad to the pin CX as short as possible, and the signal trace as thin as possible.
3. The IC and sensor traces surrounded by ground, both top and bottom layers filled with ground plane.
4. The sensor and traces away from mic, earphone line, because capacitive sensor will disturb audio line.
5. The sensor and traces away from interferences, such as communication lines.
6. The material of panel covering the PCB cannot contain metal or electric element, and the surface coating is the same.

Tape And Reel Information

REEL DIMENSIONS

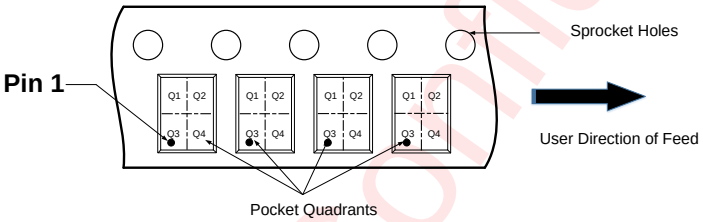


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

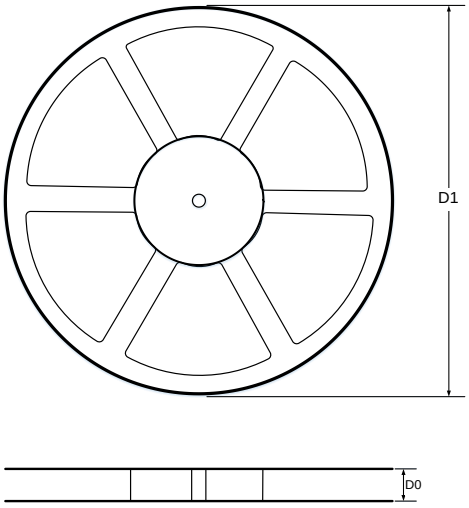
DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.4	3.3	3.2	1.4	2	4	4	8	Q3

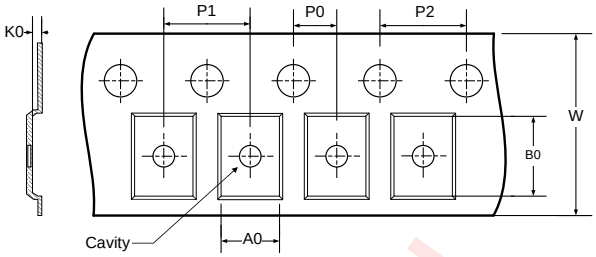
All dimensions are nominal

AW93001STR/BSTR/CSTR/DSTR Tape And Reel Information

REEL DIMENSIONS

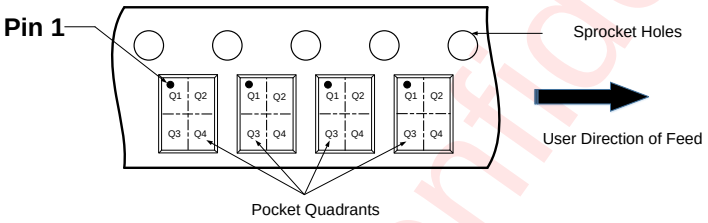


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

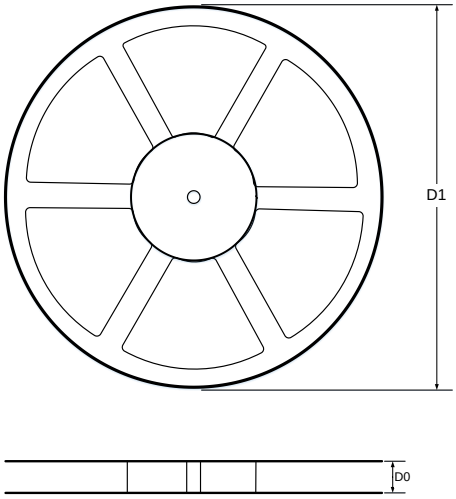
DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.4	1.12	1.72	0.7	2	4	4	8	Q1

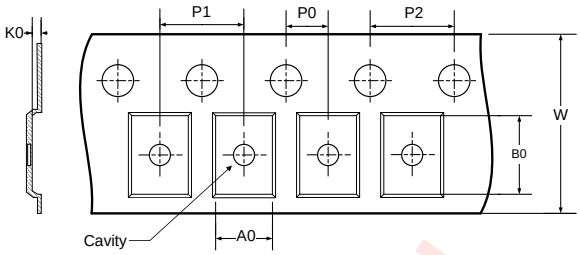
All dimensions are nominal

AW93001DNR/BDNR/HDNR/GDNR Tape And Reel Information

REEL DIMENSIONS

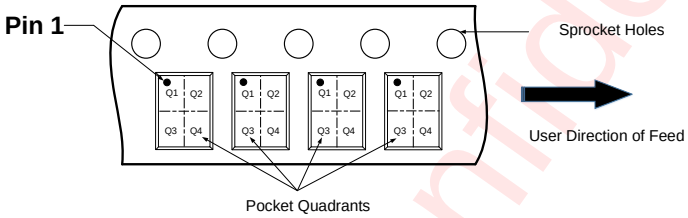


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

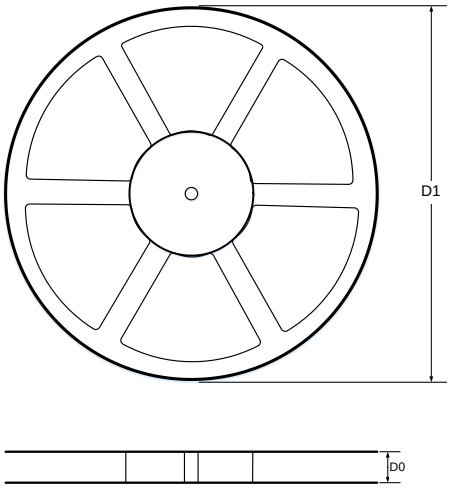
DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.4	2.3	2.3	1	2	4	4	8	Q1

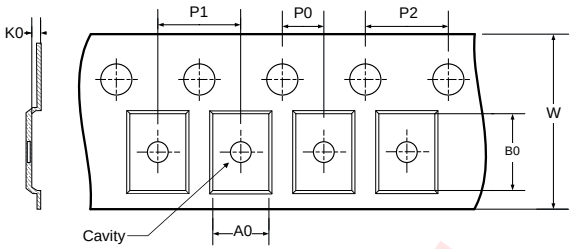
All dimensions are nominal

AW93001MDNR/LDNR Tape And Reel Information

REEL DIMENSIONS

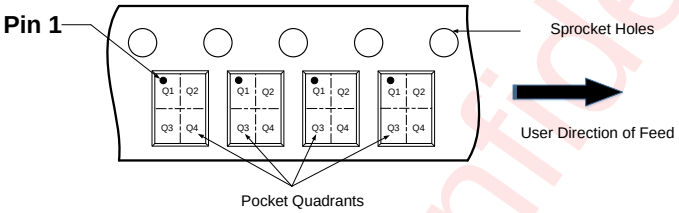


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

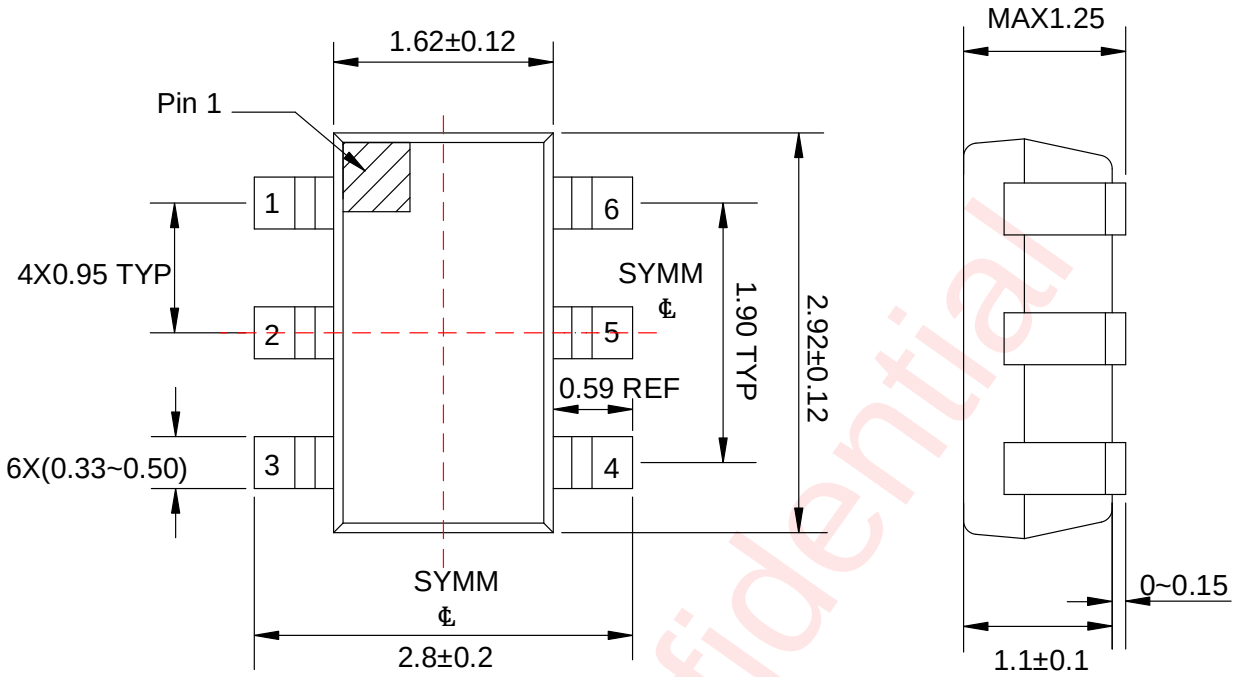
DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.4	1.15	1.15	0.5	2	4	4	8	Q1

All dimensions are nominal

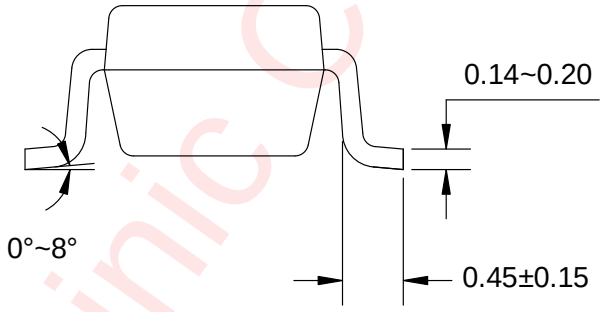
AW93001CDNR/DDNR/EDNR/FDNR Tape And Reel Information

Package Description



Top View

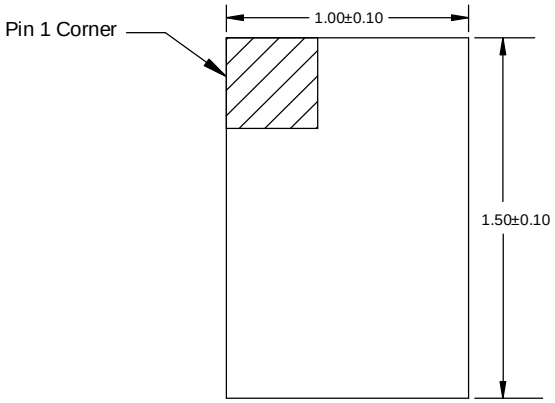
Side View



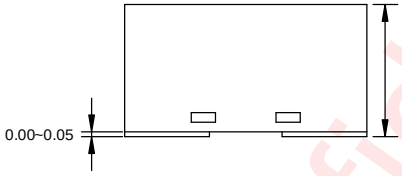
Side View

Unit: mm

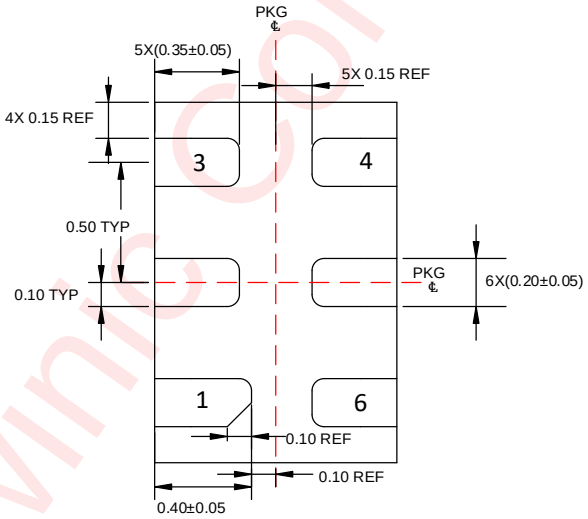
AW93001STR/BSTR/CSTR/DSTR Package Description



Top View



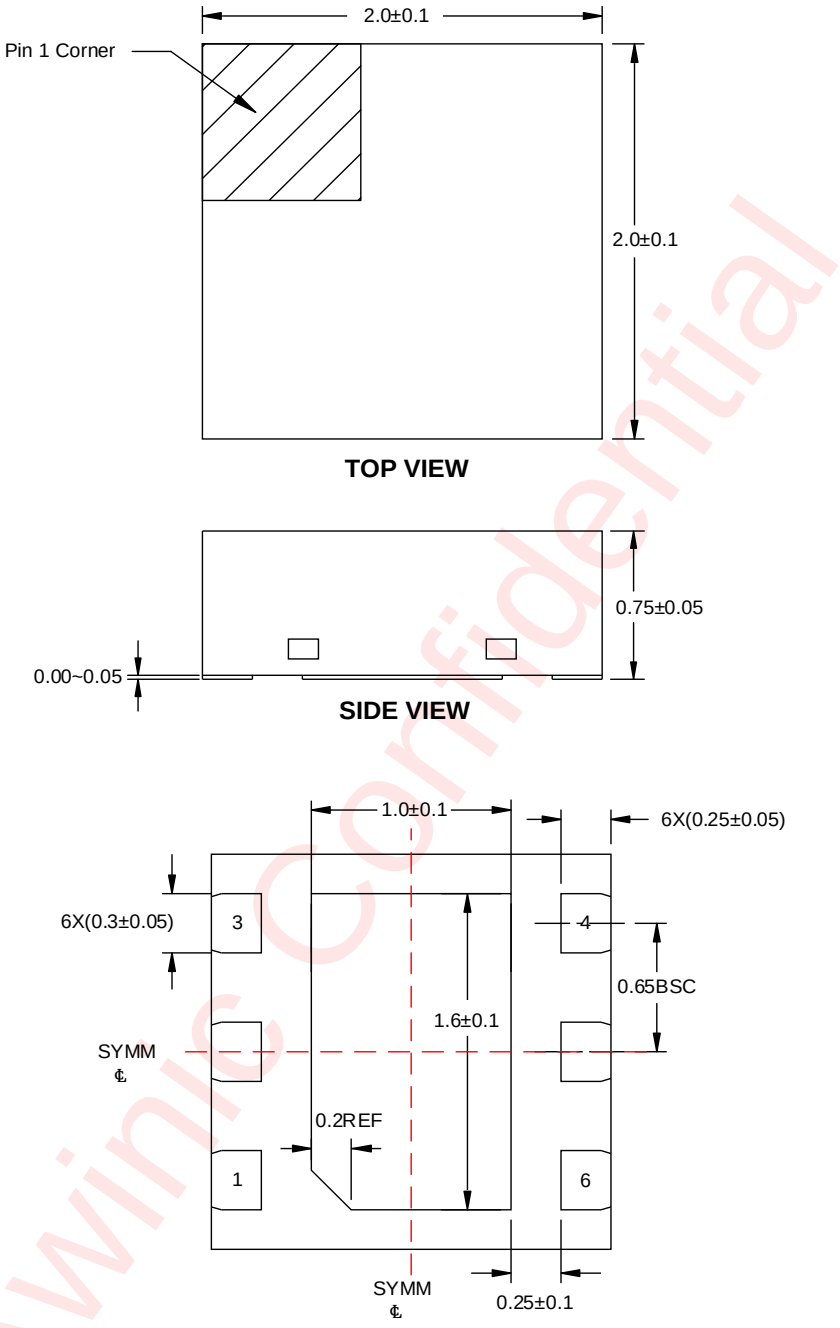
Side View



Bottom View

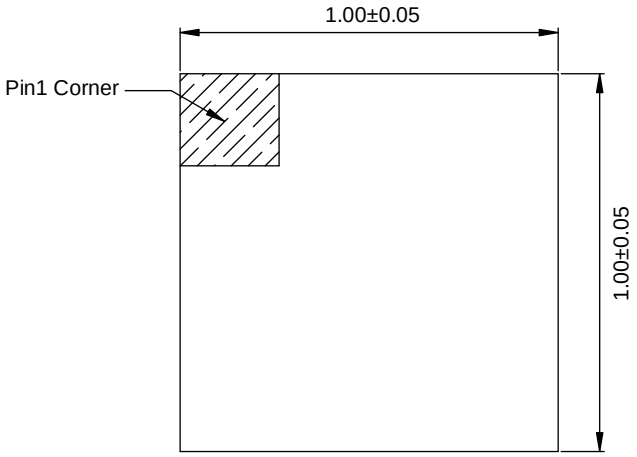
Unit：mm

AW93001DNR/BDNR/HDNR/GDNR Package Description

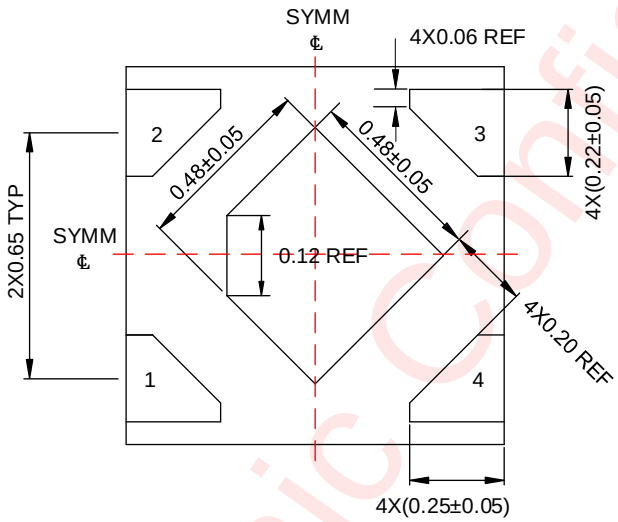


Unit:mm

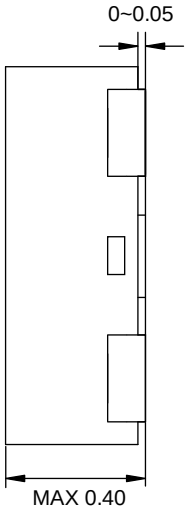
AW93001MDNR/LDNR Package Description



Top View



Bottom View

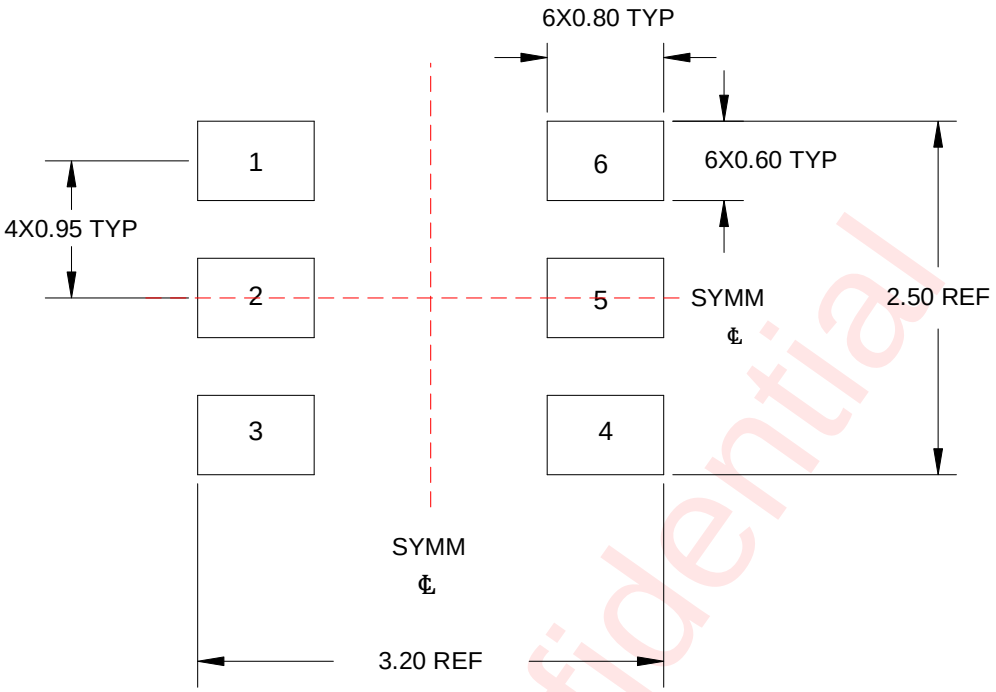


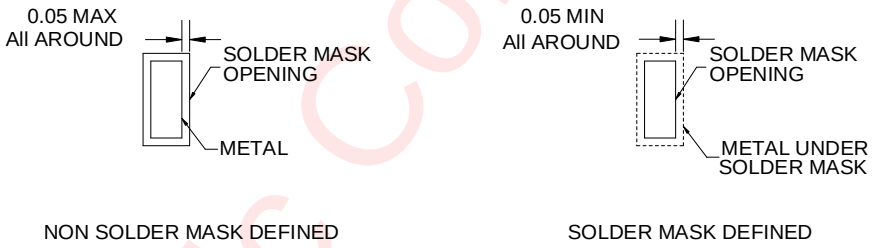
Side View

Unit:mm

AW93001CDNR/DDNR/EDNR/FDNR Package Description

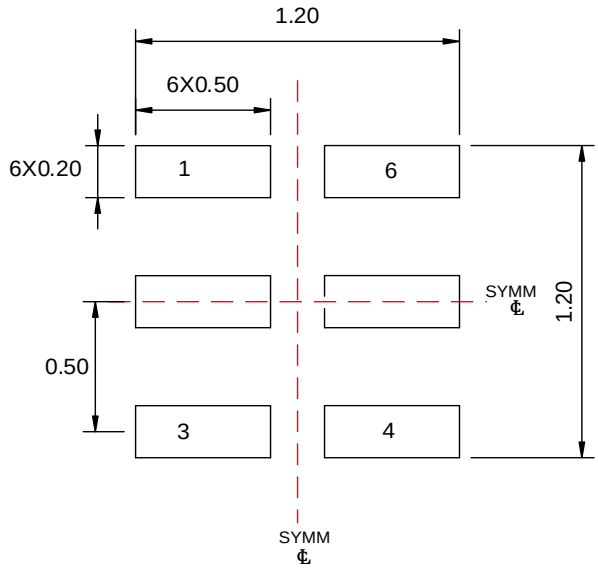
Land Pattern Data

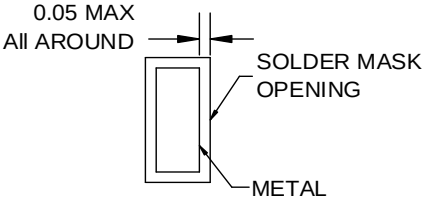




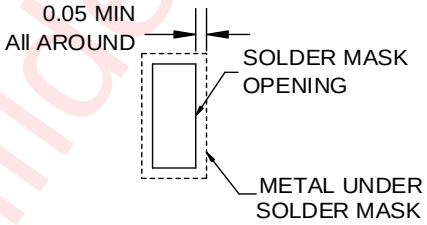
Unit：mm

AW93001STR/BSTR/CSTR/DSTR Land Pattern Data





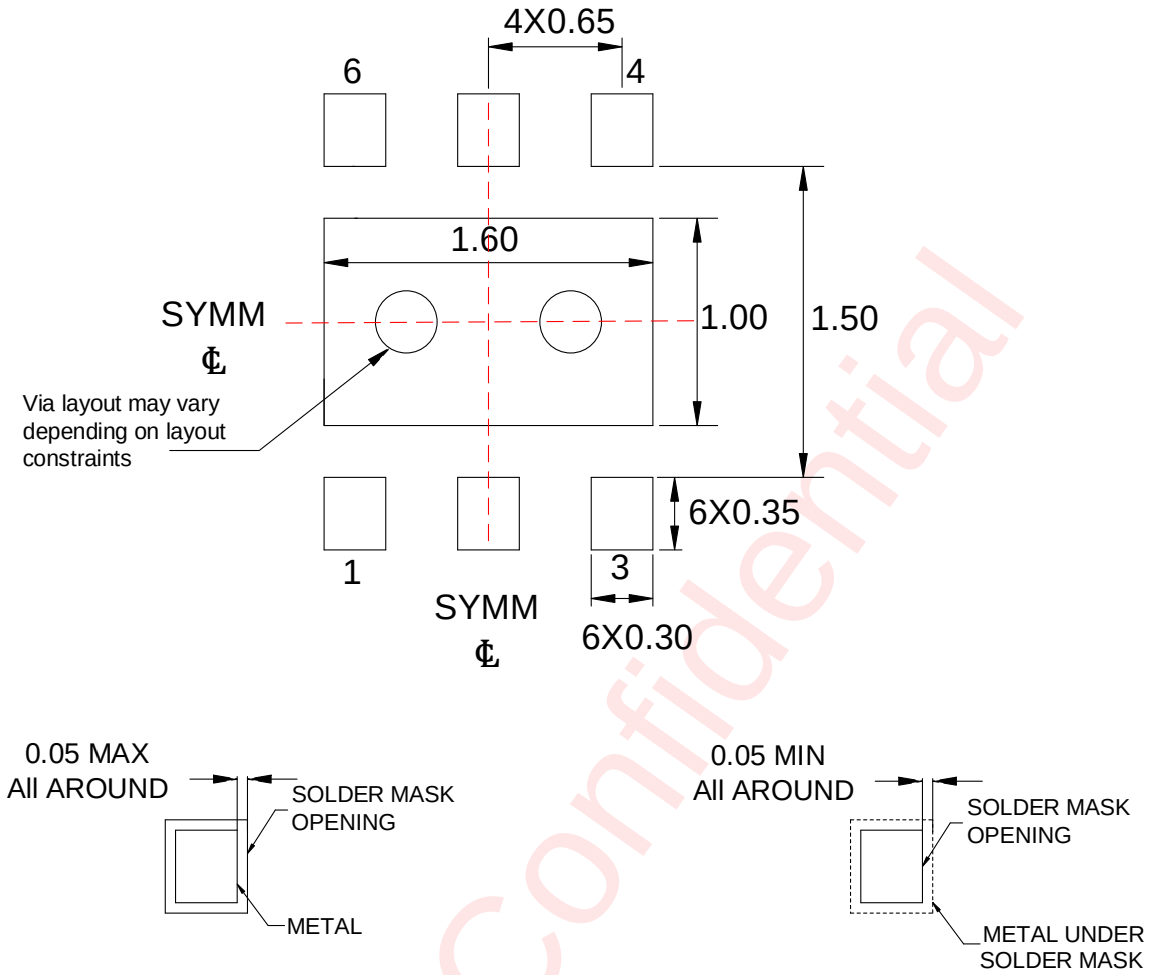
NON SOLDER MASK DEFINED



SOLDER MASK DEFINED

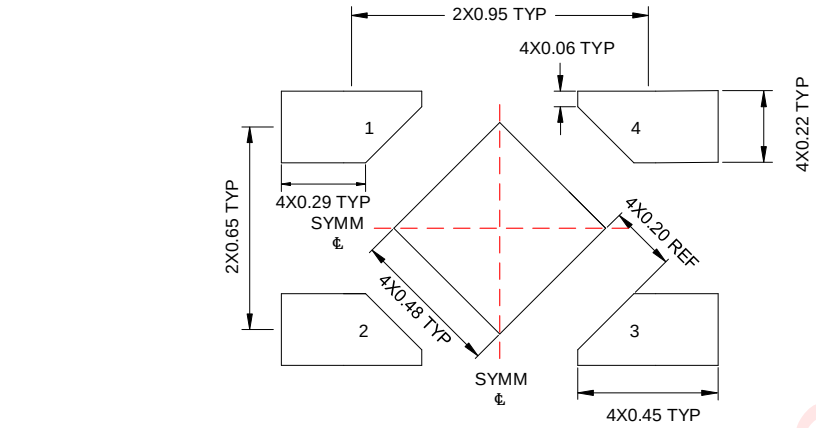
Unit: mm

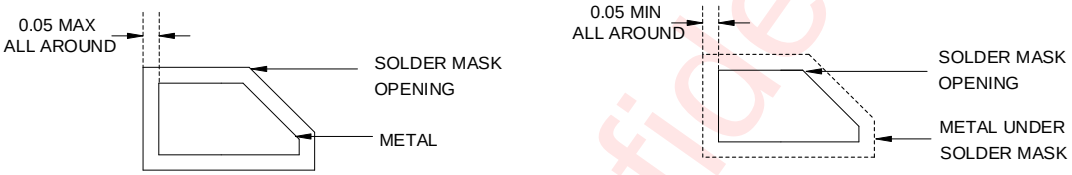
AW93001DNR/BDNR/HDNR/GDNR Land Pattern Data



Unit:mm

AW93001MDNR/LDNR Land Pattern Data





NON SOLDER MASK DEFINED SOLDER MASK DEFINED

Unit : mm

AW93001CDNR/DDNR/EDNR/FDNR Land Pattern Data

Revision History

Version	Date	Change Record
V1.0	Feb.2021	Officially released
V1.1	Feb.2021	Merge the AW93001STR/BSTR/DNR/BDNR's datasheet; Add a resistor between C_S and Touch pad in Typical Application Circuit
V1.2	May.2021	Update Ordering Information
V1.3	Jul.2021	Add the chip,AW93001HDNR's information
V1.4	Jul.2021	Correct the AW93001HDNR's tracing code, update the package DFN1510-6's POD information
V1.5	Jul.2021	Add the chip,AW93001GDNR's information, update the Device Comparison table
V1.6	Nov.2021	Add the chip,AW93001MDNR/LDNR's information, update the Device Comparison table； Correct the R3 resistor value in Recommended Components List.
V1.7	Dec.2021	Update Ordering Information
V1.8	Mar.2022	Update Device Comparison, correct the AW93001STR/BSTR/DNR/BDNR's MOT value, update Functional Block Diagram.
V1.9	May.2022	Add the chip, AW93001CSTR's information, update the Device Comparison table
V2.0	Sep.2022	Update the Absolute Maximum Ratings, correct the maximum voltage range； Update the AW93001STR/BSTR/CSTR Tape And Reel Information
V2.1	Oct.2022	Add the chip,AW93001DSTR's information, update the Device information
V2.2	Jul.2023	Add the minimum response time in the table of Electrical Characteristics (P7).
V2.3	Sep.2023	Add the part of Capacitor Cs Selection (P10~P11).
V2.4	Jan.2024	Update the description of features (P1). Delete the part of Capacitor Cs Selection (P10).
V2.5	Jul. 2024	Update the power consumption(P1 and P7)
V2.6	Jul. 2024	Add the chip: AW93001CDNR/DDNR/EDNR/FDNR
V2.7	Feb. 2025	Add the power on timing(P12)

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