9 MULTI-FUNCTION LED DRIVER WITH I²C INTERFACE

FEATURES

- 9-channel RGB LED Driver
  - Global 256-levels DC current configuration
  - Individual 4096-levels PWM for dimming
  - Individual 256-levels current for color-mixing
  - Dither function
- High-precision current sinks
  - Device-to-device error: ±5%
  - Channel-to-channel error: ±5%
- EMI and audible noise reduction
  - Phase delay and phase inverting scheme
  - Slew rate control function
- Flexible LED lighting pattern control
- LED open/short detection per channel
- Auto power save mode when all LEDs off > 32ms
- Under voltage lock out and over temperature protection
- 1MHz I²C interface, 4 selectable addresses: 20h, 21h, 24h, 25h
- Power supply: 2.7V~5.5V
- QFN 3mmX3mmX0.75mm-20L package

APPLICATIONS

Cell Phone

Keyboard

PDA/MP3/MP4/CD/Mini display

Smart home appliance

GENERAL DESCRIPTION

AW21009G is a 9-channel multi-function LED driver. Each channel has individual 8-bit DC current setting for color-mixing and maximum 12-bit PWM resolution for brightness control. The global current of each channel is recommended to be 40mA configured via register and external Resistor R_{EXT}.

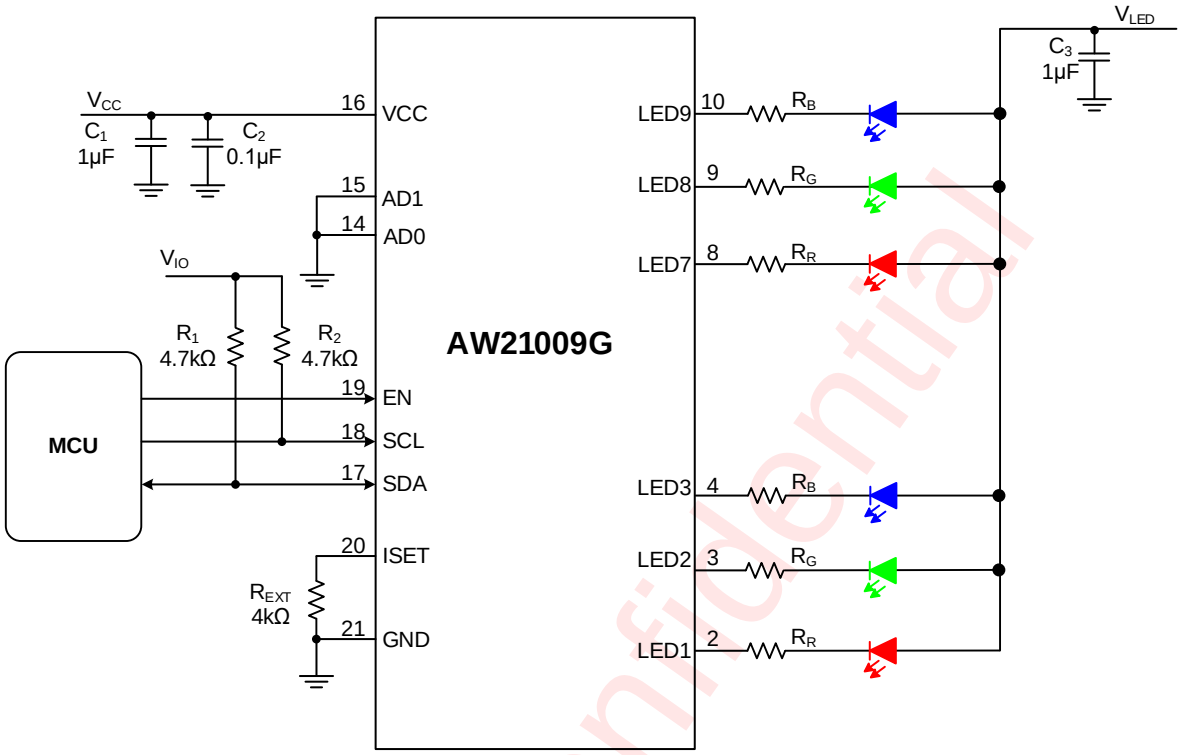
Group control mode, autonomous breathing pattern and rapid RGB control mode are provided for flexible, high efficiency lighting effect programming and fast display updating.

Programmable phase-shifting and spread spectrum technology are utilized to reduce EMI and audible noise caused by MLCC when LEDs turn on or off simultaneously.

AW21009G can be turned off with minimum current consumption by either pulling the EN pin low or using the software shutdown feature.

AW21009G is available in QFN 3mmX3mmX 0.75mm-20L package. It operates from 2.7V to 5.5V over the temperature range of -40°C to 105°C.

TYPICAL APPLICATION CIRCUIT



Note1: The resistor R_R /R_G /R_B are only thermal reduction. And they are determined by V_{LED}, VF of LED, $V_{DROPOUT}$ of LEDx and I_{LED}. R_X=(V_{LED}-VF_X-$V_{DROPOUT}$)/I_{LED}.
Note2: The resistor R_1 and R_2 are equal to 4.7kΩ at 400kHz I^2C, at 1MHz I^2C R_1 and R_2 are equal to 1kΩ.

Figure 1 AW21009G Application Circuit

PIN CONFIGURATION AND TOP MARK

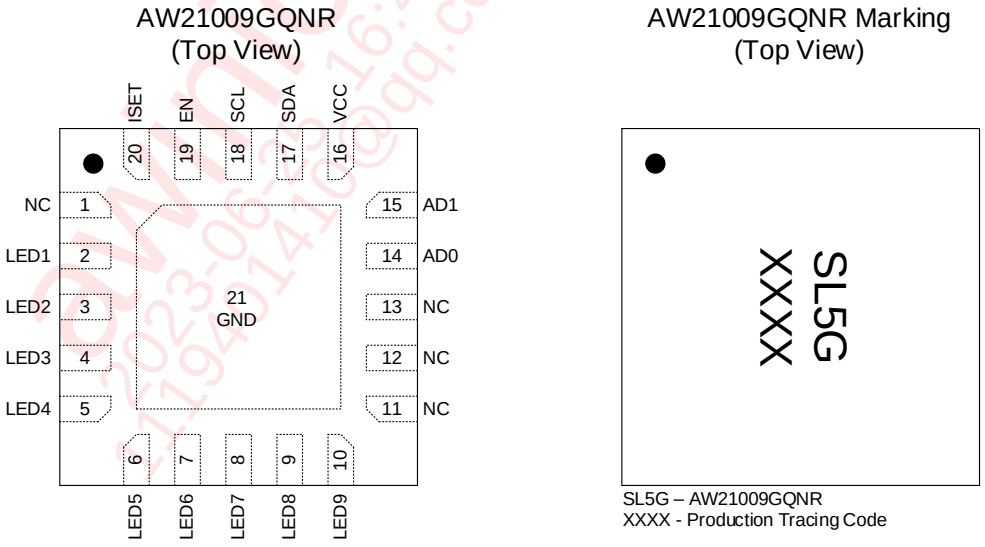


Figure 2 Pin Configuration and Top Mark

PIN DEFINITION

No.	NAME	DESCRIPTION
1	NC	Not connected.
2~10	LED1~LED9	Constant current sink, connect to LED's cathode.
11~13	NC	Not connected.
14	AD0	I²C interface device address, connects to GND, VCC for different device address of I²C.
15	AD1	I²C interface device address, connects to GND, VCC for different device address of I²C.
16	VCC	Power supply: 2.7V~5.5V.
17	SDA	Serial data I/O for I²C interface.
18	SCL	Serial clock input for I²C interface.
19	EN	Shutdown the chip when pulled low.
20	ISET	When R_{EXT}=4.0kΩ, global current of LED is 40mA.
21	GND	Ground.

FUNCTIONAL BLOCK DIAGRAM

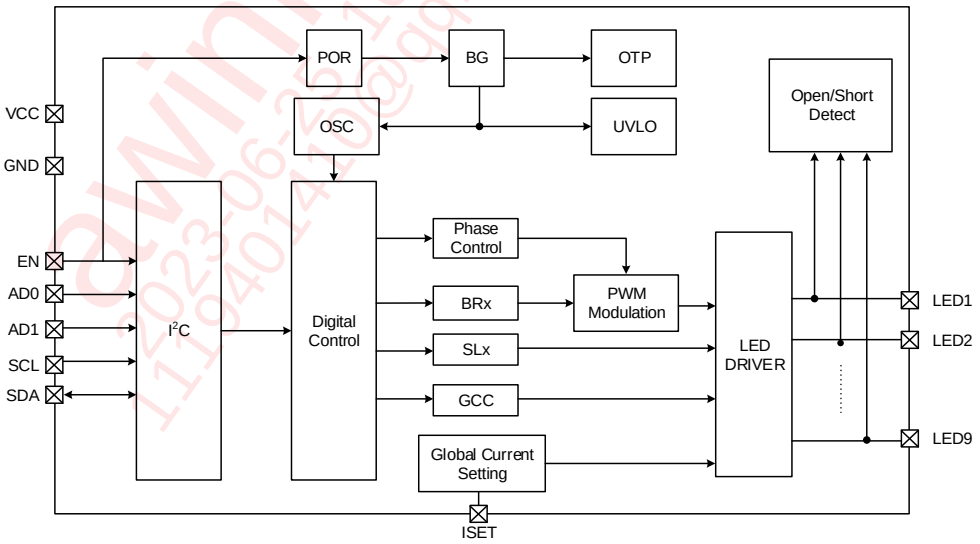
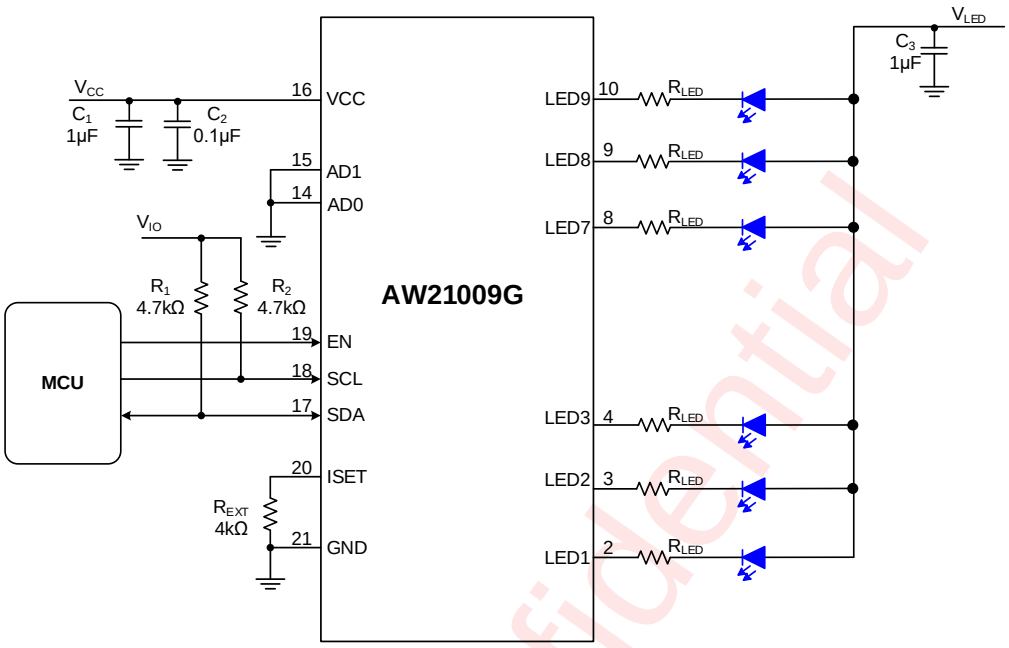


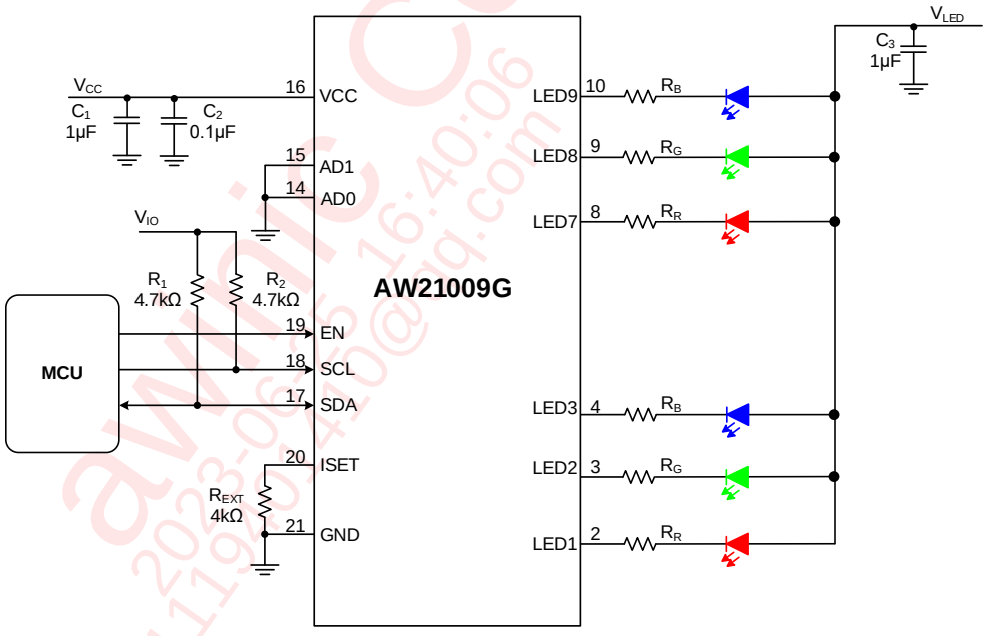
Figure 3 Functional Block Diagram

TYPICAL APPLICATION CIRCUITS



Note1: The resistor R_{LED} is only thermal reduction, and it is determined by V_{LED}, VF of LED, $V_{DROPOUT}$ of LEDx and I_{LED}. $R_{LED}=(V_{LED}-VF-V_{DROPOUT})/I_{LED}$.
Note2: The resistor R_1 and R_2 are equal to 4.7kΩ at 400kHz I^2C, at 1MHz I^2C R_1 and R_2 are equal to 1kΩ.

Figure 4 Typical Application Circuit



Note1: The resistor R_R /R_G /R_B are only thermal reduction. And they are determined by V_{LED}, VF of LED, $V_{DROPOUT}$ of LEDx and I_{LED}. $R_X=(V_{LED}-VF_X-V_{DROPOUT})/I_{LED}$.
Note2: The resistor R_1 and R_2 are equal to 4.7kΩ at 400kHz I^2C, at 1MHz I^2C R_1 and R_2 are equal to 1kΩ.

Figure 5 Typical Application Circuit (RGB)

ORDERING INFORMATION

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW21009GQNR	-40°C~105°C	QFN 3X3-20L	SL5G	MSL1	ROHS+HF	6000 units/ Tape and Reel

ABSOLUTE MAXIMUM RATINGS(NOTE1)

PARAMETERS		RANGE
Supply voltage range V_{CC}		-0.3V to 6V
Input voltage range	SCL, SDA, EN, AD0, AD1	-0.3V to V_{CC}
Output voltage range	LED1~LED9	-0.3V to V_{CC}
Junction-to-ambient thermal resistance θ_{JA}		47°C/W
Operating free-air temperature range		-40°C to 105°C
Maximum operating junction temperature T_{JMAX}		150°C
Storage temperature TSTG		-65°C to 150°C
Lead temperature (soldering 10 seconds)		260°C
ESD (NOTE 2)		
HBM		±2000V
CDM		±1500V
Latch-Up		
Test condition: JESD78D		+IT：200mA -IT：-200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: MIL-STD-883J Method 3015.9 EIA/JESD22-C101F(CDM)

ELECTRICAL CHARACTERISTICS

T_A=-40°C~105°C, V_{CC}=3.6V (unless otherwise noted), R_{EXT}=4KΩ, PWMRES=8bit..

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
Power supply voltage and current						
V_{CC}	Power supply voltage		2.7		5.5	V
I_{SD_VCC}	Shutdown current of V_{CC}	V_{EN}=GND		0.1	5	μA
I_{STB_VCC}	Standby current of V_{CC}	V_{EN}=3.6V,CHIPEN=0		3	20	μA
	Power-save mode current consumption	V_{EN}=3.6V, GCR.APSE=1, All LEDs off >32ms		3	20	μA
I_{ACT_VCC}	Quiescent current in active mode	V_{EN}=V_{CC}, GCR.CHIPEN=1		2	4	mA
		V_{EN}=V_{CC}, Iout=20mA per LEDx		8	10	mA
$I_{LEAKAGE}$	Output leakage current	V_{EN}=0V, $VLED_X$=5.5V		0.1	1	μA
I_{MAX}	Maximum global current of LED_X	GCCR.GCC=0xFF, BR_X=COL_X=0xFF	38	40	42	mA
I_{MATCH}	Output current match accuracy	GCCR.GCC=0xFF, SL_X= BRx =0XFF	-5		5	%
$V_{DROPOUT}$	Dropout voltage when the LED current has dropped 5%	$ILED_X$=20mA		100	150	mV
		$ILED_X$=40mA		120	200	mV
		$ILED_X$=60mA		180	300	mV
F_{OSC}	OSC clock frequency		14.88	16	17.12	MHz
T_{SD}	Thermal shutdown threshold			165		°C
	Thermal shutdown hysteresis			25		°C
AD0,AD1, EN						
V_{IL}	Input low level	EN			0.4	V
V_{IH}	Input high level	EN	1.4			V
V_{IL}	Input low level	AD0,AD1			0.3*V_{CC}	V
V_{IH}	Input high level	AD0,AD1	0.7*V_{CC}			V
R_{ENPD}	Internal pull down resistance	EN		1M		Ω
I²C Interface						
V_{OL}	Output low level	SDA,I_{OL} = 10 mA			0.1	V
V_{IH}	Input high level	SCL, SDA	1.2			V
V_{IL}	Input low level	SCL, SDA			0.4	V

I²C INTERFACE TIMING

PARAMETER		FAST MODE		FAST MODE PLUS		UNIT
		MIN	MAX	MIN	MAX	
F_{SCL}	Interface clock frequency	-	400	-	1000	kHz
$T_{HD:STA}$	(Repeat-start) START condition hold time	0.6	-	0.26	-	μs
T_{LOW}	Low level width of SCL	1.3	-	0.5	-	μs
T_{HIGH}	High level width of SCL	0.6	-	0.26	-	μs
$T_{SU:STA}$	(Repeat-start) START condition setup time	0.6	-	0.26	-	μs
$T_{HD:DAT}$	Data hold time	0	-	0	-	μs
$T_{SU:DAT}$	Data setup time	0.1	-	0.05	-	μs
T_R	Rising time of SDA and SCL	-	0.3	-	0.12	μs
T_F	Falling time of SDA and SCL	-	0.3	-	0.12	μs
$T_{SU:STO}$	STOP condition setup time	0.6	-	0.26	-	μs
T_{BUF}	Time between start and stop condition	1.3	-	0.5	-	μs

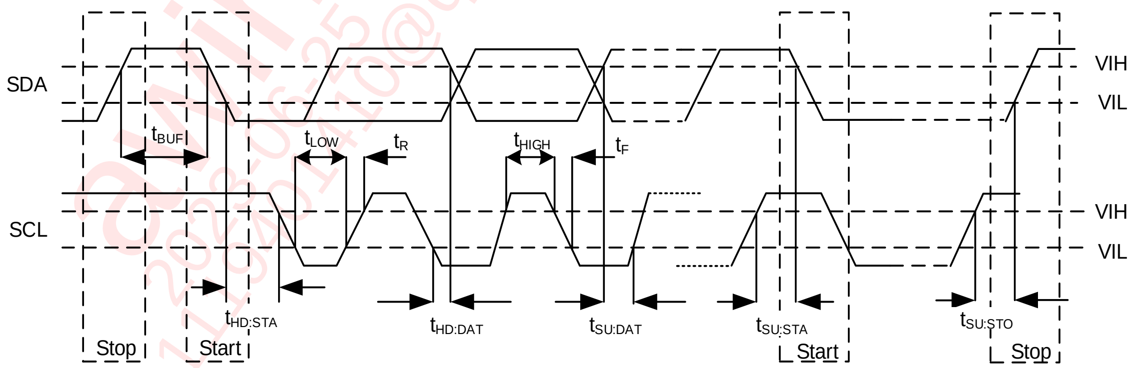


Figure 6 I²C Interface Timing

DETAILED FUNCTIONAL DESCRIPTION

OVERVIEW

AW21009G is a 9 channel multi-function LED driver. Each channel has individual 8-bit DC current setting for color-mixing and maximum 12-bit PWM resolution for brightness control. The global current of each channel is recommended to be 40mA configured via register and external Resistor R_{EXT}.

Phase-control, spread spectrum technology and slew rate control are utilized to reduce EMI and audible noise caused by MLCC. Output current of each LED can be controlled by one pattern or be configured independently. The integrated pattern controller provides breathing or group dimming control. The breathing mode includes auto breathing and manual control mode. All breathing parameters are configurable including rising/falling slope, on/off time, repeat times and brightness.

AW21009G can be turned off with minimum current consumption by either pulling the EN pin low or using the software shutdown feature.

OPERATION MODE AND RESET

RESET

Power On Reset

Upon initial power-up, the AW21009G is reset by internal power-on-reset, and all registers are reset to default value, and the chip is shut down.

Once the supply voltage V_{CC} drops below the threshold voltage V_{POR}(2.0V), the power-on-reset will reset the chip again. By reading the bit PUST of the register UVCR (address 60h), whether the chip has been reset can be detected.

When the V_{CC} ramps up above the threshold voltage V_{POR} (2.0V) and EN is '1', POR is pulled high, meanwhile the chip enters into initialization mode. The chip needs about 2ms to load the OTP information in initialization mode. After initialization, it works in lower-power mode. About 200μs delay is required after CHIPEN is pulled up, otherwise, internal OSCCLK may work incorrectly. Only in low-power and active mode, registers could be configured. The recommended operation timing is shown as bellow.

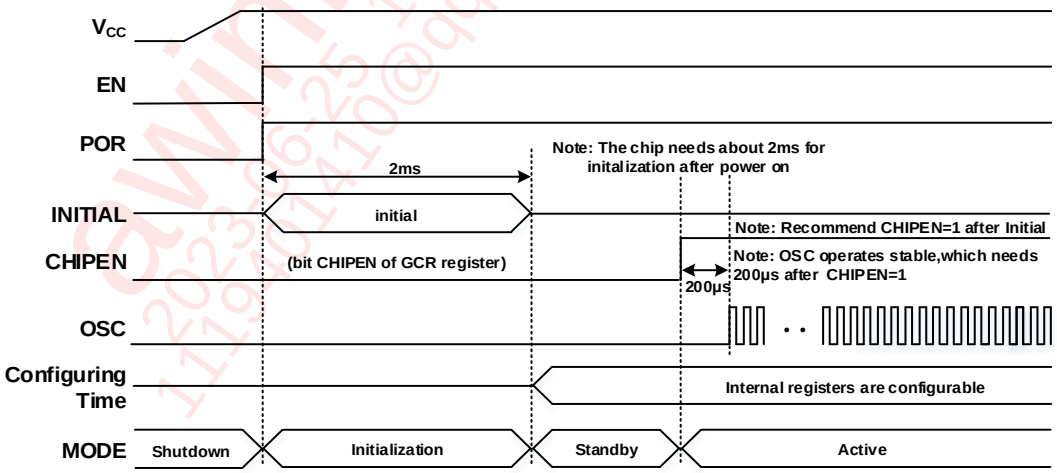


Figure 7 Power On Timing

Software Reset

By writing 00h to register RESET (address 70h), the software reset is triggered. Then all registers will be reset

to the default value and the chip enters into initialization mode.

After the software reset command is input by I²C, it needs to wait at least 2ms before any other I²C commands are accepted.

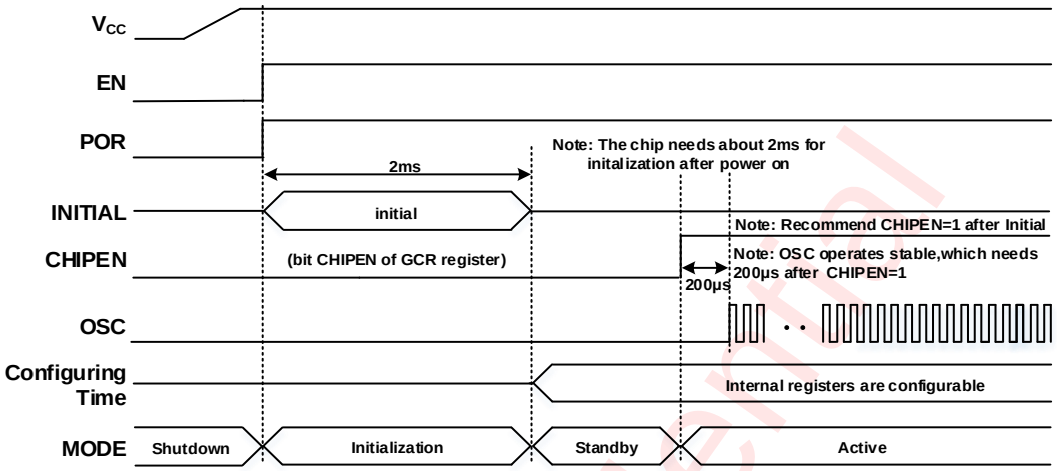


Figure 8 Software Reset Timing

OPERATING MODE

Shutdown mode

The AW21009G enters into shutdown mode automatically when EN is pulled to low. In this situation, I²C interface is not accessible, all registers will be reset and can not be configured.

Initialization mode

If EN is high, the AW21009G enters into initialization mode. During this period, all registers will be reset and chip starts loading efuse information automatically.

Standby mode

After initialization, the AW21009G enters into standby mode when the bit CHIPEN of the register GCR (address 20h) is '0', or UVLO is triggered in active mode. In this mode, only POR and I²C circuits work. I²C interface is accessible, and all registers can be configured now.

Active mode

The AW21009G enters into active mode when EN is high and the bit CHIPEN of the register GCR (address 20h) is '1'.

Power save mode

In active mode, when the bit APSE of the register GCR (address 20h) is set to "1", the auto power-save function is enabled. When all LEDs are switched off and the value of all registers BR00L~BR08H are 00h and write 00h to register UPDATE(address 45h) for more than 32ms, AW21009G automatically enters into power saving mode. In power save mode, most analog blocks are disabled to minimize power consumption, but the registers retain the data and keep it available via I²C. Once writing a non-zero value into any register among BR00L~BR08H, the chip exits power-save mode immediately.

Thermal shutdown

The AW21009G enters the thermal shutdown mode when the junction temperature exceeds 165°C(typical) automatically. In this mode, all the LEDx outputs are shut down. If the junction temperature decreases below 140°C(typical) and write '1' to bit CHIPEN of the register GCR (address 20h), the AW21009G returns to active mode.

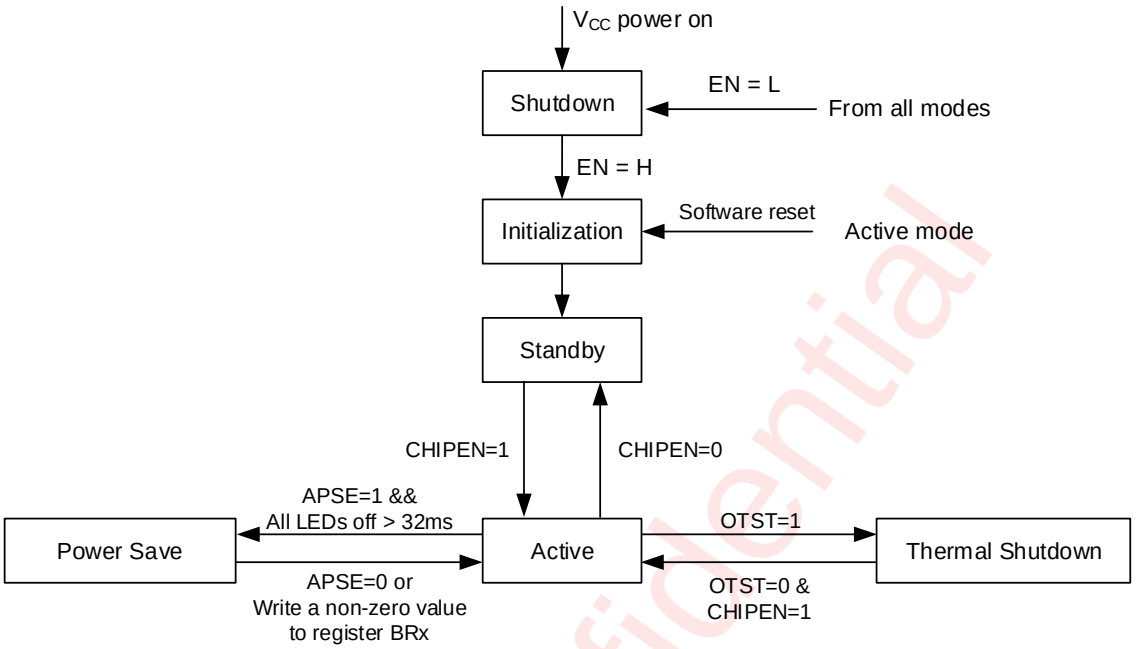


Figure 9 AW21009G operating mode transition

FEATURE DESCRIPTION

CURRENT SETTING

The average output current of LEDx (x=1~9) can be expressed by the following formula,

$$I_{OUT(x)} = I_{MAX} \times \frac{GCC}{255} \times \frac{SL_x}{255} \times \frac{BR_x}{2^{PWMRES}} \quad x = 1\sim9$$

Where I_{MAX}=40mA, GCC is the 8bit global current configured by the register GCCR (address 58h), SL is 8bit individual constant current parameter configured by the register SLx (address 46h~4Eh) , PWMRES is 8bit/9bit/12bit PWM resolution configured by the register GCR (address 20h), and BR is 8bit/9bit/12bit individual PWM modulated current parameter configured by the register BRxL/BRxH (address 21h~32h).

PWM MODULATION

Dither Function

When PWMRES[1:0] of GCR(address 20h) is 2'b11, dither function is enabled. Then the final output PWM has the frequency equal to 9 bits and resolution equal to 12 bits. It achieved by 9 bits PWM modulation and 3bits digital dither control. For 3-bit dither, every PWM in the 8 PWM group can be added one LSB or not according to the 8-bit digital dither timing.

PWM Frequency

The output PWM frequency is decided by bits CLKFRQ [2:0] and PWMRES[1:0] in register GCR (address 20h). Following table shows the relationship of PWM frequency, the CLKFRQ [2:0] and PWMRES[1:0]. To avoid the MLCC audible noise, it's recommended to use the PWM frequency lower than 500 Hz or higher than 20kHz.

BR Resolution	CLKFRQ[2:0]							
	000	001	010	011	100	101	110	111
8bit	62k	32k	4k	2k	1k	500	244	122
9bit	32k	16k	2k	1k	488	244	122	-
12bit	4k	2k	244	122	-	-	-	-
9bit+3bit dither	32k	16k	2k	1k	488	244	122	-

PWM Phase Control

To reduce the peak load current and ceramic-capacitor audible ringing, AW21009G supports 3 PWM phase shifting (Phase1~Phase3) and phase-inverting scheme. When setting PDE in register PHCR (address 59h) to '1', the phase shifting scheme is enabled, and each adjacent phase differs by 60 degrees, which meaning only 3 of 9 LEDs could switch on in the same time.

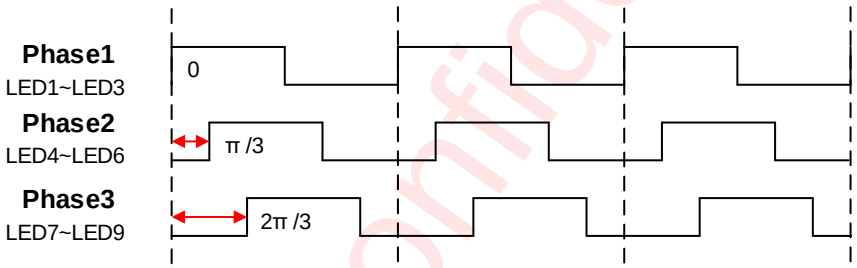


Figure 10 Phase shift scheme

When setting PINVTEn in register PHCR (address 59h, n=0~2) to '1', the PWM phase of the even-numbered channels is inverted. As shown below, if setting PINVTEn to '1', the even-numbered channels are rotated 180 degrees counterclockwise when the odd-numbered channels are not, which is good for reducing the input-current ripple. For an example, when setting PINVTE0 to '1', the channel of LED2 are rotated 180 degrees counterclockwise while the channels of LED1, LED3 are not.

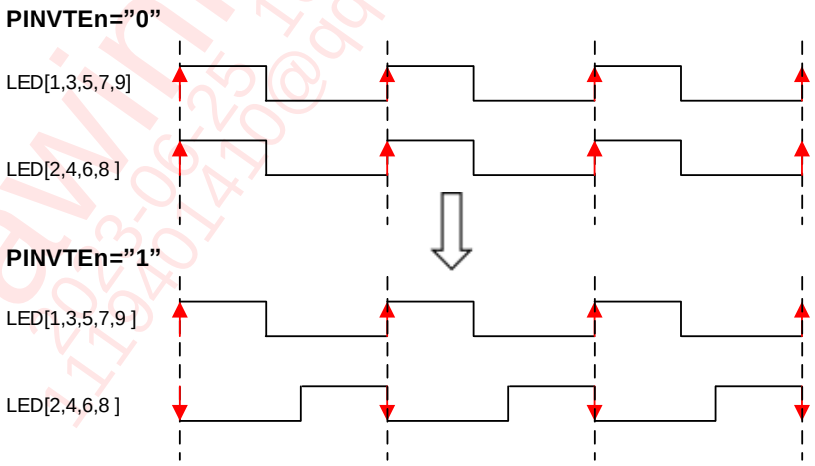


Figure 11 Phase invert scheme

PWM Disable

If the bits DCPWM[1:0] in register SSCR (address 5Fh) is set to "11", the PWM output is disabled, and the duty of each PWM is forced to 100%. In this mode, the BRx parameter is not valid, but the SLx parameter is still

effective.

It should be noted that when performing open-short detection, the bits DCPWM [1:0] need to be set to “11”.

GROUP CONTROL MODE

AW21009G supports group control mode, in this mode, all selected LEDs are controlled by the group control registers (GSLR, GSLG, GSLB). The register GCFG select which LEDs are controlled by group control register. There are total 3 control bit (GEx), each bit set adjacent 3 LED are included in or not. User can configure group control register to setting common brightness and color for all selected LED, so as to simplify lighting effect programming and speed up display refreshing via I²C interface.

If bit GSLDIS in register GCFG (address 8Bh) is ‘1’, the color parameters of the grouped LED are no longer configured by register GSLR/G/B but by individual register (SL0~SL08).

The detailed configurations are as follows.

LED	GE	Brightness		Color	
		GE=0	GE=1	GE=0 or GSLDIS=1	GE=1 and GSLDIS=0
1	GCFG[0]	BR00	GBR	SL00	GSLR
2		BR01	GBR	SL01	GSLG
3		BR02	GBR	SL02	GSLB
4	GCFG[1]	BR03	GBR	SL03	GSLR
5		BR04	GBR	SL04	GSLG
6		BR05	GBR	SL05	GSLB
7	GCFG[2]	BR06	GBR	SL06	GSLR
8		BR007	GBR	SL07	GSLG
9		BR08	GBR	SL08	GSLB

Note: GBR={GBRH,GBRL}.

SPREAD SPECTRUM

PWM is a troublesome for some application which is concerned about EMI. AW21009G has spread spectrum function to optimize the EMI performance. If bit SSE in register SSCR (address 5Fh) is set to ‘1’, spread spectrum function is enabled. By setting the bit SSR in register SSCR, four spread spectrum range ±5%/±15%/±25%/±35% can be selected. The total electromagnetic emitting energy can spread into a wider range of frequency band that significantly degrades the peak energy of EMI.

RGB CONFIGURE MODE

In RGB applications, every 3 LEDs in RGB share a same BR parameter. To achieve fast register configuration for RGB applications, AW21009G provides an RGB configuration mode by setting the bit RGBMD in register GCR2 (address 61h).

If RGBMD=1, register BR00~BR02 configure brightness parameters for corresponding 3 RGB groups . In other words, in RGB mode, only registers BR00~BR02 need to be configured, and the registers BR03~BR08 are not valid any more.

If RGBMD=0, register BR00~BR08 configure brightness parameters for corresponding 9 LEDs independently, more details as follows.

LED	BR parameter source	
	RGBMD=0	RGBMD=1
1	BR00	BR00
2	BR01	
3	BR02	
4	BR03	BR01
5	BR04	
6	BR05	
7	BR06	BR02
8	BR07	
9	BR08	

Note: BRxx = {BRxxH,BRxxL}

SINGLE BYTE CONFIGURATION MODE

By default, every LED has a 12bit BR parameter with BRxxL and BRxxH. The effective bit of BRxxH is 4bit. However, AW21009G provides an single byte configuration mode by setting the bit SBMD in register GCR2 (address 61h). In single byte applications, every LED has a 8bit BR parameter configured by BR00L~BR04L. It is worth noting that the effective bit of BRxxH(xx is 00~04) is 8 bit in single byte mode compared with default mode. More details are as follows.

LED	BR parameter source	
	SBMD=0	SBMD=1
1	{BR00H,BR00L}	BR00L
2	{BR01H,BR01L}	BR00H
3	{BR02H,BR02L}	BR01L
4	{BR03H,BR03L}	BR01H
5	{BR04H,BR04L}	BR02L
6	{BR05H,BR05L}	BR02H
7	{BR06H,BR06L}	BR03L
8	{BR07H,BR07L}	BR03H
9	{BR08H,BR08L}	BR04L

PATTERN CONTROLLERS

There is a breathing pattern controller in the chip. When bit PATE in register PATCFG (address 80h) is set to '1', breathing pattern controller is enabled. Pattern controller can be configured as autonomous breathing mode or manual-controlled mode. When corresponding GE is configured as '1', if in pattern controlled mode, each led group (consisting of three adjacent LEDs) can enter into breathing mode. When GE is '0', the three adjacent LEDs exit breathing mode directly. For example, when setting GCFG = 0x01 and in pattern controlled mode, LED1~LED3 will work in breathing mode and other LEDs will work in default mode.

Autonomous Breathing Mode

When bit PATE and PATMD in register PATCFG are set to '1', the pattern controller works in autonomous breathing mode. In this mode, the pattern controller will generate a breathing lighting effect, which is configured by the user-defined timing parameter. The waveform of the breathing lighting effect is shown in the following figure. The parameter T0~T3 define 4 key periods in a complete breathing cycle. T0~T3 composite a breathing loop, denoting the rise-time, on-time, fall-time and off-time respectively. Register GBRH (address 86h) and GBRL (address 87h) control the max and min brightness of the breathing respectively.

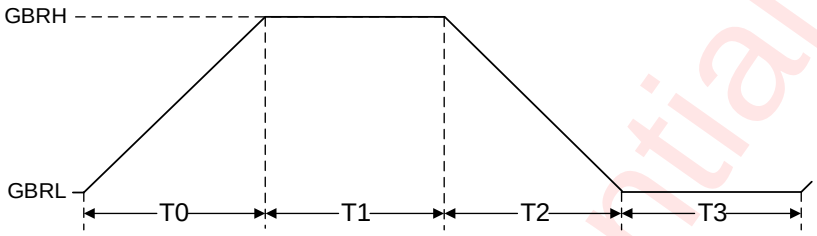


Figure 12 LED breath timing in pattern mode

The start point and end point of autonomous breathing loop are configurable. The loop starting point could be selected among T0~T3, which is set by bits LB [1:0] in register PATT2 (address 84h). The end point of the loop can only be selected between the end of T3 and the end of T1, which is determined by bits LE [1:0] in register PATT2. If bits LE [1:0] is not "00", the end point of breathing loop is the end of T1, and the loop counter increment by 1 at the end of T1. If bit LE [1:0] is "00", the loop end point is the end of T3, and the loop counter increment by 1 at the end of T3.

The repeat times is decided by bit RPT [11:8] of register PATT2 (address 84h) and RPT [7:0] of register PATT3 (address 85h). When setting RPT [11:0] to '0', the breathing pattern will run unlimited times.

After the breathing pattern is over, the status bit PATIS in register PATGO (address 81h) will be set to '1', and PATIS will be cleared to '0' after reading out through I²C bus. Once breathing loop start again or pattern controller switches to manual mode by setting PATE bit to '0', the PATIS will also be cleared.

When bit RUN in register PATGO is set to '1', breathing pattern is started. The full process of the autonomous breathing is as follows:

1. Set GSLR/G/B, GBRH/L parameter.
2. Set GCFG to select the LED in breathing pattern mode or not.
3. Configure PATT0, PATT1, PATT2, and PATT3 for parameters T0~T3, start/stop point, and repeat times.
4. Set PATE=1 to enable breathing pattern mode.
5. Set PATMD=1 to select auto breathing mode.
6. Set RUN=1 to start the breath pattern.

Manual Control Mode

If bit PATMD is set to '0', manual control mode is selected. In manual control mode, user could program the bit SWITCH of register PATCFG to control the output of pattern controller. When bit SWITCH is '1', the output of pattern controller is decided by register GBRH. When bit SWITCH is set as "0", the output is the decided by register GBRL.

If bit RAM0PE in register PATCFG is set to '1', the smooth ramp up/down will be enabled. At the same time, if SWITCH changes from "0" to '1', the output will be ramp up to GBRH smoothly. Similarly, if SWITCH changes from "1" to '0', the output of the pattern controller will ramp down to GBRL smoothly.

However, if the RAMP is set to '0', the output of the pattern controller will change to GBRH or GBR directly with no ramp as the SWITCH changes.

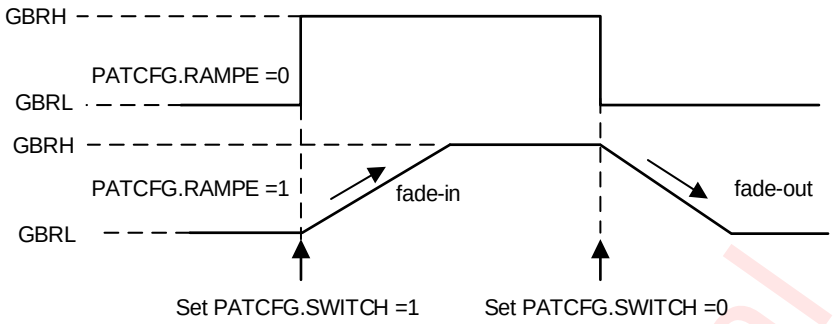


Figure 13 Manual Control Mode

PROTECTION FEATURES

Under Voltage Lock Out (UVLO)

When bit UVDIS of the register UVCR (address 60h) is set to '0', the chip monitors the voltage of V_{CC}. If the supply voltage drops below threshold (2.5V typically), the bit UVST of the register UVCR (address 60h) will be set to '1'. After read-out, the register UVCR will be clear.

If both bit UVDIS and bit UVPD of the register UVCR (address 60h) is set to '0', UVLO protection function is enabled. Once the event of under voltage occurs, the bit CHIPEN of the register GCR (address 20h) will be cleared to '0', and then the chip will enter into standby mode. If the voltage of V_{CC} rises above the UVLO threshold and then write "1" to bit CHIPEN, the chip will enter into active mode again.

By default, control bits UVDIS, UVPD are all "0". Both UVLO monitor and protection are enabled.

Over Temperature Protection (OTP)

When bit OTDIS of the register OTCR (address 5Eh) is set to '0', the over-temperature detection is enabled. Once the temperature of this chip reaches 165°C, the over-temperature condition is detected, and the bit OTST of the register OTCR (address 5Eh) will be set to '1'. The OTST will be cleared to '0' after reading the register OTCR.

If both bit OTDIS and bit OTPD of the register OTCR (address 5Eh) are set to '0', the Over-Temperature Protection (OTP) function is enabled. Once the temperature is over 165°C, the bit CHIPEN of the register GCR (address 20h) will be cleared to '0', and then the chip will enter into thermal shutdown mode. When the temperature returns below 140°C, the chip will enter into active mode again after writing "1" to bit CHIPEN.

By default, control bits OTDIS and OTPD are all "0", both OT monitor and OT protection are enable.

LED Open/Short Detection

AW21009G supports LED open/short detection. When bit OSDE[1:0] of the register OSDCR(address 5Ah) is set to "10" , short detection is enabled, and the detection results can be read out via the registers OSST0~1(5Bh~5Ch). Similarly, when set bit OSDE [1:0] of the register OSDCR (address 5Ah) to "11", open detection is enabled, and the results also can be read out via the registers OSST0~1.

The valid detect result is determined by:

- Short Detection: $V_{LED} > V_{CC} - VTH_{SHORT}$
- Open Detection: $V_{LED} < VTH_{OPEN}$

Note: VTH_{OPEN}: Threshold of open detection (When OTH=0, VTH_{OPEN} = 0.1V, else VTH_{OPEN} = 0.2V;).

VTH_{SHORT}: Threshold of short detection (When STH=0, VTH_{SHORT} = 0.5V, else VTH_{SHORT} = 1V).

We recommend the bit DCPWM[1:0] of the register SSCR (address 5Fh) being set to "11" and maintain about 1mA current of each LED when the open/short function is enabled.

I²C INTERFACE

The AW21009G supports the I²C protocol. The maximum frequency supported by the I²C is 1MHz.

The pull-up resistor for the SDA and SCL can be selected from 1kΩ to 10kΩ. Usually, 4.7kΩ is recommended for 400 kHz I²C, 1kΩ is recommended for 1 MHz I²C. The voltage from 1.8V to 3.3V is allowed for the I²C interface. Additionally, the I²C chip supports continuous read and write operations.

CHIP ADDRESS

The I²C chip address is 7-bit (A7~A1), followed by the bit R/W (A0). Set A0 to "0" for writing and "1" for reading. The values of bit A1 and A2 are depended on the pin AD0. A3 and A4 are depended on the pin AD1. There are 2 options: VCC and GND. The A7 to A5 is "010" constantly. The chip also supports using a broadcast slave address of 1Ch. All slave addresses as followed.

AD PIN	A7:A5	A4:A3	A2:A1	A0	Chip Address	Broadcast Address
GND/GND	010	00	00	0/1	20h	1Ch
GND/VCC		00	01		21h	
VCC/GND		01	00		24h	
VCC/VCC		01	01		25h	

I²C START/STOP

All transactions begin with a START and are terminated by a STOP sent by master to slave. A high-to-low transition on the SDA input/output while the SCL input is high defines a START condition. A low-to-high transition on the SDA input/output while the SCL input is high defines a STOP condition.

In particular, the bus stays busy when a repeated START (Sr) is generated instead of a STOP signal corresponding to the lastest START (S). Sr and S are usually regarded as equivalent.

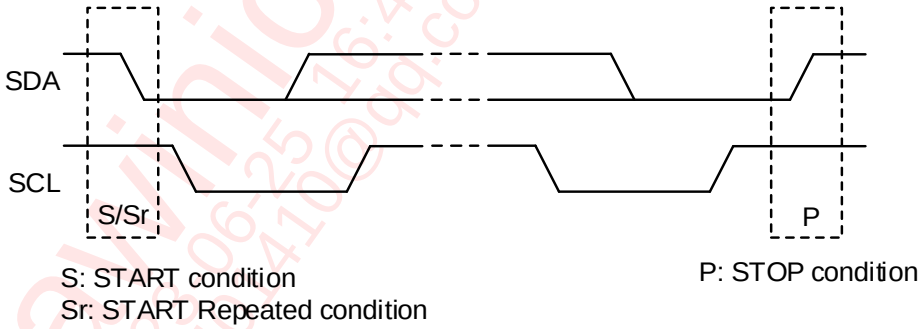


Figure 14 I²C START/STOP Condition Timing

DATA VALIDATION

When SCL is high level, SDA level must be constant. SDA can be changed only when SCL is low level.Each SCL pulse corresponds to one bit data transaction.

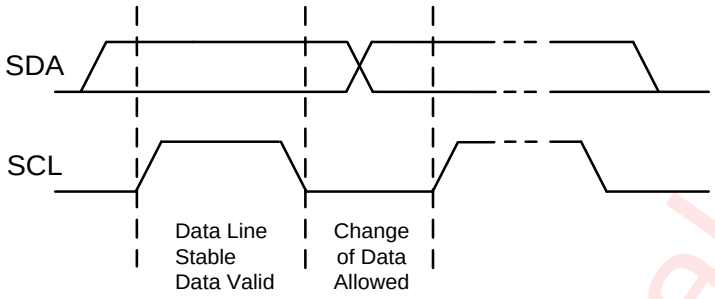


Figure 15 Data Validation Diagram

ACK (ACKNOWLEDGEMENT)

ACK means the successful transaction of I²C bus data. During writing cycle, after master sends 8-bit data, SDA must be released by master and SDA is pulled down to GND by slave chip when slave sends ACK.

During reading cycle, after slave chip sends 8-bit data, slave releases the SDA and waits for ACK from master. If master sends ACK with STOP condition, slave chip sends the next data. If master sends NACK, slave chip stops sending data and waits for I²C stop.

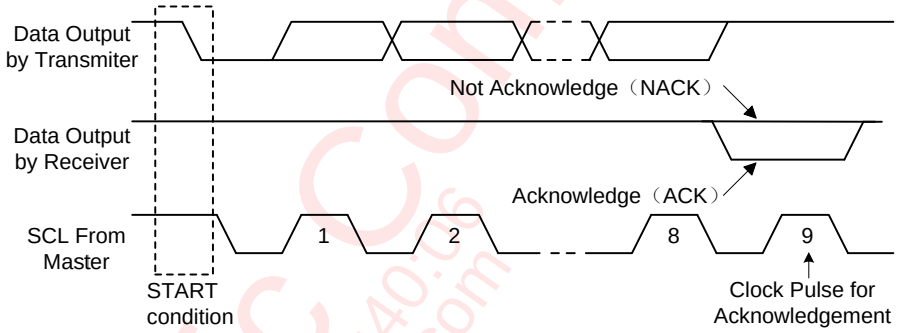


Figure 16 I²C ACK Timing

WRITE CYCLE

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line aborts the current transaction during the high state of the SCL. New data should be sent to SDA bus during the low SCL state. This protocol allows a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a start condition, a number of byte transfers and a stop condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits and is transferred with the most significant bit first. After each byte, an ACK signal must follow.

1. In a write process, the following steps should be followed:
2. Master chip generates START condition. The "START" signal is generated by pulling down the SDA signal while the SCL signal is high.
3. Master chip sends slave address (7-bit) and the data direction bit $R/\overline{W} = 0$.
4. Slave chip sends acknowledge signal if the slave address is correct.
5. Master sends control register address (8-bit).

6. Slave sends acknowledge signal.
7. Master sends data byte to write to the addressed register.
8. Slave sends acknowledge signal.
9. If master send more data bytes, the control register address will be incremented by one after acknowledge signal (repeat step f and g).
10. Master generates STOP condition to indicate write cycle ends.

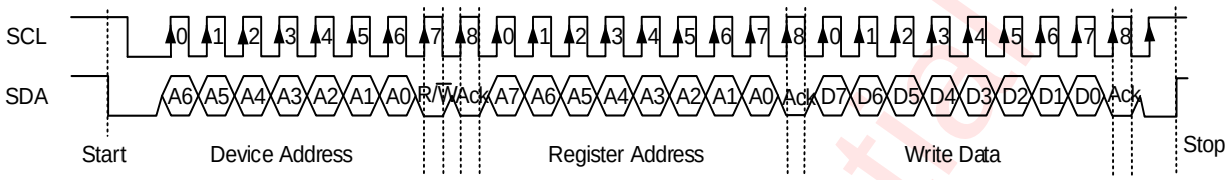


Figure 17 I²C Write Byte Cycle

READ CYCLE

In a read cycle, the following steps should be followed:

1. Master chip generates START condition
2. Master chip sends slave address (7-bit) and the data direction bit (R/W = 0).
3. Slave chip sends acknowledge signal if the slave address is correct.
4. Master sends control register address (8-bit)
5. Slave sends acknowledge signal
6. Master generates STOP condition followed with START condition or REPEAT START condition
7. Master chip sends slave address (7-bit) and the data direction bit (R/W = 1).
8. Slave chip sends acknowledge signal if the slave address is correct.
9. Slave sends data byte from addressed register.
10. If the master chip sends acknowledge signal, the slave chip will increase the control register address by one, then send the next data from the new addressed register. In particular, if register address is 00h or 01h, the slave chip will poll register address between 00h and 01h.
11. If the master chip generates STOP condition, the read cycle ends.

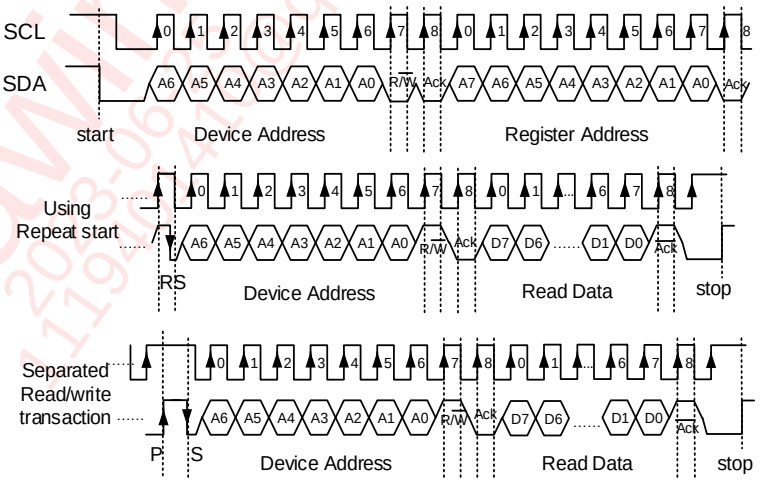


Figure 18 I²C Read Byte Cycle

REGISTER CONFIGURATION

REGISTER LIST

ADDR	R/W	NAME	D7	D6	D5	D4	D3	D2	D1	D0	DEF
20h	RW	GCR	APSE	CLKFRQ			-	PWMRES		CHIPEN	00h
21h	RW	BR00L	BR00L								00h
22h	RW	BR00H	-				BR00H				00h
…	…	…	…								…
31h	RW	BR08L	BR08L								00h
32h	RW	BR08H	-				BR08H				00h
45h	W	UPDATE	UPDATE								00h
46h	RW	SL00	SL00								00h
…	…	…	…								…
4Eh	RW	SL08	SL08								00h
58h	RW	GCCR	GCC								00h
59h	RW	PHCR	PDE	-				PINVTE			00h
5Ah	RW	OSDCR	-				OTH	STH	OSDE		00h
5Bh	R	OSST0	OP/ST [7:0]								00h
5Ch	R	OSST1	-							OP/ST [8]	00h
5Eh	RW	OTCR	TROF		TRST	OTST	OTPD	OTDIS	TRTH		00h
5Fh	RW	SSCR	-	DCPWM		SSE	SSR		CLT		00h
60h	RW	UVCR	REXT_ST		UVST	PUST	OCPTH		UVPD	UVDIS	00h
61h	RW	GCR2	-			BSDIS	UDMD		SBMD	RGBMD	00h
62h	RW	GCR3	-				APS2E	SRR	SRF[1:0]		00h
70h	RW	RESET	RESET/ID								12h
80h	RW	PATCFG	-				SWITCH	RAMPE	PATMD	PATE	00h
81h	RW	PATGO	-					PATIS	PATST	RUN	00h
82h	RW	PATT0	T0				T1				00h
83h	RW	PATT1	T2				T3				00h
84h	RW	PATT2	LE		LB		RPT[11:8]				00h
85h	RW	PATT3	RPT[7:0]								00h
86h	RW	GBRH	GBRH								00h
87h	RW	GBRL	GBRL								00h
88h	RW	GSLR	GSLR								00h
89h	RW	GSLG	GSLG								00h
8Ah	RW	GSLB	GSLB								00h
8Bh	RW	GCFG	-	GSLDIS	-			GE2	GE1	GE0	00h

REGISTER DETAILED DESCRIPTION

GCR: Global Control Register (Address 20h)

Bit	Symbol	R/W	Description	Default
7	APSE	RW	Auto power save enable 0: disable 1: enable	0
6:4	CLKFRQ	RW	OSC frequency selection 000: 16MHz 001: 8MHz 010: 1MHz 011: 512kHz 100: 256kHz 101: 125kHz 110: 62.5kHz 111: 31.25kHz	000
3	reserved	-	-	0
2:1	PWMRES	RW	Brightness resolution selection 00: 8bit 01: 9bit 10: 12bit 11: 12bit with dither enabled	00
0	CHIPEN	RW	Chip enable 0: disable 1: enable	0

BRxxL/BRxxH: Brightness Control Register (Addredd 21h~32h)

Bit	Symbol	R/W	Description	Default
7:0	BRxxL	RW	Brightness control LSB8 for LED	00h
3:0	BRxxH	RW	Brightness control MSB4 for LED	0000

UPDATE: Update Register (Address 45h)

Bit	Symbol	R/W	Description	Default
7:0	UPDATE	W	Write 00h to update BR and SL registers	00h

SLxx: Scaling Register (Address 46h~4Eh)

Bit	Symbol	R/W	Description	Default
7:0	SLxx	RW	Scaling parameter for LED	00h

GCCR: Global Current Control Register (Address 58h)

Bit	Symbol	R/W	Description	Default
7:0	GCC	RW	Global current control register	00h

PHCR: Phase Control Register (Address 59h)

Bit	Symbol	R/W	Description	Default
7	PDE	RW	PWM phase delay enable 0: disable 1: enable	0
6:3	reserved	-	-	0000
2:0	PINVTE	RW	Phase invert enable for every 3 LEDs 0: phase not invert 1: phase invert 180 degree for even LEDs	000

OSDCR: Open/Short Detect Control Register (Address 5Ah)

Bit	Symbol	R/W	Description	Default
7:4	reserved	-	-	0000
3	OTH	RW	Open threshold 0: 0.1V 1: 0.2V	0
2	STH	RW	Short threshold 0: 0.5 V 1: 1 V	0
1:0	OSDE	RW	Open/short detect enable, must set PWMDIS=111 before detecting 0x: detect disable 10: short detect enable 11: open detect enable	00

OSST: Open/Short Status Register (Address 5Bh/5Ch)

Bit	Symbol	R/W	Description	Default
7:0	OSST0	R	Open/Short Status of LED1~8 0: no open/short detected 1: open/short detected	00h
0	OSST1	R	Open/Short Status of LED9 0: no open/short detected 1: open/short detected	0

OTCR: Over Temperature Control Register (Address 5Eh)

Bit	Symbol	R/W	Description	Default
7:6	TROF	RW	Thermal roll off percentage of LED output current 00: 100% 01: 75% 10: 50% 11: 25%	00

5	TRST	R	Thermal roll off status 0: normal 1: thermal roll off occurred	0
4	OTST	R	Over temperature status 0: normal 1: over temperature occurred	0
3	OTPD	RW	Over temperature protect disable 0: OT protect enable, when OT event occurs, chip will clear GCR.CHIPEN to 0 1: OT protect disable	0
2	OTDIS	RW	Over temperature detect disable 0: OT detect enable 1: OT detect disable	0
1:0	TRTH	RW	Temperature roll off threshold 00: 140°C 01: 120°C 10: 100°C 11: 90°C	00

SSCR: Spread Spectrum Control Register (Address 5Fh)

Bit	Symbol	R/W	Description	Default
7	reserved	-	-	0
6	DCPWM1	RW	0: LED 7~9 PWM duty set by 2Dh~32h 1: LED 7~9 PWM duty set as 100%	0
5	DCPWM0	RW	0: LED 1~6 PWM duty set by 21h~2Ch 1: LED 1~6 PWM duty set as 100%	0
4	SSE	RW	Spread spectrum enable 0: disable 1: enable	0
3:2	SSR	RW	Spread spectrum range 00: ±5% 01: ±15% 10: ±24% 11: ±34%	00
1:0	CLT	RW	Spread spectrum period 00: 1980μs 01: 1200μs 10: 820μs 11: 660μs	00

UVCR: UVLO Control Register (Address 60h)

Bit	Symbol	R/W	Description	Default
7:6	REXT_ST	R	Rext status 00: normal 01: Rext is short or OCP 10: Rext is open 11: no exist	00
5	UVST	R	UVLO status 0: normal 1: UVLO detected	0
4	PUST	R	Power up status 0: normal 1: power up occurred	0
3	OCPTH	RW	OCP threshold 0: 85mA 1: 55mA	0
2	OCPD	RW	OCP disable 0: enable OCP 1: disable OCP	0
1	UVPD	RW	UVLO protect disable 0: UVLO protect enable, when UVLO occurs, chip will clear GCR.CHIPEN to 0 1: UVLO protect disable	0
0	UVDIS	RW	UVLO detect disable 0: UVLO detect enable 1: UVLO detect disable	0

GCR2: Global Control Register2 (Address 61h)

Bit	Symbol	R/W	Description	Default
7:5	reserved	-	-	000
4	BSDIS	RW	I^2C broadcast slave address disable 0: I^2C broadcast slave address enable 1: I^2C broadcast slave address disable	0
3:2	UDMD	RW	BR and SL update mode 00: BR is updated at PWM carrier boundary, and SL does not need to be updated. 01: Both BR and SL are updated at PWM carrier boundary. 10: BR is updated at fast mode, and SL does not need to be updated. 11: Both BR and SL are updated at fast mode.	00

1	SBMD	RW	Single byte mode for BR 0: disable 1: enable	0
0	RGBMD	RW	RGB mode enable 0: disable 1: enable, every 3 LEDs uses a common BR.	0

GCR3: Global Control Register3 (Address 62h)

Bit	Symbol	R/W	Description	Default
7:4	reserved	-	-	0000
3	APS2E	RW	Enable PWMIS0 function 0: disable 1: enable	0
2	SRR	RW	Slew rate control for LED output rising 0: 1ns 1: 6ns	0
1:0	SRF	RW	Slew rate control for LED output falling 00: 1 ns 01: 3 ns 10: 6 ns 11:10 ns	00

RESET: Reset Register (Address 70h)

Bit	Symbol	R/W	Description	Default
7:0	RESET	RW	Software reset/ID Write 00h will reset all registers to their default value. When read, chip ID is read out.	12h

PATCFG: PAT Configuration Register (Address 80h)

Bit	Symbol	R/W	Description	Default
7:4	reserved	-	-	0000
3	SWITCH	RW	Switch on or off at manual mode. 0: switch LED off 1: switch LED on	0
2	RAMP	RW	Ramp for manual mode 0: direct set 1: ramp enable when transition	0
1	PATMD	RW	PAT operation mode 0: manual mode 1: auto breath mode	0
0	PATE	RW	PAT Enable 0: disable 1: enable	0

PAT Run Control Register (Address 81h)

Bit	Symbol	R/W	Description	Default
7:3	reserved	-	-	00000
2	PATIS	RW	PAT loop over flag 0: pattern is non-over 1: pattern is over	0
1	PATST	RW	ABM loop state 0: pattern is in stop state 1: pattern in running	0
0	RUN	RW	PAT run enable. Transition from 0 to 1 start PAT loop.	0

PATT0：PAT Pattern Time 0 (Address 82h)

Bit	Symbol	R/W	Description	Default
7:4	T0	RW	Pattern rise time 0000: 0.00s 0001: 0.13s 0010: 0.26s 0011: 0.38s 0100: 0.51s 0101: 0.77s 0110: 1.04s 0111: 1.60s 1000: 2.10s 1001: 2.60s 1010: 3.10s 1011: 4.20s 1100: 5.20s 1101: 6.20s 1110: 7.30s 1111: 8.30s	0000
3:0	T1	RW	Pattern on time 0000: 0.00s 0001: 0.13s 0010: 0.26s 0011: 0.38s 0100: 0.51s 0101: 0.77s 0110: 1.04s 0111: 1.60s 1000: 2.10s 1001: 2.60s 1010: 3.10s 1011: 4.20s 1100: 5.20s 1101: 6.20s 1110: 7.30s 1111: 8.30s	0000

PATT1：PAT Pattern Time 1 (Address 83h)

Bit	Symbol	R/W	Description	Default
7:4	T2	RW	Pattern fall time 0000: 0.00s 0001: 0.13s 0010: 0.26s 0011: 0.38s 0100: 0.51s 0101: 0.77s 0110: 1.04s 0111: 1.60s 1000: 2.10s 1001: 2.60s 1010: 3.10s 1011: 4.20s 1100: 5.20s 1101: 6.20s 1110: 7.30s 1111: 8.30s	0000
3:0	T3	RW	Pattern off time 0000: 0.00s 0001: 0.13s 0010: 0.26s 0011: 0.38s 0100: 0.51s 0101: 0.77s 0110: 1.04s 0111: 1.60s 1000: 2.10s 1001: 2.60s 1010: 3.10s 1011: 4.20s 1100: 5.20s 1101: 6.20s 1110: 7.30s 1111: 8.30s	0000

PATT2 ： Pattern Time 2 (Address 84h)

Bit	Symbol	R/W	Description	Default
7:6	LE	RW	Loop stop point 00: stop at the start of T3 Others: stop at the start of T1	00
5:4	LB	RW	Loop start point 00: T0 01: T1 10: T2 11: T3	00
3:0	RPT[11:8]	RW	Loop repeat times 4 MSB	0000

PATT3: Pattern Time 3 (Address 85h)

Bit	Symbol	R/W	Description	Default
7:0	RPT[7:0]	RW -	Loop repeat times 8 LSB. If RPT[11:0] is all zero, PAT loop will repeat forever .	00h

GBRH/GBRL: Group Brightness Register (Address 86h/87h)

Bit	Symbol	R/W	Description	Default
7:0	GBRH	RW	When PATCFG.PATE=1, it is the max fade level of ABM; When PATCFG.PATE=0, it is the high 4bit of group brightness.	00h
7:0	GBRL	RW	When PATCFG.PATE=1, it is the min fade level of ABM; When PATCFG.PATE=0, it is the low 8 bit of group brightness.	00h

GSLR/GSLG/GSLB: Group SL Register (Address 88h/89h/8Ah)

Bit	Symbol	R/W	Description	Default
7:0	GSLR	RW	When LEDx (x=1, 4, 7) works in group mode, its SL scaling is decided by GSLR.	00h
7:0	GSLG	RW	When LEDx (x=2, 5, 8) works in group mode, its SL scaling is decided by GSLG.	00h
7:0	GSLB	RW	When LEDx (x=3, 6, 9) works in group mode, its SL scaling is decided by GSLB.	00h

GCFG: Group Configure Register (Address 8Bh)

Bit	Symbol	R/W	Description	Default
7	reserved	RW	-	0
6	GSLDIS	RW	Group SL disable: 0: Group SL enable, all LEDs in group/pattern mode share the common SL parameters decided by GSLR/G/B. 1: Group SL disable, all LEDs' color parameter in group/pattern mode is configured by their respective register SL	0
5:3	reserved	-	-	000
2:0	GEx	RW	Group mode enable If bit PATEN inregister PATCFG is set to "0", GE[0]=1: LED1~3 work in group mode GE[1]=1: LED4~6 work in group mode GE[2]=1: LED7~9 work in group mode If bit PATEN inregister PATCFG is set to "1", GE[0]=1: LED1~3 work in auto breath pattern mode GE[1]=1: LED4~6 work in auto breath pattern mode GE[2]=1: LED7~9 work in auto breath pattern mode	000

Application Information

REXT

The selection of R_{EXT} determined the maximum LED1~LED9 current I_{max} as described in below formula.

$$I_{max} = \frac{K}{R_{EXT}}$$

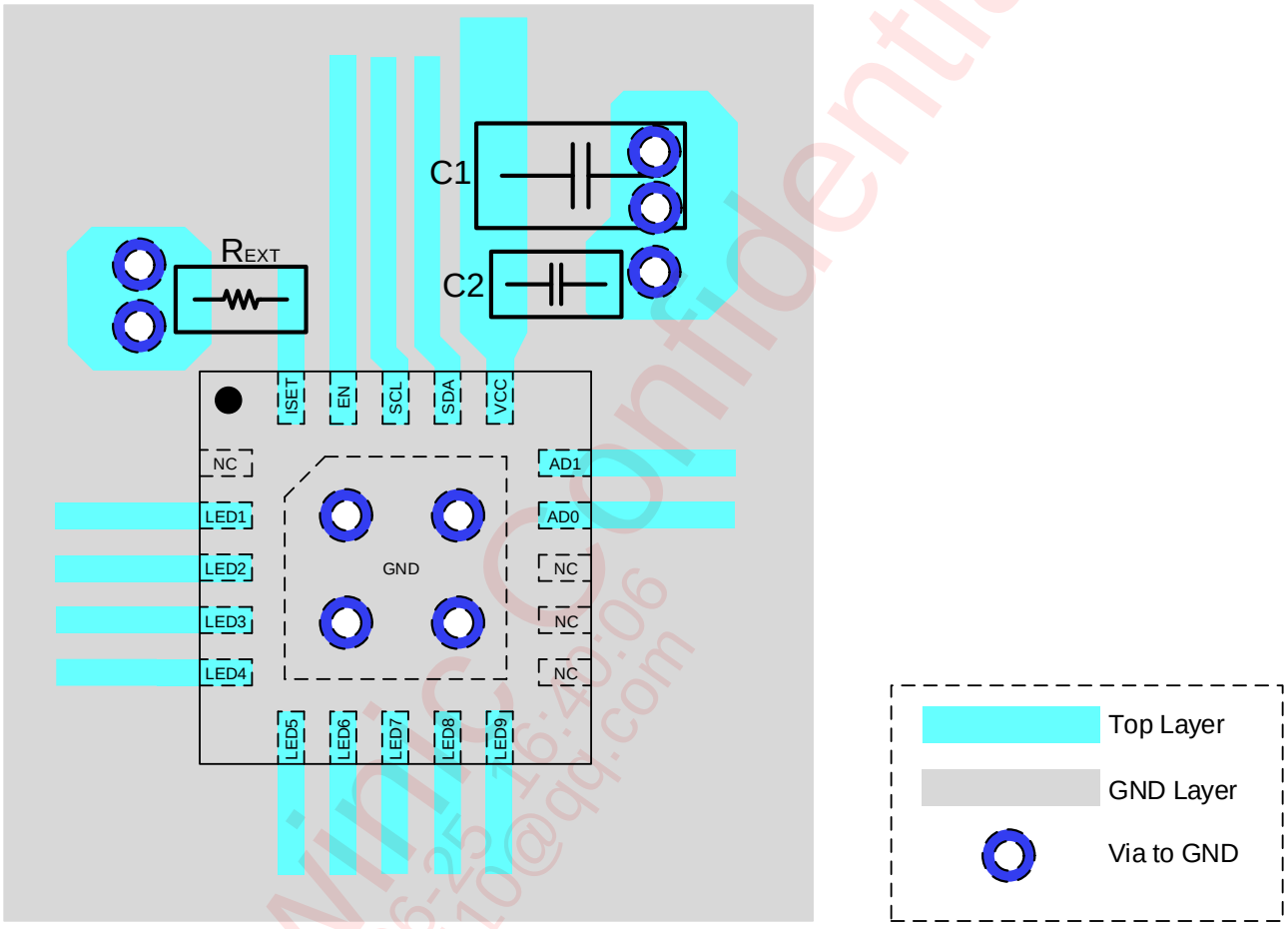
Where K = 160V, the recommended minimum value of R_{EXT} is 2KΩ.

When R_{EXT} = 4KΩ, I_{max} = 40mA

PCB LAYOUT CONSIDERATION

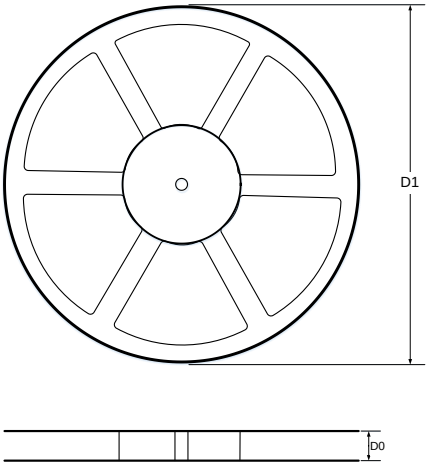
AW21009G is a 9-channel multi-function LED driver. When all ports are operating, the device power dissipation is large. To obtain the good thermal performance and avoid thermal shutdown, PCB layout should be considered carefully. Here are some guidelines:

1. The C_1、C_2、should be placed as close to the chip as possible.
2. The R_{EXT} should be placed as close to the chip as possible.
3. The Thermal PAD must be well connecting to the GND of the PCB, and add as many thermal vias as possible beneath the thermal PAD on the PCB for the heat conductivity of the device and PCB.

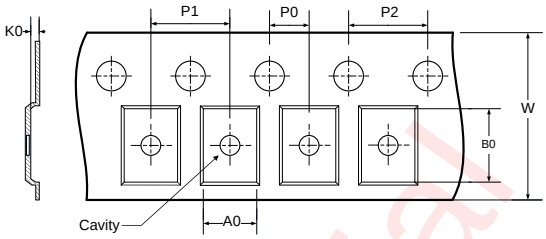


TAPE AND REEL INFORMATION

REEL DIMENSIONS

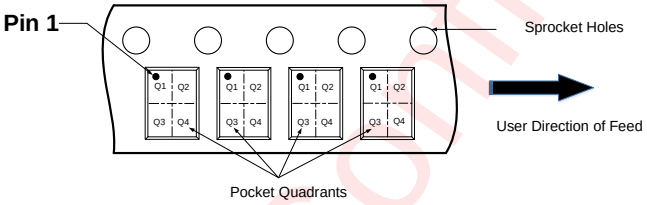


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



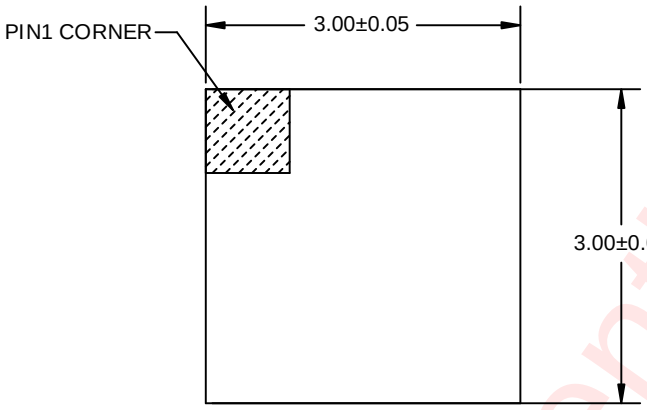
Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

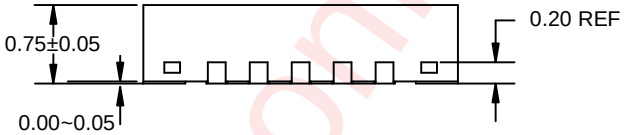
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330	12.4	3.3	3.3	1.1	2	8	4	12	Q1

All dimensions are nominal

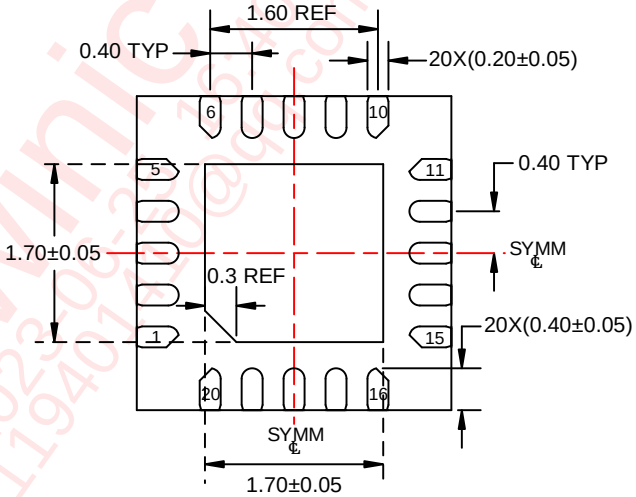
PACKAGE DESCRIPTION



TOP VIEW



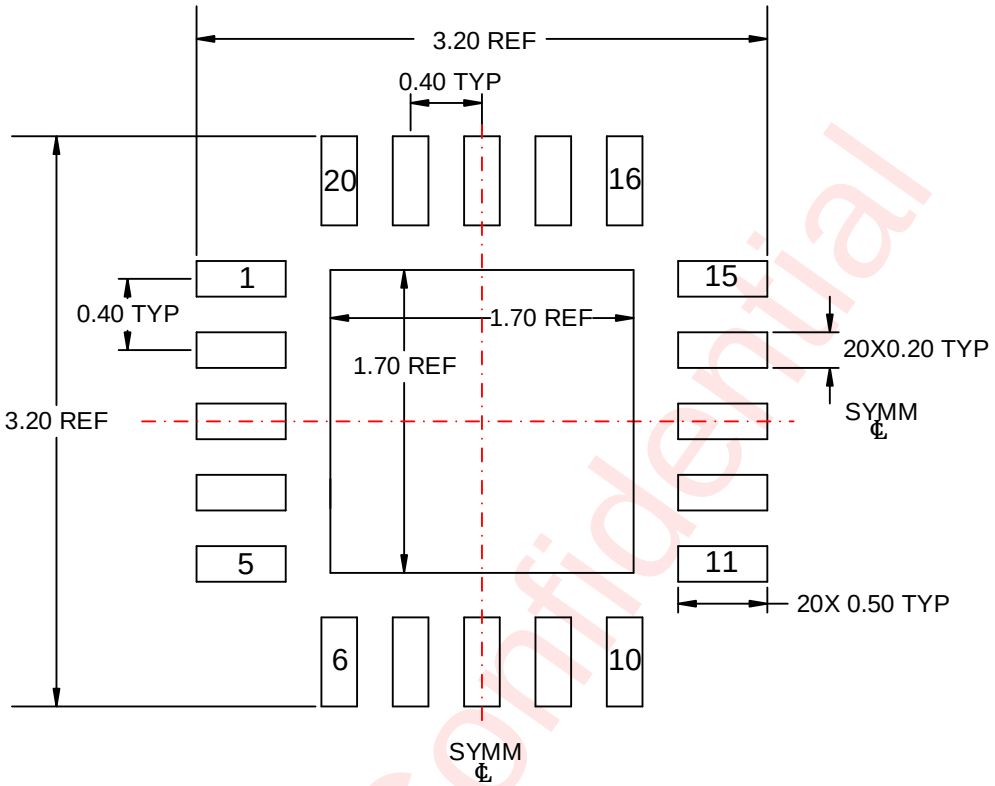
SIDE VIEW

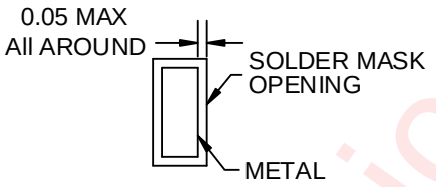


BOTTOM VIEW

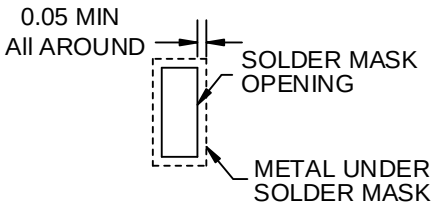
Unit：mm

LAND PATTERN DATA





NON-SOLDER MASK DEFINED



SOLDER MASK DEFINED

Unit: mm

REVISION HISTORY

Version	Date	Change Record
V1.0	Jun. 2022	Officially released
V1.1	Jul. 2022	Modified T_A of Electrical Characteristics

DISCLAIMER

All trademarks are the property of their respective owners. Information in this document is believed to be accurate and reliable. However, Shanghai AWINIC Technology Co., Ltd (AWINIC Technology) does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

AWINIC Technology reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. Customers shall obtain the latest relevant information before placing orders and shall verify that such information is current and complete. This document supersedes and replaces all information supplied prior to the publication hereof.

AWINIC Technology products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an AWINIC Technology product can reasonably be expected to result in personal injury, death or severe property or environmental damage. AWINIC Technology accepts no liability for inclusion and/or use of AWINIC Technology products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications that are described herein for any of these products are for illustrative purposes only. AWINIC Technology makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

All products are sold subject to the general terms and conditions of commercial sale supplied at the time of order acknowledgement.

Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Reproduction of AWINIC information in AWINIC data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. AWINIC is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of AWINIC components or services with statements different from or beyond the parameters stated by AWINIC for that component or service voids all express and any implied warranties for the associated AWINIC component or service and is an unfair and deceptive business practice. AWINIC is not responsible or liable for any such statements.

单击下面可查看定价，库存，交付和生命周期等信息

>>AWINIC(艾为)