AW3571X Two-Channel High-Speed Differential 1:2 Switch

Features

- Operating voltage 2.7 to 3.6V
- Compatible with USB3.1, PCIe-Gen3, MIPI DSI/CSI
- Data rates up to 10Gbps
- -3dB bandwidth:
  - Typ. 10GHz AW35710QNR
  - Typ. 9.1GHz AW35711QNR
- Wide common mode voltage 0 to 2.2V
- Insertion loss:
  - -1.5dB @4GHz AW35710QNR
  - -1.6dB @4GHz AW35711QNR
- Return loss: -20dB @4GHz
- Off isolation: -22dB @4GHz
- QFN 4.5mm X2.5mm X0.5mm-20L package
  QFN 2.0mm X2.0mm X0.55mm-18L package

Applications

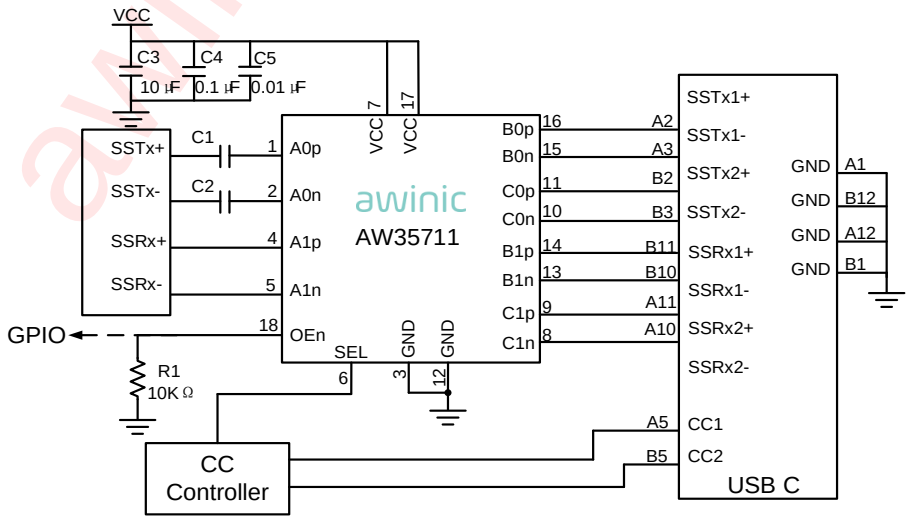
Desktop and Notebook PCs
Mobile phones
Type-C Ecosystem

General Description

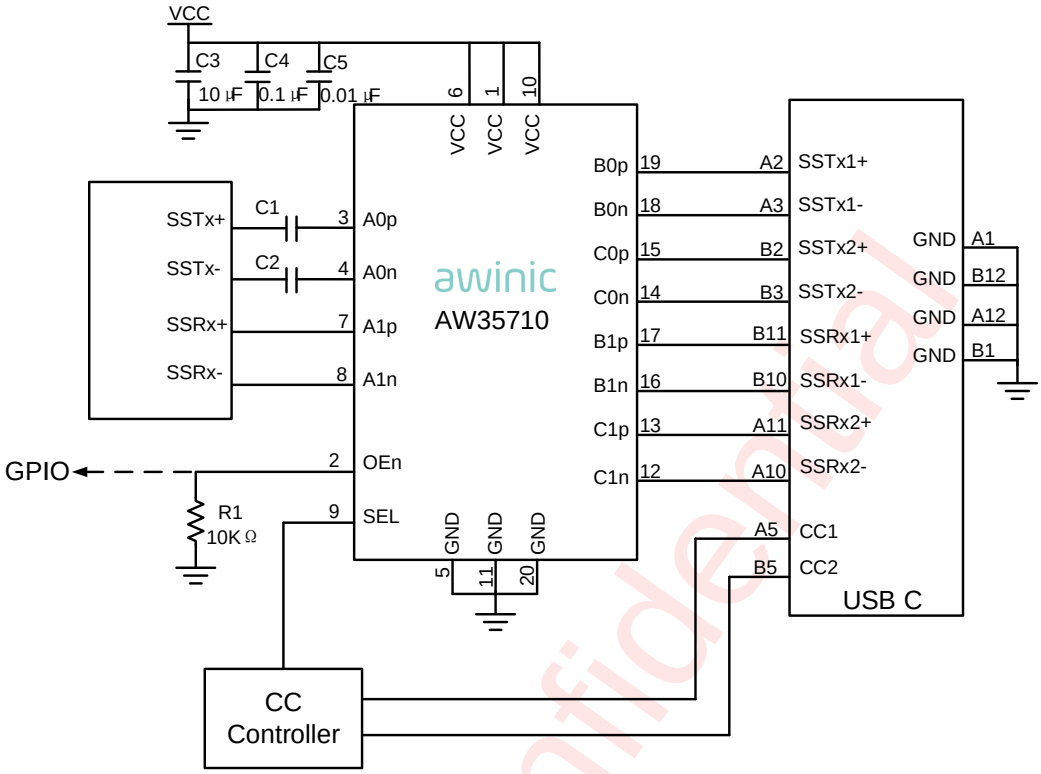
The AW3571X is a high-speed differential 1:2 switch. It can support high speed data transmission protocols such as USB 3.1 Gen 1 and Gen 2, PCI-Gen3, MIPI DSI/CSI. The device supports switching on differential channels between Port B or Port C to Port A under the control of pin SEL.

The AW3571X is an analog differential passive switch. The device can operate on any high-speed interface applications in the range of 0 to 2.2V common mode voltage. With employing adaptive tracking, it ensures that the channel holds constant within the entire common mode voltage range.

Typical Application Circuit



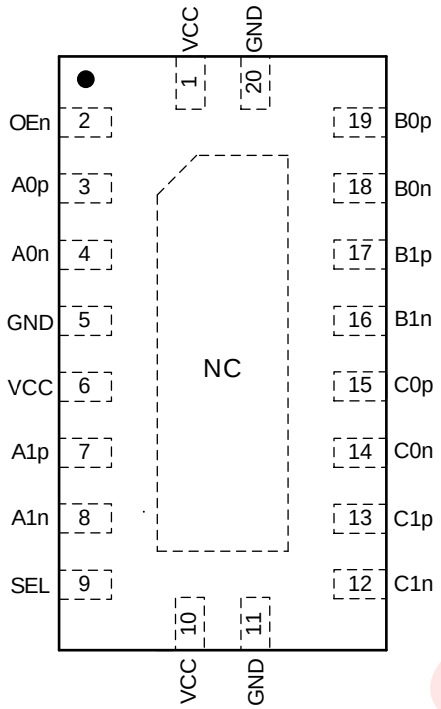
Typical Application Circuit of AW35711



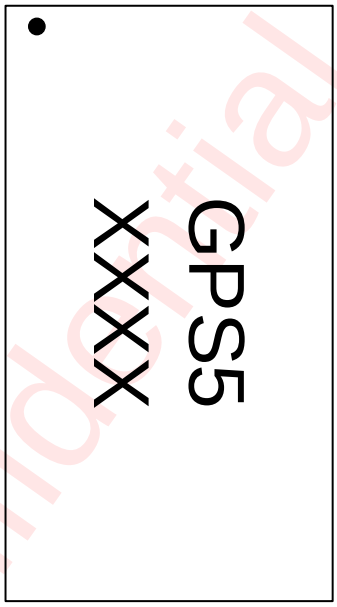
Typical Application Circuit of AW35710

Pin Configuration And Top Mark

AW35710QNR
(Top View)

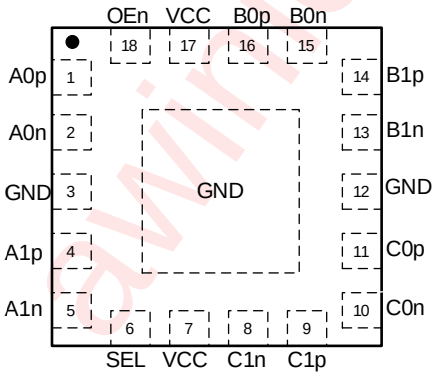


AW35710QNR Marking
(Top View)

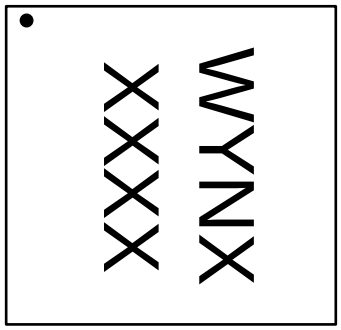


GPS5 – AW35710QNR
XXXX - Production Tracing Code

AW35711QNR
(Top View)



AW35711QNR Marking
(Top View)

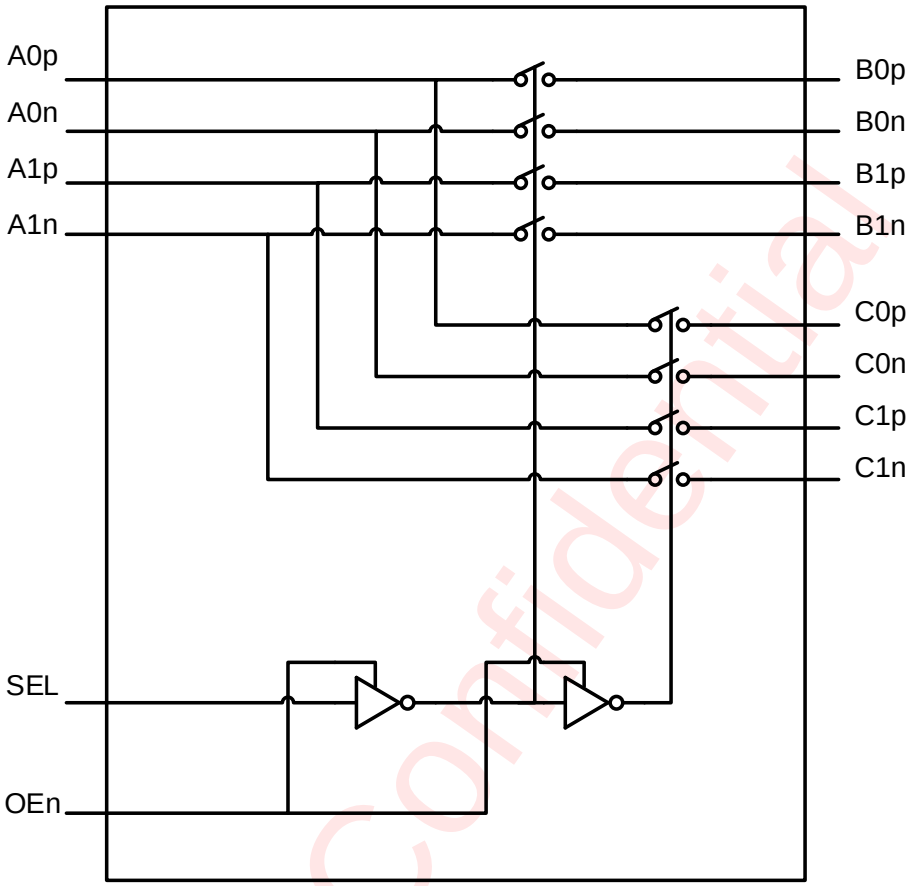


WYNX – AW35711QNR
XXXX - Production Tracing Code

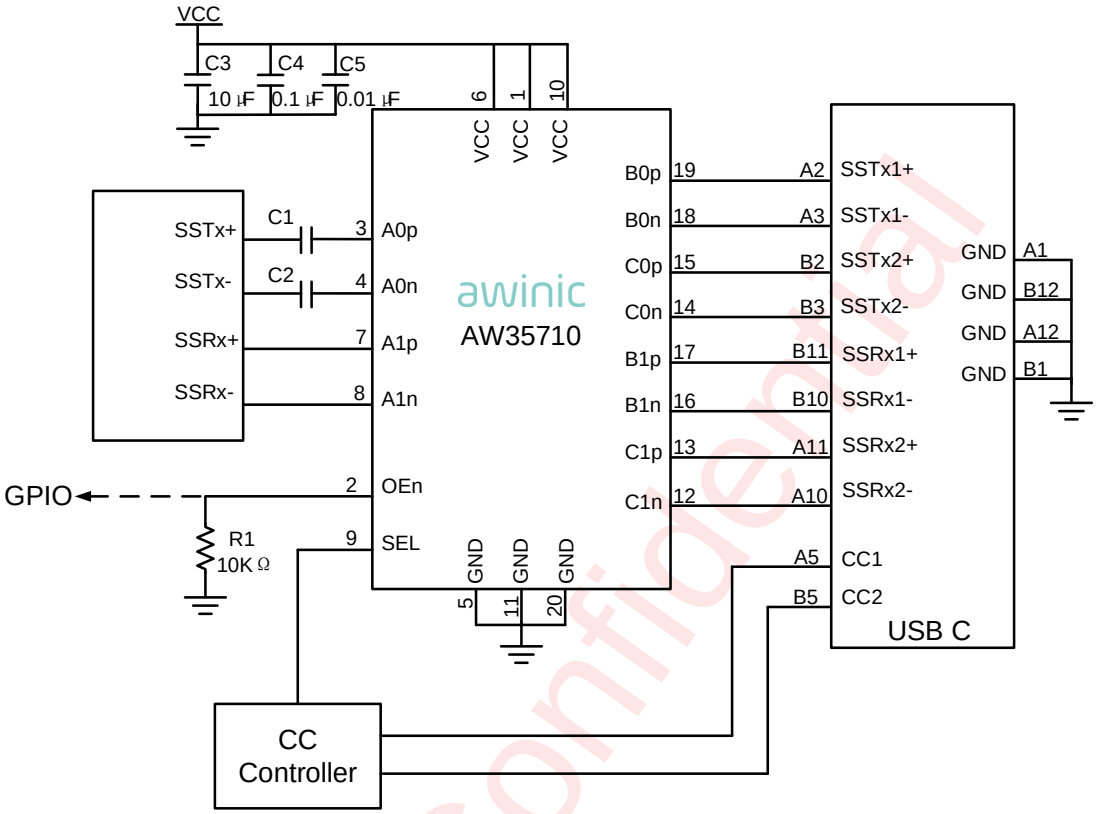
Pin Definition

Pin No.		NAME	DESCRIPTION
AW35710	AW35711		
1	17	VCC	Power
2	18	OEn	Chip enable L: Normal operation H: Shutdown
3	1	A0p	Port A, channel 0, high-speed positive signal
4	2	A0n	Port A, channel 0, high-speed negative signal
5	3	GND	Ground
6		VCC	Power
7	4	A1p	Port A, channel 1, high-speed positive signal
8	5	A1n	Port A, channel 1, high-speed negative signal
9	6	SEL	Port select pin. L: Port A to Port B H: Port A to Port C
10	7	VCC	Power
11	12	GND	Ground
12	8	C1n	Port C, channel 1, high-speed negative signal
13	9	C1p	Port C, channel 1, high-speed positive signal
14	10	C0n	Port C, channel 0, high-speed negative signal
15	11	C0p	Port C, channel 0, high-speed positive signal
16	13	B1n	Port B, channel 1, high-speed negative signal
17	14	B1p	Port B, channel 1, high-speed positive signal
18	15	B0n	Port B, channel 0, high-speed negative signal
19	16	B0p	Port B, channel 0, high-speed positive signal
20		GND	Ground

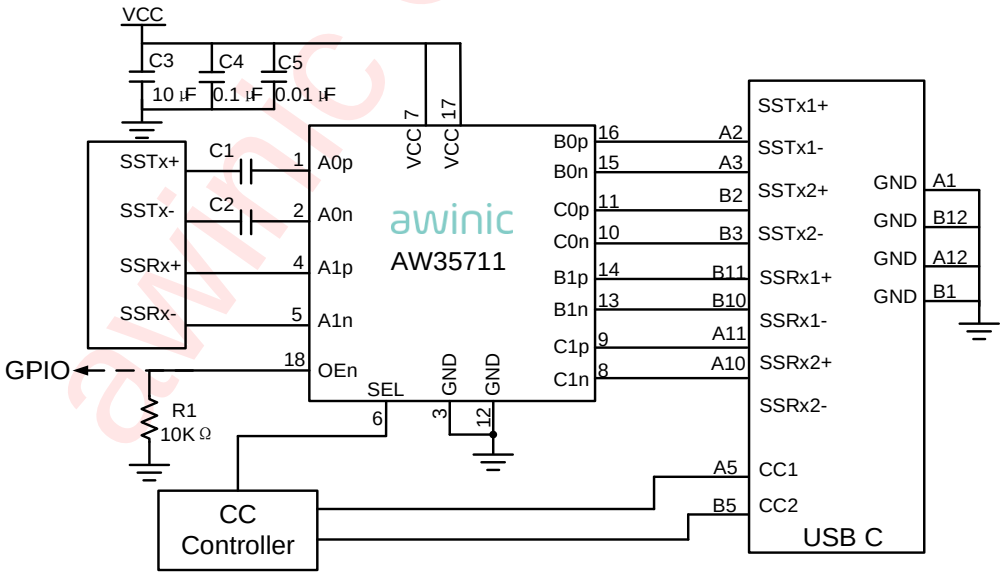
Functional Block Diagram



Typical Application Circuits



AW35710 Application Circuit: Down Facing Port for USB3.1 Type C Connector



AW35711 Application Circuit: Down Facing Port for USB3.1 Type C Connector

Notice for typical application circuits:

1.If AC couple is needed, the capacitance of C1 and C2 is recommended 100nF.

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW35710QNR	-40℃～85℃	QFN 4.5mmX2.5mm-20L	GPS5	MSL1	ROHS+HF	9000 units/ Tape and Reel
AW35711QNR	-40℃～85℃	QFN 2.0mmX2.0mm-18L	WYNX	MSL1	ROHS+HF	4500 units/ Tape and Reel

Absolute Maximum Ratings(NOTE1)

PARAMETERS		RANGE
Supply voltage range V_{CC}		-0.5V to 4V
Input voltage range	Differential I/O	-0.5V to 2.7V
	Control pins	-0.5V to V_{CC}
Junction-to-ambient thermal resistance θ_{JA}(NOTE2)		107°C /W
Operating free-air temperature range		-40°C to 85°C
Maximum operating junction temperature T_{JMAX}		150°C
Storage temperature T_{STG}		-65°C to 150°C
Lead temperature (soldering 10 seconds)		260°C
ESD		
HBM(NOTE3)		±2kV
CDM(NOTE4)		±1.5kV
Latch-Up		
Test condition(NOTE5)		+IT：200mA -IT：-200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: Thermal resistance from junction to ambient is highly dependent on PCB layout.

NOTE3: All pins. Test Condition: ANSI/ESDA/JEDEC JS-001 2017.

NOTE4: All pins. Test Condition: JEDEC EIA/JESD22-C101F .

NOTE5: All pins. Test Condition: JEDEC STANDARD NO.78E NOVEMBER 2016 .

Recommended Operating Conditions

SYMBOL	PARAMETERS	RANGE
VCC	Supply voltage	2.7V to 3.6V
V_{IH}	Input high voltage (SEL, OEn pins)	Min 1.2V
V_{IL}	Input low voltage (SEL, OEn pins)	Max 0.5V
Vdiff	High-speed signal pins differential voltage	0V to 1.8V
V_{CM}	High speed signal pins common mode voltage	0V to 2.2V
T_A	Operating free-air temperature	-40°C to 85°C

DC Electrical Characteristics

VCC=2.7 to 3.6V, OEn=0, T_A=-40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
I_{CC}	Device active current	VCC=2.7 to 3.6V, OEn=0		0.2	0.6	mA
I_{STDN}	Device shutdown current	VCC=2.7V, OEn=VCC		0.6	10	μA
		VCC=3.3V, OEn=VCC		2	20	μA
		VCC=3.6V, OEn=VCC		5	30	μA
C_{ON}	Output ON capacitance			0.6		pF
C_{OFF}	Output OFF capacitance			0.8		pF
R_{ON}	Output ON resistance	VCC=2.7 to 3.6V, V_{CM}=0 to 2V IO=-8mA		7.5	12	Ω
ΔR_{ON}	On-resistance match between pairs of the same channel	VCC=2.7 to 3.6V, -0.35V≤V_{IN} ≤2.35V,IO=-8mA		0.1	0.5	Ω
R_{FLAT_ON}	On-resistance flatness R_{ON}(MAX)-R_{ON}(MIN)	VCC=2.7 to 3.6V, -0.35V≤V_{IN} ≤2.35V			1	Ω
$I_{IH,CTRL}$	Input high current, control pins(SEL, OEn)				1	μA
$I_{IL,CTRL}$	Input low current ,control pins(SEL, OEn)				1	μA
$I_{IH,HS}$	Input high current, high-speed pins[Ax/Bx/Cx][p/n]	V_{IN}=2V for selected port, A and B with SEL=0,and A and C with SEL=VCC			1	μA
$I_{IH,HS}$	Input high current, high-speed pins[Ax/Bx/Cx][p/n]	V_{IN}=2V for non-selected C with SEL=0, and B with SEL=VCC(1)		160		μA
$I_{IL,HS}$	Input low current, high-speed pins[Ax/Bx/Cx][p/n]				1	μA

(1) There is a 20-kΩ pull-down in non-selected port.

AC Electrical Characteristics

VCC=2.7 to 3.6V, OEn=0, T_A=-40°C to 85°C (unless otherwise noted)

PARAMETER			TEST CONDITION	MIN	TYP	MAX	UNIT
I_L	Differential insertion loss	AW35710	f=4GHz	-1.7	-1.5		dB
			f=5GHz	-1.8	-1.7		
		AW35711	f=4GHz	-1.7	-1.6		dB
			f=5GHz	-2.5	-2.4		
BW	-3dB bandwidth	AW35710		8	10		GHz
		AW35711		8	9.1		GHz
R_L	Differential return loss		f=4GHz		-20	-16	dB
			f=5GHz		-16	-14	
O_{IRR}	Differential OFF isolation		f=4GHz		-22	-20	dB
			f=5GHz		-20	-18	
X_{TALK}	Differential crosstalk		f=4GHz		-42	-38	dB
			f=5GHz		-40	-36	
t_{PD}	Switch propagation delay (1) (2)			13	45	70	ps
t_{SEL_ON}	Switching time SEL to Switch ON		RL=50Ω		30	250	ns
t_{SEL_OFF}	Switching time SEL to Switch OFF		RL=50Ω		40	250	ns
t_{OEn_ON}	Switching time OEn to Switch ON		RL=50Ω		20	30	μs
t_{OEn_OFF}	Switching time OEn to Switch OFF		RL=50Ω		1.3	2.0	μs
t_{SK_INTRA}	Intra-pair output skew			0.5	5.3	6	ps
t_{SK_INTER}	Inter-pair output skew			0.5	8	20	ps

(1) The coaxial cable's bandwidth should > 8GHz.

(2) When test t_{PD} characteristic, should keep the input and output coaxial cable's characteristic impedance same.

Typical Characteristics

Test Information

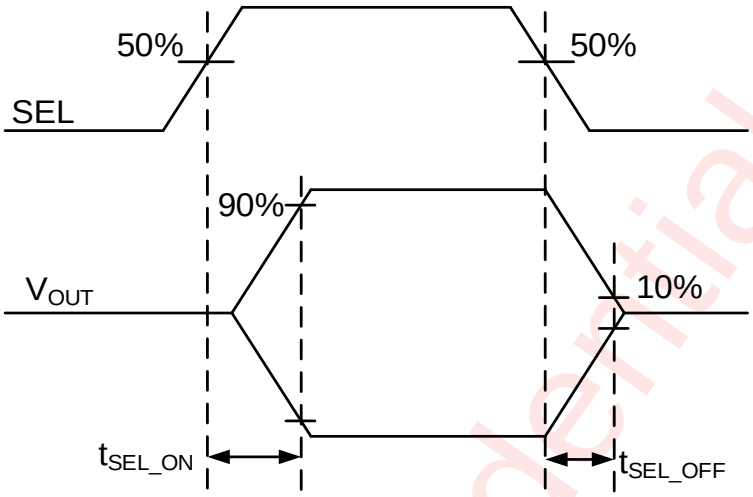


Figure1 Swtich on and off

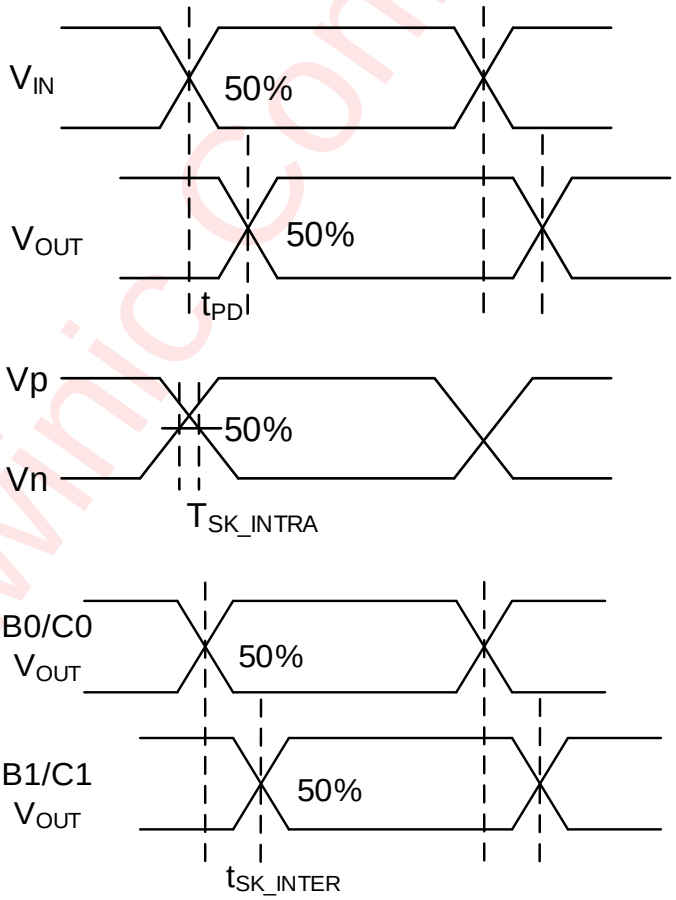
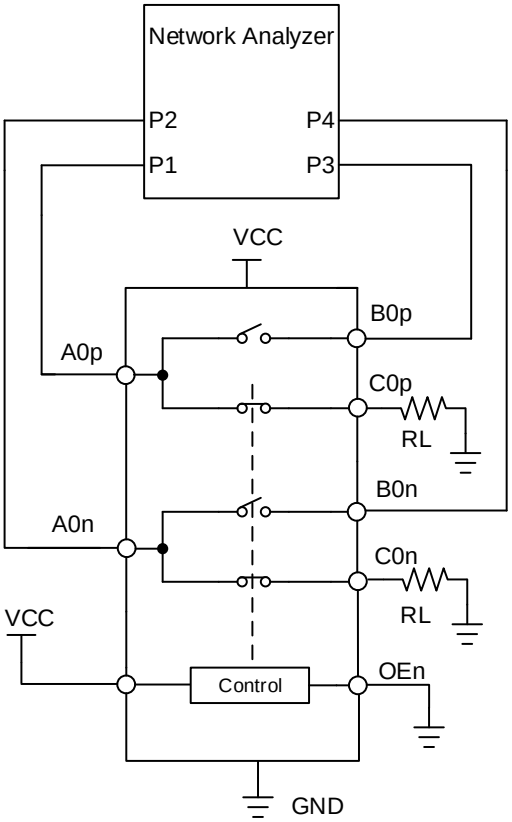
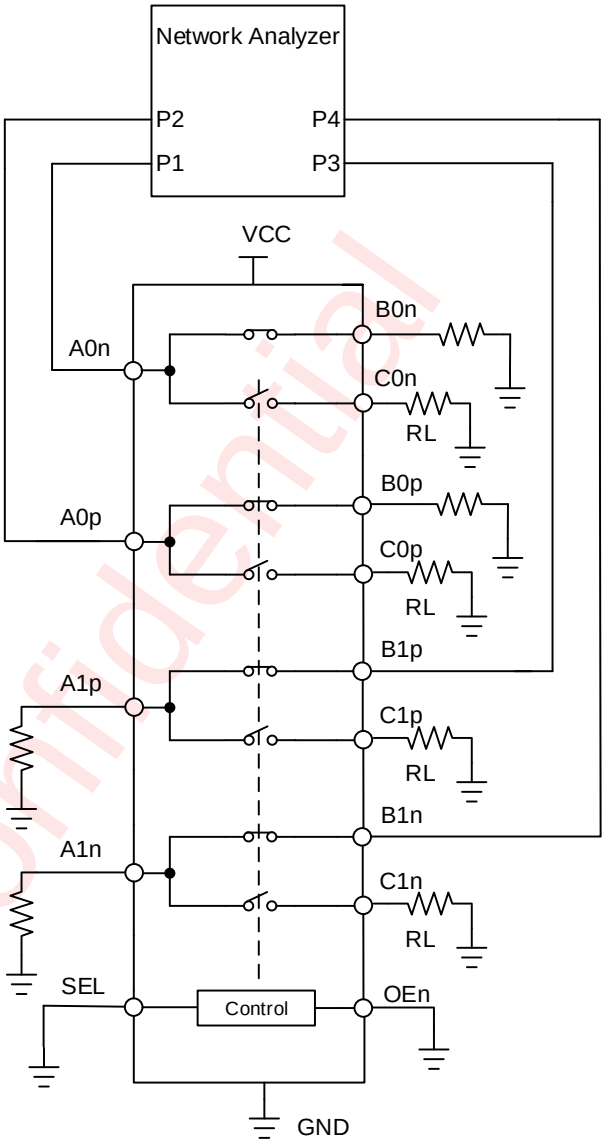


Figure2 Timing Diagrams



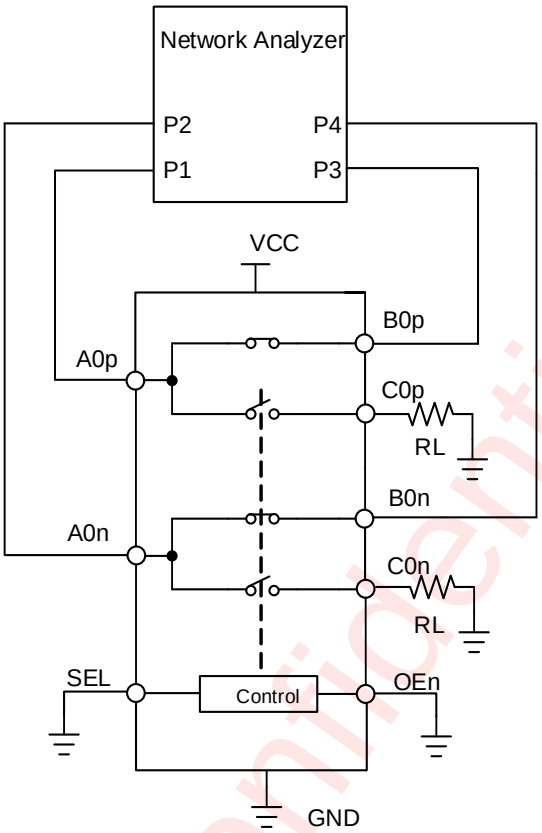
RL=50Ω
All unused ports are connected to GND through a 50Ω pull-down resistors

Figure3 Isolation



RL=50Ω
All unused ports are connected to GND through a 50Ω pull-down resistors

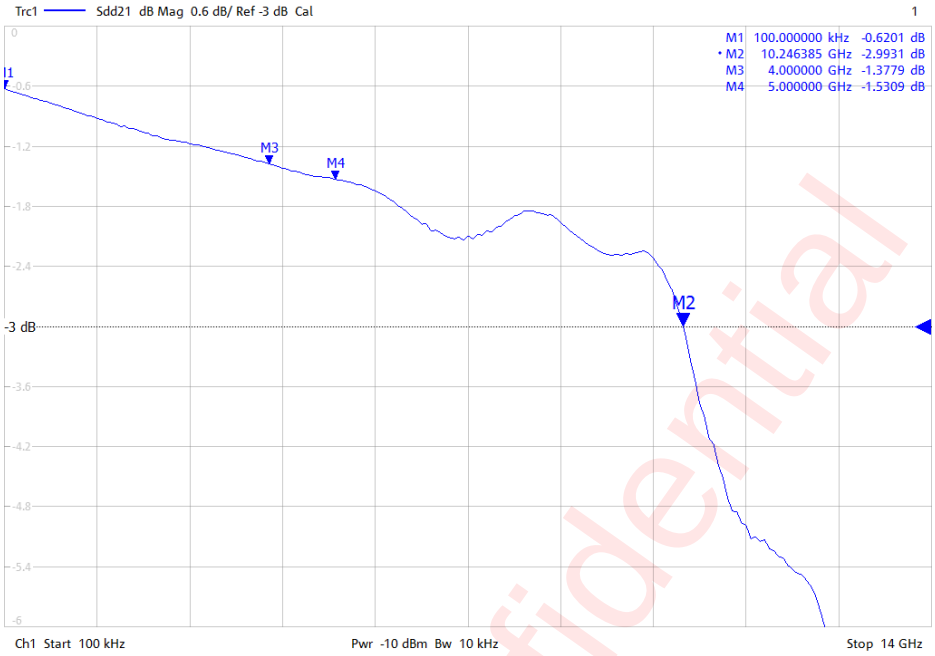
Figure4 Crosstalk



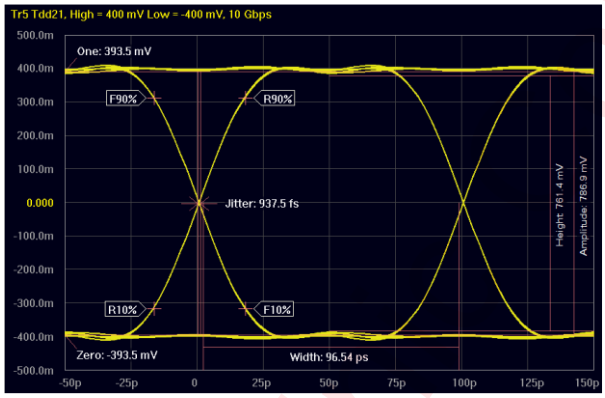
RL=50Ω
All unused ports are connected to GND through a 50Ω pull-down resistors

Figure5 -3dB Bandwidth, Differential return loss, Differential insertion loss

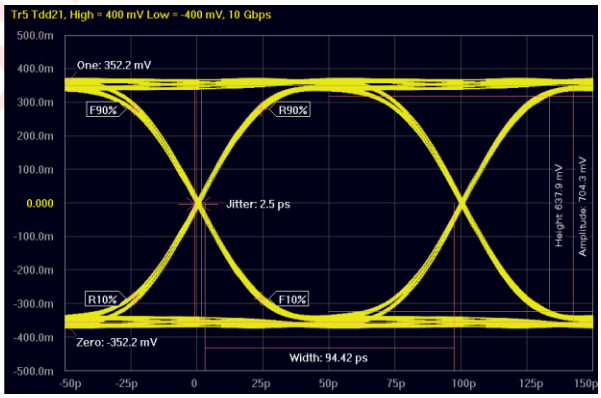
Typical Curve TA=25°C



-3dB Bandwidth Diagram



Before AW35710QNR



After AW35710QNR

10Gbps Output Eye Diagram

Detailed Functional Description

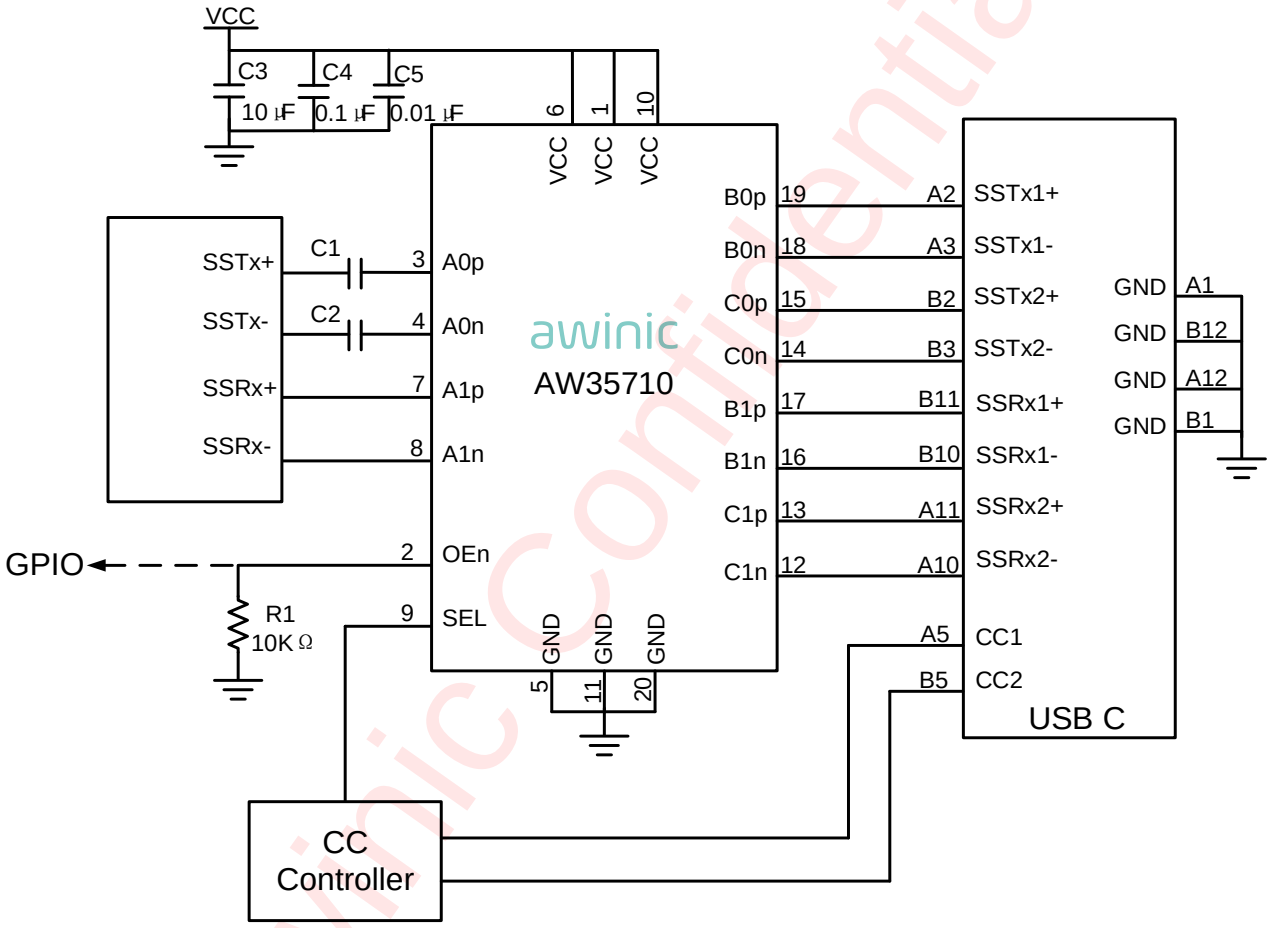
The AW3571X is a class of analog differential passive switch. The device can operate on any high-speed interface applications in the range of 0 to 2.2V common mode voltage. With employing adaptive tracking ,it ensures that the channel holds constant within the entire common mode voltage range.

The device has excellent dynamic characteristics, which allows high-speed switching with minimum attenuation with little extra jitter to the signal eye diagram.

Application Information

The AW3571X is a high-speed bidirectional passive switch, which can be configured in either mux or demux switch to meet the requirement of any high-speed interface application. The AW3571X supports signals with common mode voltage from 0V to 2.2V and differential amplitude up to 1800mVpp. The device adopts adaptive tracking to ensure that the channel remains unchanged in the whole common mode voltage range.

Many interfaces require AC coupling between the transmitter and receiver. The 0402 capacitor is best, and the value should match for the signal pairs. Place them along the TX pairs on the system board. The best way to place AC coupling capacitors is to keep them symmetric on the top layer of the board.



AW35710 Application Circuit: Down Facing Port for USB3.1 Type C Connector

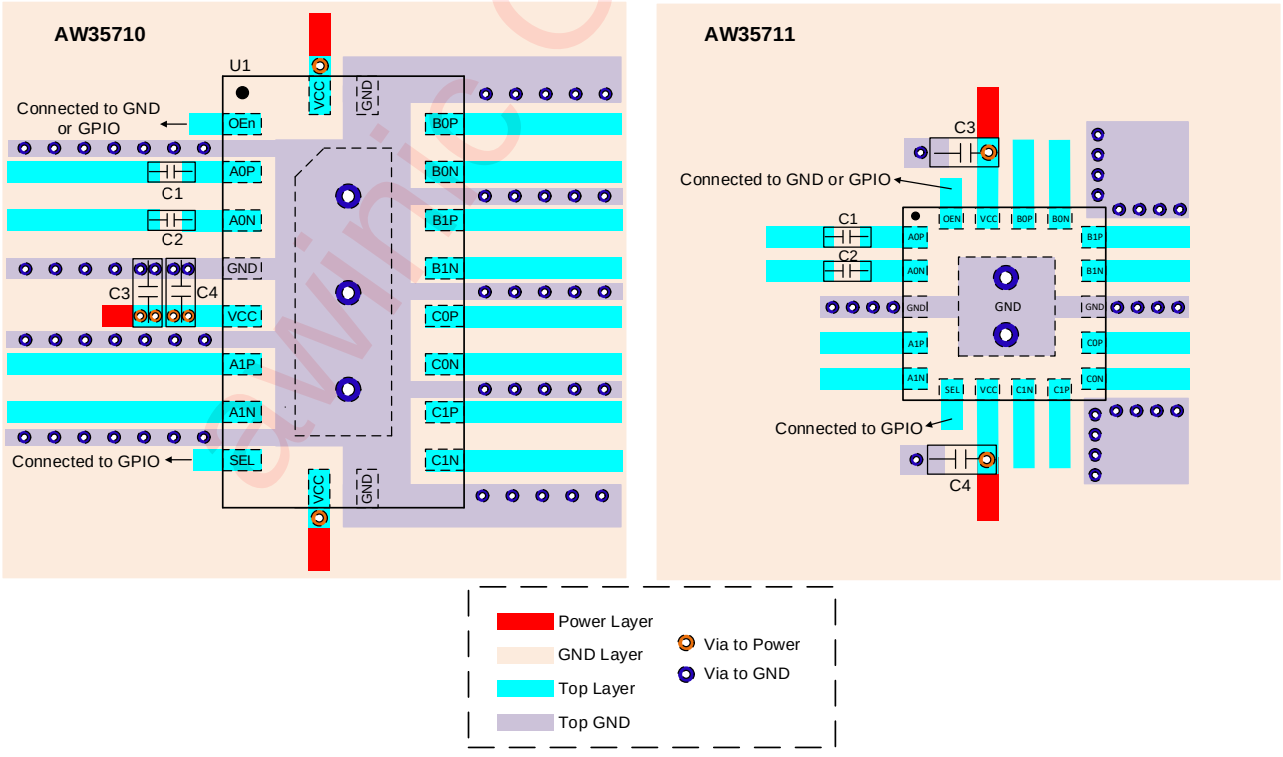
PCB Layout Information

Layout Guidelines

To obtain the optimal performance of AW3571X, PCB layout should be considered carefully. Here are some guidelines:

1. Place supply bypass capacitors as close to VCC and GND pin as possible and avoid placing the bypass capacitors near the high-speed traces.
2. The characteristic impedance of the traces must match that of the receiver and transmitter to maintain signal integrity.
3. Route the high-speed signals using a minimum amount of vias and corners which reduces signal reflections and impedance changes. When it becomes necessary to make the traces turn 90°, use an arc instead of making a single 90° turn.
4. Do not route high-speed traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or ICs that use or duplicate clock signals.
5. Avoid stubs on the high-speed signal lines because they cause signal reflections.
6. Route all high-speed signal traces over continuous GND planes, with no interruptions.
7. High speed differential traces ensures equal width, line length and line spacing.

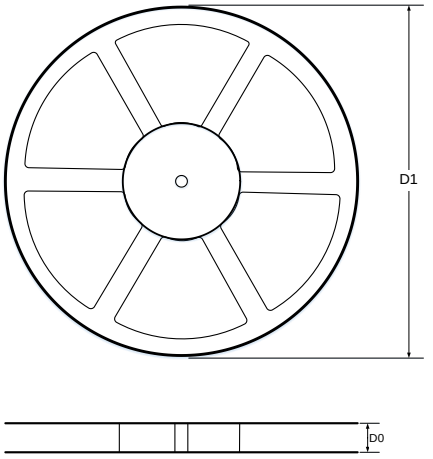
Layout Example



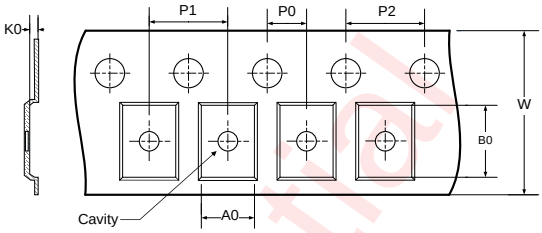
Tape And Reel Information

QFN 4.5mmX2.5mm-20L

REEL DIMENSIONS

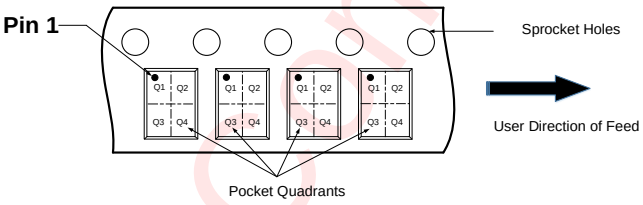


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



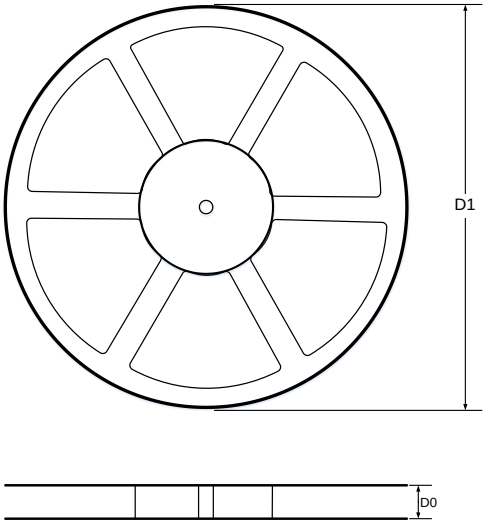
DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330	12.4	2.75	4.75	0.75	2	4	4	12	Q1

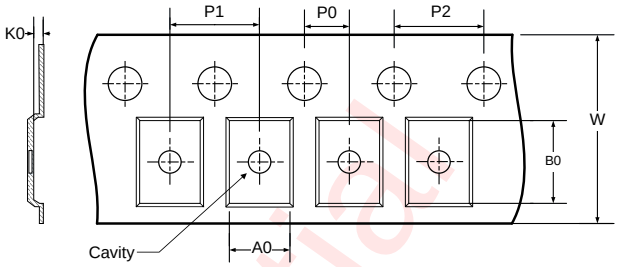
All dimensions are nominal

QFN 2.0mmX2.0mm-18L

REEL DIMENSIONS



TAPE DIMENSIONS



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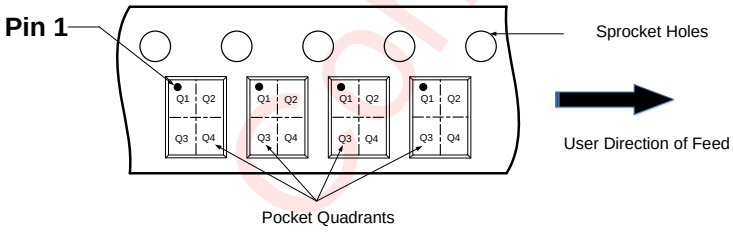


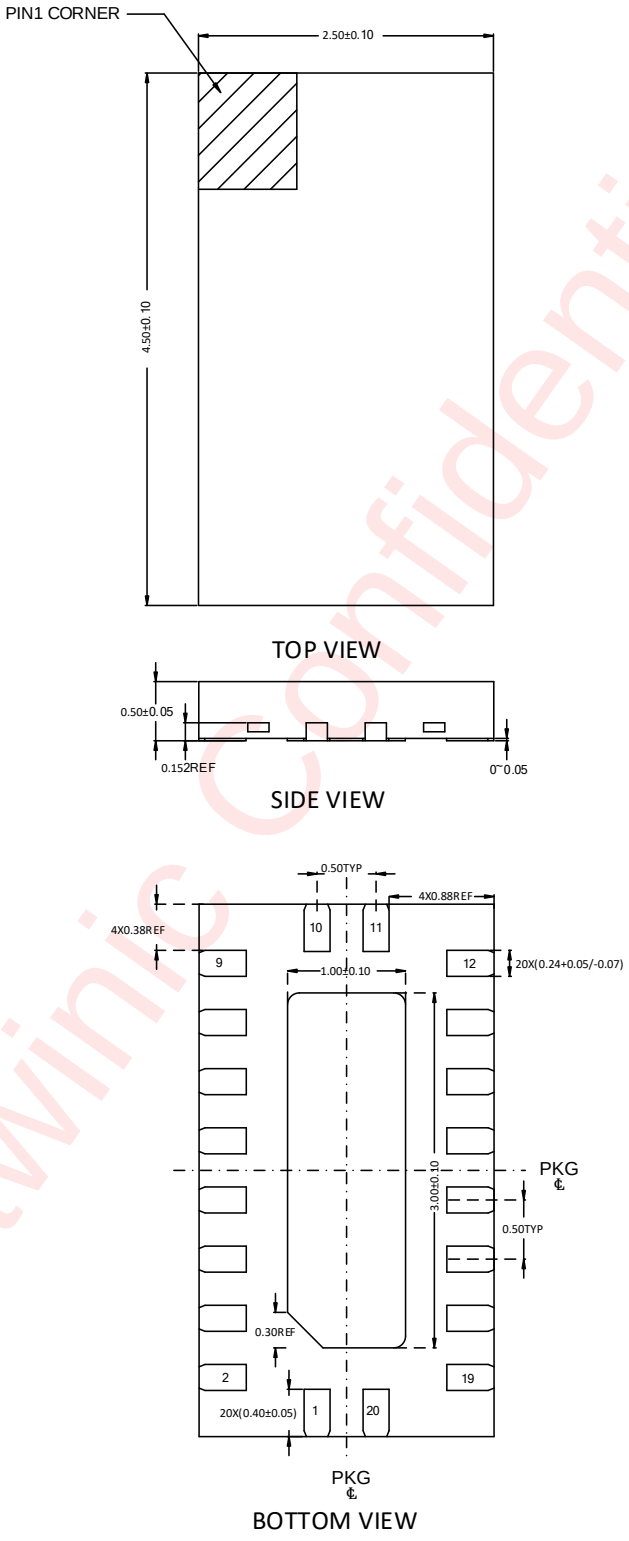
DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.4	2.25	2.25	0.75	2	4	4	8	Q1

All dimensions are nominal

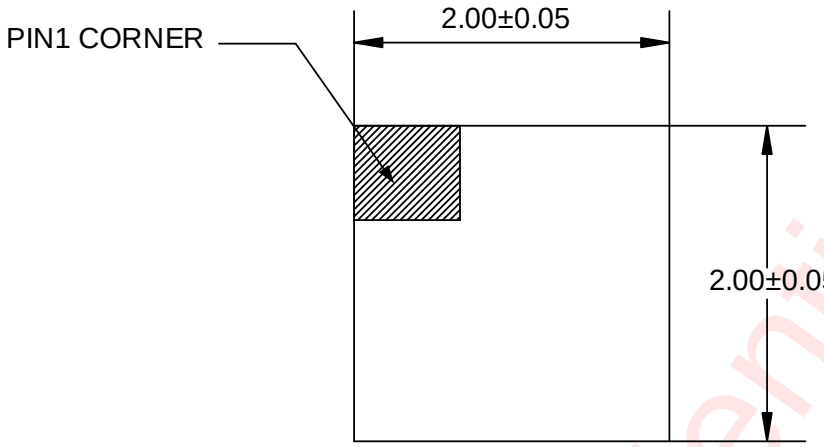
Package Description

QFN 4.5mmX2.5mm-20L

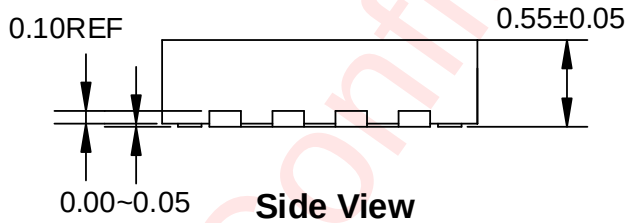


Unit: mm

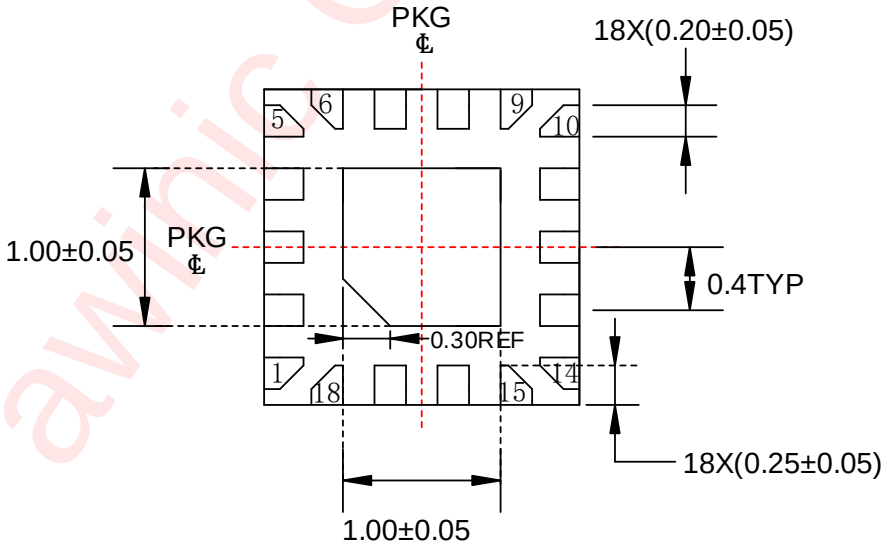
QFN 2.0mmX2.0mm-18L



Top View



Side View

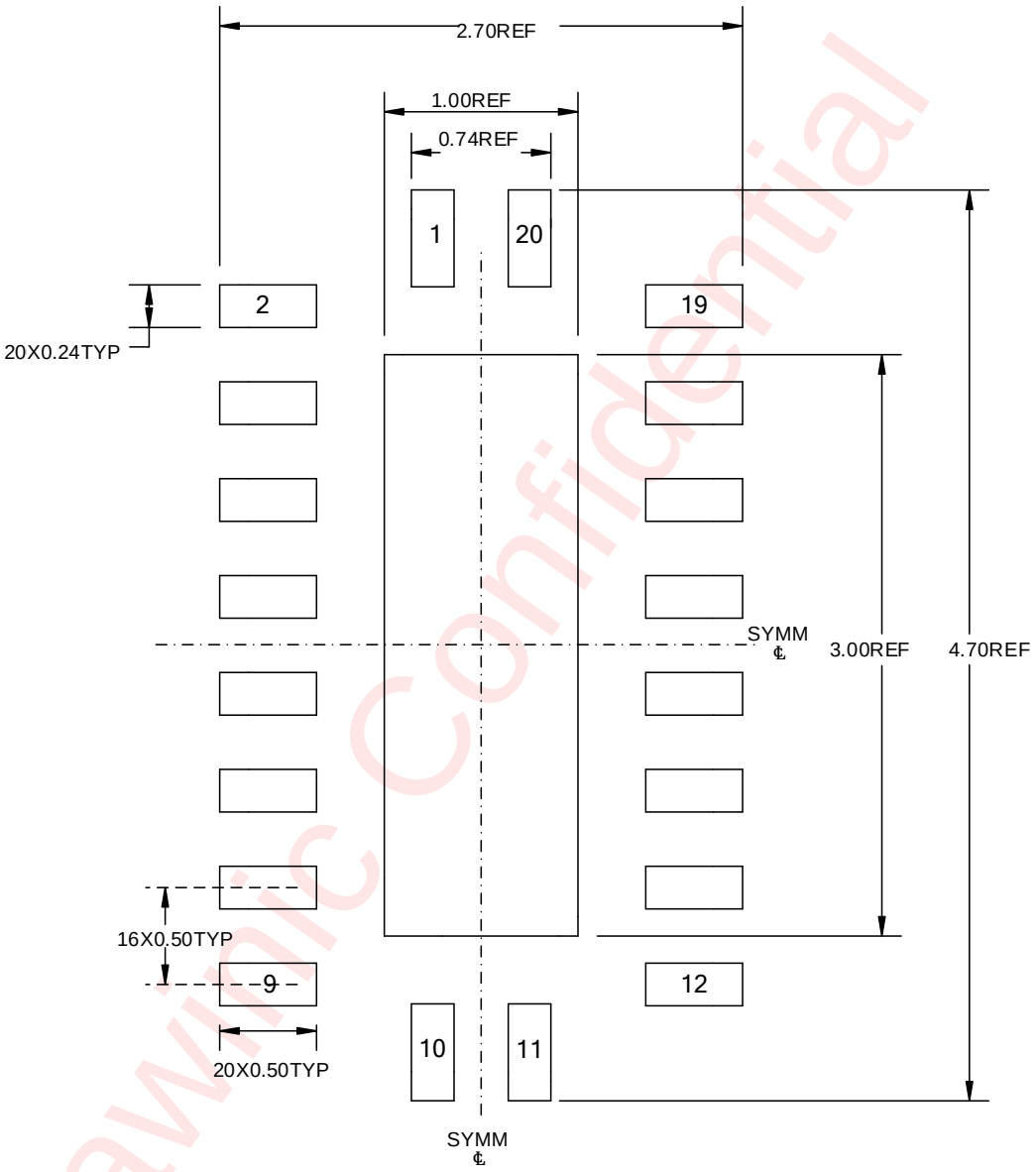


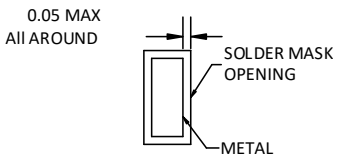
Bottom View

Unit：mm

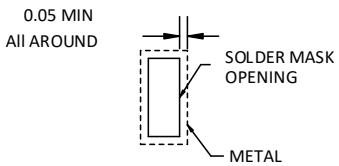
Land Pattern Data

QFN 4.5mmX2.5mm-20L





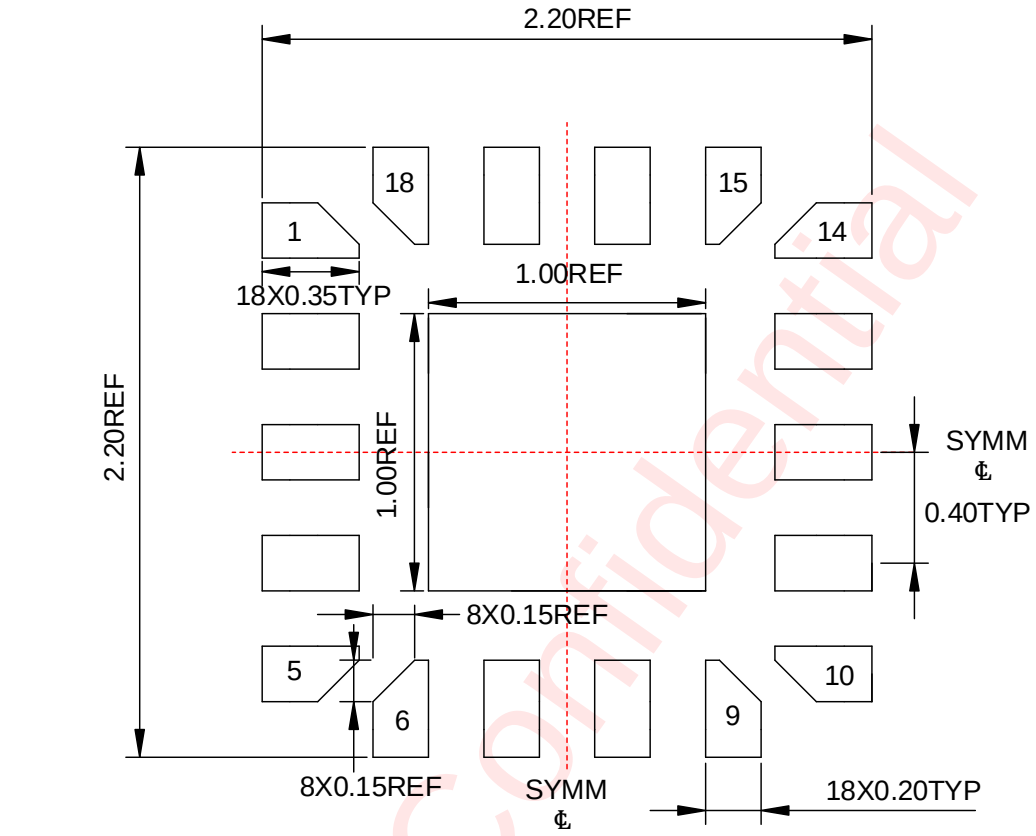
NON SOLDER MASK DEFINED

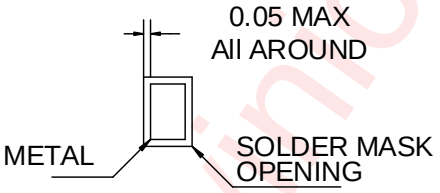


SOLDER MASK DEFINED

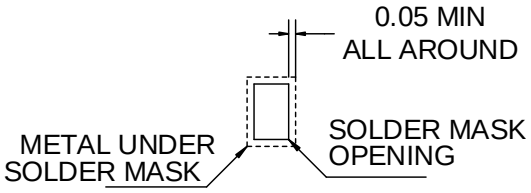
Unit: mm

QFN 2.0mmX2.0mm-18L





NON-SOLDER MASK DEFINED



SOLDER MASK DEFINED

Unit: mm

Revision History

Version	Date	Change Record
V1.0	July 2020	Officially released
V1.1	November 2020	Add t_{PD}, t_{SK_INTRA}, t_{SK_INTER} min characteristics
V1.2	January 2021	Add ΔR_{ON} TYP characteristic
V1.3	April 2021	Update the DC and AC Electrical Characteristics
V1.4	September 2021	Add AW35711QNR
V1.5	November 2021	Add 2.7V and 3.6V characteristics
V1.6	November 2021	Add t_{PD} characteristic's test condition
V1.7	June 2022	Update Pin Configuration and Absolute Maximum Ratings

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