8-Channel Capacitive In-Ear Detection and Touch Key Controller

FEATURES

- 8-channel capacitive sensor
  - Self/Mutual capacitive sensing
  - Capacitance resolution down to 1aF
  - Auto-Offset-Tuning (AOT)
  - Adaptive Temperature Compensation
  - Effective waterproof
  - Independent configurations per channel
- Built-in gesture/event recognition:
  - Click/Wear detection
  - Linear slide detection
  - Capacitive force detection
- 400kHz I²C interface，address: 0x12
- External interrupt pin INTN, open-drain output
- Built-in brown-out reset(BOR)
- Accurate and reliable low-power in-ear detection
- Touch key detection, support slider application
- Low power consumption
  - Active mode: 15.5μA
  - Doze mode: 6.5μA
  - Sleep mode: 5.0μA
  - Deep Sleep mode: 2.5μA
- 2.7V~3.6V power supply
- WLCSP 1.75mm×1.19mm×0.57mm-15B package

APPLICATIONS

Mobile phones, Tablets, Notebooks

Wearable devices, TWS

Household appliances, Desk lamp, Smart locks

GENERAL DESCRIPTION

AW93208CSR is an 8-channel capacitive proximity and touch controller mainly used for wear detection, touch key, linear slider, wheel slider, etc. The chip can realize accurate position detection for lamp dimming, volume adjustment, etc.

AW93208CSR can recognize various gestures, such as single/double/triple click, short/long press, linear slide and wheel slide with the high-resolution capacitive sensing. The chip integrates mutual capacitive technology and dedicated algorithm, which greatly improve the waterproof performance for touch key.

The built-in ultra-low-power MCU and 16KB flash realize AFE sampling control, signal filtering, RF noise suppression, adaptive temperature compensation, baseline tracking, touch/wearing status determination, etc. The chip can flexibly customize the program and support online upgrade function.
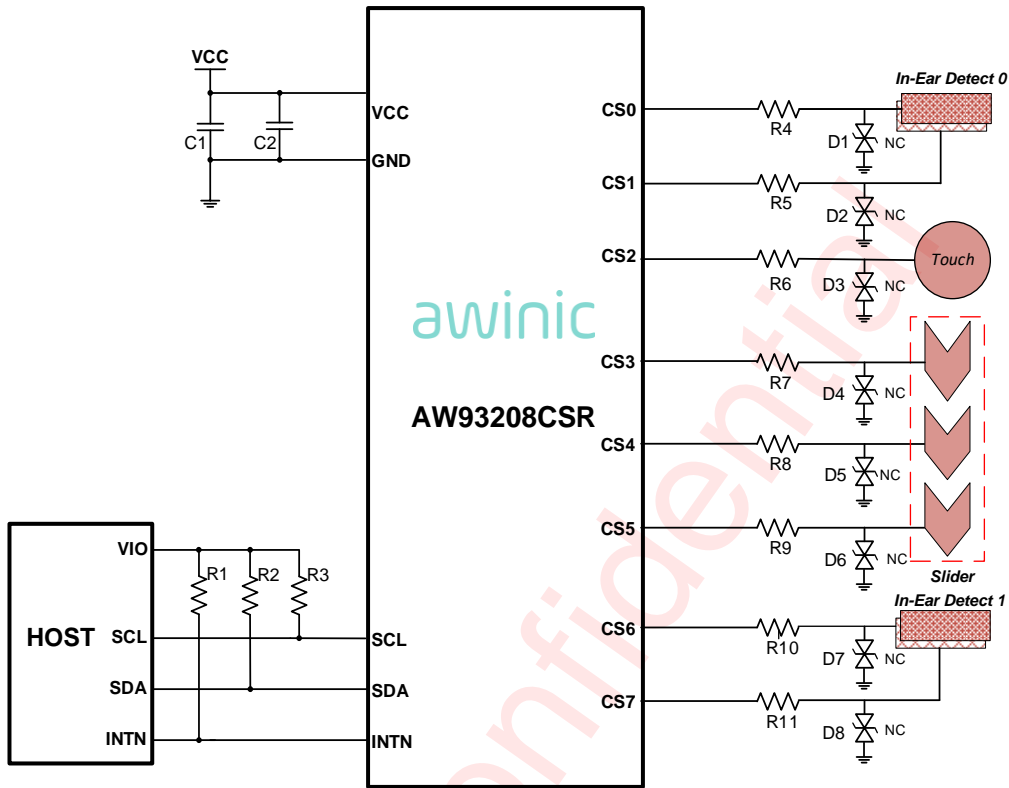

TYPICAL APPLICATION CIRCUIT

Figure 1   AW93208CSR Typical Application Circuit (touch, in-ear and slide)
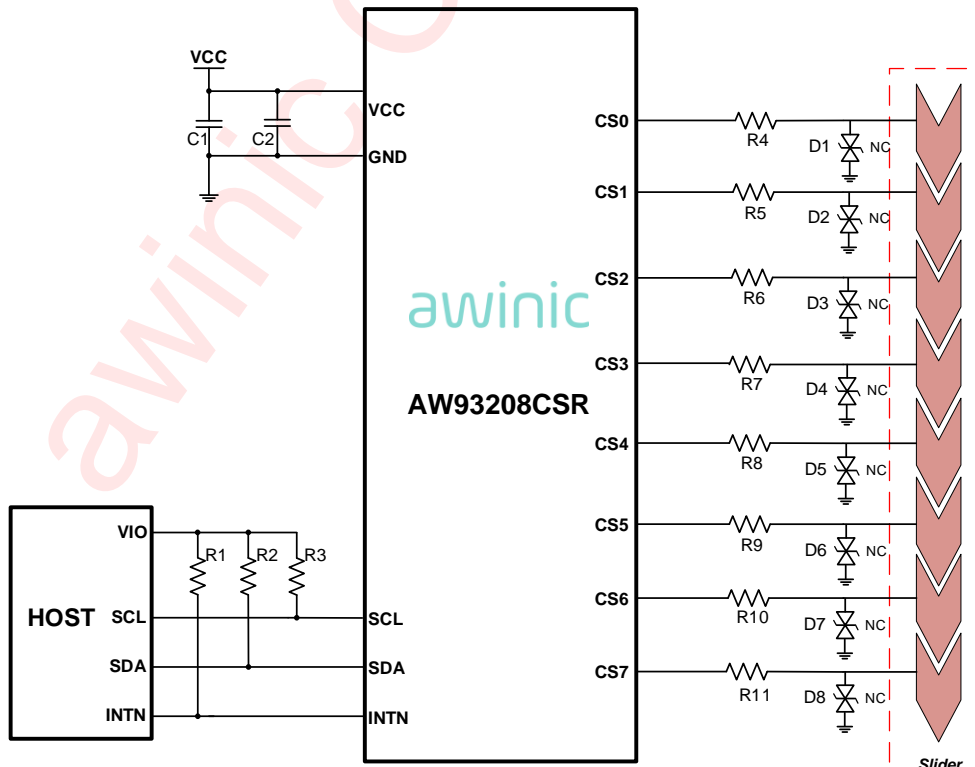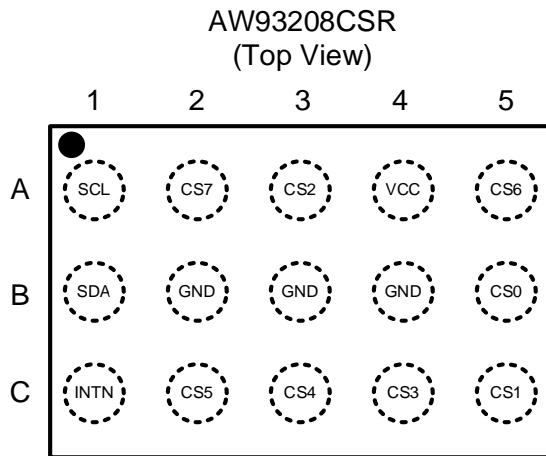

Figure 2   AW93208CSR Typical Application Circuit (slide)

PIN CONFIGURATION AND TOP MARK

AW93208CSR
(Top View)

	1	2	3	4	5
A	SCL	CS7	CS2	VCC	CS6
B	SDA	GND	GND	GND	CS0
C	INTN	CS5	CS4	CS3	CS1

AW93208CSR Marking
(Top View)

	1	2	3	4	5
A	Z6PA				
B		XXXX	XXXX	XXXX	XXXX
C					
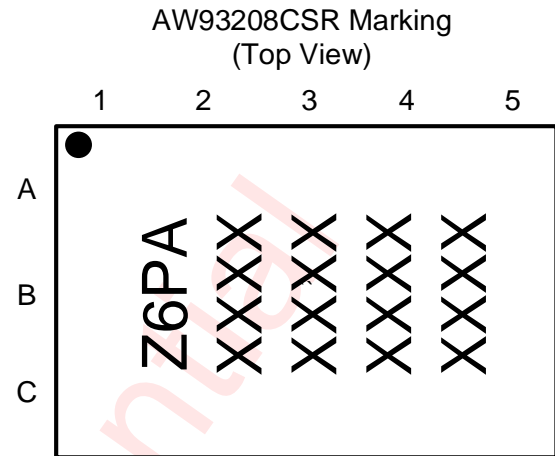
Z6PA – AW93208CSR
XXXX – Production Tracing Code

PIN DEFINITION

No.	NAME	DESCRIPTION
A1	SCL	Serial clock input for I²C interface
A2	CS7	Sensor electrode or digital I/O
A3	CS2	Sensor electrode or digital I/O
A4	VCC	Power supply(2.7V~3.6V)
A5	CS6	Sensor electrode or digital I/O
B1	SDA	Serial data I/O for I²C interface
B2	GND	Ground
B3	GND	Ground
B4	GND	Ground
B5	CS0	Sensor electrode or digital I/O
C1	INTN	Interrupt output (open drain)
C2	CS5	Sensor electrode or digital I/O
C3	CS4	Sensor electrode or digital I/O
C4	CS3	Sensor electrode or digital I/O
C5	CS1	Sensor electrode or digital I/O

FUNCTIONAL BLOCK DIAGRAM
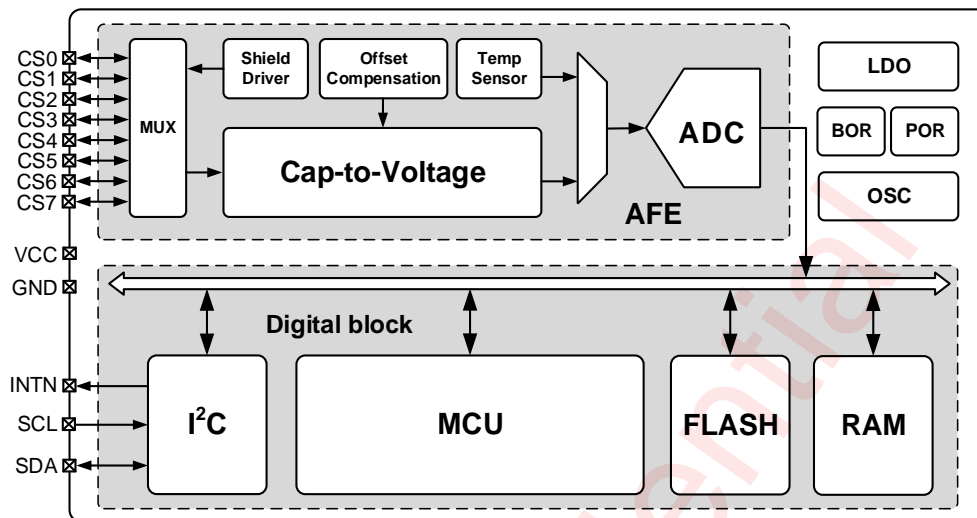
Notes: AFE means Analog Front-End.

Figure 3   Functional Block Diagram

ORDERING INFORMATION

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW93208CSR	-40℃～85℃	WLCSP 1.75mmx1.19mmx0.57 mm- 15B	Z6PA	MSL1	ROHS+HF	4500 units/ Tape and Reel

ABSOLUTE MAXIMUM RATINGS(NOTE1)

PARAMETERS		RANGE
Supply voltage range VCC		-0.5V to 3.6V
Input voltage range	CSx, SCL, SDA, INTN	-0.5V to 3.6V
Output voltage range	CSx, SCL, SDA, INTN	-0.5V to 3.6V
Operating free-air temperature range		-40°C to 85°C
Maximum operating junction temperature T_{JMAX}		150°C
Storage temperature T_{STG}		-65°C to 150°C
Lead temperature (soldering 10 seconds)		260°C
ESD(Including HBM CDM)(NOTE 2)		
HBM		±8kV
CDM		±1.5kV
Latch-Up		
Test condition: according to JESD78E		+IT：350mA -IT：-350mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The HBM test method: ESDA/JEDEC JS-001-2017 ,the CDM test method: ESDA/JEDEC JS-002-2018.

RECOMMENDED OPERATING CONDITIONS

| PARAMETERS	SYMBOL	MIN	MAX	UNIT
Supply voltage	VCC	2.7	3.6	V
Pull-up voltage	VIO	1.6	3.6	V
Ambient temperature	T_A	-40	85	°C

ELECTRICAL CHARACTERISTICS

Note:Typical values are given for T_A = +25°C, VCC=2.8V unless otherwise specified.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
CHIP CURRENTS						
$I_{DEEPSLEEP}$	Deep Sleep Mode Current	LDO on, OSC off I²C listening		2.5		µA
I_{SLEEP}	Sleep Mode Current	LDO on, OSC on I²C listening		5.0		µA
I_{DOZE}	Doze Mode Current	SCANPERIOD = 400ms FREQ = 100kHz; CDCRES = 6 CHEN = b000001 Digital filter features OFF I²C listening. No load		6.5		µA
I_{ACTIVE}	Active Mode Current	SCANPERIOD = 30ms FREQ = 100kHz CDCRES = 6 CHEN = b000001 Digital filter features OFF I²C listening. No load		15.5		µA
CAPACITANCE SENSING						
C_{RANGE}	Measurement Range		±0.55	±2.2	±9.9	pF
N_{BIT}	Measurement Resolution			21		bits
C_{RES}			1			aF
F_{OSC}	Nominal OSC Frequency			4		MHz
F_{Trim}	OSC Trim Accuracy	Around Nominal Value, Ta=25°C, VCC=2.8V	-4		4	%
F_{Temp}	OSC Temp. Dependency	Around Nominal Value, Full Ta range, VCC=2.8V	-1		1	%
F_{VCC}	OSC VCC Dependency	Around Nominal Value, Ta=25°C, Full VCC range	-0.6		0.6	%
Fs	Nominal Sampling Freq	Programmable with FREQ			250	kHz

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
C_{DCEXT}	External DC Cap. to GND per Measurement Phase	One CSx as measured input			220	pF
R_{FILTIN}	Input driving Res		0		30	kΩ
R_{INT}	Compensation Res		125		1000	Ω
TEMPERATURE SENSING						
$T_{INRANGE}$	Input Range	Ambient Temperature(T_A)	-40		85	°C
$T_{OUTRANGE}$	Output Range		0		32767	LSB
I²C INTERFACE						
I_{OL} （SDA，INTN）	Output low current	$V_{OL} \leqslant 0.4V$	8			mA
V_{IH}	Input high level	SCL, SDA	0.84		3.6	V
V_{IL}	Input low level	SCL, SDA	-0.5		0.36	V
t_{DEG_SDA}	SDA deglitch time	SDA		88		ns
t_{DEG_SCL}	SCL deglitch time	SCL		77		ns

I²C INTERFACE TIMING

PARAMETER		MIN	TYP	MAX	UNIT
F_{SCL}	Interface Clock frequency			400	kHz
$T_{HD:STA}$	(Repeat-start) Start condition hold time	0.6			µs
T_{LOW}	Low level width of SCL	1.3			µs
T_{HIGH}	High level width of SCL	0.6			µs
$T_{SU:STA}$	(Repeat-start) Start condition setup time	0.6			µs
$T_{HD:DAT}$	Data hold time	0			µs
$T_{SU:DAT}$	Data setup time	0.1			µs
T_R	Rising time of SDA and SCL			0.3	µs
T_F	Falling time of SDA and SCL			0.3	µs
$T_{SU:STO}$	Stop condition setup time	0.6			µs
T_{BUF}	Time between start and stop condition	1.3			µs
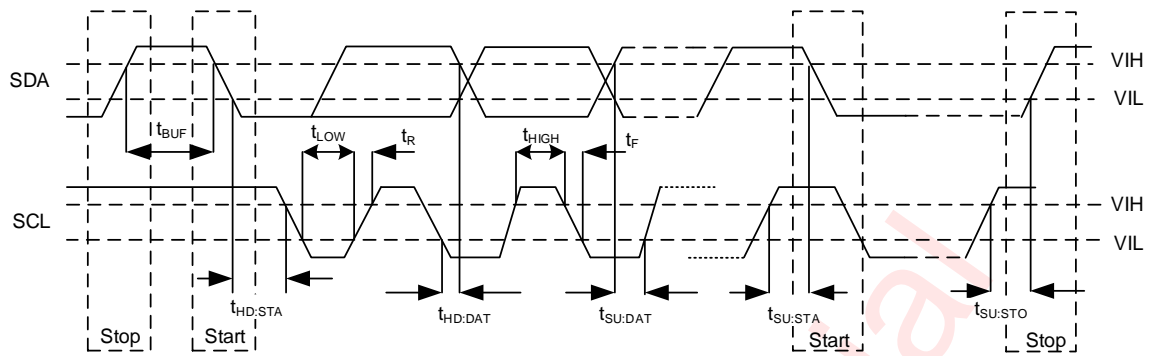
Figure 4 I²C Interface Timing

DETAILED FUNCTIONAL DESCRIPTION

OVERVIEW

AW93208CSR is a capacitive in-ear detection and touch key controller with a built-in ultra-low-power MCU. Each sensor channel can be configured as mutual capacitance detection or self-capacitance detection. AW93208CSR is composed of AFE, MCU, FLASH, RAM, OSC, I²C, etc. AFE is mainly used to drive the sensor and shield electrodes, and convert the capacitance of sensor to digital data. MCU executes the algorithm program in the FLASH, and performs basic operations such as signal filtering, baseline calculation, automatic compensation for environmental drift, radio frequency(RF) noise suppression, proximity detection, etc. It is able to accurately identify single/double/triple click, short/long press, linear slide and wheel slide, etc.

CAPACITIVE SENSOR INTRODUCTION

When a conductive object, such as a finger, comes in contact or close proximity with the sensing electrode, the capacitance of one or more sensors changes. The figure below shows the basic structure and equivalent model of a capacitive sensor. The top layer is the frontpanel, and the middle green area below is a copper sensor pad. The sensor is usually surrounded by ground, resulting in a parasitic capacitance(C_{PARA}).

There are two main operational modes in the capacitance sensing circuits: self-capacitance sensing and mutual capacitance sensing. An electric field is created around the sensor when system is working. In the self-capacitance sensing mode, with target object approaching, some of the electric field lines couple to the target object and add a small amount of finger capacitance (C_{PROX}) to the existing C_{PARA}. This feature can be used to detect proximity or touch action.

At least two electrodes are needed in the mutual capacitance sensing mode: one is a transmitter (Tx) and the other is a receiver (Rx). Tx and ground will form a capacitance (C_{PARAT}); Rx and ground will form a capacitance (C_{PARAR}); Tx and Rx will form a capacitance (C_M). When target object approaches, Tx and Rx will form a capacitance ($C_{M'}$) which is less than C_M.

Self-capacitance Sensing Mode
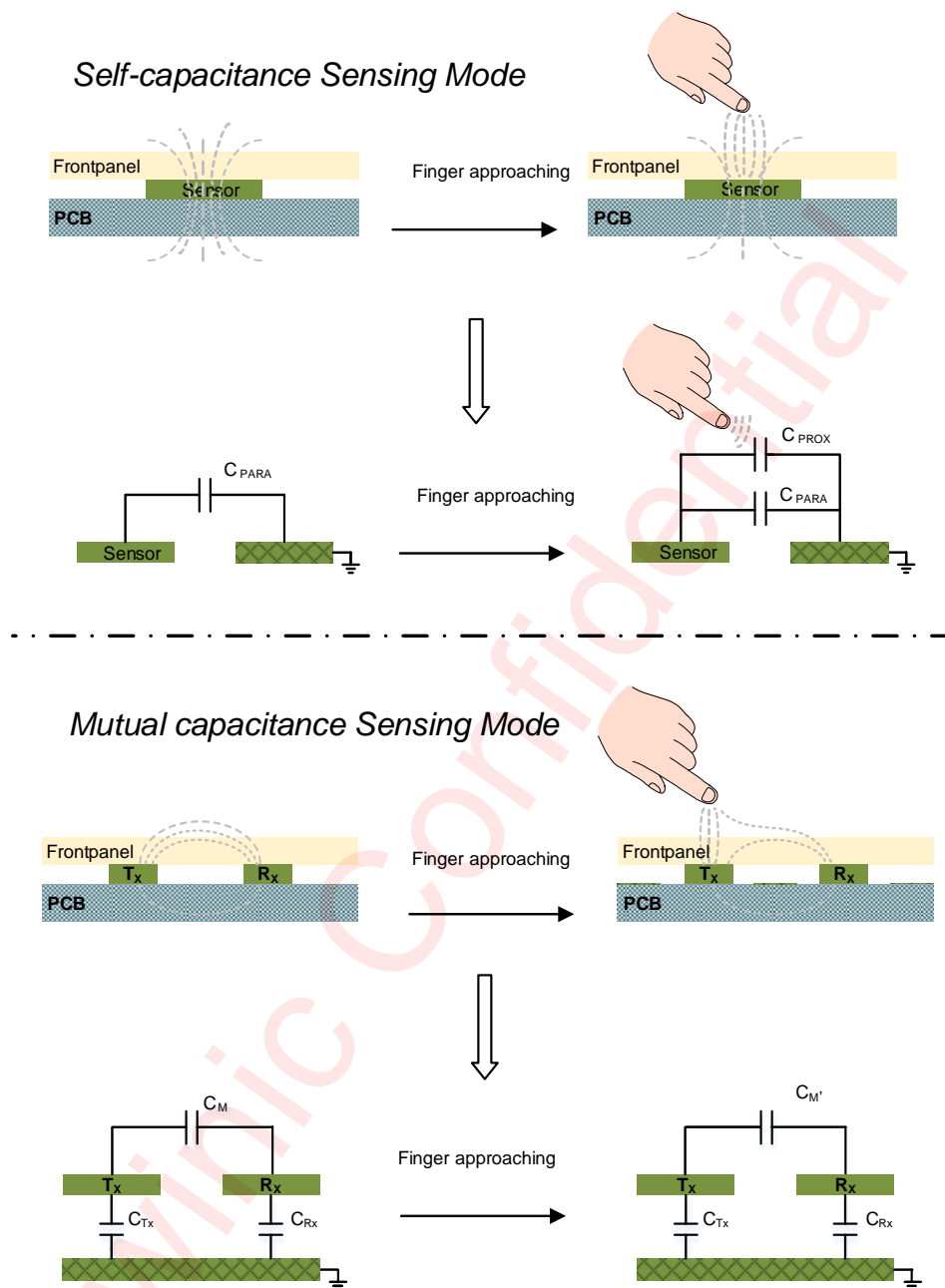
Mutual capacitance Sensing Mode

Figure 5 Capacitive sensor structure

CAPACITIVE SENSING TECHNIQUES

The proximity sensing system consists of three parts: capacitive sensor, AFE and DSP. Among them, the function of AFE is to drive the capacitive sensor and the shield electrode, and convert the sensor capacitance into digital data. The function of DSP is to process the data from AFE and transmit the sensor capacitance value (CapDiff, CapValid) together with proximity state to the host. When the target object is approaching or moving away, the proximity sensing system will transmit key information to the host after dedicated processing.
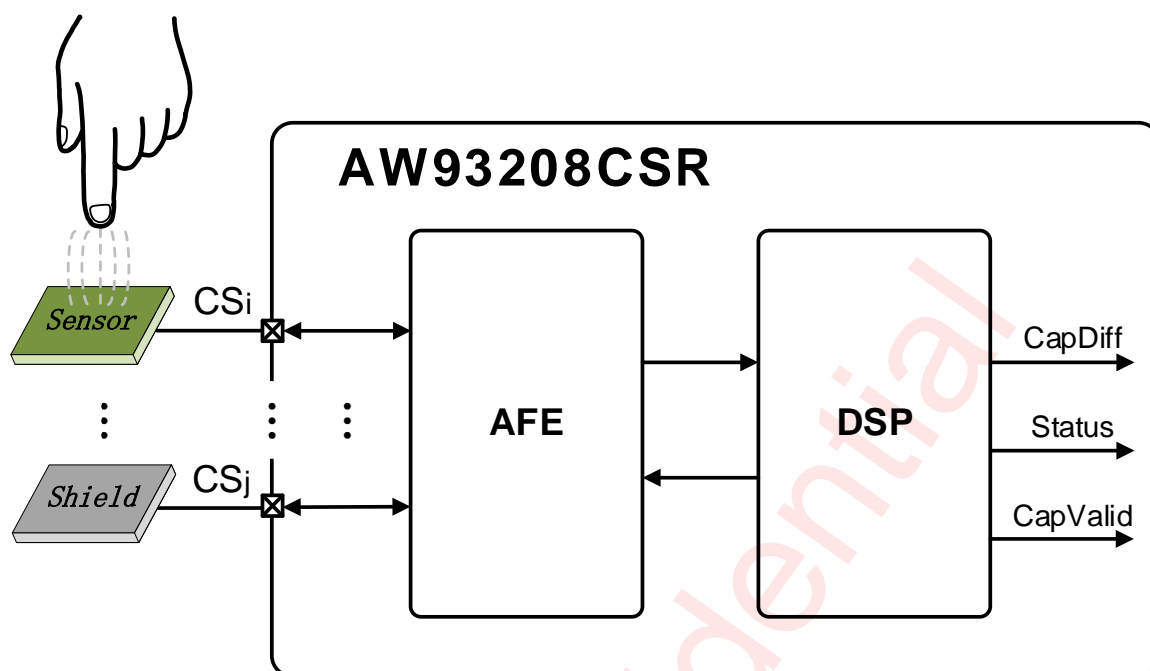
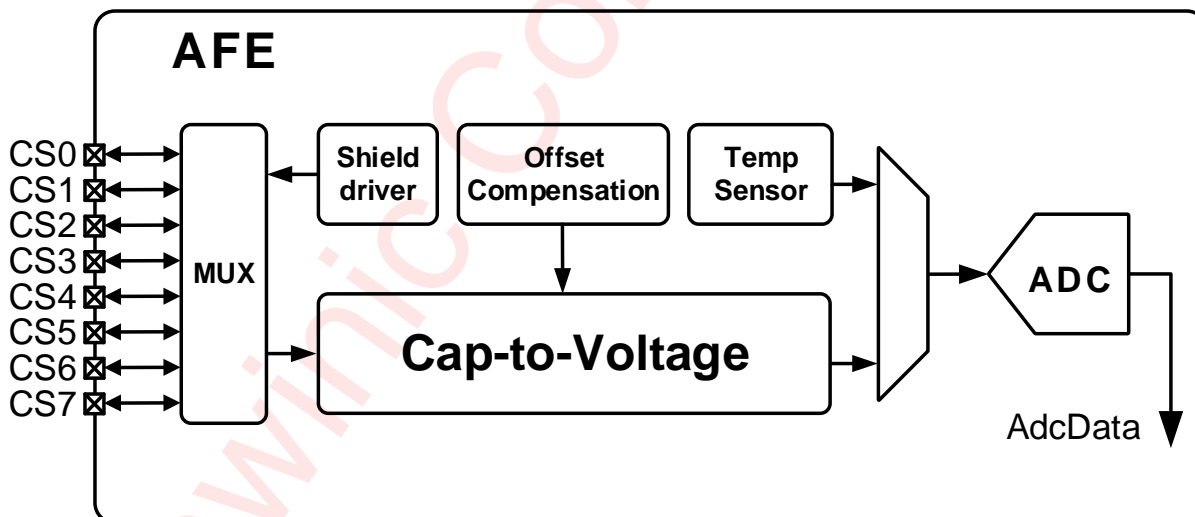**Figure 6 Proximity Sensor Operation Overview**

AFE DESCRIPTION

Figure 7 AFE Block Diagram

※ MUX selects CSx as capacitance measurement input or shield output

※ If CSx is used as shield electrode, it is excited by shield driver. The driven shield signal is a replica of the sensor signal. Shield electrode around can protect the sensor from environmental interference，and reduce the parasitic capacitance.

※ Cap-to-Voltage integrates a charge amplifier, it detects the sensor capacitance with a charge-transfer method. The capacitance is converted into a voltage signal, which is the input of ADC.

※ Offset Compensation measures parasitic capacitance(C_{PARA}), which is compensated during the process of charge transferring of Cap-to-Voltage. Thus, the input capacitance of Cap-to-Voltage is nearly C_{PROX} alone.

※ Temp Sensor measures the temperature of the chip, and the output is converted by ADC to digital data. The temperature data can be used as reference to correct the capacitance measurement result.

※ ADC converts voltage signals obtained by Cap-to-Voltage or Temp Sensor into AdcData.
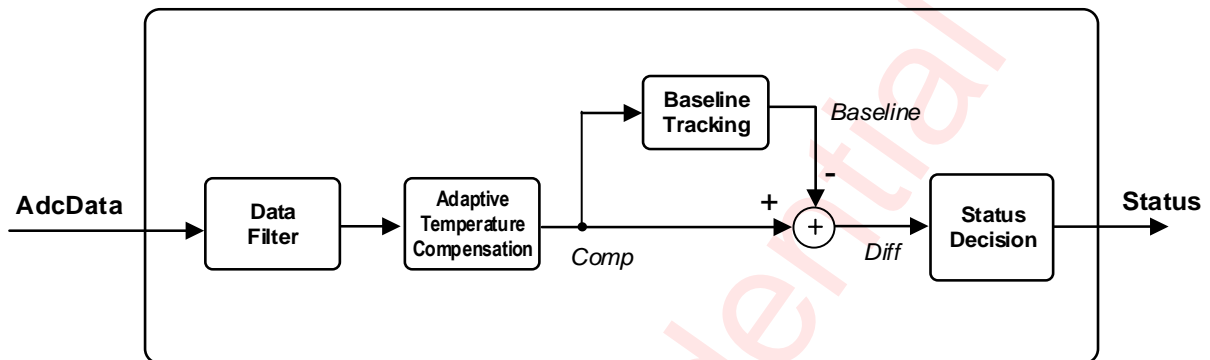
DSP DESCRIPTION

Figure 8 Digital signal processing diagram

※ DSP processes the AdcData from the AFE, and finally outputs a series of reliable proximity state.

※ Data Filter effectively filters the high-frequency noise and interference, which greatly improves the signal-to-noise ratio(SNR).

※ The adaptive temperature compensation module can automatically compensate for environmental drift in real time, especially temperature drift. Thereby it can be ensured that the final proximity state will not be misjudged due to temperature drift.

※ The role of the Baseline is to further track the slowly varying data caused by the residual temperature compensation or other gradual environmental drift.

※ Finally, the State Decision module outputs a certain and reliable proximity state based on the Diff data and the proximity threshold etc.
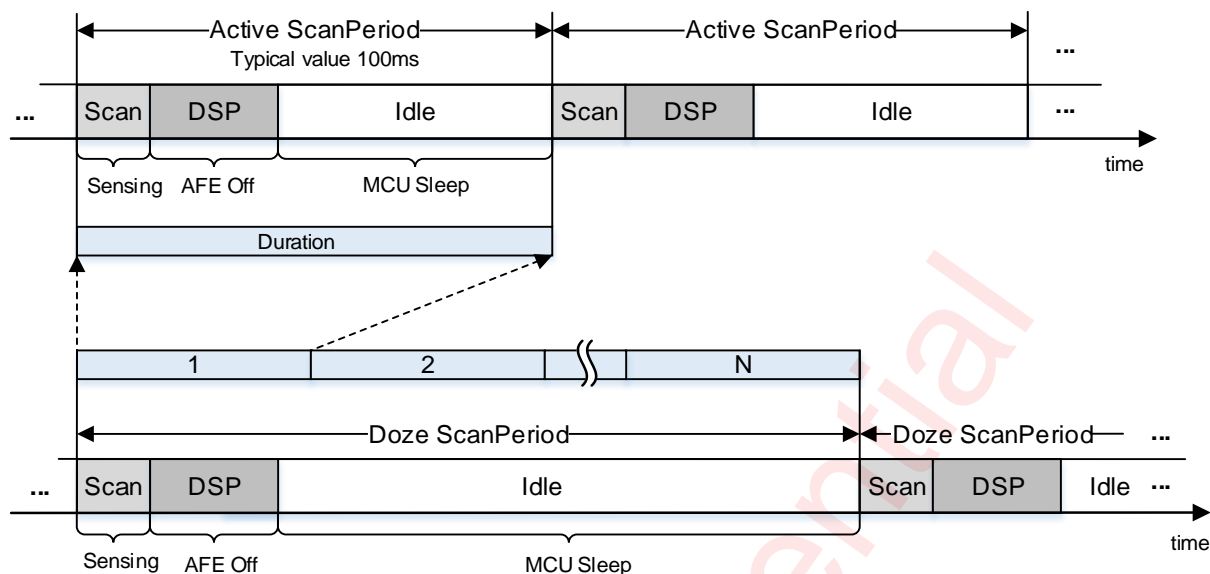
SCAN PERIOD

Figure 9 Active mode and Doze mode scan period

Each scan period can be divided into three stages. In the first stage, the selected sensor channel is scanned and AdcData is generated. In the second stage, the AFE is closed and the AdcData obtained by the DSP module is processed. In the last stage, all data processing has been completed and the chip enters idle state, in order to reduce power consumption, neither AFE nor MCU will work.

The figure above shows the composition and meaning of the active mode and doze mode scan periods. The scan period of active mode and doze mode can be configured by register SCANCTRL1(Address: 0x1A04) and AFECFG3_CHx (x=0,...,7). Generally, doze mode consumes much lower power than active mode.

CLOCK

The chip uses a built-in 4MHz OSC clock.

RESET

POWER ON RESET (POR)

Reset operation is triggered during power up. When nRST released, the initialization process starts to perform and it will last for about 20ms. INTN will be set to low when the initialization process is completed, then I²C can communicate normally.
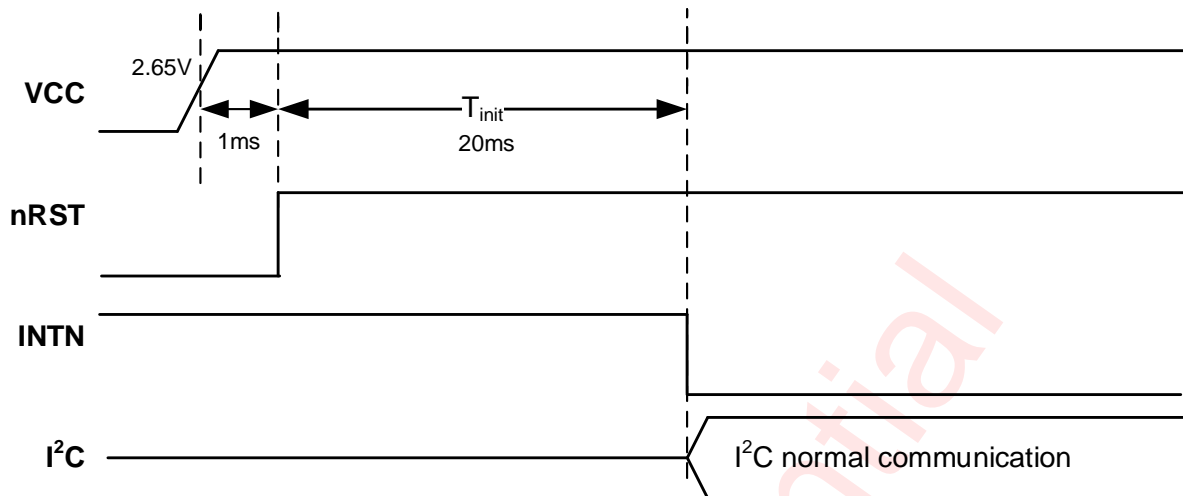
Figure 10 Power On Timing

BROWN OUT RESET (BOR)

Reset operation is triggered when VCC drop to the threshold of BOR. After the reset operation, all the registers will be reset to the default value. The chip returns to normal operation mode until the power supply rises to a normal value.

Figure 11 Brown Out Timing

SOFT RESET

The soft reset operation can be triggered by writing "0x3C" to the soft reset register (Address: 0xFF18). After the reset operation is completed, all the registers will be reset to the default value.

Figure 12 Sof2t Reset Timing

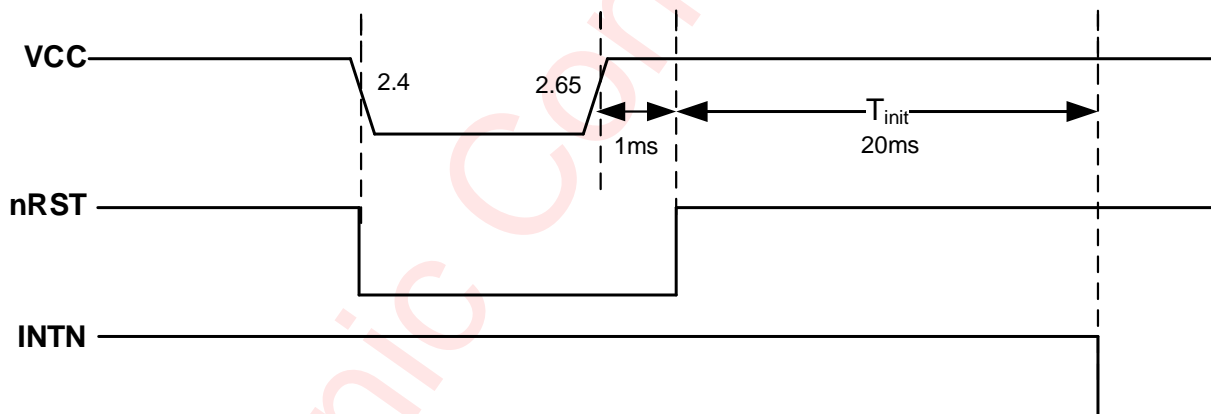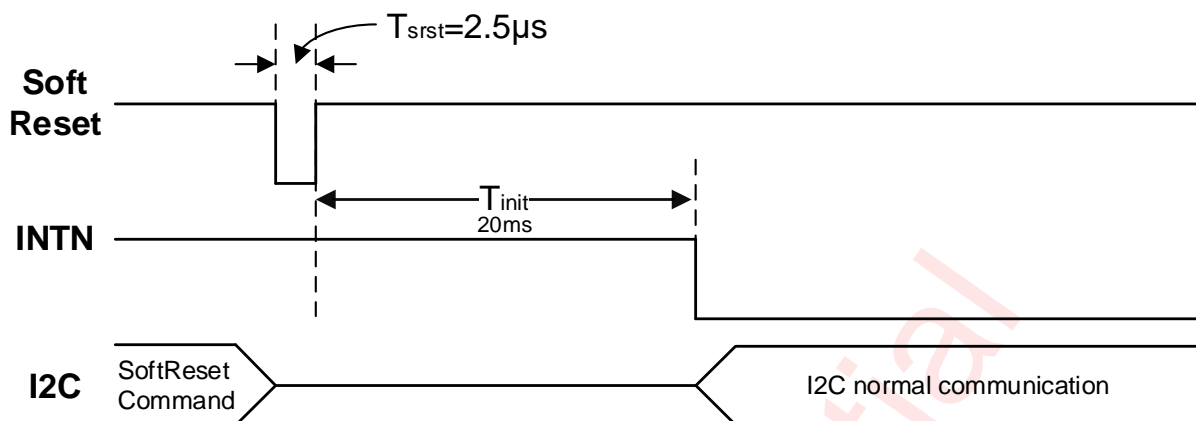## INITIALIZATION

After power on, OSC runs normally, and MCU starts to execute the initialization program in FLASH. It performs the following operations.

> ➢ Read information from NVR Flash
> ➢ Issue an interrupt after initialization and then enters into sleep mode.

OPERATION MODE

There are four operation modes in the chip: Deep Sleep, Sleep, Active and Doze.

DEEPSLEEP

The device power consumption is lowest in this mode. OSC and AFE are closed, CPU is sleeping, only I²C interface is active.

SLEEP

The device is in a low power state. OSC is on, AFE is off, and CPU is sleeping, waiting for interrupt to wake up.

ACTIVE

The device works at full speed. All modules including AFE, MCU, OSC, etc., are running normally. When no touch or proximity has been detected for some time, it will automatically switch to Doze mode. In this mode the external HOST can send SLEEP command to switch the device into sleep mode.

DOZE

Scan period is long, MCU and AFE work intermittently. During most of the period, quite a bit of modules are in idle state. So the average power consumption is lower.

Once a proximity is detected in doze mode, it will automatically return to active mode. The external HOST can also send SLEEP command to switch the device to sleep mode.
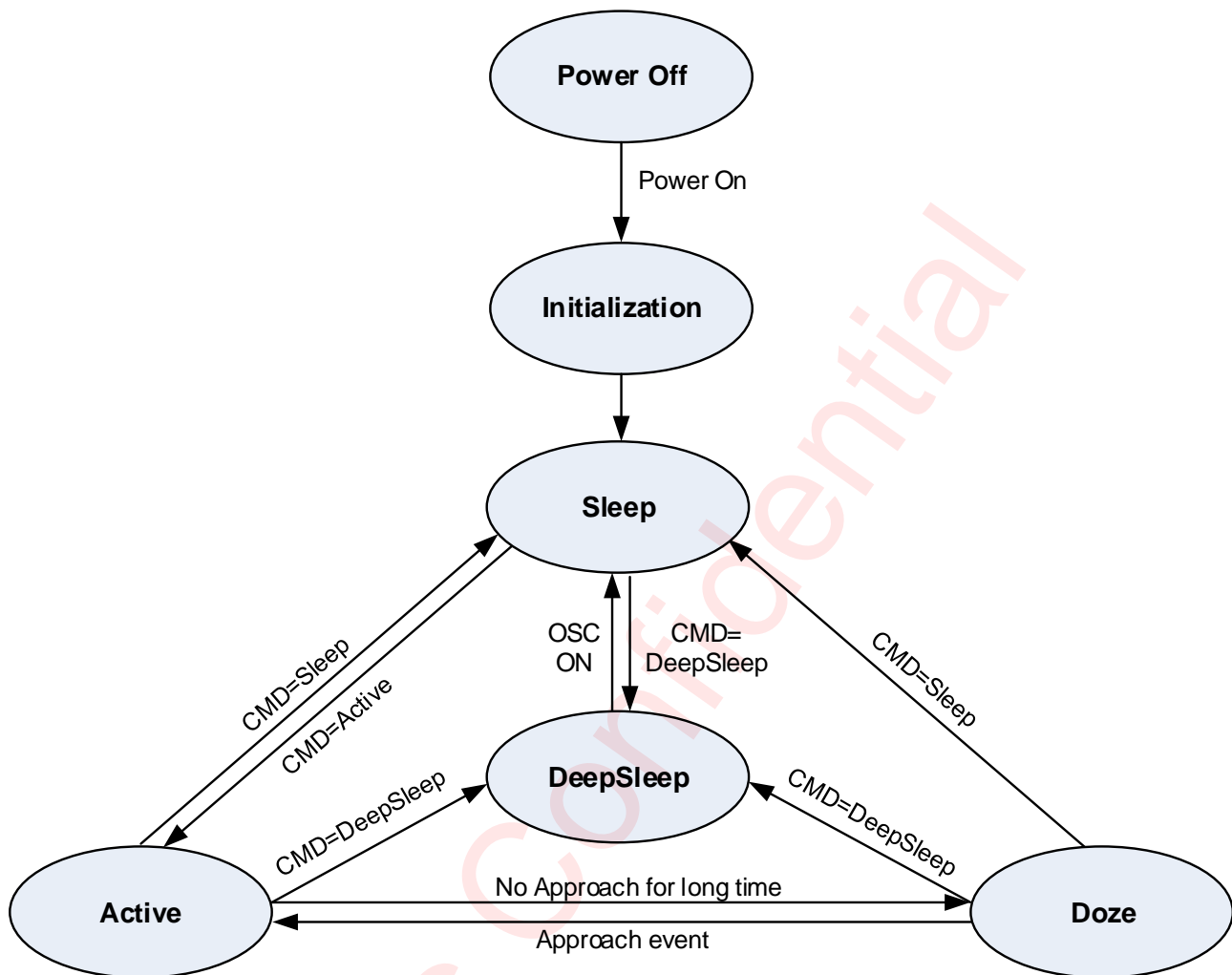
Figure 13 Operation Mode Switching

INTERRUPT

The chip reports the interrupt signal to the host through the INTN pin. Register IRQSRC (Address: 0x4410) stores interrupt information, including the gestures, completion of parasitic capacitance calibration, scan cycle completion, and so on. Register IRQSRC is cleared after host read. The specified interrupt signal can be shielded by configuring IRQEN (Address: 0x4414).

I²C INTERFACE

AW93208CSR supports the I²C serial bus and data transmission protocol in fast mode at 400kHz. It operates as a slave on the I²C bus. Connections to the bus are made via the open-drain I/O pins SCL and SDA. The pull-up resistor can be selected in the range of 1k~10kΩ and the typical value is 4.7kΩ. AW93208CSR can support different high level of the I²C interface. Additionally, the I²C device supports continuous read and write operations. The I²C register address is 16-bit and register data is 32-bit, and the data transmission is in big-endian mode.

DEVICE ADDRESS

The I^{2}C device address (7-bit, followed by the R/W bit(Read=1/Write=0)) of AW93208CSR is 0x12, and can not be changed.

I^{2}C START/STOP

I^{2}C start: SDA changes from high level to low level when SCL is high level.

I^{2}C stop: SDA changes from low level to high level when SCL is high level.

S : START condition
Sr: START Repeated condition
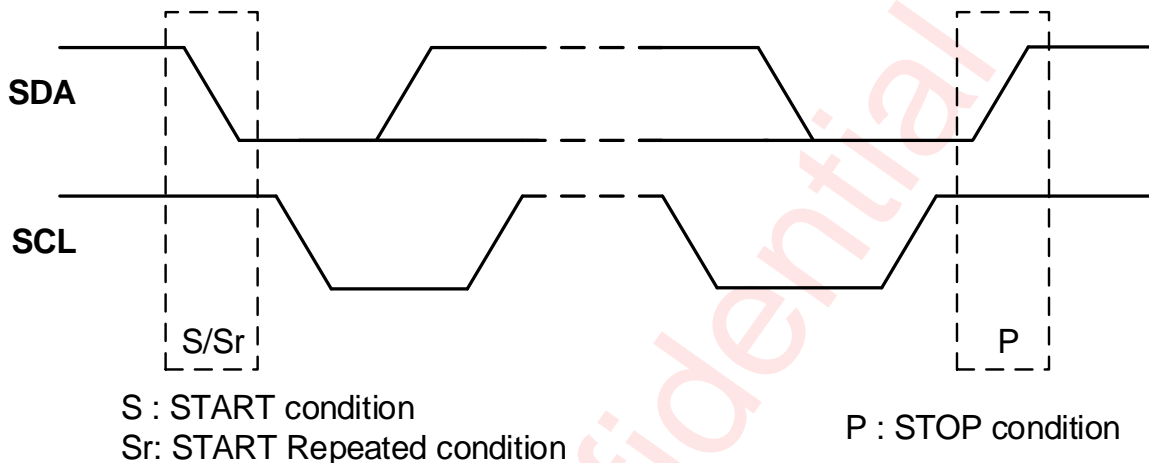
P : STOP condition

Figure 14 I^{2}C Start/Stop Condition Timing

DATA VALIDATION

When SCL is high level, SDA level must be constant. SDA can be changed only when SCL is low level.

Data Line Satble
Data Valid

Change
of Data
Allowed
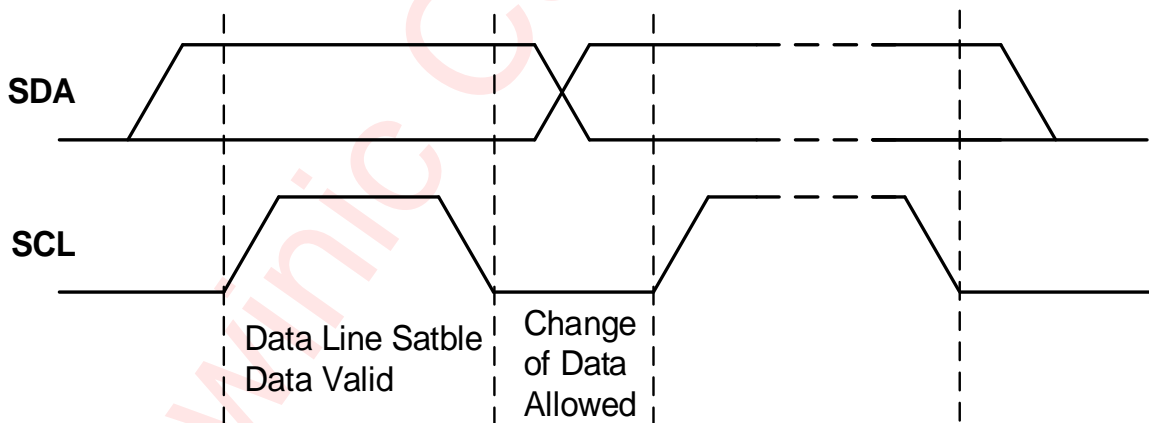
Figure 15 Data Validation Diagram

ACK (ACKNOWLEDGEMENT)

ACK means the successful transfer of I^{2}C bus data. After master sends an 8-bit data, SDA must be released; SDA is pulled down to GND by slave device when slave acknowledges.

When master reads, slave device sends 8-bit data, releases the SDA and waits for ACK from master. If ACK is sent and I^{2}C stop is not sent by master, slave device sends the next data. If ACK is not sent by master, slave device stops to send data and waits for I^{2}C stop.

Figure 16 I²C ACK Timing

WRITE CYCLE

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol allows a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a start condition, a number of byte transfers (set by the software) and a stop condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow.

I²C Register address is 16-bit and register data is 32-bit. Note that I²C also support 8-bit data transfer. Writing process of I²C is showed as below picture.

Write

| S | SA[6:0] | 0 | A | RA[15:8] | A | RA[7:0] | A | WD0[31:24] | A | WD0[23:16] | A | WD0[15:8] | A | WD0[7:0] | A | WD1[31:24] | ······ | WDn[7:0] | A | P |

S	Start	A	Acknowledge
Sr	Repeat Start	N	Not Acknowledge
P	Stop		
SA	7bit Slave address	RA	16bit Register address
WDn	32bit Write Data	RDn	32bit Read Data

Figure 17 I²C Write Byte Cycle

READ CYCLE

I²C supports read operation data format with repeated start conditions, so there are two formats of I²C read operations. Read process of I²C is showed as below picture.

Read Format 1

| S | SA[6:0] | 0 | A | RA[15:8] | A | RA[7:0] | A | Sr | SA[6:0] | 1 | A | RD0[31:24] | A | RD0[23:16] | A | RD0[15:8] | A | RD0[7:0] | A | RD1[31:24] | ⋯⋯ | RDn[7:0] | N | P |

Read Format 2

| S | SA[6:0] | 0 | A | RA[15:8] | A | RA[7:0] | A | P | S | SA[6:0] | 1 | A | RD0[31:24] | A | RD0[23:16] | A | RD0[15:8] | A | RD0[7:0] | A | RD1[31:24] | ⋯⋯ | RDn[7:0] | N | P |

From master

From slave

S	Start	A	Acknowledge
Sr	Repeat Start	N	Not Acknowledge
P	Stop		
SA	7bit Slave address	RA	16bit Register address
WDn	32bit Write Data	RDn	32bit Read Data

Figure 18 I²C Read Byte Cycle

GESTURES

AW93208CSR can implement several gestures on the button and slider, including **single-click**, **double-click triple-click**, **triple-click**, **short-press**, **long-press** and **slide**.

Single-click

Single-click refers to a quick tap event, when a touch is triggered and then released in the same location within a short period of time. *clickth* is defined as the maximum touch time of a valid **single-click**. After the time of configurable *intervalth* , a **single-click** will be reported. **Single-click** event is based on the following conditions:

> 1st condition: The time of the touch state must be less than the *clickth*.

> 2nd condition: The time between two touch states must be more than the *intervalth.*

The clickth and intervalth threshold can be adjusted according to practical application requirements. After touch is released, the interrupt is triggered when the time reaches *intervalth*.
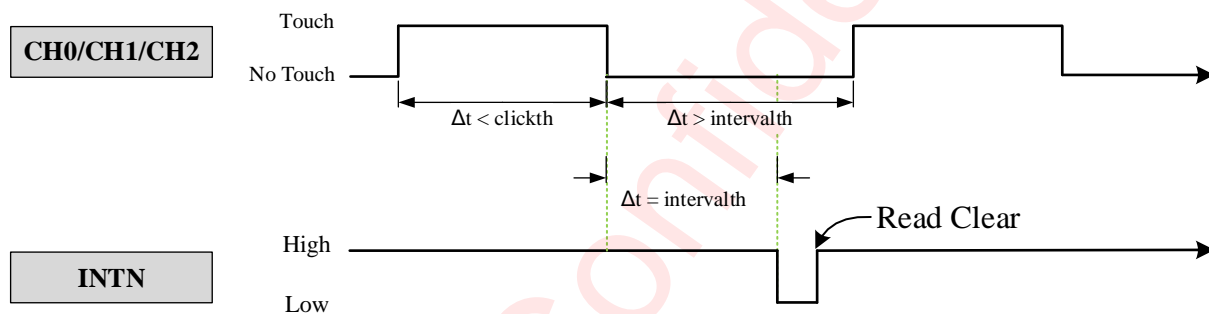
Figure 19 Single-click sequence diagram

Double-click and Triple-click

The definition of **double-click** and **triple-click** are different in the number of taps.
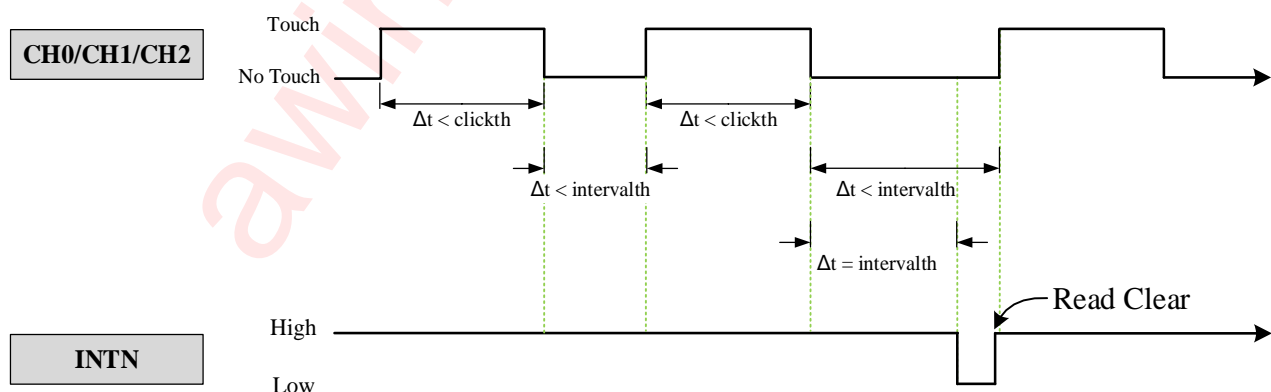
Figure 20 Double-click sequence diagram

Short-press

Short-press refers to a short time touch event. **Short-press** gesture is based on the following condition: The time during the touch state must be less than the *longpressth* and more than *shortpressth*.

Short-press will generate two interrupt messages. The first interrupt is reported when the touch time reaches the *shortpressth*. The second interrupt is reported when the touch state is released.
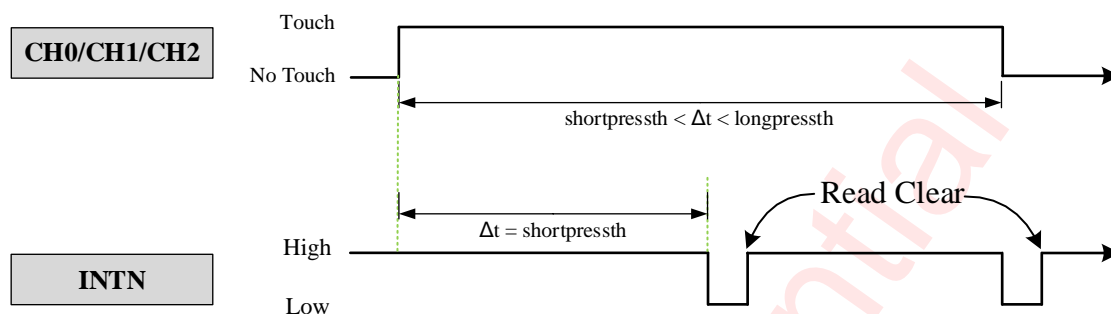

Figure 21 Short-press sequence diagram

Long-press

Long-press refers to a long time touch event. **Long-press** is based on the following condition: The time during the touch state must be more than the *longpressth*.

Long-press will generate two interrupt messages. The first interrupt is reported when the touch time reaches the *shortpressth*. The second interrupt is reported when the touch time reachs the *longpressth* threshold.
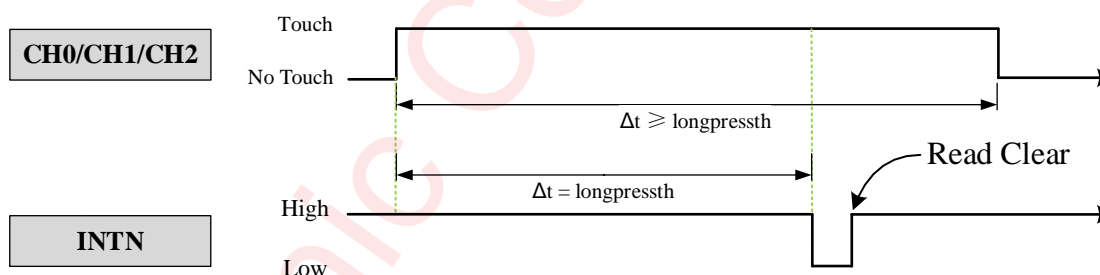

Figure 22 Long-press sequence diagram

Slide

Slide is based on the following condition: The coordinate change during the touch state must be more than the *slideth*.

A click(or press) is more difficultly recognized as a **slide** with a higher *slideth*. A **slide** is more difficultly recognized as a click(or press) with a lower *slideth*.
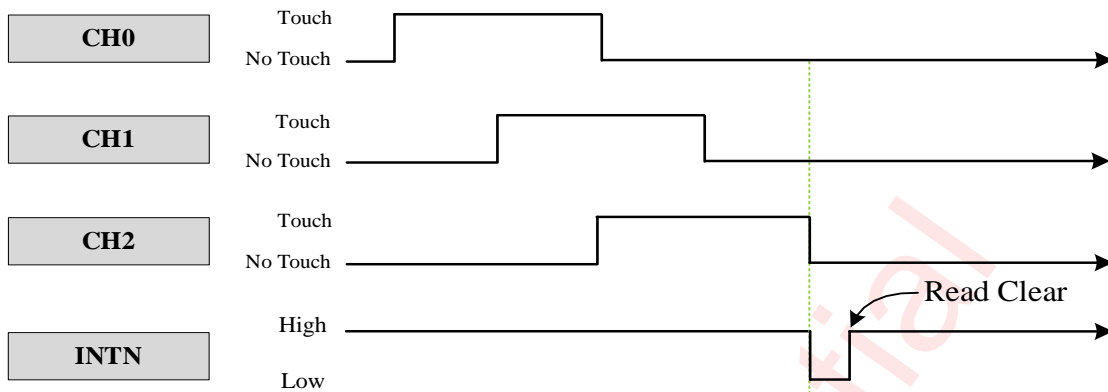
Figure 23 Slide sequence diagram

Single sliding definition: The finger touches the slide bar, slide for distance on the slide bar, and the sliding event is reported after the finger leaves. There are two slide speed levels: fast sliding and slow sliding.
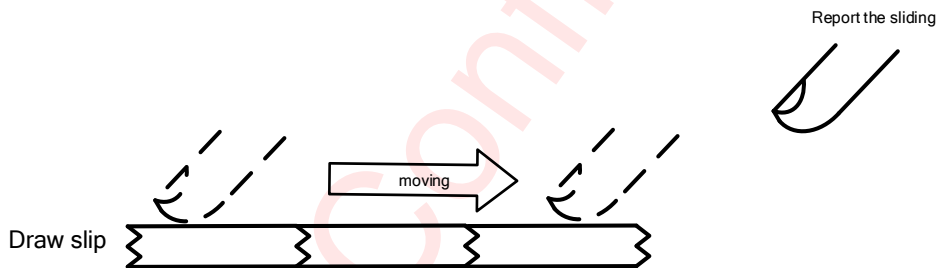

Figure 24 Single sliding diagram
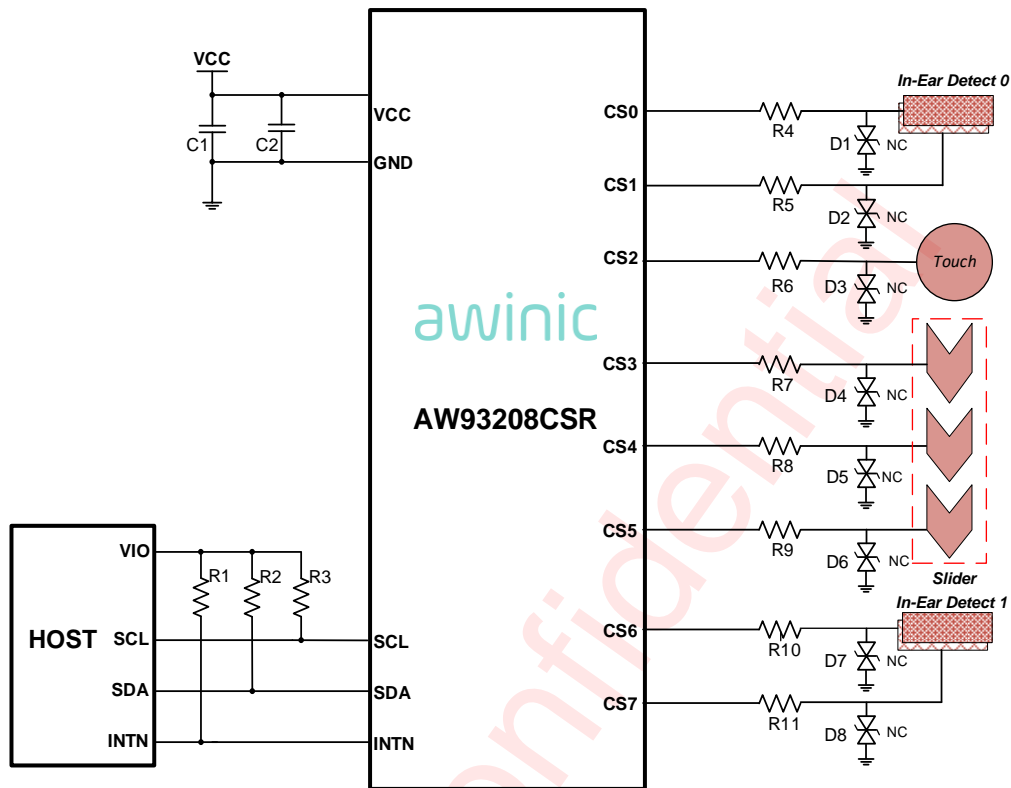
APPLICATION INFORMATION

Figure 25 AW93208CSR Typical Application Circuit (touch, in-ear and slide)
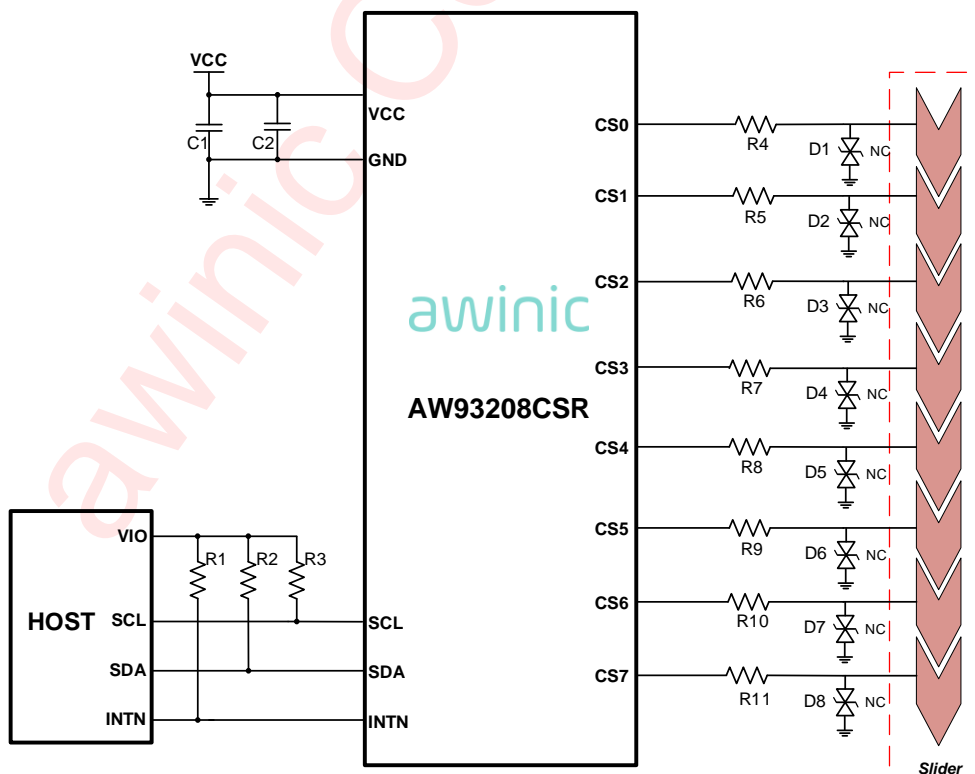

Figure 26 AW93208CSR Typical Application Circuit (slide)

Capacitors Selection

The recommended value of the capacitance C1 is 1μF and C2 is 0.1μF.

Resistor Selection

The recommended values of the resistor R1~R3 , which were applied in SCL,SDA and INTN pins, are 4.7kΩ.
The recommended values of the resistor R4~R11, which were applied in CS0~7 pin, are 390Ω.
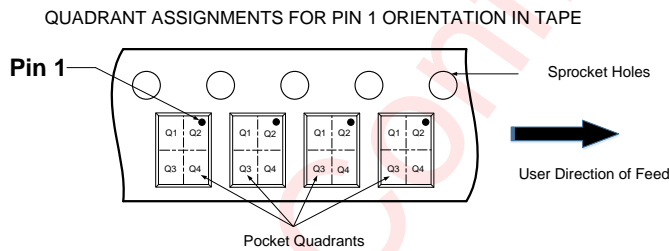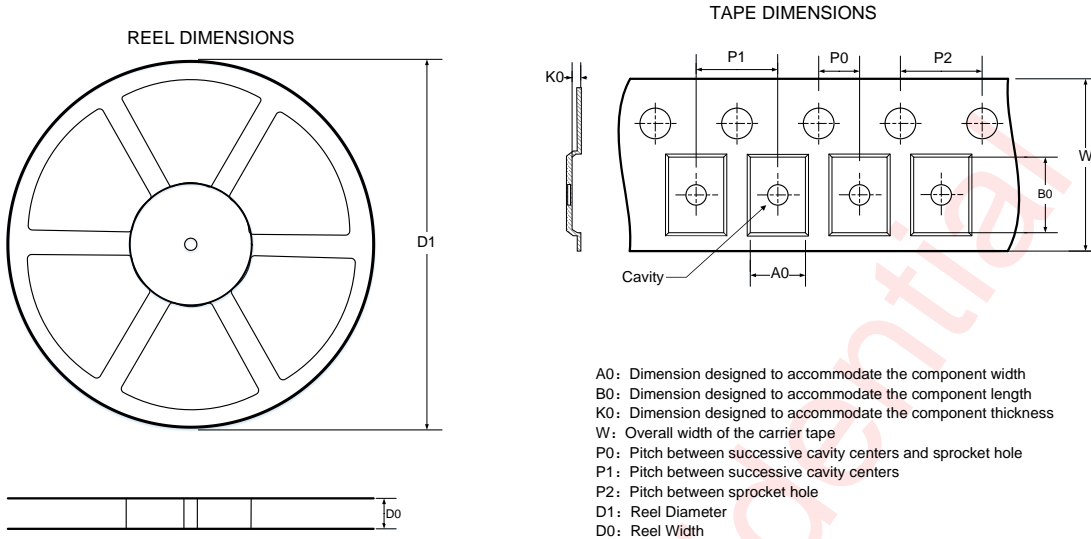
RECOMMENDED COMPONENTS LIST

Component	Name	Description	TYP.	Unit
C	C1	-	1	μF
	C2	-	0.1	μF
R	R1,R2,R3	5% resolution	4.7	kΩ
	R4~R10	5% resolution	390	Ω

PCB LAYOUT CONSIDERATION

AW93208CSR is a 8-channel capacitive in-ear detection and touch key controller, to obtain the optimal performance, PCB layout should be considered carefully. Here are some guidelines:

1. All peripheral components should be placed as close to the chip as possible. C1 and C2 should be close to VCC. Avoid connecting peripheral devices and chip pins with two different layers of copper, use the same layer of copper instead.

2. Place the chip close to capacitive sensor and make trace as short as possible.

3. Make sure the sensor and traces be away from mic, earphone line in case of disturbing audio line.

4. Place reference channel along with sensor channel to get better performance.

5. Use low noise power supply for SAR sensor.

Tape And Reel Information

REEL DIMENSIONS

TAPE DIMENSIONS

A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

Pin 1

Sprocket Holes

User Direction of Feed

Pocket Quadrants

DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
179.00	9.00	1.31	1.87	0.71	2.00	4.00	4.00	8.00	Q2

All dimensions are nominal

PACKAGE DESCRIPTION

PIN 1 CORNER

1.750 ±0.025

1.190 ±0.025

Top View

0.608 MAX

0.410±0.018

0.160±0.020

BALL TYP

Side View

15X(∅0.210±0.020)

0.245REF

0.700 TYP

0.350 TYP

0.350 TYP

1.400 TYP

0.175 REF

SYMM ₵

SYMM ₵

Bottom View
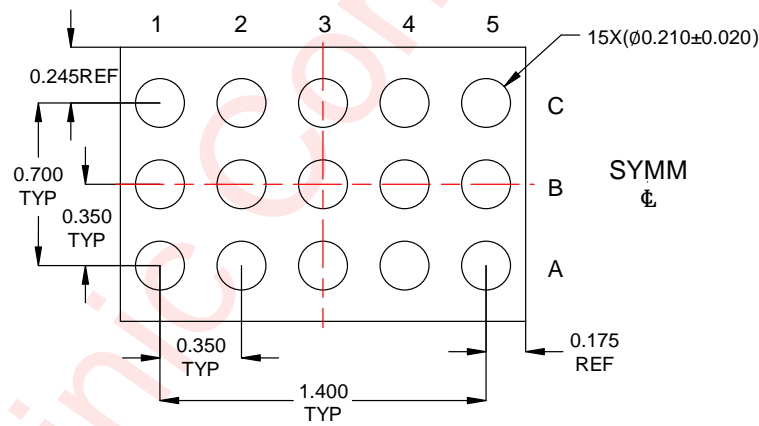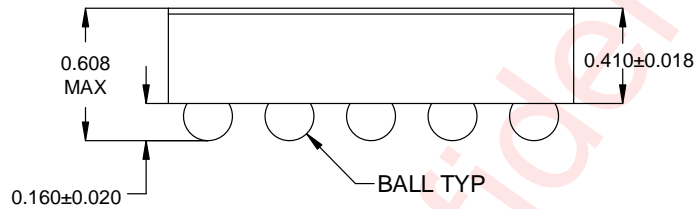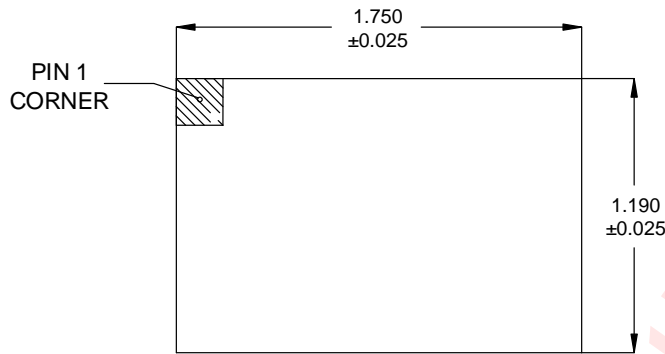
Unit:mm

LAND PATTERN DATA

```
        1     2     3     4     5
                                        15XØ0.180
      ◯    ◯    ◯    ◯    ◯    A

      ◯    ◯    ◯    ◯    ◯    B      SYMM
                                             ₵
  0.350
   TYP
      ◯    ◯    ◯    ◯    ◯    C

        0.350
         TYP
                SYMM
                  ₵
```

```
  0.05 MAX                              0.05 MIN
  All AROUND        SOLDER MASK         All AROUND         SOLDER MASK
                    OPENING                                OPENING

                                                           METAL UNDER
                    METAL                                  SOLDER MASK

  NON-SOLDER MASK DEFINED               SOLDER MASK DEFINED
```
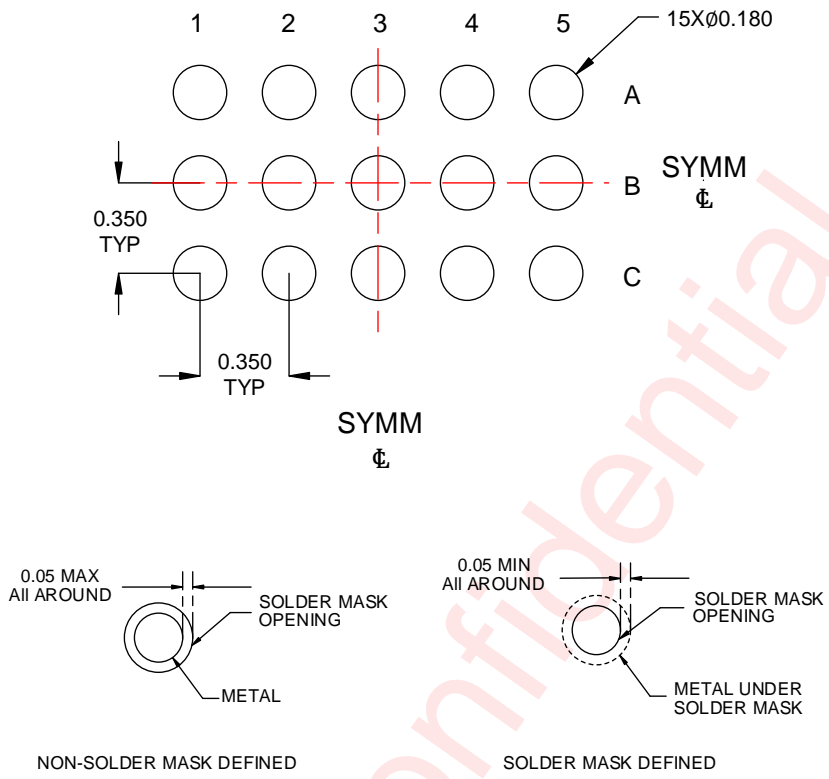
Unit: mm

Revision History

Version	Date	Change Record
V1.0	Jun.2021	Officially released.

DISCLAIMER

All trademarks are the property of their respective owners. Information in this document is believed to be accurate and reliable. However, Shanghai AWINIC Technology Co., Ltd (AWINIC Technology) does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

AWINIC Technology reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. Customers shall obtain the latest relevant information before placing orders and shall verify that such information is current and complete. This document supersedes and replaces all information supplied prior to the publication hereof.

AWINIC Technology products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an AWINIC Technology product can reasonably be expected to result in personal injury, death or severe property or environmental damage. AWINIC Technology accepts no liability for inclusion and/or use of AWINIC Technology products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications that are described herein for any of these products are for illustrative purposes only. AWINIC Technology makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

All products are sold subject to the general terms and conditions of commercial sale supplied at the time of order acknowledgement.

Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Reproduction of AWINIC information in AWINIC data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. AWINIC is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of AWINIC components or services with statements different from or beyond the parameters stated by AWINIC for that component or service voids all express and any implied warranties for the associated AWINIC component or service and is an unfair and deceptive business practice. AWINIC is not responsible or liable for any such statements.

单击下面可查看定价，库存，交付和生命周期等信息

>>AWINIC(艾为)