0.1-4.2GHz SPDT Switch for 3G/4G/5G TX

Features

- Broadband frequency range: 0.1 to 4.2 GHz
- Low insertion loss: 0.4dB typical @ 2.7 GHz
- High isolation: >23dB @ 2.7 GHz
- Integrated logic
- DFN 1.1mm X0.7mm X0.55mm-6L package

Applications

Cellular 3G/4G/5G N77/N78 TX

Cellular modems , tablets and USB Devices

Other RF front-end modules

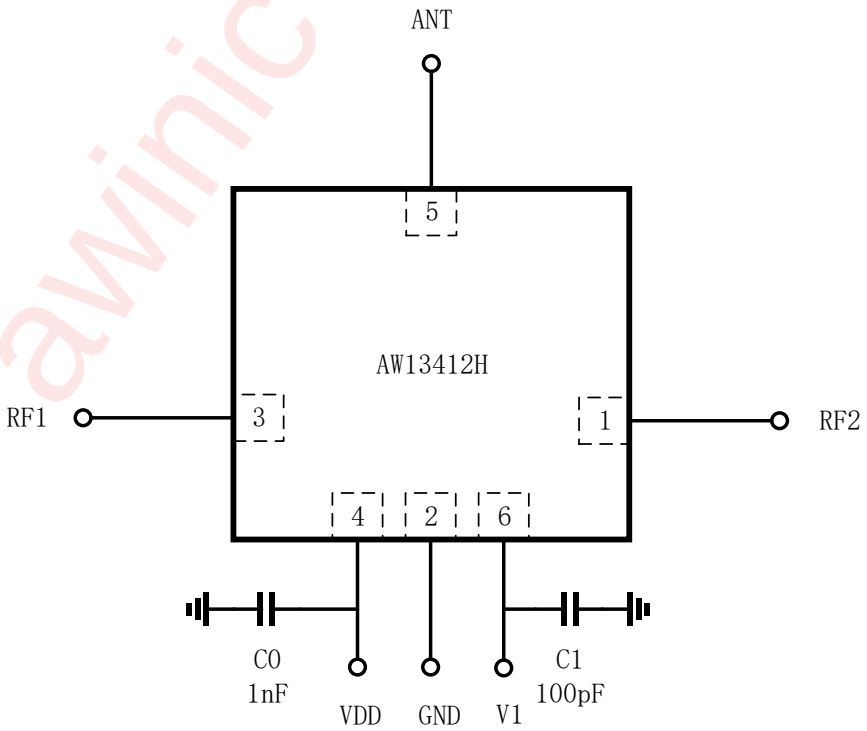
General Description

The AW13412H is a SPDT switch with low insertion loss and high Isolation. It can be used to support band switching and mode switching for cellular 3G/4G/5G, data cards and tablets.

The symmetrical design of internal ports makes it convenient for PCB routing and adjustment of receiving and transmitting signals. The band/mode switching is realized by the GPIO pins as referenced in the chip block diagram and the control logic.

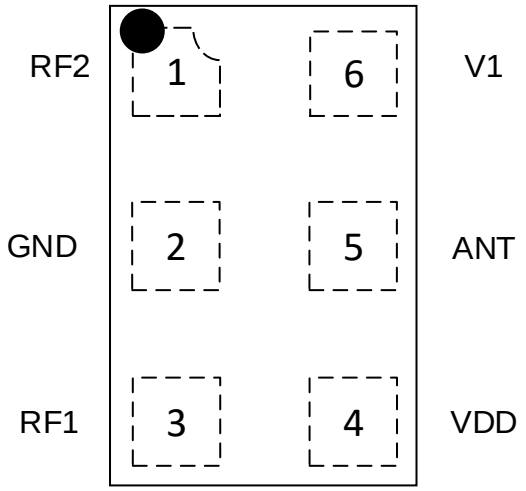
The AW13412H is provided in a compact DFN 1.1mm x 0.7mm x 0.55mm-6L package.

Typical Application Circuit

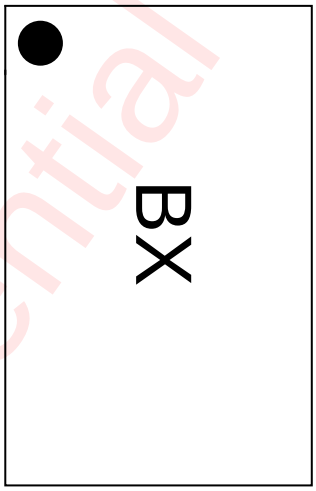


Pin Configuration And Top Mark

AW13412H
(TOP VIEW)



AW13412H Marking
(TOP VIEW)

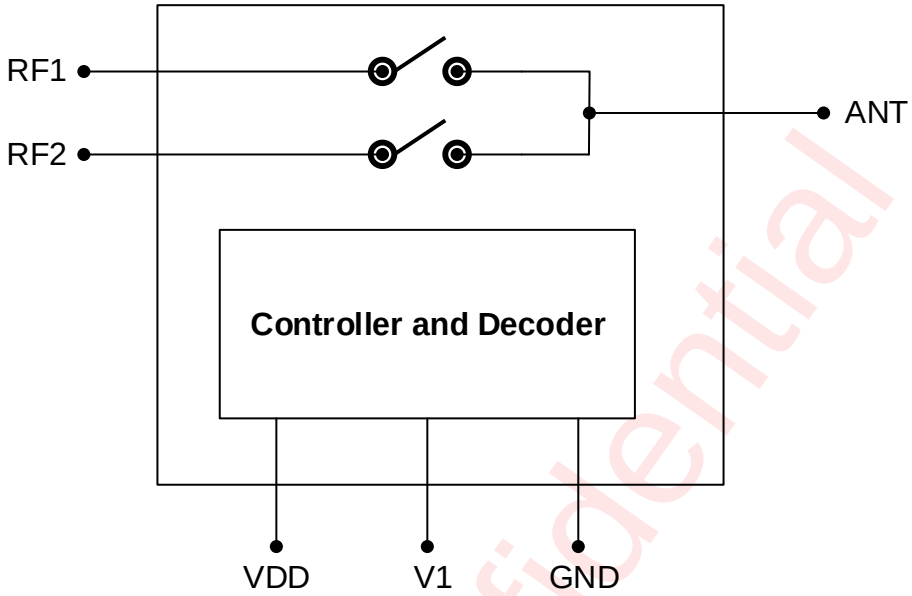


B – AW13412HDNR
X-Production Tracing Code

pin Definition

No.	NAME	DESCRIPTION
1	RF2	RF I/O path 2
2	GND	Ground
3	RF1	RF I/O path 1
4	VDD	DC power supply
5	ANT	Antenna port
6	V1	DC control voltage 1

Functional Block Diagram



Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW13412HDNR	-40℃～85℃	DFN 1.1mmX0.7mm X0.55mm-6L	B	MSL1	ROHS+HF	3000 units/ Tape and Reel

Absolute Maximum Ratings(NOTE1)

PARAMETERS		RANGE
Supply Voltage Range VDD		-0.3V to 3.6V
Control Voltage Range	V1	-0.3V to 3.6V
RF input power(RF1/RF2)		35dBm
Operating Free-air Temperature Range		-40°C to 85°C
Storage Temperature T_{STG}		-65°C to 150°C
Lead Temperature (Soldering 10 Seconds)		260°C
ESD (NOTE 2)		
HBM		±1000V
CDM		±500V

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2017. CDM test method ESDA/JEDEC JS -002-2018.

Electrical Characteristics

VDD=2.8V, V1=0/1.8V, PIN=0dBm, Temp=+25℃, Z_0=50Ω. (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
DC Specifications						
VDD	Supply Voltage		2.5	2.8	3.3	V
IDD	Supply Current			26	50	μA
VCTL_H VCTL_L	Control Voltage High Low		1 0		VDD 0.3	V
T_{PUP}	Power Up Setting Time	50% of VDD voltage to 90% of final RF power, switching between RF1/2			10	μs
T_{SW}	Switching On/Off Time	50% of final control voltage to 10%/90% of final RF power, switching between RF1/2		0.7	1.2	μs
RF Specifications						
IL	Insertion loss(ANT pin to RF1/RF2)	0.1-1.0G 1.0-2.0G 2.0-2.7G 2.7-4.2G		0.3 0.34 0.36 0.53	0.4 0.45 0.50 0.67	dB dB dB dB
ISO	Isolation (ANT pin to RF1/RF2)	0.1-1.0G 1.0-2.0G 2.0-2.7G 2.7-4.2G	33 26 23 18	37 29 27 23		dB dB dB dB
RL	Input return loss (ANT pin to RF1/RF2)	0.1-1.0G 1.0-2.0G 2.0-2.7G 2.7-4.2G	22 20 18 12	30 28 23 15		dB dB dB dB
2fo	Second harmonics (ANT pin to RF1/RF2)	PIN=+26dBm, 900MHz		88		dBc
3fo	Third harmonics (ANT pin to RF1/RF2)	PIN=+26dBm, 900MHz		83		dBc
$P_{0.1dB}$	0.1dB Compression Point (ANT pin to RF1/RF2)	0.1-4.2GHz		35		dBm

Detailed Functional Description

It is very important that the user adheres to the correct power-on/off sequence in order to avoid damaging the device. The control signal V1 should be set to 0V unless VDD is set in the operating voltage range.

Power ON:

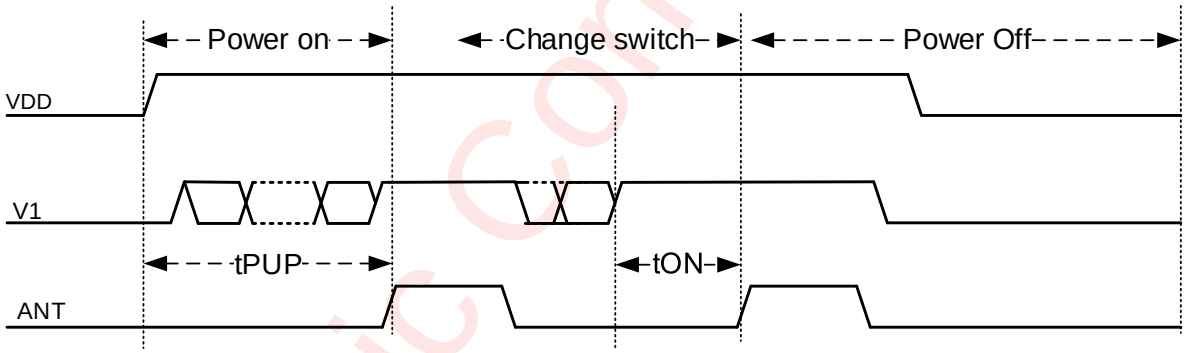
1) Apply voltage supply --- VDD
2) Set Controls---V1
3) Apply RF input

Change switch position from one RF port to another:

1) Remove RF input
2) Change control voltages V1 to set the switch to desired RF port
3) Apply RF input

Power OFF:

1) Remove RF input
2) Remove control voltages-V1
3) Remove VDD input



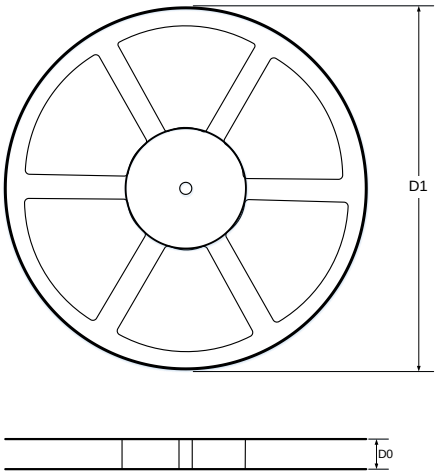
Power on/Change switch/Power off sequence

Control Logic

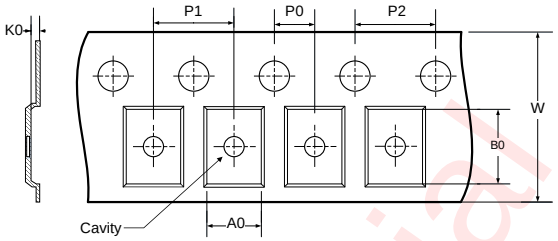
Control Pins	Switch RF I/O	
V1	RF1	RF2
0	ON	Isolation
1	Isolation	ON

Tape And Reel Information

REEL DIMENSIONS

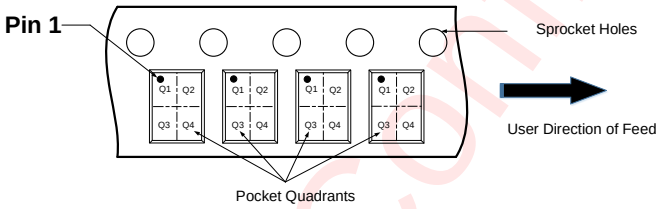


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



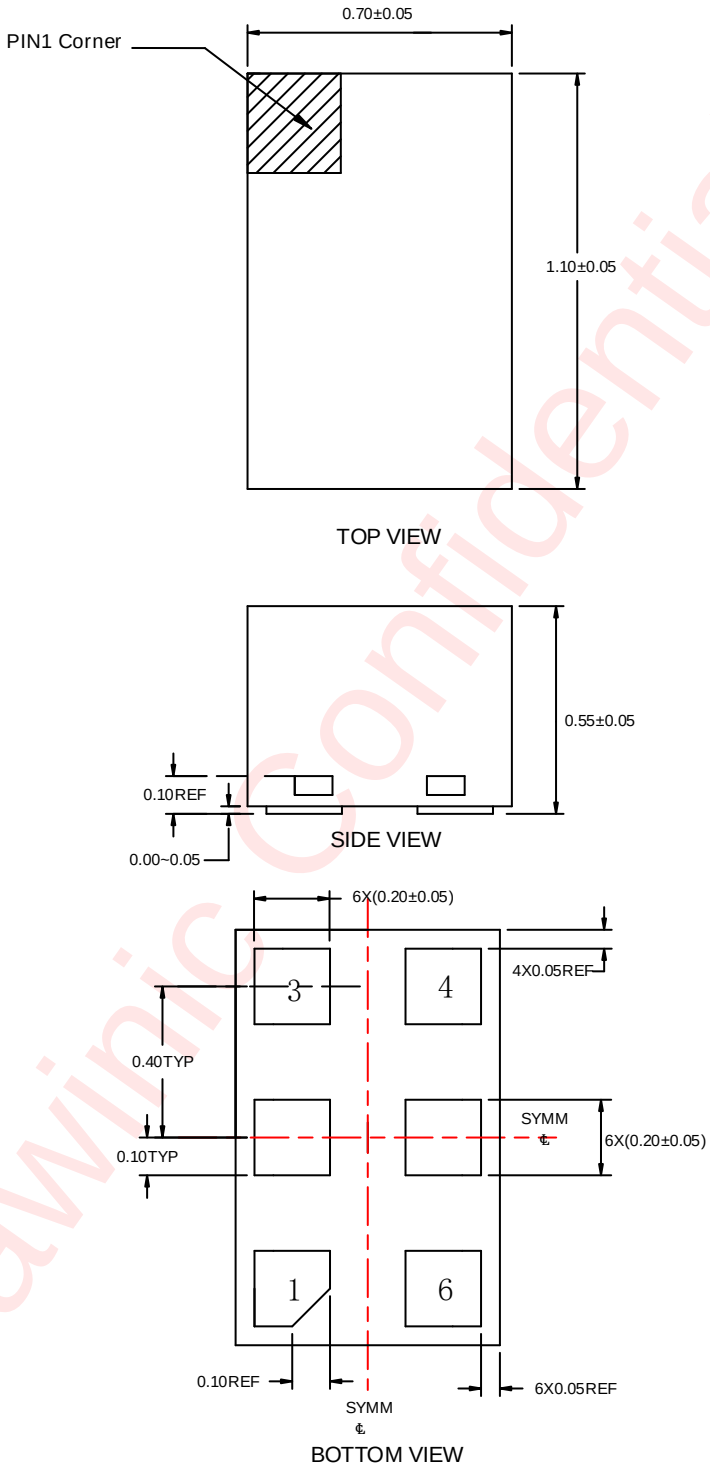
Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.4	0.82	1.22	0.66	2	2	4	8	Q1

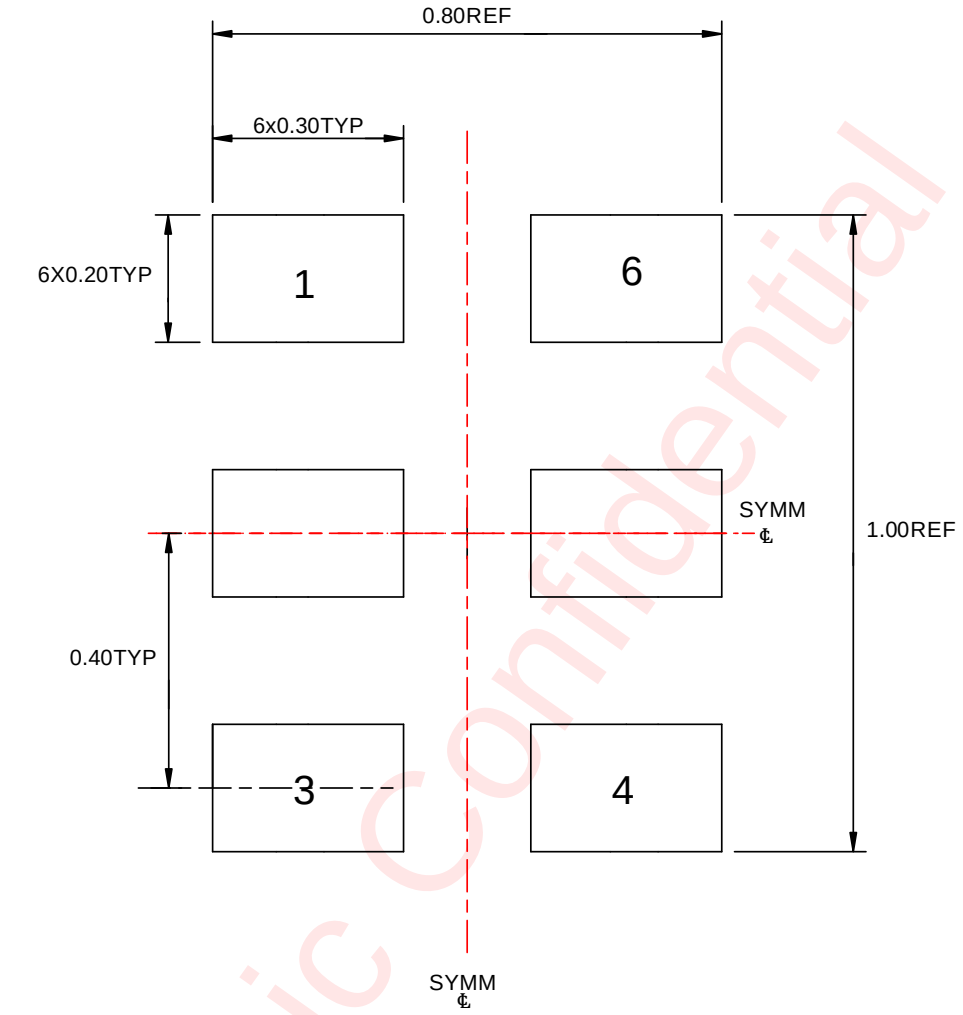
All dimensions are nominal

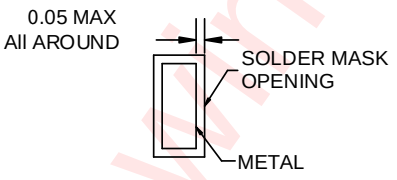
Package Description



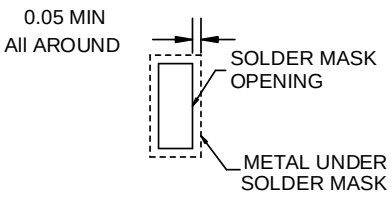
Unit: mm

Land Pattern Data





NON SOLDER MASK DEFINED



SOLDER MASK DEFINED

Unit: mm

Revision History

Version	Date	Change Record
V1.0	Oct. 2021	Officially released
V1.1	Aug. 2022	Update ordering information and AMR

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