

Ultra-Low Noise Amplifier for Global Navigation Satellite Systems (GNSS)

FEATURES

- Reduce RF environment Interference with patented Smart-Linearity-Technology (SLT);
- Ultra low current=7.8mA;
- Ultra low noise figure(NF)=0.75dB;
- High power gain=19dB;
- High input 1dB-compression point=-10.5dBm;
- GPS L1 requires only one input matching inductor;
- RF output internally matched to 50 ohm for GPS L1;
- Supply voltage: 1.5V to 3.3V;
- Operating frequencies: 1550~1615MHz; 1164~1215MHz;
- DFN 1.1 mmX0.7 mmX0.37 mm-6L package
- ± 3 kV HBM ESD protection (including RFIN and RFOUT pin)

APPLICATIONS

- Smart Phones, Feature Phones;
- Tablet PCs;
- Personal Navigation Devices;
- Digital Still Cameras, Digital Video Cameras;
- RF Front End modules;
- Complete GPS chipset modules;
- Theft protection(laptop, ATM);

GENERAL DESCRIPTION

The AW15145DNR is a Low Noise Amplifier designed for Global Navigation Satellite Systems (GNSS) as GPS, Beidou, GLONASS, Galileo and Compass. With on-chip DC blocking capacitors at RFIN and RFOUT, The AW15145DNR can be close to the antenna, requires only one external input matching inductor for GPS L1, and reduces assembly complexity and the PCB area, enabling a cost-effective solution.

The AW15145DNR with patented Smart Linearity Technology (SLT) achieves ultra-low noise figure, high linearity, high gain, over a wide range of supply voltages from 1.5V up to 3.3V. All these features make AW15145DNR an excellent choice for GNSS LNA as it improves sensitivity with low noise figure and high gain, provide better immunity against out-of-band jammer signals with high linearity, reduces filtering requirement of preceding stage and hence reduces the overall cost of the GNSS receiver.

The AW15145DNR is available in a small lead-free, RoHS-Compliant, DFN 1.1 mm X 0.7 mm X 0.37 mm-6L package.

TYPICAL APPLICATION CIRCUIT

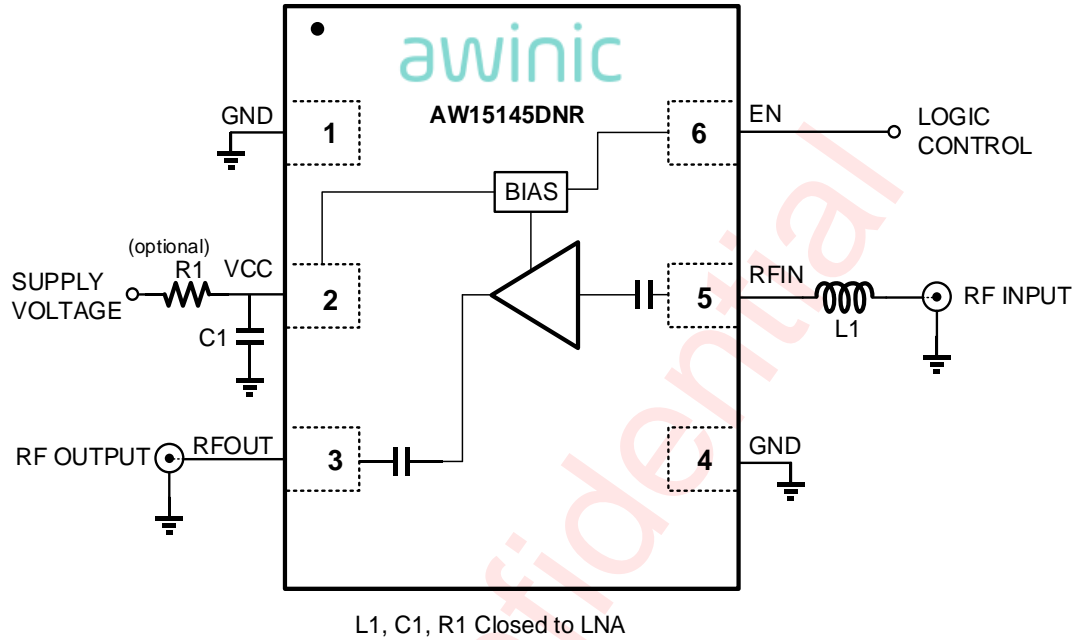


Figure 1(a) Typical Application Circuit of AW15145DNR for GPS L1

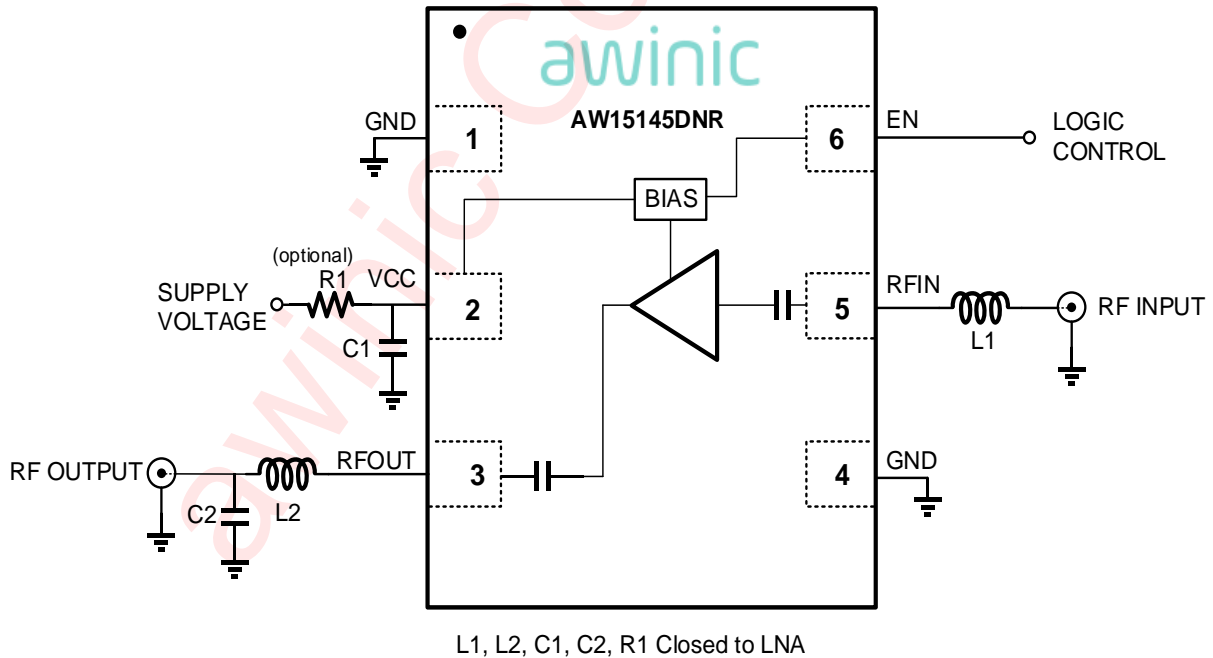


Figure 1(b) Typical Application Circuit of AW15145DNR for GPS L5

RECOMMENDED COMPONENTS LIST

Table1 and table2 list the recommended inductor types and values; Table 3 lists the recommended capacitor types and values.

Table1: list of inductor for GPS L1

Component	Part Number	Inductance	Q(min)	Q Test Frequency	Supplier	Size
	Units	nH		MHz		
L1	LQW15A	10	25	250	Murata	0402
L1	SDWL1005C	10	24	250	Sunlord	0402

Table2: list of inductor for GPS L5

Component	Part Number	Inductance	Q(min)	Q Test Frequency	Supplier	Size
	Units	nH		MHz		
L1	LQW15A	18	25	250	Murata	0402
L2	LQW15A	9.1	25	250	Murata	0402

Table2: list of capacitor

Component	Part Number	Capacitance	Rated Voltage	Supplier	Size
	Units	pF	V		
C1	GRM155	1000	50	Murata	0402
C2	GRM155	1.5	50	Murata	0402

PIN CONFIGURATION AND TOP MARK

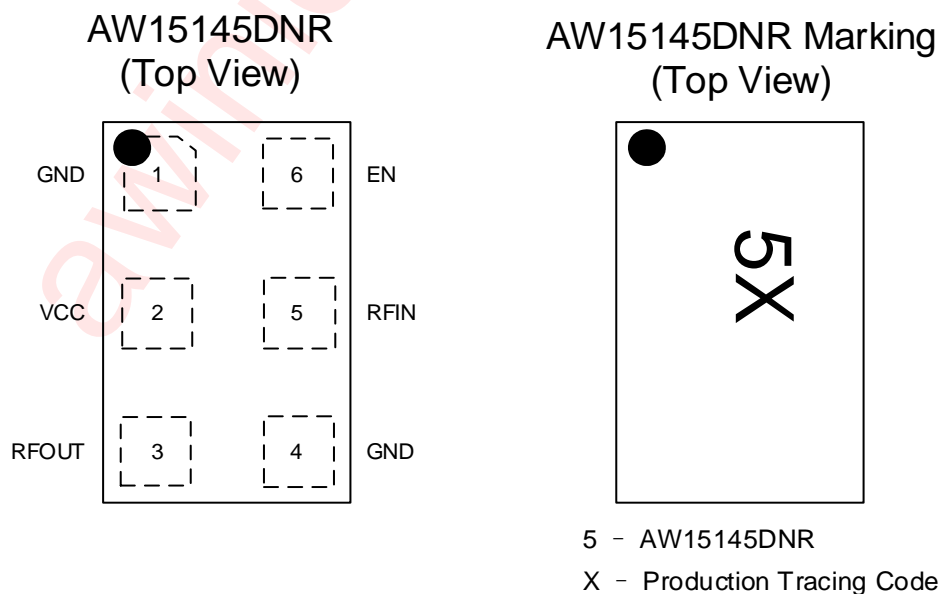


Figure 2 Pin Configuration and Top Mark

PIN DEFINITION

No.	NAME	DESCRIPTION
1	GND	Ground
2	VCC	DC Supply
3	RFOUT	LNA output
4	GND	Ground
5	RFIN	LNA input
6	EN	Logic control

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FUNCTIONAL BLOCK DIAGRAM

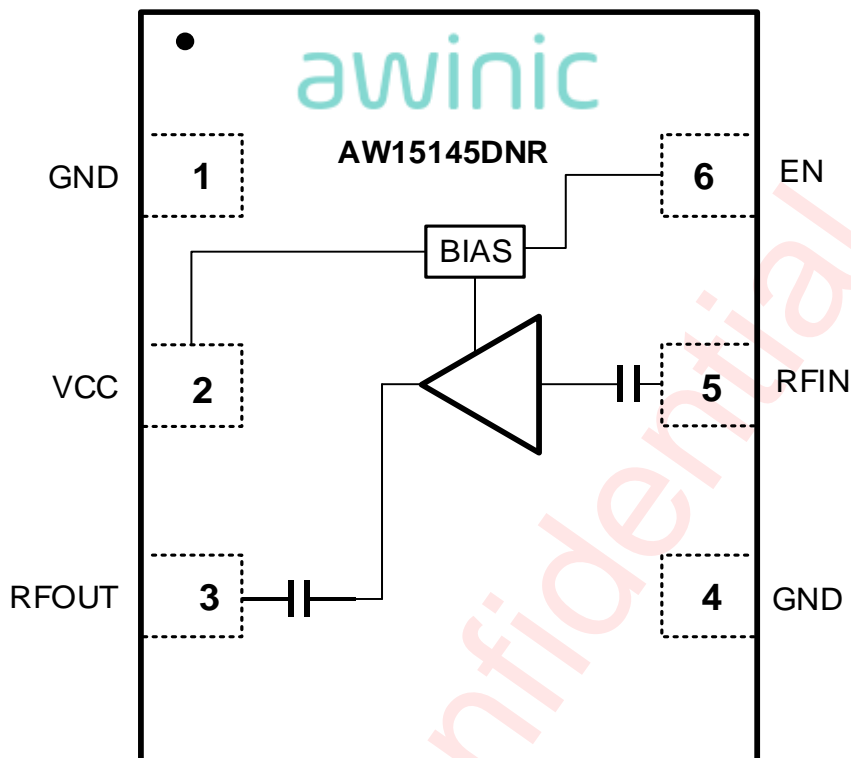


Figure 3 Functional Block Diagram

ORDERING INFORMATION

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW15145DNR	-40°C ~ 85°C	DFN 1.1mmx0.7mm-6L	5	MSL1	ROHS+HF	9000 units/ Tape and Reel

ABSOLUTE MAXIMUM RATINGS^[1]

PARAMETERS	Symbol	Values			
		Min.	Typ.	Max.	
Supply Voltage at pin VCC	V _{CC}	-0.3	-	3.6	V
Voltage at pin EN ^[2]	V _{EN}	-0.3	-	3.6	V
Current into pin VCC	I _{CC}	-	-	30	mA
RF input power ^[3]	P _{IN}	-	-	10	dBm
Package thermal resistance	θ _{JA}	-	148	-	°C/W
Junction temperature	T _J	-	-	150	°C
Storage temperature range	T _{STG}	-65	-	150	°C
Ambient temperature range	T _{amb}	-40	-	85	°C
Solder temperature(10s)		-	260	-	°C
ESD range					
HBM ^[4]			±3000		V
CDM ^[4]			±2000		V
Latch-up					
Test condition: JESD78E			+IT: +200 -IT: -200		mA mA

Note1: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Note2: Warning: due to internal ESD diode protection, the applied DC voltage should not exceed 3.6V in order to avoid excess current.

Note3: The RF input and RF output are AC coupled through internal DC blocking capacitor.

Note4: HBM standard: ESDA/JEDEC JS-001. CDM standard: ESDA/JEDEC JS-002.

ELECTRICAL CHARACTERISTICS

(AW15145DNR EVB^[1]; Typical values are at $V_{CC}=V_{EN}=2.8V$ and $T_A=+25^{\circ}C$, $f=1575.42MHz$, unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
DC ELECTRICAL CHARACTERISTICS						
V_{CC}	Supply Voltage		1.5	-	3.3	V
I_{SD}	Shut-Down Current	EN=Low			2	μA
I_{CC}	Supply Current	EN=High		7.8	12	mA
V_{EN}	Digital Input-Logic High		1.0		3.3	V
V_{EN}	Digital Input-Logic Low				0.3	V
AC ELECTRICAL CHARACTERISTICS						
G_p	Power Gain		17.5	19	20.5	dB
RL_{in}	Input Return Loss		8	10		dB
RL_{out}	Output Return Loss		10	16		dB
ISL	Reverse Isolation		20	27		dB
NF	Noise Figure ^[2]	$Z_s=50\text{ ohm};$ No jammer		0.75	1.2	dB
Kf	Stability factor	$f=20MHz\dots 10GHz$	1			
IP1dB	Inband input 1dB-compression point	$f=1575.42MHz$	-12	-10.5		dBm
IIP3 _{ib}	Inband input 3 rd -order intercept point	$f_1=1574.42MHz;$ $f_2=1575.42MHz;$ $P_{in}=-25dBm;$	-5	-2		dBm
IIP3 _{oob}	Out-of-band input 3 rd -order intercept point ^[3]	$f_1=1713MHz;$ $f_2=1851MHz;$ $P_{in_f1}=-20dBm;$ $P_{in_f2}=-65dBm;$	-3	-1		dBm
IMD3	3 rd -order intermodulation distortion	$f_1=1713MHz;$ $f_2=1851MHz;$ $P_{in_f1}=-20dBm;$ $P_{in_f2}=-65dBm;$		-83		dBm
t_{on}	turn-on time	time from V_{EN} ON to 90% of the final gain			2	μs
t_{off}	turn-off time	time from V_{EN} OFF to 10% of the gain			1	μs

Note1: input matched to 50 ohm using a high quality-factor 10nH inductor.

Note2: PCB losses are subtracted.

Note3: $IP_3=P_1+(P_2+Gain_{1575MHz}-IM_3)/2$

(AW15145DNR EVB^[1]; Typical values are at $V_{CC}=V_{EN}=1.8V$ and $T_A=+25^{\circ}C$, $f=1575.42MHz$, unless otherwise noted)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
DC ELECTRICAL CHARACTERISTICS					
V_{CC}	Supply Voltage	1.5	-	3.3	V
I_{SD}	Shut-Down Current	EN=Low		2	μA
I_{CC}	Supply Current	EN=High	6.7	10	mA
V_{EN}	Digital Input-Logic High	1.0		3.3	V
V_{EN}	Digital Input-Logic Low			0.3	V
AC ELECTRICAL CHARACTERISTICS					
G_p	Power Gain	17	18.5	20	dB
RL_{in}	Input Return Loss	8	9.5		dB
RL_{out}	Output Return Loss	10	16		dB
ISL	Reverse Isolation	20	27		dB
NF	Noise Figure ^[2]	Zs=50 ohm; No jammer	0.78	1.2	dB
Kf	Stability factor	f=20MHz...10GHz	1		
IP1dB	Inband input 1dB-compression point	f=1575.42MHz	-14	-12.5	dBm
IIP3 _{ib}	Inband input 3 rd -order intercept point	f1=1574.42MHz; f2=1575.42MHz; Pin=-25dBm;	-5.5	-3.5	dBm
IIP3 _{oob}	Out-of-band input 3 rd -order intercept point ^[3]	f1=1713MHz; f2=1851MHz; Pin_f1=-20dBm; Pin_f2=-65dBm;	-5	-3	dBm
IMD3	3 rd -order intermodulation distortion	f1=1713MHz; f2=1851MHz; Pin_f1=-20dBm; Pin_f2=-65dBm;		-80	dBm
t _{on}	turn-on time	time from V _{EN} ON to 90% of the final gain		2	μs
t _{off}	turn-off time	time from V _{EN} OFF to 10% of the gain		1	μs

Note1: input matched to 50 ohm using a high quality-factor 10nH inductor.

Note2: PCB losses are subtracted.

Note3: $IP3=P1+(P2+Gain_{1575MHz}-IM3)/2$.

(AW15145DNR EVB^[1]; Typical values are at $V_{CC}=V_{EN}=2.8V$ and $T_A=+25^{\circ}C$, $f=1176.45MHz$, unless otherwise noted)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
DC ELECTRICAL CHARACTERISTICS					
V_{CC}	Supply Voltage	1.5	-	3.3	V
I_{SD}	Shut-Down Current	EN=Low		2	μA
I_{CC}	Supply Current	EN=High	7.8	12	mA
V_{EN}	Digital Input-Logic High	1.0		3.3	V
V_{EN}	Digital Input-Logic Low			0.3	V
AC ELECTRICAL CHARACTERISTICS					
G_p	Power Gain	17.5	18.6	20	dB
RL_{in}	Input Return Loss	7	9		dB
RL_{out}	Output Return Loss	10	18		dB
ISL	Reverse Isolation	20	29.5		dB
NF	Noise Figure ^[2]	$Z_s=50\text{ ohm};$ No jammer	0.78	1.2	dB
Kf	Stability factor	$f=20MHz\dots 10GHz$	1		
IP1dB	Inband input 1dB-compression point	$f=1176.45MHz$	-15	-13.1	dBm
IIP3 _{ib}	Inband input 3 rd -order intercept point	$f_1=1176.45MHz;$ $f_2=1177.45MHz;$ $P_{in}=-30dBm;$	-5.6	-3.6	dBm
IIP3 _{oob}	Out-of-band input 3 rd -order intercept point ^[3]	$f_1=1800MHz;$ $f_2=2400MHz;$ $P_{in_f1}=-30dBm;$	-9	-7.3	dBm
ton	turn-on time	time from VEN ON to 90% of the final gain			2 μs
toff	turn-off time	time from VEN OFF to 10% of the gain			1 μs

Note1: input matched to 50 ohm using a high quality-factor 18nH inductor. Output matching using 9.1nH inductor and 1.5pF capacitor.

Note2: PCB losses are subtracted.

(AW15145DNR EVB^[1]; Typical values are at $V_{CC}=V_{EN}=1.8V$ and $T_A=+25^{\circ}C$, $f=1176.45MHz$, unless otherwise noted)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
DC ELECTRICAL CHARACTERISTICS					
V_{CC}	Supply Voltage	1.5	-	3.3	V
I_{SD}	Shut-Down Current	EN=Low		2	μA
I_{CC}	Supply Current	EN=High	6.7	10	mA
V_{EN}	Digital Input-Logic High	1.0		3.3	V
V_{EN}	Digital Input-Logic Low			0.3	V
AC ELECTRICAL CHARACTERISTICS					
G_p	Power Gain	17	17.8	20	dB
RL_{in}	Input Return Loss	6.5	8.5		dB
RL_{out}	Output Return Loss	10	18		dB
ISL	Reverse Isolation	20	29		dB
NF	Noise Figure ^[2]	$Z_s=50\text{ ohm};$ No jammer	0.82	1.2	dB
Kf	Stability factor	$f=20MHz\dots 10GHz$	1		
IP1dB	Inband input 1dB-compression point	$f=1176.45MHz$	-16	-14.3	dBm
IIP3 _{ib}	Inband input 3 rd -order intercept point	$f_1=1176.45MHz;$ $f_2=1177.45MHz;$ $P_{in}=-30dBm;$	-7.2	-5.2	dBm
IIP3 _{oob}	Out-of-band input 3 rd -order intercept point ^[3]	$f_1=1800MHz;$ $f_2=2400MHz;$ $P_{in_f1}=-30dBm;$	-11	-9	dBm
ton	turn-on time	time from V_{EN} ON to 90% of the final gain			2 μs
toff	turn-off time	time from V_{EN} OFF to 10% of the gain			1 μs

Note1: input matched to 50 ohm using a high quality-factor 18nH inductor. Output matching using 9.1nH inductor and 1.5pF capacitor.

Note2: PCB losses are subtracted.

TEST CIRCUITS

DC Characteristics

The following is the test bench for power supply, pin voltage, supply current, standby current

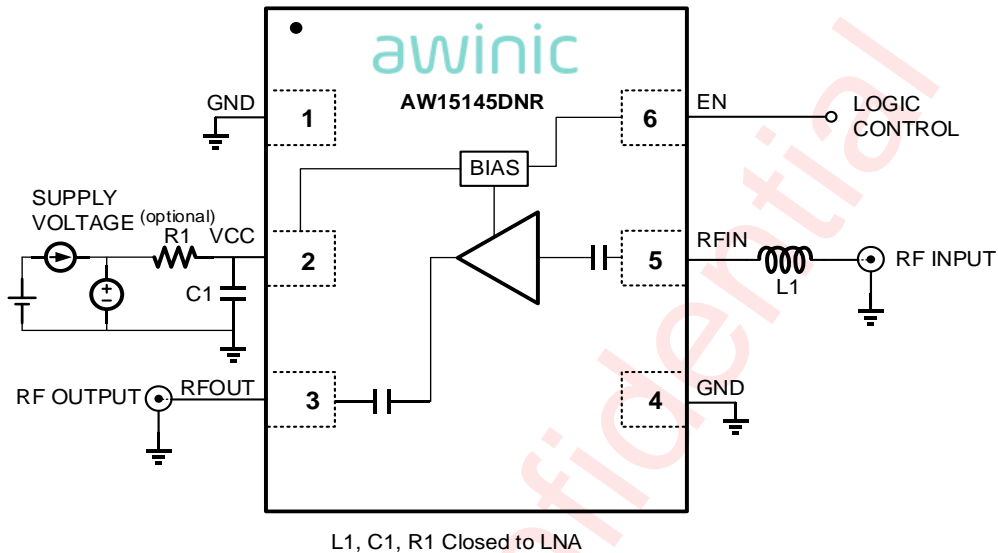


Figure 4 Test Circuits

S Parameter

The following is the test bench for input return loss, output return loss, reverse isolation, forward gain, and 1dB gain compression.

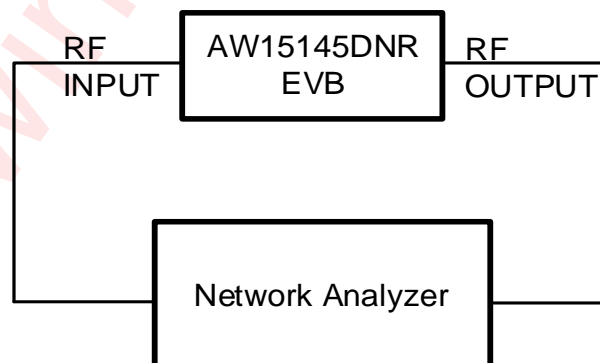


Figure 5 S Parameter Test Bench

Noise Figure

The following is the test bench for noise figure, power gain.

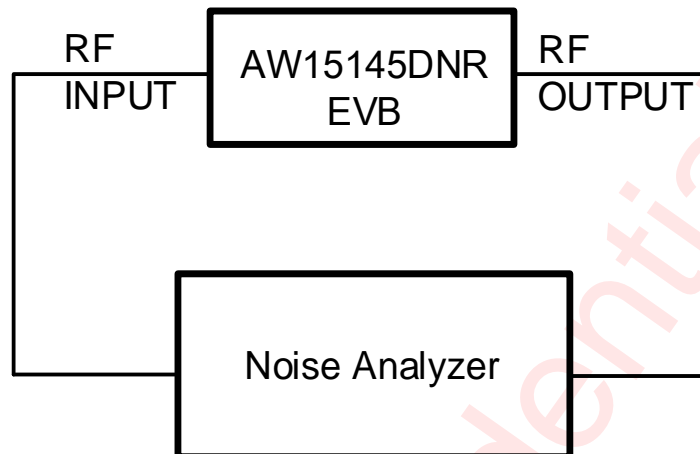


Figure 6 Noise Figure Test Bench

Intermodulation distortion

The following is the test bench for third-order intercept point and second-order intercept point.

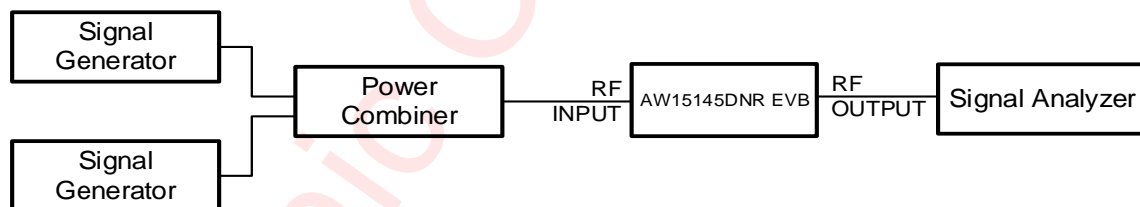
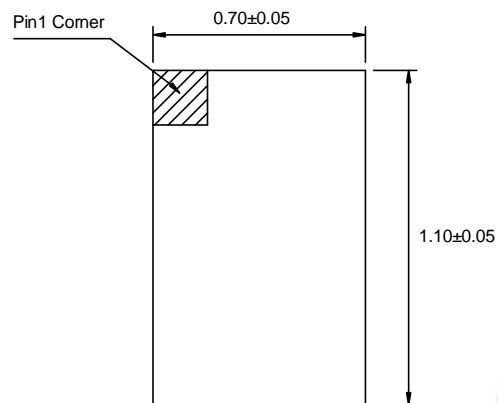
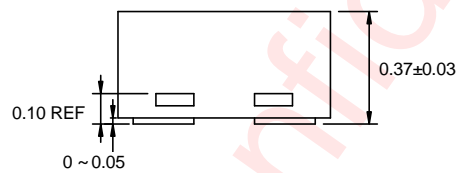


Figure 7 IIP3 Test Bench

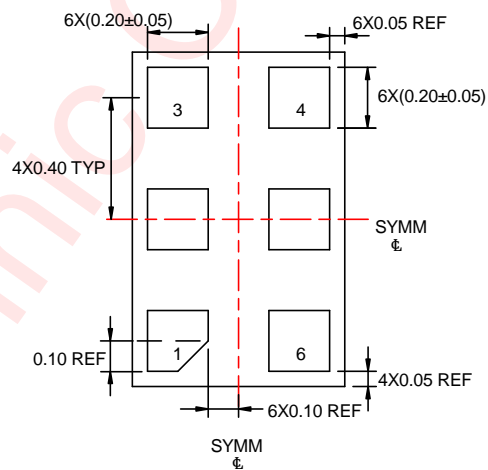
Package Description



TOP VIEW



SIDE VIEW

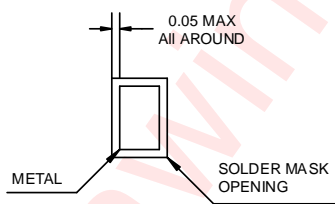
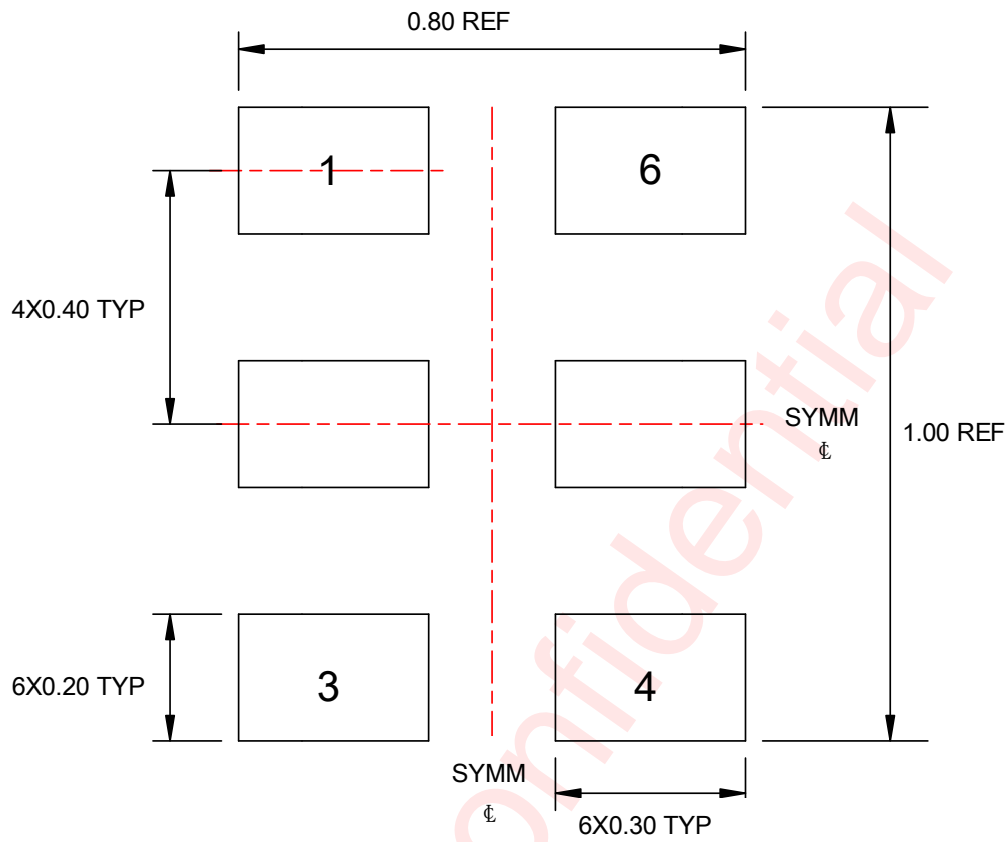


BOTTOM VIEW

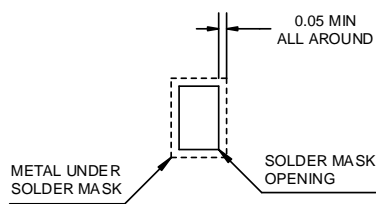
Unit : mm

Package Outline

LAND PATTERN



NON-SOLDER MASK DEFINED

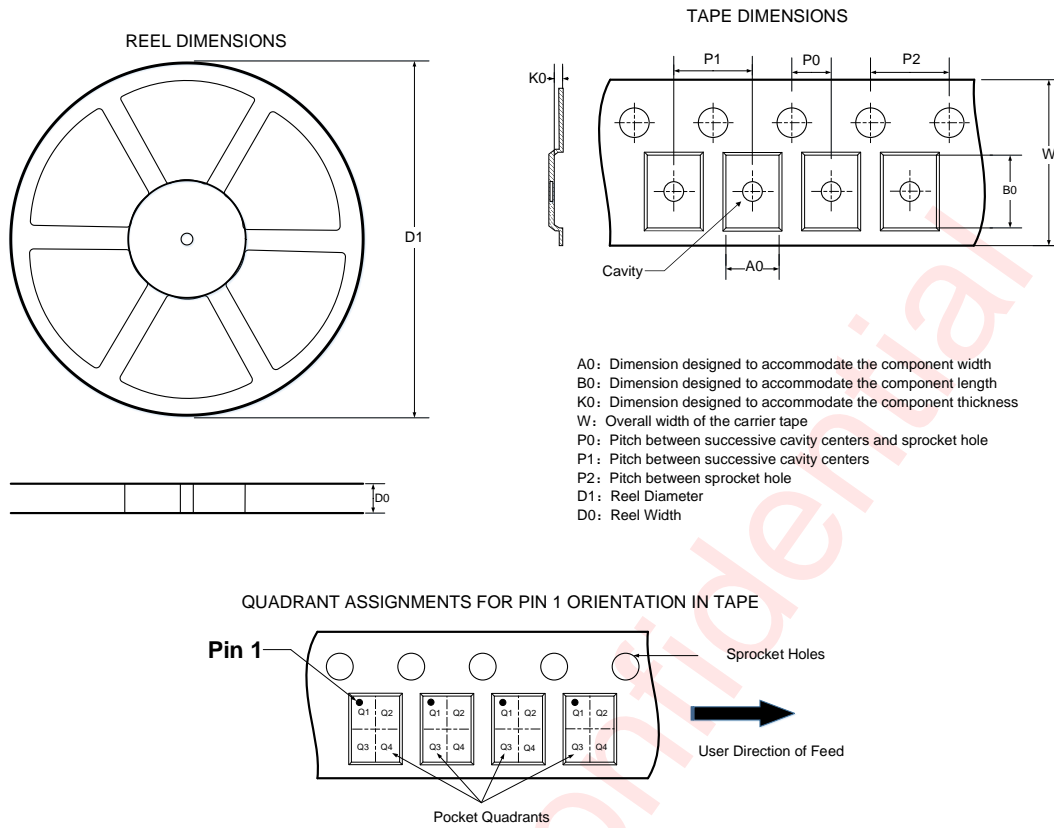


SOLDER MASK DEFINED

Unit: mm

Figure 9 Land Pattern

TAPE & REEL DESCRIPTION



A0: Dimension designed to accommodate the component width
 B0: Dimension designed to accommodate the component length
 K0: Dimension designed to accommodate the component thickness
 W: Overall width of the carrier tape
 P0: Pitch between successive cavity centers and sprocket hole
 P1: Pitch between successive cavity centers
 P2: Pitch between sprocket hole
 D1: Reel Diameter
 D0: Reel Width

DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.4	0.82	1.22	0.46	2	2	4	8	Q1

All dimensions are nominal

Figure 10 Tape & Reel Description

REVISION HISTORY

Version	Date	Change Record
V1.0	Nov. 2020	Officially Released
V1.1	Nov. 2020	Added P1dB/ IIP3 _{ib} / IIP3 _{oob} OF L5 BAND

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