6 Multi-Function LED Driver and GPIO Controller with I²C Interface

FEATURES

- 6 multi-function I/O, each for LED drive (current-source dimming) or GPIO mode
- OUT0~5 support 2 intelligent breathing mode: BLINK and SMART-FADE, breathing time is adjustable
- Support 256 steps linearity dimming
- SDA, SCL, SHDN and all GPIO can accept in 1.8V logic input
- Any GPIO can be configured as an input or an output independently
- Support interrupt, 8μs deglitch, low-level active
- Standard I²C interface, AD1/AD0 select I²C device address
- Support shutdown function, low level effective
- 2.5V~5.5V power supply
- TQFN 3mmX3mmX0.75mm-20L Package

APPLICATIONS

Mobile Phones/ Portable Media Player

Home Appliances

GENERAL DESCRIPTION

AW9106C is a 6-channel LED controller with I²C interface. Each channel can be used for GPIO. LED dimming combined with extended GPIO function, which can give full play to the application value of single chip.

AW9106C configures the current level to realize 256 steps linear dimming with I²C interface. The default I_{MAX} current is 37mA.

When OUTx works in a GPIO input mode, AW9106C detected input state to occur interrupt with internal 8μs debounce.

AW9106C supports two intelligent breathing modes: BLINK mode and SMART-FADE mode. BLINK mode allows LED automatic to flash periodically according the setting time parameter.

AW9106C is available in TQFN 3mmX3mmX 0.75mm-20L package. The operating voltage range is 2.5V~5.5V.

TYPICAL APPLICATION CIRCUIT

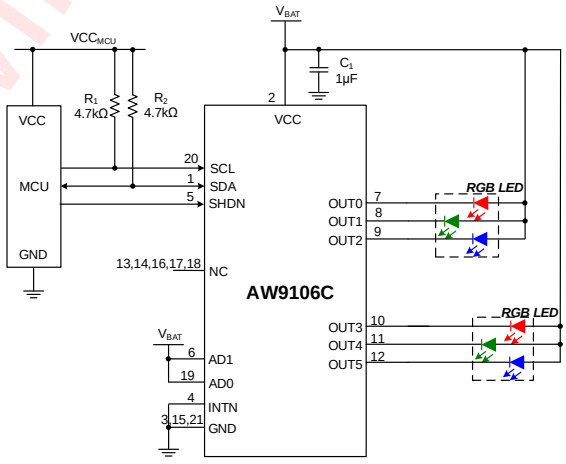
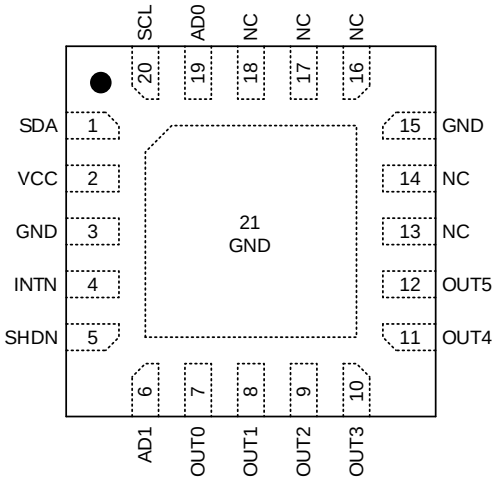


Figure 1 AW9106C Typical Application Circuit

1 PIN CONFIGURATION AND TOP MARK

AW9106CQNR
(Top View)



AW9106CQNR Marking
(Top View)

X6TS – AW9106CQNR
XXXX - Production Tracing Code

2 PIN DEFINITION

No.	NAME	DESCRIPTION
1	SDA	Serial Data I/O for I²C Interface
2	VCC	Power Supply
3	GND	Ground
4	INTN	Interrupt Output, Low Active
5	SHDN	Shutdown Pin, Low Active
6	AD1	I²C Address Pin
7	OUT0	Defaults to GPIO, LED driver configurable, support intelligence breathing mode. The default state after power on according to the level of AD1/AD0 PIN
8	OUT1	Defaults to GPIO, LED driver configurable, support intelligence breathing mode. The default state after power on according to the level of AD1/AD0 PIN
9	OUT2	Defaults to GPIO, LED driver configurable, support intelligence breathing mode. The default state after power on according to the level of AD1/AD0 PIN
10	OUT3	Defaults to GPIO, LED driver configurable, support intelligence breathing mode. The default state after power on according to the level of AD1/AD0 PIN
11	OUT4	Defaults to GPIO, LED driver configurable, support intelligence breathing mode. The default state after power on according to the level of AD1/AD0 PIN
12	OUT5	Defaults to GPIO, LED driver configurable, support intelligence breathing mode. The default state after power on according to the level of AD1/AD0 PIN
13	NC	NC
14	NC	NC
15	GND	Ground
16	NC	NC
17	NC	NC
18	NC	NC
19	AD0	I²C Address Pin
20	SCL	Serial Clock Input for I²C Interface
21	GND	Ground

3 FUNCTIONAL BLOCK DIAGRAM

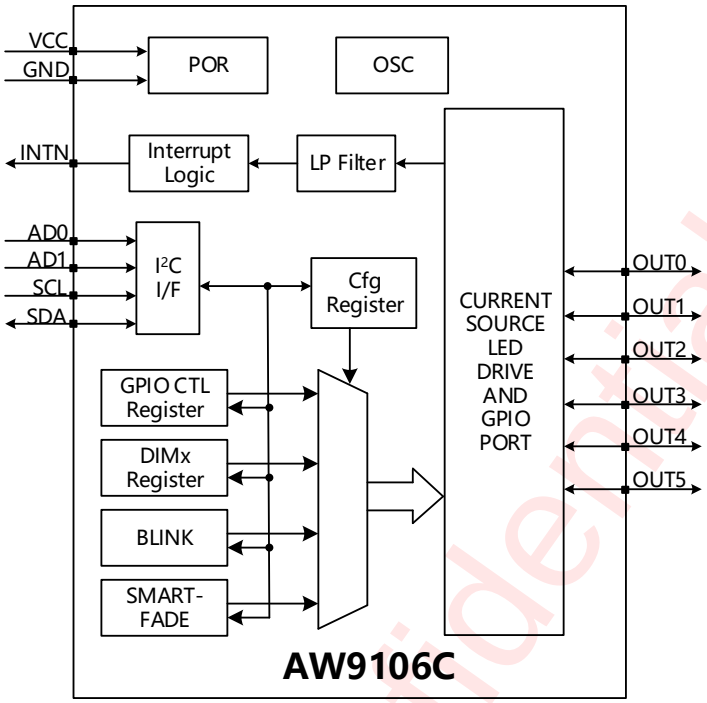
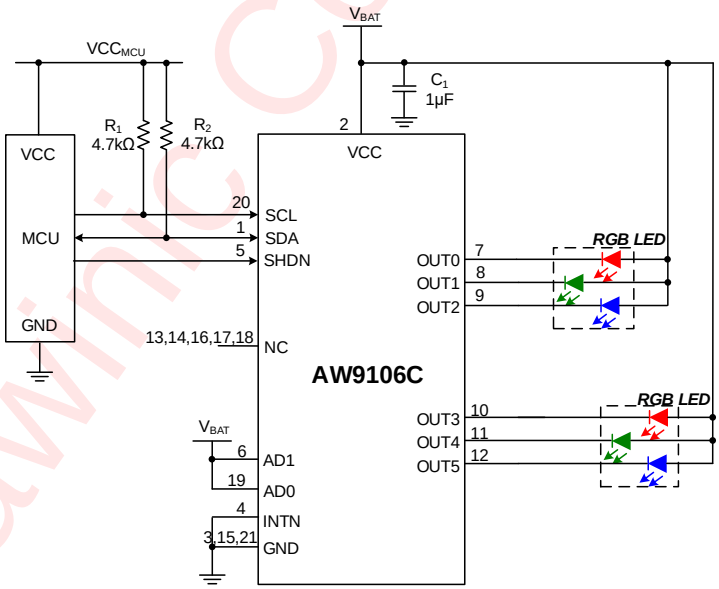


Figure 2 FUNCTIONAL BLOCK DIAGRAM

4 TYPICAL APPLICATION CIRCUITS



Note: When the anode of LED is connected to VBAT, AD1/AD0 of the chip should be connected to VBAT to ensure the default electricity state of GPIO is high or high resistance and the LED will be off. The default electricity state of GPIO is decided by AD1/AD0 level.

* For LED application，INTN should be connect to GND to avoid external leakage.

5 ORDERING INFORMATION

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW9106CQNR	-40℃～85℃	QFN3×3-20L	X6TS	MSL3	ROHS+HF	6000 units/ Tape and Reel

6 ABSOLUTE MAXIMUM RATINGS(NOTE 1)

Parameter	Range
Supply Voltage range V_{CC}	-0.3V to 6V
SCL,SDA,AD0,AD1,INTN,SHDN,OUT0-5 PINS voltage range	-0.3V to V_{CC}
Max power dissipation (P_{Dmax}, package@ T_A=25℃)	3.2 W
Package thermal resistance θ_{JA}	31℃/W
Maximum Junction temperature T_{Jmax}	125℃
Storage temperature range	-65℃ to 150℃
Lead temperature (Soldering 10 Seconds)	260℃
ESD(NOTE2)	
HBM(All Pins)	±2kV
CDM(All Pins)	±1.5kV
Latch-up	
Test Condition：JEDEC STANDARD NO.78E NOVEMBER 2016	+IT：200mA -IT：-200mA

NOTE1: *Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.*

NOTE2: *The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: MIL-STD-883J Method 3015.9(HBM) JEDEC EIA/JESD22-C101F(CDM).*

7 ELECTRICAL CHARACTERISTICS

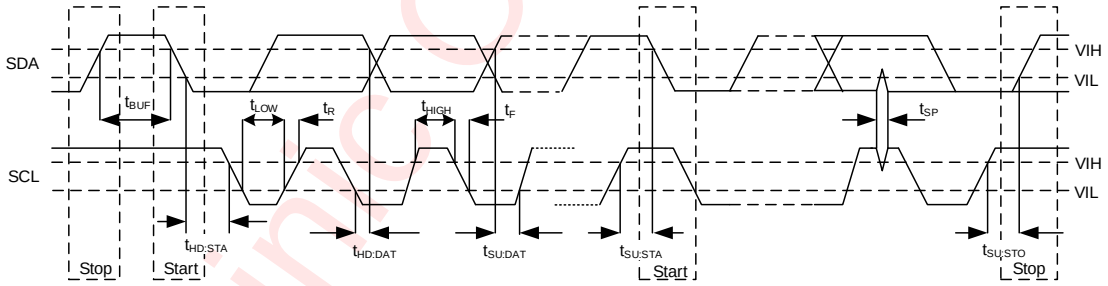
V_{CC}=3.8V, T_A=25℃ for typical values (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
Power supply voltage and current						
V_{CC}	Input voltage	T_A=-40℃~85℃	2.5		5.5	V
V_{POR}	Power on reset voltage	T_A=-40℃~85℃		1.8	2.3	V
$I_{SHUTDOWN}$	Current in Shutdown mode	SHDN=INTN=0V, SCL=SDA =0V, AD0=AD1=V_{CC}		0.4	5	μA
		SHDN=INTN=0V, SCL=SDA=1.8V, AD0=AD1=V_{CC}		1	10	μA
$I_{STANDBY}$	Current in Standby mode	Smart-fade mode, fade-off state INTN=0V,AD0=AD1=V_{CC}		50	70	μA
I_{ACTIVE}	Current in GPIO mode(SHDN=V_{CC})	INTN=0V, P0WKMD=0x03, P1WKMD=0x0F, GCR<4>=1, P0DIR=0x03, P1DIR=0x0F, AD0=AD1=V_{CC}		6	100	μA
		INTN=0V, P0WKMD=0x03, P1WKMD=0x0F, GCR<4>=1, P0DIR=0x00, P1DIR =0x00, P0DO=0x03, P1DO=0x0F, AD0=AD1=V_{CC}		6	100	μA
	Current in LED mode(SHDN=V_{CC})	INTN=0V, P0WKMD=0x00, P1WKMD=0x00, GCC<1:0>=11, DIMx=0xFF		1.3	3	mA
Digital output						
V_{OH}	Output high level(OUT0~5)	V_{CC}=2.5V,I_{SOURCE}=20mA	V_{CC}-350	Vcc-360	V_{CC}-50	mV
		V_{CC}=3.6V,I_{SOURCE}=20mA	V_{CC}-250	Vcc-240	V_{CC}-30	mV
		V_{CC}=5V,I_{SOURCE}=20mA	V_{CC}-200	Vcc-180	V_{CC}-20	mV
V_{OL}	Output low level(OUT0~5)	V_{CC}=2.5V,I_{SINK}=20mA	60	90	400	mV
		V_{CC}=3.6V,I_{SINK}=20mA	40	60	300	mV
		V_{CC}=5V,I_{SINK}=20mA	30	50	250	mV
	Output low level (SDA,INTN)	V_{CC}=2.5V,I_{SINK}=6mA	40	70	300	mV
		V_{CC}=3.6V,I_{SINK}=6mA	20	50	150	mV
		V_{CC}=5V,I_{SINK}=6mA	10	40	120	mV
Digital input						

V_{IH}	Logic high level (SCL,SDA,SHDN,AD0,AD1,OUT0~5)		1.4			V
V_{IL}	Logic low level (SCL,SDA,SHDN,AD0,AD1,OUT0~5)				0.4	V
I_{IH},I_{IL}	Input current (SCL,SDA,AD0,AD1,OUT0~5)	V_I=V_{CC} or GND	-0.2		+0.2	μA
$R_{\_SHDN}$	Resistance of shutdown pin			100k		Ω
C_I	Input capacitor (SCL,SDA,SHDN,AD0,AD1,OUT0~5)	V_I=V_{CC} or GND		3		pF
t_{SP_SHDN}	Pulse width that SHDN PIN can filter	SHDN=V_{CC}		10		μs
LED driver						
I_{MAX1}	Current Source	GCC<1:0>=11,DIMx=FFH	7.863	9.25	10.638	mA
I_{MAX2}	Current Source	GCC<1:0>=10,DIMx=FFH	15.725	18.5	21.275	mA
I_{MAX3}	Current Source	GCC<1:0>=01,DIMx=FFH	23.588	27.75	31.913	mA
I_{MAX4}	Current Source	GCC<1:0>=00,DIMx=FFH	31.450	37	42.550	mA
V_{drop1}	OUT0~5 output voltage drop	I_{OUT}=21mA,GCC<1:0>=01, DIMx=C0H		60	200	mV
F_{osc}	Oscillator Frequency		0.72	0.8	0.88	MHz
T_{FD_ON}	Fade on time	FDON_TMR<1:0>=010	441	630	819	ms
T_{FD_OFF}	Fade off time	FDOFF_TMR<1:0>=010	441	630	819	ms

8 I²C INTERFACE TIMING

PARAMETER		FAST MODE		FAST MODE PLUS		UNIT
		MIN	MAX	MIN	MAX	
F_{SCL}	Interface clock frequency	-	400	-	1000	kHz
$T_{HD:STA}$	(Repeat-start) START condition hold time	0.6	-	0.26	-	μs
T_{LOW}	Low level width of SCL	1.3	-	0.5	-	μs
T_{HIGH}	High level width of SCL	0.6	-	0.26	-	μs
$T_{SU:STA}$	(Repeat-start) START condition setup time	0.6	-	0.26	-	μs
$T_{HD:DAT}$	Data hold time	0	-	0	-	μs
$T_{SU:DAT}$	Data setup time	0.1	-	0.05	-	μs
T_R	Rising time of SDA and SCL	-	0.3	-	0.12	μs
T_F	Falling time of SDA and SCL	-	0.3	-	0.12	μs
$T_{SU:STO}$	STOP condition setup time	0.6	-	0.26	-	μs
T_{BUF}	Time between start and stop condition	1.3	-	0.5	-	μs



9 FUNCTIONAL DESCRIPTION

AW9106C is a 6 channel co-anode current breathing led driver. There are 256 current levels configurable with DIM0~DIM5. The maximum LED current (I_{MAX4}) of each channel is 37mA.

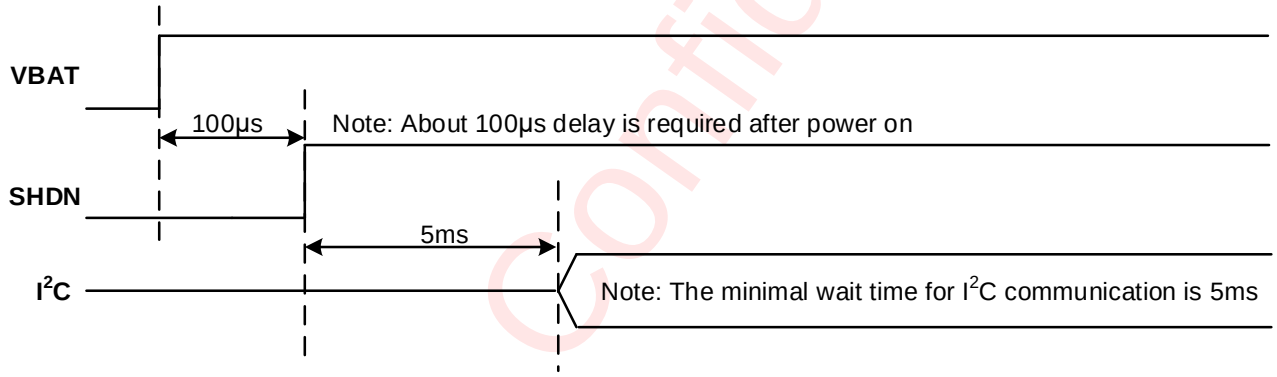
The led driver and GPIO can switch to another one with configuring register P0WKMD/P1WKMD. The default status of OUT0~OUT5 are used for GPIO function.

AW9106C supports two types of intelligent breathing modes: BLINK and SMART-FADE. In BLINK mode, AW9106C completes “fade-on” and “fade-off” breathing periodically. In SMART-FADE mode, AW9106C runs “fade-on” and “fade-off” independently with register P0DO/ P1DO configuration.

9.1 SHUTDOWN AND RESET

After power-up, about 100μs delay is required before SHDN set to high, otherwise, the device may work incorrectly. The minimal wait time for I²C communication is 5ms, during this period, some internal modules (such as LDO) start to work and reach a stable state.

Below is the recommended operation timing：



AW9106C offers 3 kinds of reset function：

- Power on reset – 5ms after power on, the chip is reset to the default state.
- Hardware reset – keep SHDN low level over 20 μs, reset all internal circuit.
- Software reset – write 00H to register 7FH, reset all internal circuit.

When AW9106C is reset, the default state of OUTx pin is GPIO.

9.2 LED DIMMING FUNCTION

AW9106C led driver uses co-anode current source. In default status, the maximum driving current I_{MAX} is 37mA.

After power on, OUTx(x=0~5) used for GPIO. AW9106C can switch OUTx to led driver mode with configuring P0WKMD/P1WKMD, shown in Table 4 and 5.

AW9106C configures four dimming range by GCR[1:0], 0~I_{MAX4} (default),0~ I_{MAX3}, 0~ I_{MAX2} or 0~ I_{MAX1}, which means 256 steps dimming range. GCR[1:0] configuration is refer to Table 3.

The dimming level of each channel is configured by DIMx(x=0~5) register. 8-bits DIMx can be configured to 256 levels, from 00H to FFH.

DIMx bit								Dimming level
7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	OFF
0	0	0	0	0	0	0	1	1/255×I_{MAX}
0	0	0	0	0	0	1	0	2/255×I_{MAX}
……								……
1	1	1	1	1	1	0	1	253/255×I_{MAX}
1	1	1	1	1	1	1	0	254/255×I_{MAX}
1	1	1	1	1	1	1	1	255/255×I_{MAX}

9.3 GPIO FUNCTION

When AW9106C is used in GPIO, the direction of OUTx is configured by P0DIR / P1DIR (Table13, 14). When OUTx is configured to output, write P0DO or P1DO register (Table11, 12) driver high or low level.

The following table shows OUTx default output driving value after power on.

AD1	AD0	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0
GND	GND	0	0	0	0	0	0
GND	VCC	Hi-Z	Hi-Z	1	1	1	1
VCC	GND	0	0	0	0	0	0
VCC	VCC	Hi-Z	Hi-Z	1	1	1	1

When OUTx is configured to input mode, the logic level of OUTx can be acquired with reading P0DI or P1DI register (Table 9, 10). AW9106C can support 1.8V level logic input.

OUT0~OUT3 are default to PUSH-PULL mode. OUT4~OUT5 are default to OPEN-DRAIN mode and can be configured as PUSH-PULL mode with GCR.GPMD0 (Table 3).

9.4 INTERRUPT FUNCTION

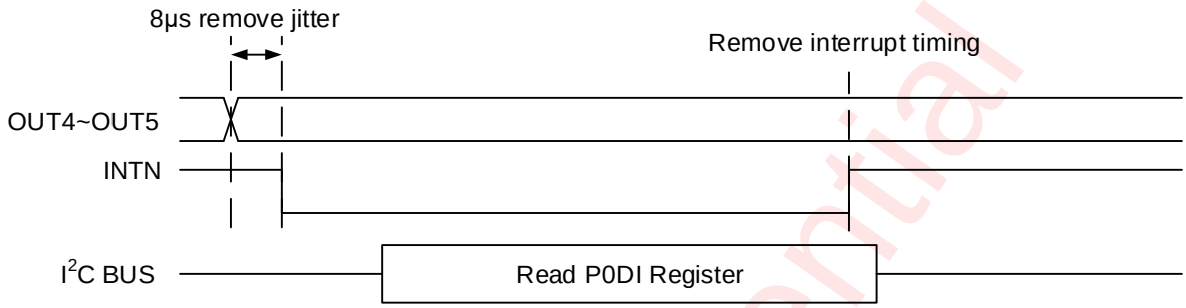
When OUTx is used for GPIO input, AW9106C detects the input state and produces interrupt request. Low level of INTN is active. INTN should be connected to pull-up resistor.

AW9106C has built-in debounce filter. The input state with 8μs low-pass filter will be steady. The interrupt request will not be produced when input state changes in 8μs.

In default status, GPIO interrupt is enabled (P0MSK or P1MSK setting, Table15,16). Only enable interrupt function and configured to GPIO input mode, the interrupt will be produced on INTN.

Clear the interrupt by reading register P0DI, P1DI register. The interrupt of OUT4~OUT5 only be cleared by reading P0DI register. The interrupt of OUT0~OUT3 only be cleared by reading P1DI register. The interrupts status can't be cleared by the other group.

When AW9106C produces the interrupt request, the interrupt request will be reserved until reading P0DI or P1DI register. The interrupt will be not cleared even if AW9106C switches to GPIO output, or disable GPIO interrupt function.



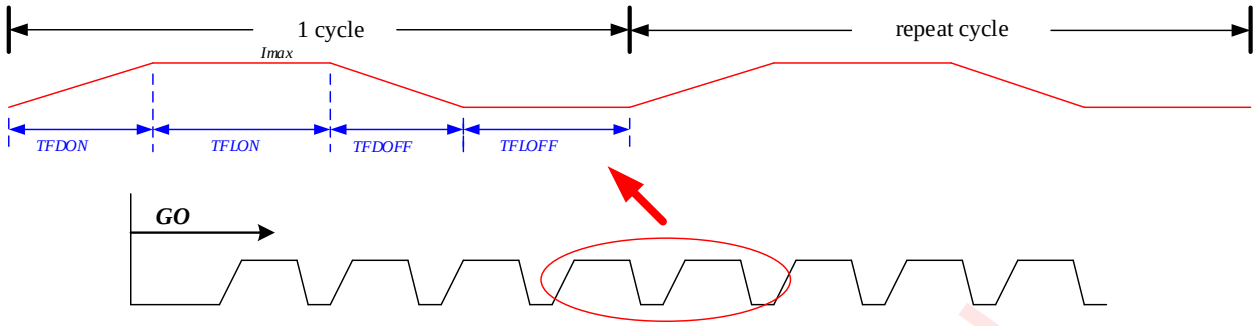
9.5 BLINK BREATHING MODE

OUTx of AW9106C supports BLINK breathing mode. In this mode, AW9106C will complete periodic blink effect automatically until exit the BLINK mode or close breathing function.

1. Configure OUTx to LED driver mode. According to application situation, set register PATEN to enable breathing mode. Set P0DIR/P1DIR (Table 13,14,pay attention to the switch of GPIO and breathing function) to open BLINK function.
2. Configure the timing parameter for BLINK breathing effects:
   - Fade-on process——FDTMR.TFDON(Table 7). The time of fade-on effect has 6 kinds of choice (0ms~5040ms). The fade-on has 64 step dimming level and LED turns on gradually from dark.
   - Full on process——FUTMR.TFLON (Table 8). Full on state has 6 kinds of choice(0ms~5040ms). The LED driving current of this period is decided by GCR[1:0].
   - Fade-off process——FDTMR.TFDOFF(Table 7). The time of fade-off effect has 6 kinds of choice (0ms~5040ms). The fade-off has 64 step dimming level and LED turns off gradually from bright.
   - Full off process——FUTMR.TFLOFF (Table 8). Full off state has 6 kinds of choice(0ms~5040ms). The LED driving current is 0 in this period.
3. After setting blinking parameter, enable GO control bit and the LED in BLINK mode starts blink periodically and automatically. It is allowed to enable GO control bit only once. Before re-enabling GO control bit, it demands soft reset or hard reset, which means a reconfiguration of registers.

All ports share the same fade-on/ fade-off/ full-on/ full-off parameter. None of these parameters can be set to zero**.** They can not be modified during blinking.

AW9106C exits BLINK mode by disable P0DIR/P1DIR corresponding bit or disable PATEN setting. The difference is AW9106C will exit BLINK immediately by disable PATEN, but we must wait it complete breathing period by another one. During BLINK mode, it is invalid to write dimming code. If the process of BLINK mode is interrupted, dimming code will maintain inner programmed code. So dimming code should be written after the end of an entire BLINK mode.



9.6 SMART-FADE MODE

The SMART-FADE mode of AW9106C is semi-automatic breathing, which will simplify 64 steps fade-on and fade-off interface operation into 1bit writing operation: Writing '1' means current of LED fade-on to Imax; Writing '0' means current of LED fade-off to zero.

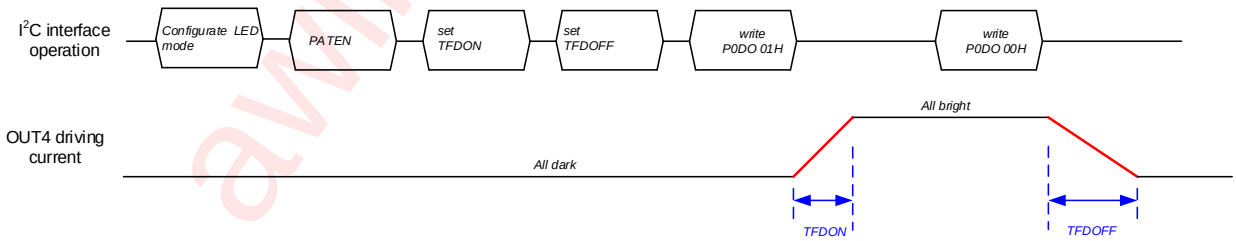
Configure SMART-FADE mode:

1. Set PATEN register and open breathing mode according to the application;
2. Set P0DIR/P1DIR (View Table 13,14, pay attention to the switch of GPIO and breathing function), SMART-FADE mode is default;
3. Set P0DO/P1DO bit to complete fade-on or fade-off (View Table 11,12, pay attention to the switch of GPIO and breathing function).

All ports share the same fade-on/ fade-off parameter. **These parameters must not be all zero and not be modified during fading on or off.**

During fading, it is not allowed to switch fade mode. For example, writing "0" to corresponding P0DO/P1DO is not allowed when fading on. Until reaching the maximum brightness, it is allowed to writing "0" to corresponding P0DO/P1DO.

AW9106C exits SMART-FADE mode by disable PATEN. During SMART-FADE mode, it is invalid to write dimming code. If the process of SMART-FADE mode is interrupted, dimming code will maintain inner programmed code. So dimming code should be written after the end of an entire SMART-FADE mode.



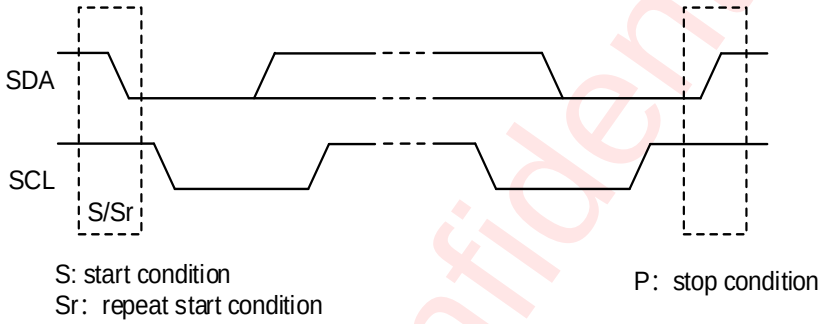
10 I²C INTERFACE

AW9106C supports the I²C serial bus and data transmission protocol at 400kHz and 1MHz. AW9106C operates as a slave on the I²C bus. Connections to the bus are made via the open-drain I/O pins SCL and SDA. The pull-up resistor can be selected in the range of 1k~10kΩ and the typical value is 4.7kΩ. AW9106C can support different high level (1.8V~3.3V) of this I²C interface.

10.1 Start and Stop Condition

I²C start: SDA changes from high level to low level when SCL is high level.

I²C stop: SDA changes from low level to high level when SCL is high level.

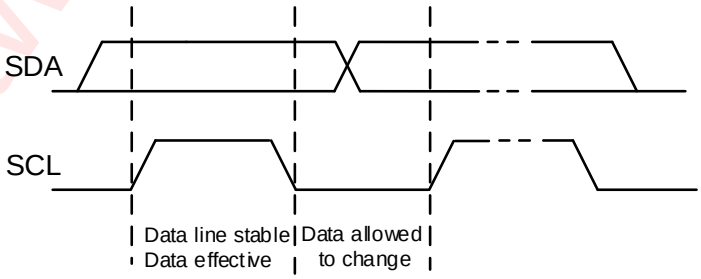


10.2 Data Transmission

After the start condition, I²C bus sent an address of slave. AW9106C wait to receive slave address When receiving start condition. If the address from I²C bus is same as the address of AW9106C, the slave pull SDA to acknowledge.

10.3 Data Validity

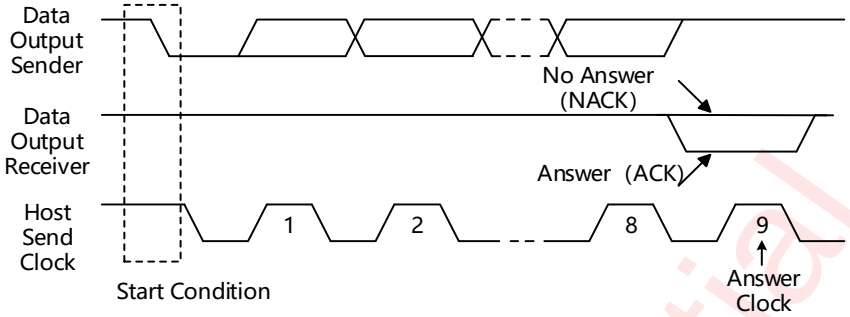
When SCL is in high level, SDA must remain one level stationary .Except start condition and stop condition, SDA level can change just in low level of SCL.



10.4 Acknowledge

ACK means the successful transfer of I²C bus data. After master sends 8bits data, SDA must be released; SDA is pulled to GND by slave device when slave acknowledges.

When master reads, slave device sends 8bit data, releases the SDA and waits for ACK from master. If ACK is sent and I²C stop is not sent by master, slave device sends the next data. If ACK is not sent by master, slave device stops to send data and waits for I²C stop.



10.5 Address

AW9106C supply two address pins AD1,AD0. This allows single I²C bus can use four AW9106C at the same time. The high five bit of slave address is “10110”, the bit2 is AD1, and the bit1 is AD0. The bit0(LSB) is writing and reading flag bit, which define the next operation writing or reading. ‘1’ is read and ‘0’ is write.

1	0	1	1	0	AD1	AD0	R/$\overline{W}$

(The value of AD1 and AD0 is same as AD1 and AD0 PIN)

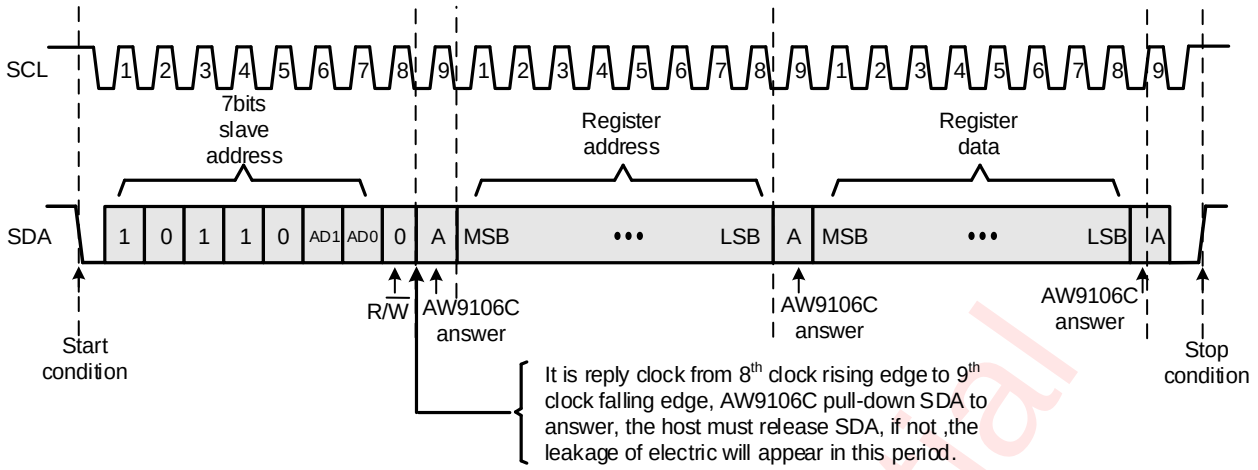
10.6 Writing Operation

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock’s high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol permits a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a Start Condition, a number of byte transfers (set by the software) and a Stop Condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit firstly. After each byte, an Acknowledge signal must follow.

In a write process, the following steps should be followed:

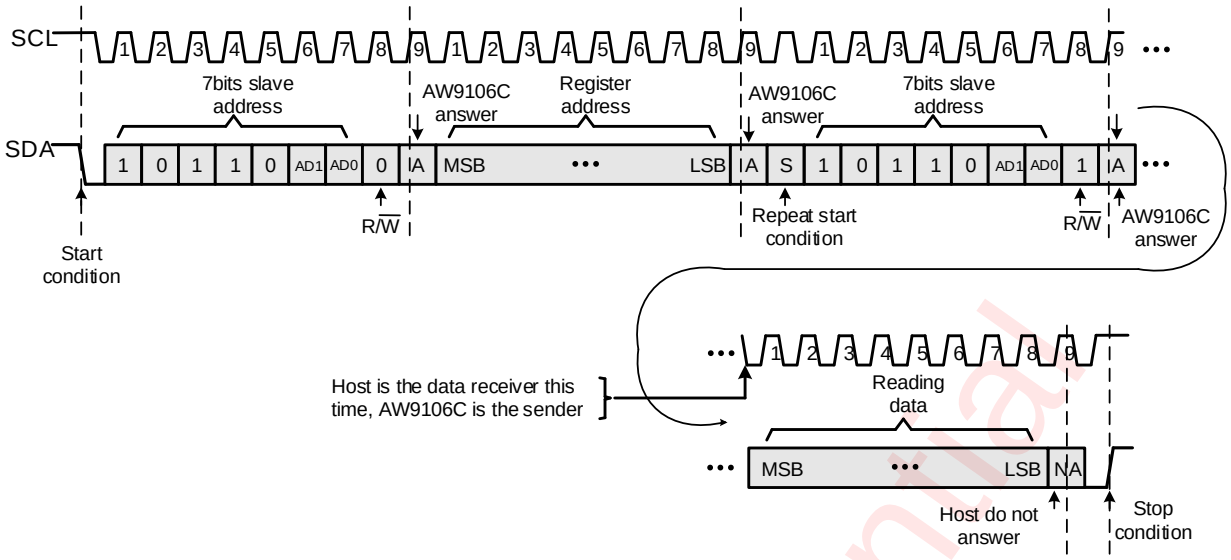
1) Master device generates START condition. The “START” signal is generated by lowering the SDA signal while the SCL signal is high.
2) Master device sends slave address (7-bit) and the data direction bit (W= 0).
3) Slave device sends acknowledge signal if the slave address is correct.
4) Master sends control register address (8-bit)
5) Slave sends acknowledge signal
6) Master sends 8Bit data to be written to the addressed register
7) Slave sends acknowledge signal
8) Master generates STOP condition to indicate write cycle end



10.7 Reading Operation

In a read cycle, the following steps should be followed:

1) Master device generates START condition
2) Master device sends slave address (7-bit) and the data direction bit (W = 0).
3) Slave device sends acknowledge signal if the slave address is correct.
4) Master sends control register address (8-bit)
5) Slave sends acknowledge signal
6) Master generates STOP condition followed with START condition or REPEAT START condition
7) Master device sends slave address (7-bit) and the data direction bit (R= 1).
8) Slave device sends acknowledge signal if the slave address is correct.
9) Slave sends 8Bit data from addressed register.
10) Master sends acknowledge signal
11) If the master device sends acknowledge signal, the slave device will increase the control register address by one, then send the next data from the new addressed register. If master sends no acknowledge signal, the slave device stop to send data and wait for STOP condition.
12) If the master device generates STOP condition, the read cycle is ended.



11 REGISTER DESCRIPTION

11.1 REGISTER OVERVIEW

Table 1. AW9106C registers list

Address (HEX)	W/R	Default Value (HEX)	Name	Description
00H	R	xxH	P0DI	OUT4～OUT5 port GPIO input state
01H	R	xxH	P1DI	OUT0～OUT3 port GPIO input state
02H	W/R	Depend on AD1/ AD0	P0DO	OUT4～OUT5 port GPIO output state; In SMART-FADE mode, OUT4~OUT5 can be used for “fade-on” and “fade-off” dimming control.
03H	W/R	Depend on AD1/ AD0	P1DO	OUT0～OUT3 port GPIO output state; In SMART-FADE mode, OUT0~OUT3 can be used for “fade-on” and “fade-off” dimming control.
04H	W/R	00H	P0DIR	OUT4～OUT5 port GPIO input and output direction control; In breathing mode, control OUT4~OUT5 to enter into BLINK mode or SMART-FADE mode.
05H	W/R	00H	P1DIR	OUT0～OUT3 port GPIO input and output direction control; In breathing mode, control OUT0～OUT3 to enter into BLINK mode or SMART-FADE mode.
06H	W/R	00H	P0MSK	OUT4～OUT5 enable interrupt function

07H	W/R	00H	P1MSK	OUT0～OUT3 enable interrupt function
08H~09H	-	-	-	Reserved
10H	R	23H	ID	ID code
11H	W/R	00H	GCR	Global Control
12H	W/R	FFH	P0WKMD	Switch OUT4～OUT5 LED driver mode or GPIO mode
13H	W/R	FFH	P1WKMD	Switch OUT0～OUT3 LED driver mode or GPIO mode
14H	W/R	00H	PATEN	Enable LED breathing mode
15H	W/R	00H	FDTMR	In BLINK or SMART-FADE mode, LED “fade-on” or “fade-off” time parameter
16H	W/R	00H	FLTMR	In BLINK mode, LED light all on or all off time parameter
17H~1FH	-	-	-	Reserved
20H	W	00H	DIM0	OUT0 port 256 steps dimming control
21H	W	00H	DIM1	OUT1 port 256 steps dimming control
22H	W	00H	DIM2	OUT2 port 256 steps dimming control
23H	W	00H	DIM3	OUT3 port 256 steps dimming control
24H	W	00H	DIM4	OUT4 port 256 steps dimming control
25H	W	00H	DIM5	OUT5 port 256 steps dimming control
26H~7EH	-	-	-	Reserve
7FH	W/R	01H	RESET	Write 00H,reset by software, 01H is read as chip ID.

11.2 REGISTER DETAIL

Table 2. DIM0~DIM5(20H~25H),256 steps dimming configuration register

Bit	Symbol	Description	Default
D[7:0]	DIM	256 steps dimming level choice 20H~25H corresponding to OUT0~OUT5 dimmer instruction; D[7:0] code from 0 to 255 corresponding to the current 0~I_{MAX}	00H

Table 3. GCR(11H),Global control register

Bit	Symbol	Description	Default
D7	GO	Writing 1 to enable breathing in BLINK mode.	0
D[6:5]	-	-	Remain

D4	GPMD0	OUT4～OUT5 driver option in GPIO mode 0：OPEN-DRAIN 1：PUSH-PULL	0
D[3:2]	-	-	Remain
D[1:0]	GCC	256 dimming range option 00：0～I_{MAX4} 01：0～I_{MAX3} 10：0～I_{MAX2} 11：0～I_{MAX1}	00

Table 4. P0WKMD(12H), GPIO control switch to LED driver register

Bit	Symbol	Description	Default
D[7:2]	-	-	Remain
D1	P0WKMD[1]	OUT5 mode control 0：LED mode 1：GPIO mode	1
D0	P0WKMD[0]	OUT4 mode control 0：LED mode 1：GPIO mode	1

Table 5. P1WKMD(13H), GPIO control switch to LED driver register

Bit	Symbol	Description	Default
D[7:4]	-	-	Remain
D3	P1WKMD[3]	OUT3 mode control 0：LED mode 1：GPIO mode	1
D2	P1WKMD[2]	OUT2 mode control 0：LED mode 1：GPIO mode	1
D1	P1WKMD[1]	OUT1 mode control 0：LED mode 1：GPIO mode	1

D0	P1WKMD[0]	OUT0 mode control 0：LED mode 1：GPIO mode	1

Table 6. PATEN(14H),Enable Breathing REGISTER

Bit	Symbol	Description	Default
D[7:6]	-	-	Remain
D5	PATEN[5]	OUT5 enable breath mode 0：disable 1：enable	0
D4	PATEN[4]	OUT4 enable breath mode 0：disable 1：enable	0
D3	PATEN[3]	OUT3 enable breath mode 0：disable 1：enable	0
D2	PATEN[2]	OUT2 enable breath mode 0：disable 1：enable	0
D1	PATEN[1]	OUT1 enable breath mode 0：disable 1：enable	0
D0	PATEN[0]	OUT0 enable breath mode 0：disable 1：enable	0

Table 7. FDTMR(15H),Fade-on or fade-off time setting register in BLINK or SMART-FADE

Bit	Symbol	Description	Default
D[7:6]	-	-	Remain
D[5:3]	TFDOFF	Fade-off time setting 000：0ms 001：315ms 010：630ms	000

		011：1260ms 100：2520ms 101：5040ms 110/111：0ms	
D[2:0]	TFDON	Fade-on time setting 000：0ms 001：315ms 010：630ms 011：1260ms 100：2520ms 101：5040ms 110/111：0ms	000

Table 8. FULL_TMR(16H),All-on or all-off time setting register in BLINK mode.

Bit	Symbol	Description	Default
D[7:6]	-	-	Remain
D[5:3]	TFLOFF	All-off time setting 000：0ms 001：315ms 010：630ms 011：1260ms 100：2520ms 101：5040ms 110/111：0ms	000
D[2:0]	TFLON	All-on time setting 000：0ms 001：315ms 010：630ms 011：1260ms 100：2520ms 101：5040ms 110/111：0ms	000

Table 9. P0DI(00H),GPIO input state register

Bit	Symbol	Description	Default
D[7:2]	-	-	Remain
D1	P0DI[1]	OUT5 pin state 0：Low level 1：High level	x
D0	P0DI[0]	OUT4 pin state 0：Low level 1：High level	x

Table 10. P1DI(01H),GPIO input state register

Bit	Symbol	Description	Default
D[7:4]	-	-	Remain
D3	P1DI[3]	OUT3 pin state 0：Low level 1：High level	x
D2	P1DI[2]	OUT2 pin state 0：Low level 1：High level	x
D1	P1DI[1]	OUT1 pin state 0：Low level 1：High level	x
D0	P1DI[0]	OUT0 pin state 0：Low level 1：High level	x

Table 11. P0DO(02H),GPIO output state register or as driver control in SMART-FADE mode

Bit	Symbol	Description	Default
D[7:2]	-	-	Remain
D1	P0DO[1]	P0WKMD[1]=1,as driving OUT5 pin state 0：Low level 1：High level P0WKMD[0]=0 & PATEN[5]=1, OUT5 in SMART-FADE mode	Depend on AD0 and AD1

		0->1：fade-on 1->0：fade-off	
D0	P0DO[0]	P0WKMD[0]=1,as driving OUT4 pin state 0：Low level 1：High level P0WKMD[0]=0 & PATEN[4]=1, OUT4 in SMART-FADE mode 0->1：fade-on 1->0：fade-off	

Table 12. P1DO(03H),GPIO output state register or as driver control in SMART-FADE mode

Bit	Symbol	Description	Default
D[7:4]	-	-	Remain
D3	P1DO[3]	P1WKMD[3]=1,as driving OUT3 pin state 0：Low level 1：High level P1WKMD[3]=0 &PATEN[3]=1,OUT3 in SMART-FADE mode 0->1：fade-on 1->0：fade-off	Depend on AD0 and AD1
D2	P1DO[2]	P1WKMD[2]=1,as driving OUT2 pin state 0：Low level 1：High level P1WKMD[2]=0 &PATEN[2]=1,OUT2 in SMART-FADE mode 0->1：fade-on 1->0：fade-off	
D1	P1DO[1]	P1WKMD[1]=1,as driving OUT1 pin state 0：Low level 1：High level P1WKMD[1]=0 &PATEN[1]=1,OUT1 in SMART-FADE mode 0->1：fade-on 1->0：fade-off	
D0	P1DO[0]	P1WKMD[0]=1,as driving OUT0 pin state 0：Low level 1：High level P1WKMD[0]=0 &PATEN[0]=1,OUT0 in SMART-FADE mode	

		0->1：fade-on 1->0：fade-off	

Table 13. P0DIR(04H),GPIO input or output select register or as BLINK,SMART-FADE Mode select

Bit	Symbol	Description	Default
D[7:2]	-	-	Remain
D1	P0DIR[1]	P0WKMD[1]=1, OUT5 input or output choice 0：output 1：input P0WKMD[1] =0 & PATEN[5]=1, OUT5 BLINK or SMART-FADE mode choice 0：SMART-FADE mode 1：BLINK mode	0
D0	P0DIR[0]	P0WKMD[0] =1, OUT4 input or output choice 0：output 1：input P0WKMD[0] =0 & PATEN[4]=1, OUT4 BLINK or SMART-FADE mode choice 0：SMART-FADE mode 1：BLINK mode	0

Table 14. P1DIR(05H),GPIO input or output selection register, or used for BLINK,SMART-FADE mode choice

Bit	Symbol	Description	Default
D[7:4]	-	-	Remain
D3	P1DIR[3]	P0WKMD[3] =1 , OUT3 input or output choice 0：output 1：input P0WKMD[3]=0 & PATEN[3]=1, OUT3 BLINK or SMART-FADE mode choice 0：SMART-FADE mode 1：BLINK mode	0
D2	P1DIR[2]	P0WKMD[2] =1 , OUT2 input or output choice 0：output 1：input	0

		P0WKMD[2]=0 & PATEN[2]=1, OUT2 BLINK or SMART-FADE mode choice 0：SMART-FADE mode 1：BLINK mode	
D1	P1DIR[1]	P0WKMD[1] =1 , OUT1 input or output choice 0：output 1：input P0WKMD[1]=0 & PATEN[1]=1, OUT1 BLINK or SMART-FADE mode choice 0：SMART-FADE mode 1：BLINK mode	0
D0	P1DIR[0]	P0WKMD[0] =1 , OUT0 input or output choice 0：output 1：input P0WKMD[0]=0 & PATEN[0]=1, OUT0 BLINK or SMART-FADE mode choice 0：SMART-FADE mode 1：BLINK mode	0

Table 15. P0MSK(06H),GPIO Mask Interrupt Register

Bit	Symbol	Description	Default
D[7:2]	-	-	Remain
D1	P0MSK[1]	OUT5 enable interrupt 0：enable 1：disable	0
D0	P0MSK[0]	OUT4 enable interrupt 0：enable 1：disable	0

Table 16. P1MSK (07H),GPIO Mask Interrupt Register

Bit	Symbol	Description	Default
D[7:4]	-	-	Remain
D3	P1MSK[3]	OUT3 enable interrupt 0：enable 1：disable	0

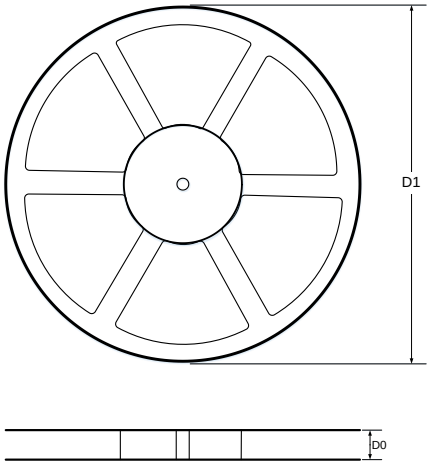
D2	P1MSK[2]	OUT2 enable interrupt 0：enable 1：disable	0
D1	P1MSK[1]	OUT1 enable interrupt 0：enable 1：disable	0
D0	P1MSK[0]	OUT0 enable interrupt 0：enable 1：disable	0

Table 17. RESETN(7FH), Software Reset Register

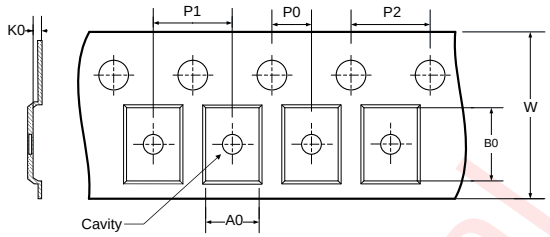
Bit	Symbol	Description	Default
D[7:0]	RESETN	Write 00H,reset by software 01H is read as chip ID	01H

12 TAPE AND REEL INFORMATION

REEL DIMENSIONS

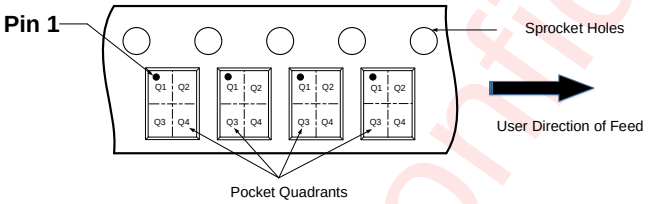


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

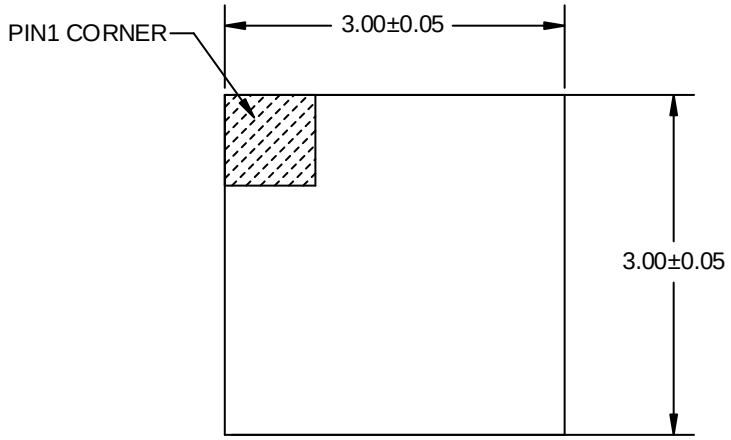


DIMENSIONS AND PIN1 ORIENTATION

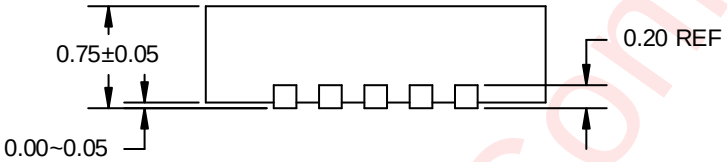
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330	12.4	3.3	3.3	1.1	2	8	4	12	Q1

All dimensions are nominal

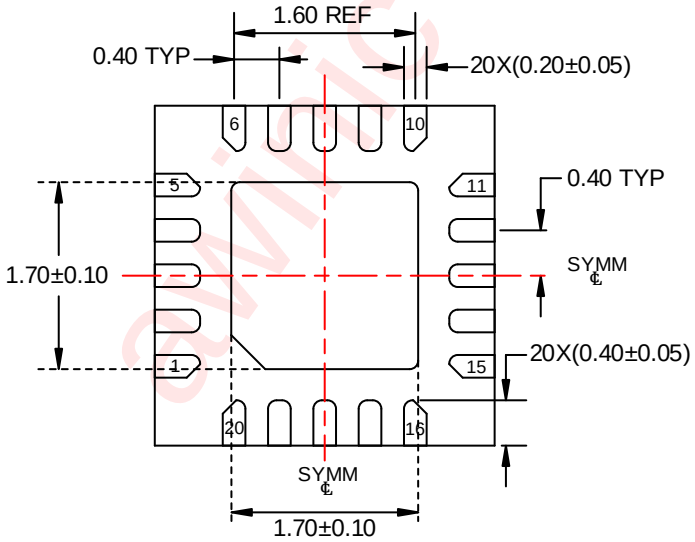
13 PACKAGE DESCRIPTION



TOP VIEW



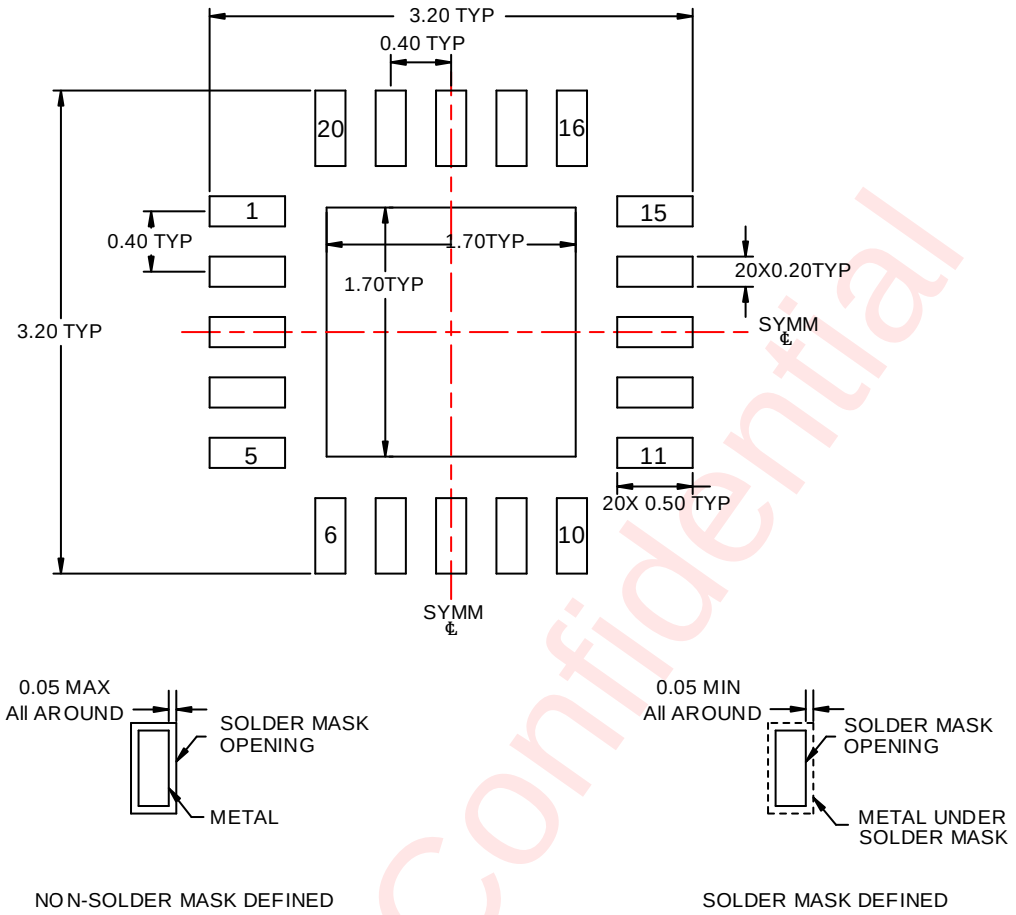
SIDE VIEW



BOTTOM VIEW

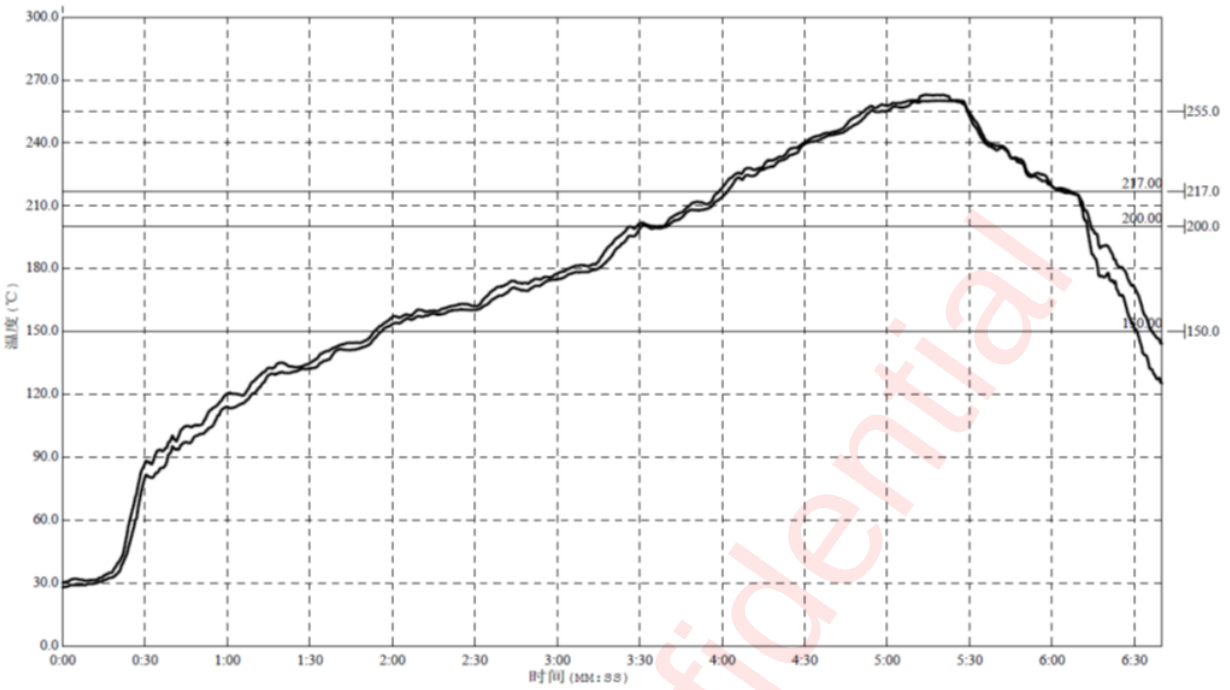
Unit: mm

14 RECOMMENDED LAND PATTERN



Unit：mm

15 REFLOW



Reflow Note	Spec
Average ramp-up rate (217°C to peak)	Max. 3°C /sec
Time of Preheat temp. (from 150°C to 200°C)	60-120sec
Time to be maintained above 217°C	60-150sec
Peak Temperature	>260°C
Time within 5°C of actual peak temp	20-40sec
Ramp-down rate	Max. 6°C /sec
Time from 25°C to peak temp	Max. 8min

Package Reflow Standard Profile

NOTE 1: All data are compared with the package-top temperature, measured on the package surface;

NOTE 2: AW9106C adopted the Pb-Free assembly.

16 REVISION HISTORY

Version	Date	Revision Record
V1.0	Aug 2021	First officially release

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