6MHz, 750mA DC-DC Buck Converter for RF Power Amplifiers

FEATURES

- 6MHz PWM Switching Frequency at Heavy Load
- Input Voltage 2.2V to 5V
- Adjustable Output Voltage 0.5V to 3.4V through VCON Voltage
- Automatic PWM-PFM Mode Change
- Spread Spectrum PWM Frequency Dithering
- 27μA PFM Quiescent Current at Light Load
- 750mA Output Current Capacity
- Cycle-by-Cycle Peak Current Limit Protection
- Thermal Overload Protection
- Small Chip Inductor in 0805 Case Size Allowed
- 0402 Case Size and 6.3V Ceramic Capacitor for C_{IN} and C_{OUT}
- FCDFN 1.5mm X1.0mm X0.55mm-6L Package

APPLICATIONS

Battery-Powered 2G, 3G and 4G Power Amplifiers

Battery-Powered RF Devices

NB-IoT Devices

GENERAL DESCRIPTION

AW37416 is a 6MHz DC-DC step-down converter suitable for RF power amplifiers supplied by a single battery. The device provides a regulated adjustable output voltage from 0.5V to 3.4V, 2.2V to 5V input voltage range.

The AW37416 works in three operation modes. At heavy load, the device operates in 6MHz fixed frequency PWM mode to minimize the RF interference. At light load, the AW37416 enters peak-current-control PFM mode automatically to reduce the switching losses. In PFM mode, the quiescent current consumed by the part is reduced to 27μA for the purpose to extend the battery life. The device is off in Shutdown mode and reduces the supply current to 0.1μA(typical).

AW37416 is available in a FCDFN 1.5mm X1.0mm X0.55mm-6L package. The high switching frequency 6MHz allows the use of the economic size-saving external components, two ceramic capacitors and one 0.47μH inductor are required.

TYPICAL APPLICATION CIRCUIT

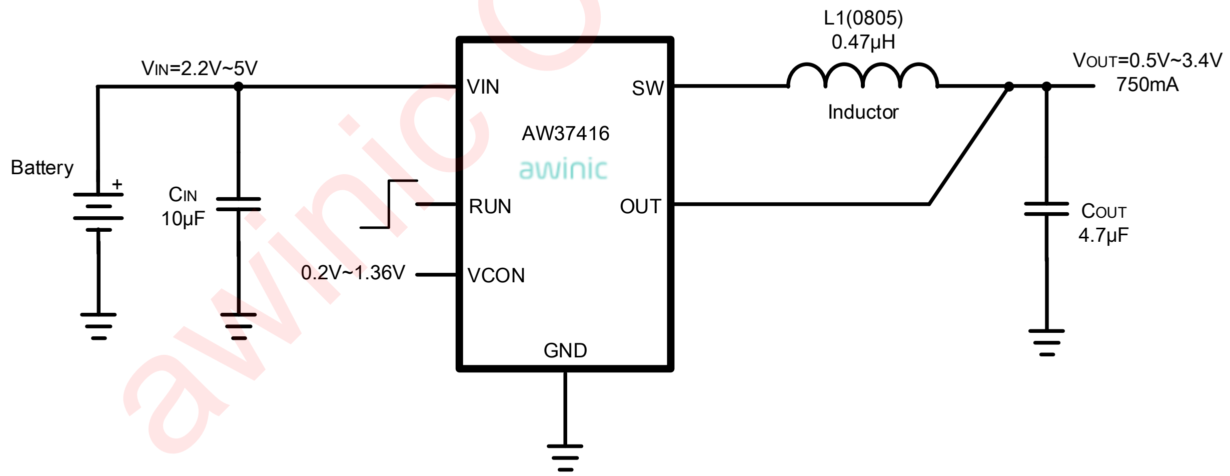

Figure 1 Typical Application Circuit of AW37416

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PIN CONFIGURATION AND TOP MARK

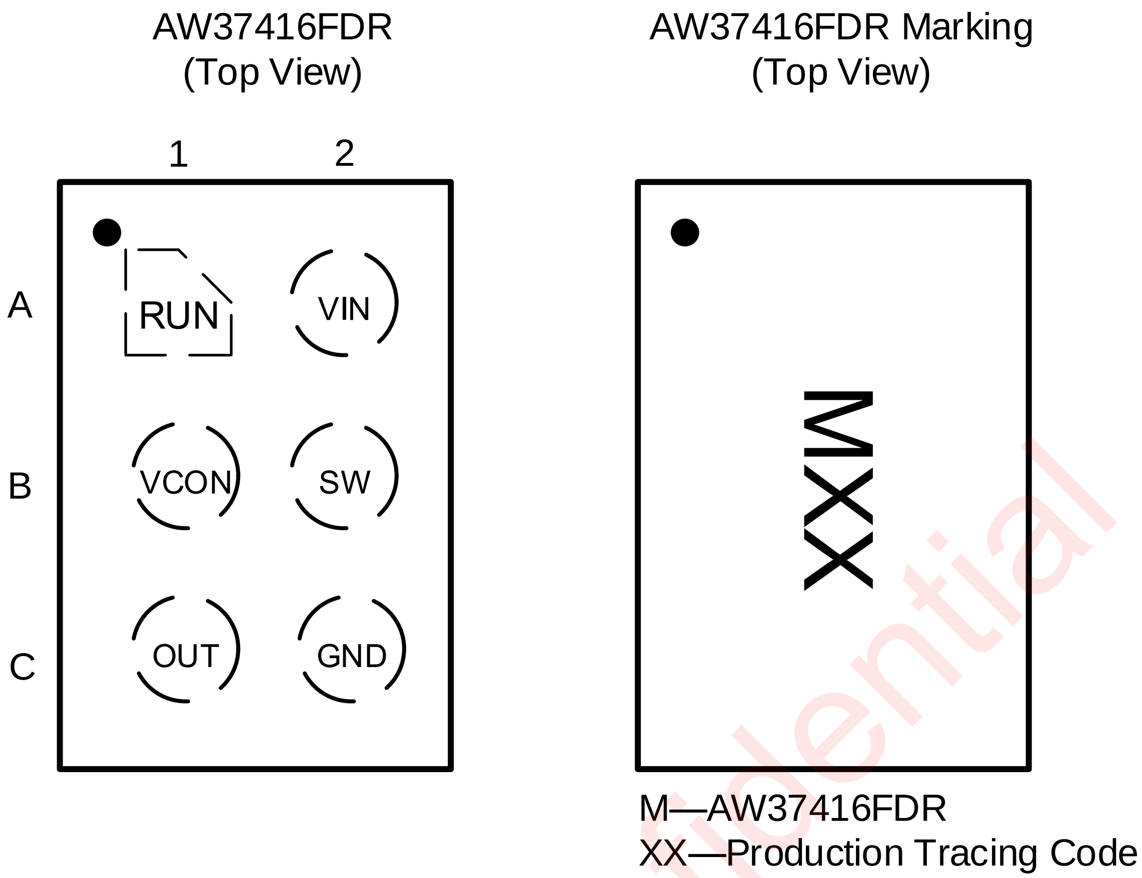


Figure 2 Pin Configuration and Top Mark

PIN DEFINITION

No.	NAME	DESCRIPTION
A1	RUN	Enable Input. Set a digital input high to enable the part. Set low to shut down the AW37416. Do NOT leave the RUN pin floating.
A2	VIN	Power Supply Input. Put a 10μF bypass capacitor close to this pin.
B1	VCON	Analog Voltage Control Input. Do NOT leave the VCON pin floating. Put an analog input voltage at this pin to set up the output voltage. VOUT=2.5 x VCON.
B2	SW	Switching Node Output.
C1	OUT	Output Voltage Feedback Input. Connect this pin to output supply at the output inductor.
C2	GND	Ground.

FUNCTIONAL BLOCK DIAGRAM

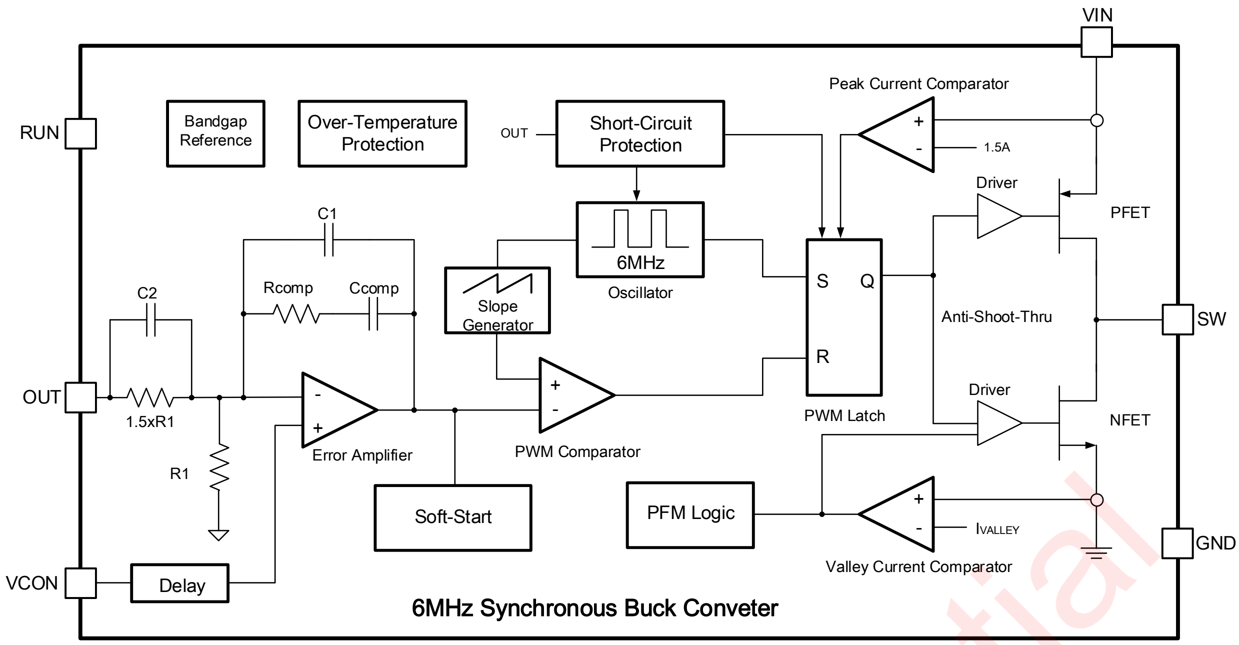


Figure 3 Function Block Diagram

TYPICAL APPLICATION CIRCUITS

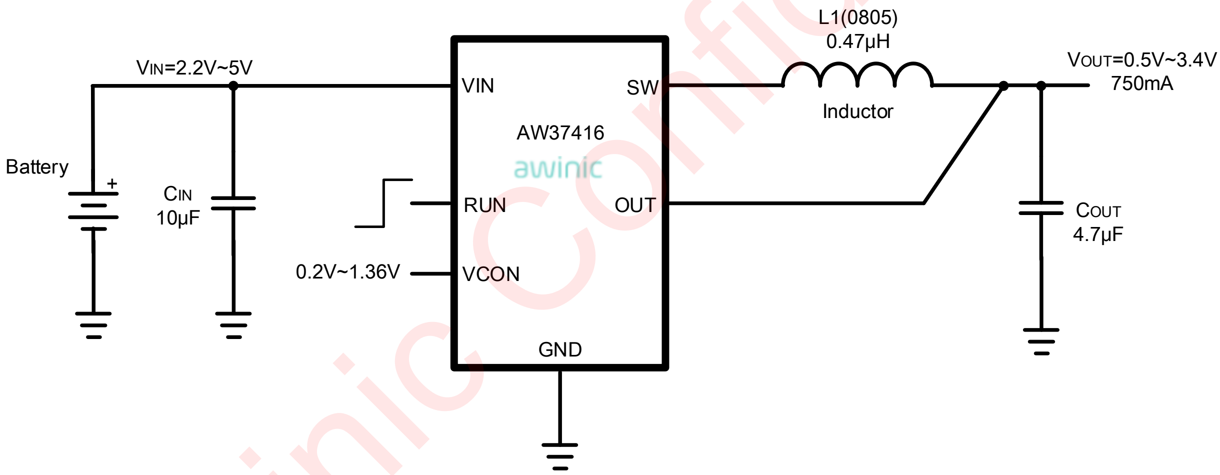


Figure 4 AW37416 Application Circuit

ORDERING INFORMATION

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW37416FDR	-40°C～85°C	FCDFN 1.5mmX1.0mm -6L	M	MSL1	ROHS+HF	3000 Units/ Tape & Reel

ABSOLUTE MAXIMUM RATINGS(NOTE1)

PARAMETERS		RANGE
Supply Voltage Range V_{IN}		-0.3V to 6V
Output Voltage Range	SW, VCON, OUT, RUN	(GND-0.3)V to (VIN+0.3)V
Junction-to-ambient Thermal Resistance θ_{JA}		169°C /W
Operating Free-air Temperature Range		-40°C to 85°C
Junction Temperature Range		-40°C to 125°C
Maximum Junction Temperature T_{JMAX}		150°C
Storage Temperature T_{STG}		-65°C to 150°C
Lead Temperature (Soldering 10 Seconds)		260°C
ESD(NOTE 2)		
HBM (Human Body Model)		±2kV
CDM		±1.5kV
Latch-Up		
Test Condition: JEDEC STANDARD No.78B DECEMBER 2008		+IT：200mA -IT：-200mA

NOTE1: Conditions out of those ranges listed in “absolute maximum ratings” may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in “recommended operating conditions”. Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: MIL-STD-883H Method 3015.8

ELECTRICAL CHARACTERISTICS

All typical values are tested at VIN=3.6V, T_A=25°C. (unless otherwise noted) Minimum and Maximum limits are specified by design, test, or statistical analysis, applying over full ambient temperature range (-40°C≤T_A ≤85°C) and over VIN range of 2.2V to 5V.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range		2.2		5	V
I_{LOAD}	Recommended load current		0		750	mA
OUTPUT VOLTAGE						
$V_{OUT,MIN}$	OUT pin voltage at minimum setting	PWM mode, V_{IN}=3.6V VCON=0.2V	0.45	0.5	0.55	V
$V_{OUT,MAX}$	OUT pin voltage at maximum setting	PWM mode, V_{IN}=3.9V, VCON=1.36V	3.3	3.4	3.5	V
SUPPLY CURRENT						
I_{SHDN}	Supply current in shutdown mode	V_{RUN}=0V, V_{IN}=3.6V			1	μA
		V_{RUN}=0V, V_{IN}=5V			1.5	μA
I_{Q_PWM}	PWM mode quiescent current	PWM mode. 100% Duty Ratio. VCON=0.8V, V_{OUT}=1V			1.2	mA
I_{Q_PFM}	Power save mode quiescent current	PFM mode. No Load, Closed loop		27	45	μA
POWER FET SWITCHES						
$R_{DSON(P)}$	P-type power switch on resistance	I_{SW}=200mA		130	260	mΩ
$R_{DSON(N)}$	N-type power switch on resistance	I_{SW}=-200mA		80	160	mΩ
STEP-DOWN CONVERTER						
I_{LIM}	P-type power switch peak current limit			1.5		A
		V_{IN}=3.6V, Open Loop Condition	1.3		1.7	A
f_{OSC}	Center switching frequency	Average Value		6		MHz
		V_{IN}=3.6V, Open Loop Condition	5.4		6.6	MHz
	Frequency Dithering			7		%
V_{RUN_H}	RUN pin logic high input threshold voltage		1.2			V
V_{RUN_L}	RUN pin logic low input threshold voltage				0.4	V

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
Gain	VCON to V_{OUT} gain			2.5		V/V
I_{VCON}	VCON pin leakage current				1	μA
T_{CON_TR}	V_{OUT} step rise time from 0.6V to 3.4V	VCON=0.24V to 1.36V, T_R=1μs, R_{LOAD}=10Ω			30	μs
	V_{OUT} step fall time from 3.4V to 0.6V	VCON=1.36V to 0.24V, T_F=1μs, R_{LOAD}=10Ω			30	μs
D_{MAX}	Maximum duty ratio		100			%
T_{ON}	Turn on time (time for output voltage to reach 95% final value after RUN low to high transition)	V_{RUN}=Low-to-High, V_{IN}=4.2V, V_{OUT}=3.4V, I_{OUT}<=1mA, C_{OUT}=4.7μF			55	μs
η	Efficiency	V_{OUT}=0.8V, I_{OUT}=10mA		75		%
		V_{OUT}=2V, I_{OUT}=200mA		89		%
		V_{IN}=3.9V, V_{OUT}=3.3V, I_{OUT}=500mA		93		%

TYPICAL CHARACTERISTICS

Table 1 TABLE OF FIGURES

$V_{IN}=V_{RUN}=3.6V$; TA=25°C, C_{IN} =10 µF, C_{OUT} = 4.7 µF and L=0.47 µH, unless otherwise noted.

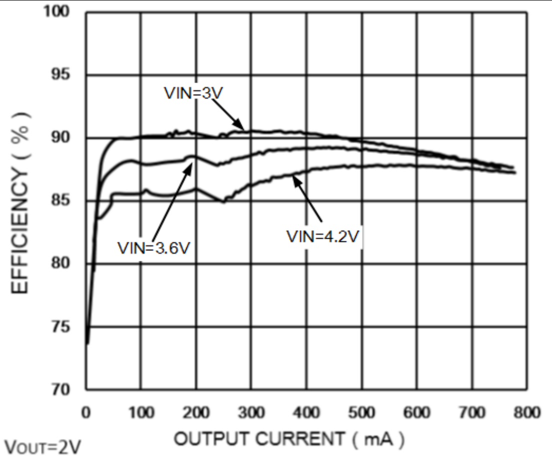


Figure 5 Efficiency vs Output Current VOUT=2V

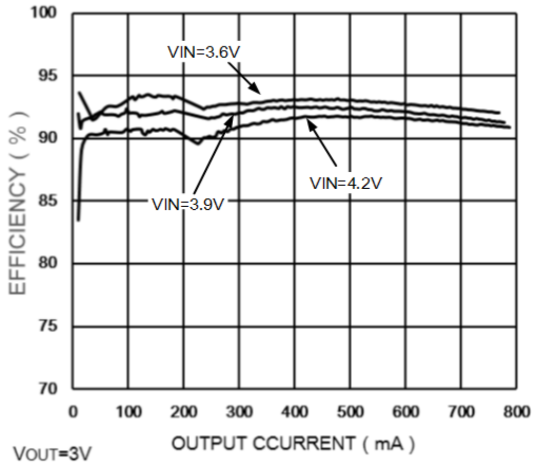


Figure 6 Efficiency vs Output Current VOUT=3V

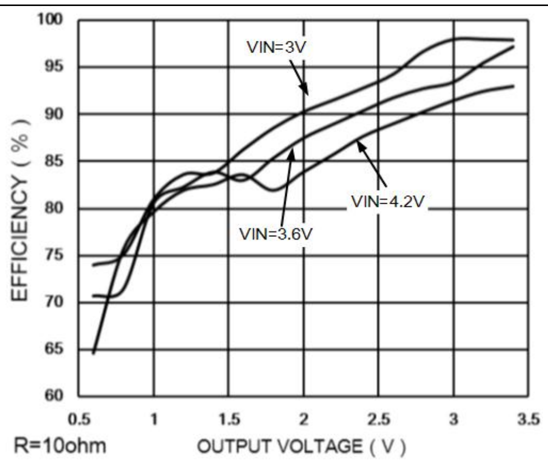


Figure 7 Efficiency vs Voltage

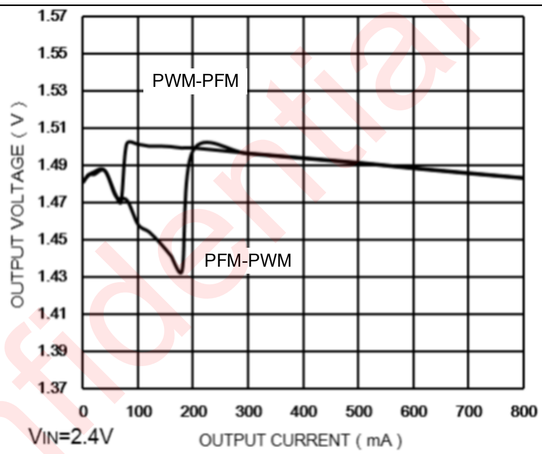


Figure 8 Output Voltage vs Output Current

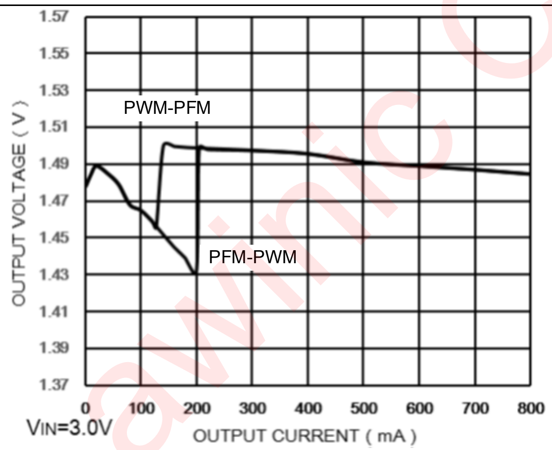


Figure 9 Output Voltage vs Output Current

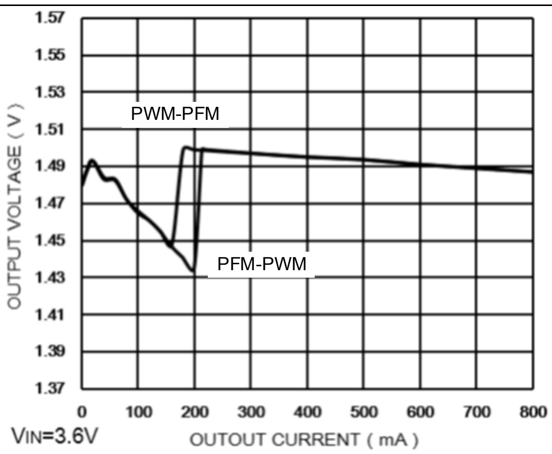


Figure 10 Output Voltage vs Output Current

V_{IN}=V_{RUN}=3.6V; TA=25°C, C_{IN} =10 µF, C_{OUT} = 4.7 µF and L=0.47 µH, unless otherwise noted.

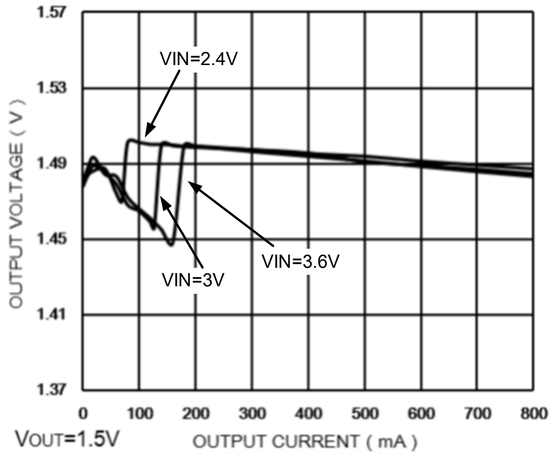


Figure 11 Output Voltage vs Output Current

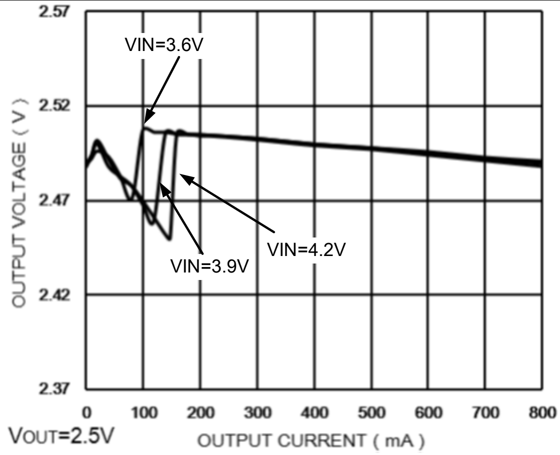


Figure 12 Output Voltage vs Output Current

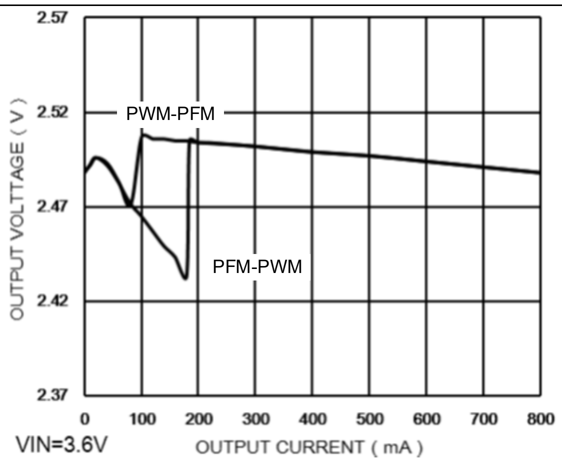


Figure 13 Output Voltage vs Output Current

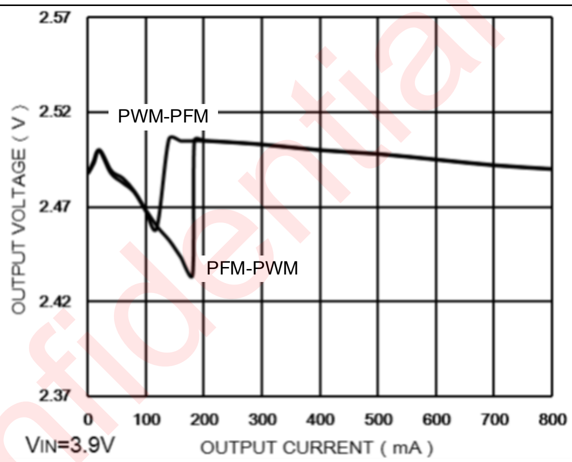


Figure 14 Output Voltage vs Output Current

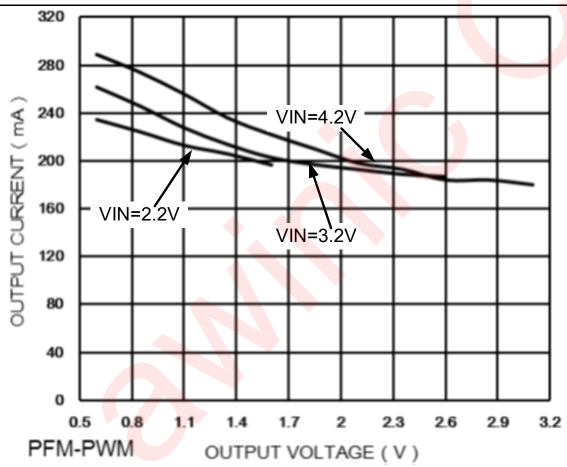


Figure 15 PFM-PWM Mode Threshold Voltage vs Output Voltage

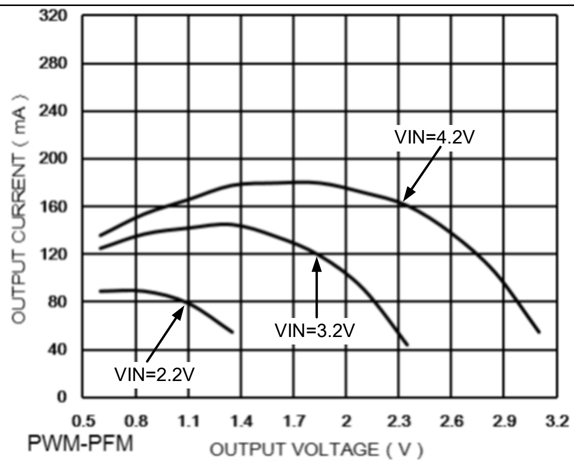


Figure 16 PWM-PFM Mode Threshold Voltage vs Output Voltage

V_{IN}=V_{RUN}=3.6V; TA=25°C, C_{IN} =10 μF, C_{OUT} = 4.7 μF and L=0.47 μH, unless otherwise noted.

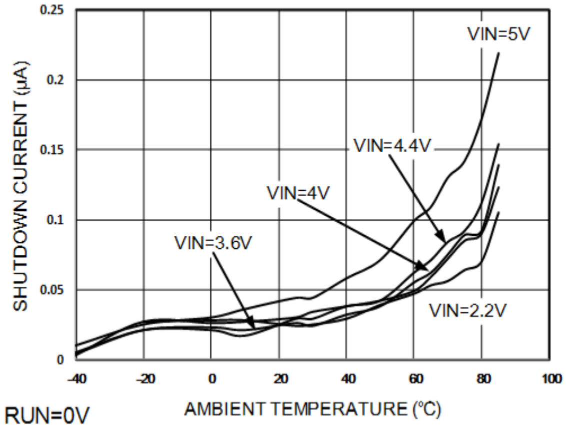


Figure 17 Shutdown Current vs Temperature

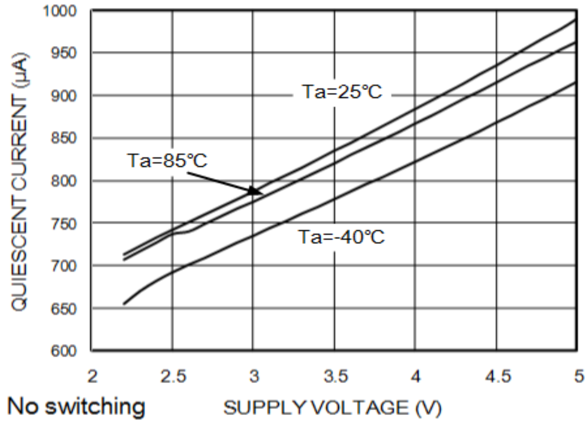


Figure 18 Quiescent Current vs Supply Voltage

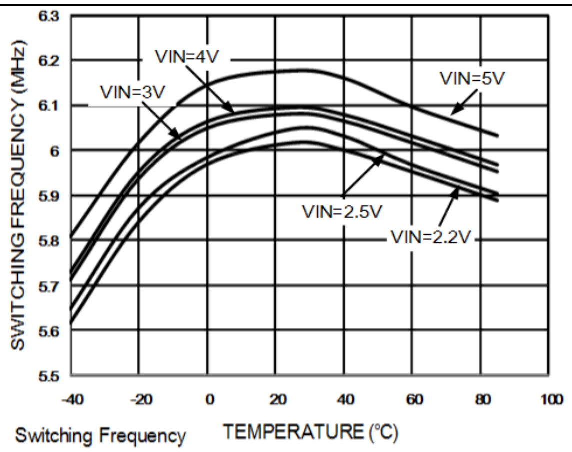


Figure 19 Switching Frequency vs Temperature

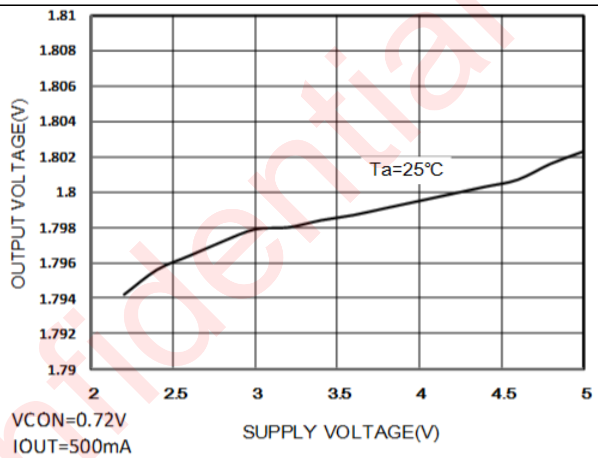


Figure 20 Output Voltage vs Supply Current

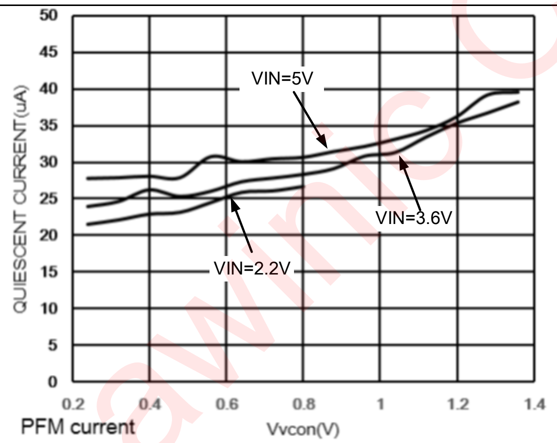


Figure 21 PFM Mode Quiescent Current

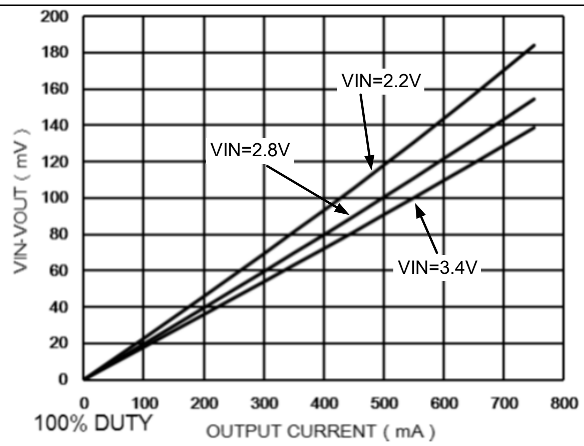
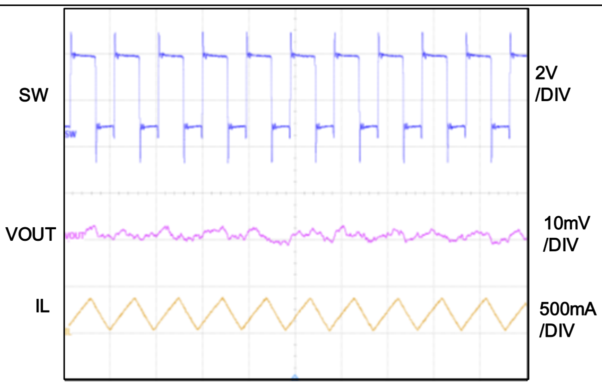


Figure 22 V_{IN}-V_{OUT} vs Output Current

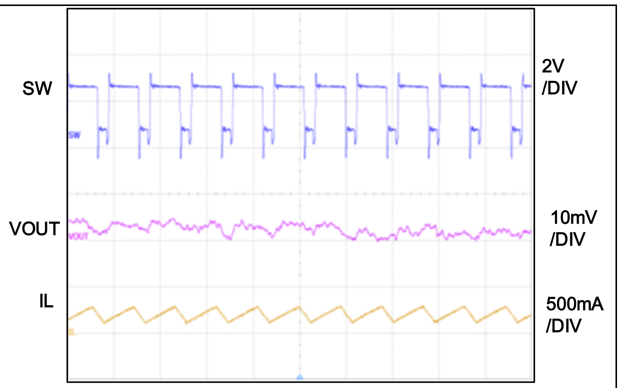
V_{IN}=V_{RUN}=3.6V; T_A=25°C, C_{IN} =10 µF, C_{OUT} = 4.7 µF and L=0.47 µH, unless otherwise noted.



200ns/DIV

VOUT=2V IOUT=200mA

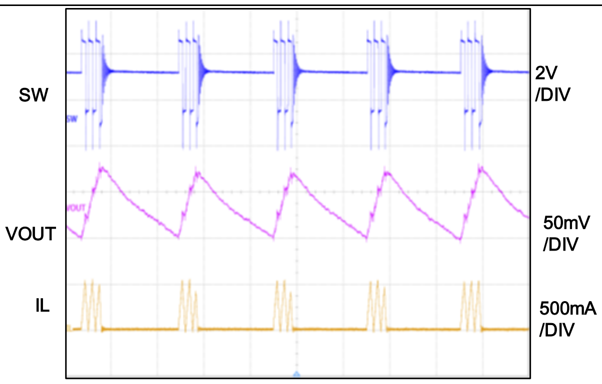
Figure 23 Output Voltage Ripple in PWM Mode



200ns/DIV

VIN=2.2V VOUT=1.5V IOUT=200mA

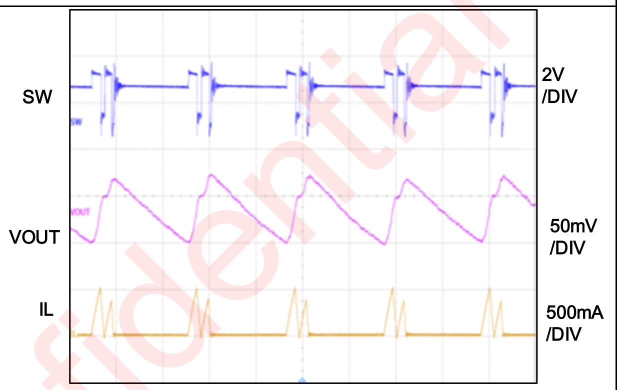
Figure 24 Output Voltage Ripple in PWM Mode



200ns/DIV

VOUT=2V IOUT=50mA

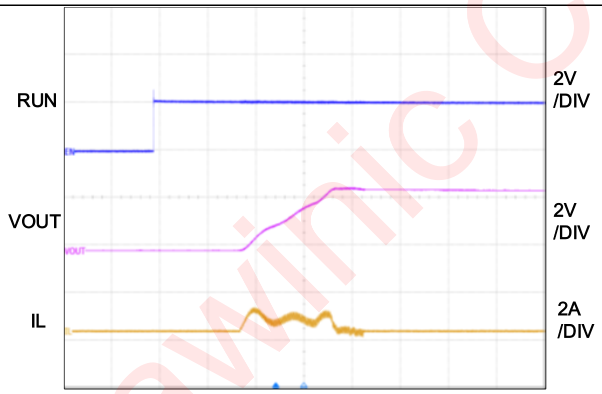
Figure 25 Output Voltage Ripple in PFM Mode



200ns/DIV

VIN=2.2V VOUT=1.5V IOUT=50mA

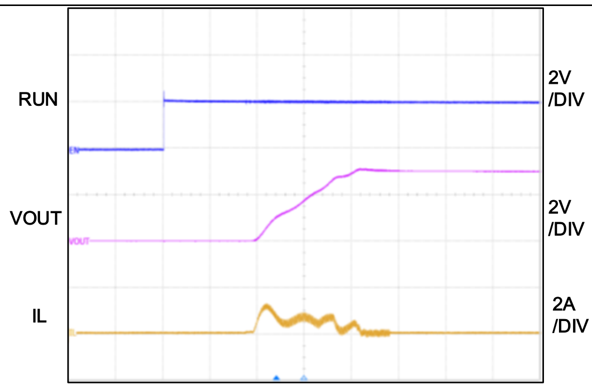
Figure 26 Output Voltage Ripple in PFM Mode



10µs/DIV

VIN=3.6V VOUT=2.5V R_{LOAD}=3.7 kΩ

Figure 27 Startup



10µs/DIV

VIN=4.2V VOUT=3V R_{LOAD}=3.7 kΩ

Figure 28 Startup

$V_{IN}=V_{RUN}=3.6V$; $T_A=25°C$, C_{IN} =10 µF, C_{OUT} = 4.7 µF and L=0.47 µH, unless otherwise noted.

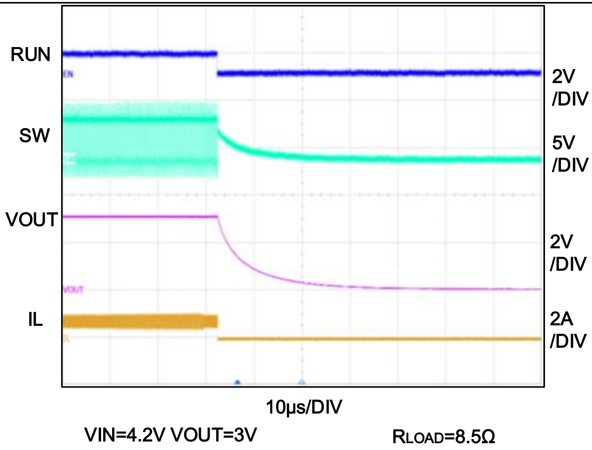


Figure 29 Shutdown

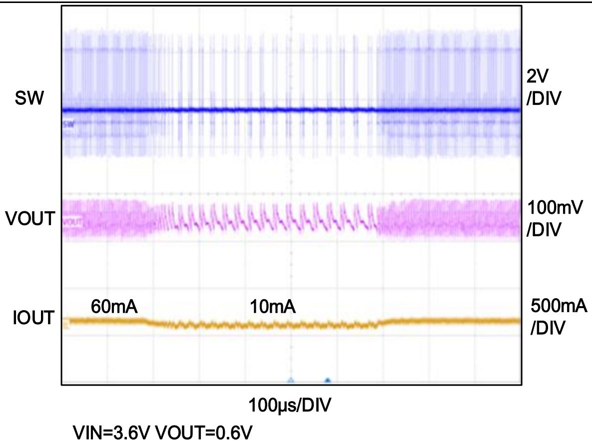


Figure 30 Load Transient Response

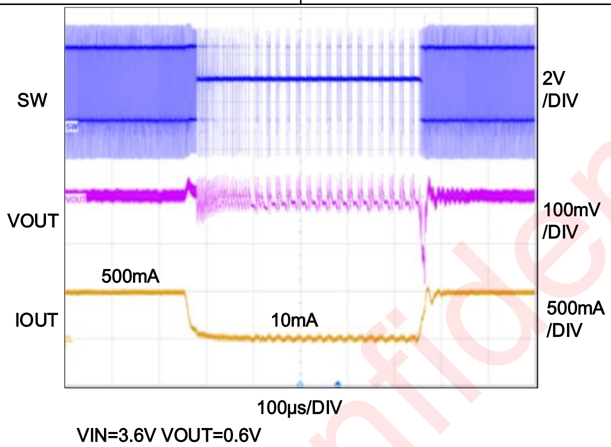


Figure 31 Load Transient Response

DETAILED FUNCTIONAL DESCRIPTION

The AW37416 is a single output step-down DC-DC converter suiting for powering RF power amplifiers in battery-powered portable RF devices. The AW37416 utilizes voltage-mode PWM control with synchronous rectification to provide maximum load current up to 750mA in high efficiency. The 6MHz switching frequency of AW37416 allows the utilization of small external components to reduce the size of the solutions. Maximum load range may vary from this depending on input voltage, output voltage, and the inductor chosen.

The AW37416 operates in three modes depending on load current demand: Pulse-Width-Modulation (PWM), Pulse-Frequency-Modulation (PFM) and Shutdown mode. In heavy load current condition, the AW37416 operates in PWM mode and automatically switches into PFM mode in light load condition. Shutdown mode turns off the device completely and reduces the current consumption to 0.1μA (typical).

Precision of the DC PWM-mode output voltage is ±3% for 3.4V. Efficiency is around 93%(typical) for a 500mA load with a 3.3V output and 3.9V input. The output voltage is dynamically programmable from 0.5V to 3.4V by adjusting the VCON pin voltage without the need of external feedback resistors. This feature extends battery life by capable of changing the power amplifier supply voltage dynamically depending on its transmitting power.

High-side power PFET cycle-by-cycle current limit protection, low-side power NFET cycle-by-cycle sinking current limit, short-circuit-protection and on-chip thermal protection are also available on the AW37416.

The AW37416 is available in 1.5mm X 1.0mm X 0.55mm 6-lead flip-chip package. This package provides the smallest size for space-critical applications, while 6MHz operating switching frequency reducing the size of external components, only three external power components are requires careful board design and precision assembly equipment. Use of this package is best suited for opaque-case applications, where its edges are not subject to high-intensity ambient red or infrared light. Also the system controller should set RUN low during power-up and other low supply voltage conditions.

FEATURE DESCRIPTION

CIRCUIT OPERATION

At the beginning of each switching cycle, the 6MHz clock pulses set the PWM latch to turn on the internal high-side P-type power FET switch. The current flows from the input node to the output capacitor and loading through the PFET switch. The inductor limits the current to a ramp with a slope $(V_{IN}-V_{OUT})/L$, by storing energy in a magnetic field. During the second part of each cycle, as the internal saw-tooth waveform voltage exceeds the output voltage of the error amplifier, the PWM comparator trips and resets the PWM latch to turn off the high-side PFET switch and to turn on the low-side NFET switch. As a result, the magnetic field of the inductor collapses, generating a voltage that forces the current from ground through the NFET switch to the output capacitor and load. The inductor current ramps down with a slope around V_{OUT}/L when the NFET switch is on.

By sending a duty-cycle modulated rectangular wave at SW to the inductor and output filter capacitor low-pass filter, the output voltage is regulated. The output voltage is equal to the average voltage at the SW pin.

BUCK DC-to-DC CONVERTER OPERATING

The AW37416 is a synchronous rectifier type buck converter with both high-side and low-side switches integrated on die. The AW37416 uses an internal NFET as a synchronous rectifier to reduce rectifier forward voltage drop and associated power loss. Synchronous rectification provides a significant improvement is efficiency whenever the output voltage is relatively low compared to the voltage drop across an ordinary rectifier diode.

In PWM operation, the NFET synchronous rectifier is turned on in the second part of each cycle and turned off prior to the next cycle. No external transistors and diodes are required.

The device operates in three modes: Shutdown mode (RUN=Low), PFM mode as operating at light load and PWM mode as operating at heavy load.

SHUTDOWN MODE

The AW37416 enters shutdown mode as the voltage at RUN pin below 0.4V or the input voltage below UVLO threshold voltage (1.8V). In shutdown mode, the typical current consumption of the whole chip is 0.1μA. Putting the voltage at the RUN pin above 1.2V will enable the device.

PWM MODE OPERATION

In heavy load condition, the AW37416 operates in PWM mode from a fixed clock (6MHz). In PWM mode operation, the converter operates as a voltage-mode controller. The voltage mode PWM control allows the converter to achieve excellent load and line regulation. The output voltage is regulated by switching at a constant frequency and then modulating the energy per cycle to control power to the load. At the beginning of each clock cycle the PFET switch is on and the inductor current ramps up until the comparator trips and the control logic turns off the switch. Then the NFET switch is turned on and the inductor current ramps down. The next cycle is initialed by the clock turning off the NFET switch and turning on the PFET switch.

PFM MODE OPERATION

At light load condition, the AW37416 enters the PFM mode operation to save power and improve efficiency. During PFM mode operation, the AW37416 works in the peak-current-control, the inductor peak current is limited to 500mA. The output voltage is regulated by varying the switching frequency, proportional to loading current.

INDUCTOR PEAK CURRENT LIMITATIONS

During PWM mode operation, peak inductor current is monitored and limited by the AW37416 current limiting circuitry. In PWM mode, the cycle-by-cycle current limit is 1500mA.

SHORT-CIRCUIT PROTECTION

If an excessive load pulls the output voltage below 0.3V, AW37416 disables the NFET, and the cycle-by-cycle current limit is reduced to 500mA. When the output voltage becomes less than 0.15V(typical), the switching frequency decreases to 3MHz to protecting the part from excess current and thermal stress damages.

DYNAMICALLY ADJUSTABLE OUTPUT VOLTAGE

To eliminate the need for external feedback resistors, the output voltage can be set from 0.5V to 3.4V by changing the voltage on the VCON pin. In PA applications where peak power is needed only when the handset is far away from the base station or when data is being transmitted. Therefore the supply power to the PA can be controlled by adjusting the voltage at VCON, to optimizing the battery life.

The AW37416 moves into Pulse-Skipping mode when the duty cycle ratio is up to approximately 88% or less than approximately 15%. The output voltage ripple increases slightly.

THERMAL PROTECTION

The thermal capability of IC can be exceeded due to buck converter output stage power level, therefore a thermal protection circuitry is implemented to prevent device from thermal damage. When the junction temperature exceeds around 150°C, the output rectifier stops switching, both PFET and NFET off. The AW37416 resumes switching as the junction temperature drops below 125°C.

SOFT-START

The AW37416 features a soft-start circuit to limit in-rush current during start-up. During start-up, the duty ratio of the SW voltage waveform is increased slowly until the output voltage reaches the setting value. Soft-start is activated if RUN pin voltage goes from low to high after V_{IN} reaches 2V.

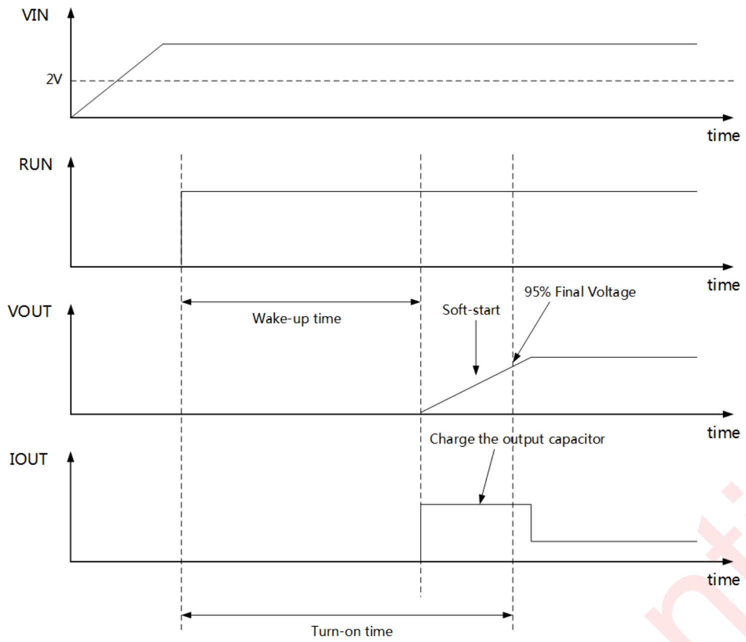
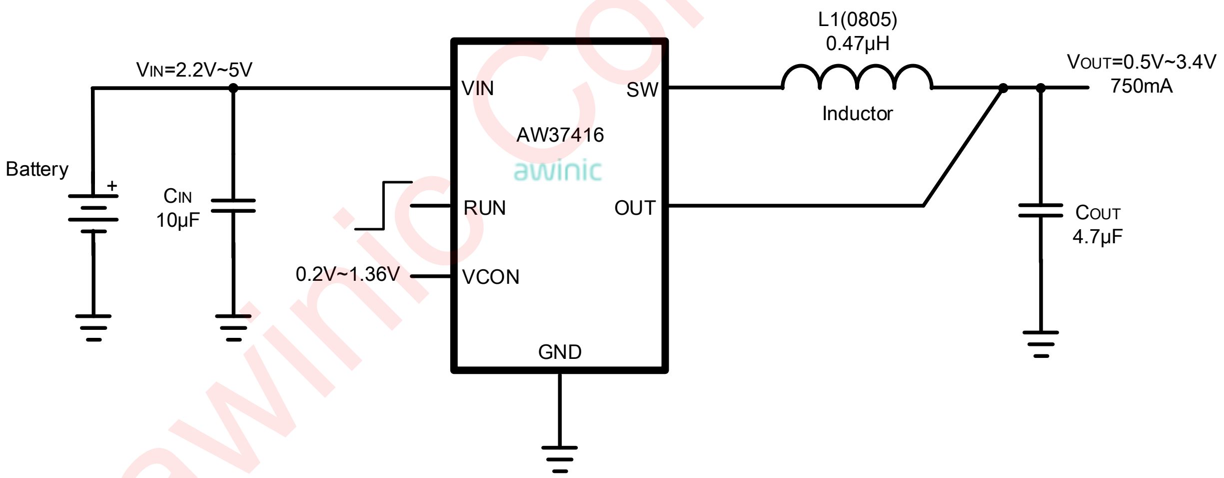


Figure 32 Power On Sequence

APPLICATION INFORMATION

TYPICAL APPLICATION



INDUCTOR SELECTION

Two main considerations must be considered when choosing an inductor: the inductor should not saturate and the inductor current ripple should be small enough to achieve the desired output voltage ripple.

The minimum value of inductance to ensure good performance is 0.3μH at bias current over the ambient temperature range. Shielding inductors radiates less noise and should be preferred.

The saturation current should be greater than the sum of the maximum load current and the worst case average to peak inductor current.

$$I_{SAT} > I_{OUT\_MAX} + I_{RIPPLE}$$

Where

- I_{OUT_MAX} is the maximum load current (750mA)
- I_{RIPPLE} is the average-to-peak inductor current.

$$I_{RIPPLE} = \frac{V_{IN} - V_{OUT}}{2L} \times \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f}$$

Where

- V_{IN} is the maximum input voltage in application.
- V_{OUT} is the output voltage
- L is the minimum inductor value including worst-case tolerances (30% drop can be considered)
- f is the minimum switching frequency

A more conservative and recommended approach is to choose an inductor that can support the maximum current limit of 1500mA.

CAPACITORS SELECTION

The AW37416 is designed for use with ceramic capacitors for its input and output filters. Use a 10μF ceramic capacitor for the input bypass filter and a 4.7μF ceramic for the output. The effective output capacitance should remain at least 3μF at DC bias and temperature conditions for stability reason. 25V of rated-voltage ceramic capacitors are suitable for full range output voltage applications. Ceramic capacitors type such as X5R, X7R, and B are recommended for both filters. These types provide optimal balance between small size, cost, reliability, and performance for cell phones and similar applications.

The output filter capacitor absorbs the voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low equivalent series resistance (ESR) to perform these functions. The ESR of the filter capacitors is generally a major factor in voltage ripple. The output capacitor selection is determined by output voltage ripple and load transient response requirement. For high transient load performance high output capacitor value must be use. For a given peak-to-peak ripple current I_{LPP} in the inductor od the output filter, the output ripple across the output capacitor is the sum of three components as below.

$$V_{OUTPP} = V_{OUTPP©} + V_{OUTPP(ESR)} + V_{OUTPP(ESL)}$$

Where

- $V_{OUTPP©}$ is the ripple component coming from an equivalent total capacitance of the output capacitors.
- $V_{OUTPP(ESR)}$ is a ripple component from an equivalent ESR of the output capacitors.
- $V_{OUTPP(ESL)}$ is a ripple component from an equivalent ESL of the output capacitors.

In PWM operation mode, the three ripple components can be obtained by

$$V_{OUTPP(C)} = \frac{f_{L\_PP}}{8 \times C \times f_{SW}}$$

$$V_{OUTPP(ESR)}=I_{LPP}\ x\ ESR$$

$$V_{OUTPP(ESL)}=\frac{ESL}{ESL+L}\ x\ V_{IN}$$

And the peak-to-peak ripple current is:

$$I_{LPP}=\frac{(PV_{IN}-V_{OUT})\ x\ V_{OUT}}{PV_{IN}\ x\ F_{SW}\ x\ L}$$

In applications with all ceramic output capacitors, the main ripple component of the output ripple is $V_{OUTPP©}$. So that the minimum output capacitance can be calculated regarding to a given output ripple requirement V_{OUTPP} in PWM operation mode.

$$C_{MIN}=\frac{I_{LPP}}{8\ x\ V_{OUTPP}\ x\ f_{SW}}$$

DC bias characteristics of the capacitors must be considered when selecting the voltage rating and case size of the capacitor. For C_{IN}, use of an 0805(2012) size nay also be considered if room is available on the system board.

The input filter capacitor supplies AC current drawn by the PFET switch of the AW37416 in the first part of each cycle and reduce the voltage ripple imposed on the input power source. One of the input capacitor selection guides is the input voltage ripple requirement. To minimize the input voltage ripple and get better decoupling in the input power supply rail. Ceramic capacitor is recommended due to low ESR and ESL. The minimum input capacitance regarding the input ripple voltage V_{INPP} is

$$C_{INMIN}=\frac{I_{LPP}\ x\ (D-D^2)}{V_{INPP}\ x\ f_{SW}}$$

Where $D=V_{OUT}/V_{IN}$.

In addition the input capacitor needs to be able to absorb the input current, which has a RMS value of:

$$I_{INRMS}=I_{OUTMAX}\ x\sqrt{(D-D^2)}$$

The input capacitor needs also to be sufficient to protect the device from over voltage spike and a minimum of 4.7μF capacitor is required. The input capacitor should be located as close as possible to the IC. PGND is connected to the ground terminal of the input cap which then connects to the ground plane. The PV_{IN} is connected to the V_{BAT} terminal of the input capacitor which then connects to the V_{BAT} plane.

RECOMMENDED COMPONENTS LIST

Component	PART No.	DESCRIPTION	MFR	TYP.	UNIT
L_1	MIPSZ2012D0R5	2.0×1.2×1.0 (mm^3)	FDK	0.47	μH
	LQM21PNR54MG0	2.0×1.25×0.9 (mm^3)	Murata	0.47	μH
	LQM2MPNR47NG0	2.0×1.6×0.9 (mm^3)	Murata	0.47	μH
	TFM201610A-R47M-T00	2.0x1.6x1 (mm^3)	TDK	0.47	μH
	TFM201210A-R47M-T00	2.0x1.2x1 (mm^3)	TDK	0.47	μH
	DFE201610R-R47M-T00	2.0x1.6x1 (mm^3)	Toko	0.47	μH
	DFE201610R-R47M-T00	2.0x1.6x1 (mm^3)	Toko	0.47	μH
C_{OUT}	C1608X5R0J475M080AC	6.3V, X5R, 0603	TDK	4.7	μF
	C1005X5R0J475M050BC	6.3V, X5R, 0402	TDK	4.7	μF
	CL05A475MQ5NRNC	6.3V, X5R, 0402	Samsung	4.7	μF
	C1608X5R1E475M080AC	25V, X5R, 0603	TDK	4.7	μF
	GRM188R61E475KE11D	25V, X5R, 0603	Murata	4.7	μF
C_{IN}	C1608X5R0J106M	6.3V, X5R, 0603	TDK	10	μF
	CL05A106MQ5NUNC	6.3V, X5R, 0402	Samsung	10	μF
	GRM188R60J106ME47D	6.3V, X5R, 0603	Murata	10	μF

PCB LAYOUT CONSIDERATION

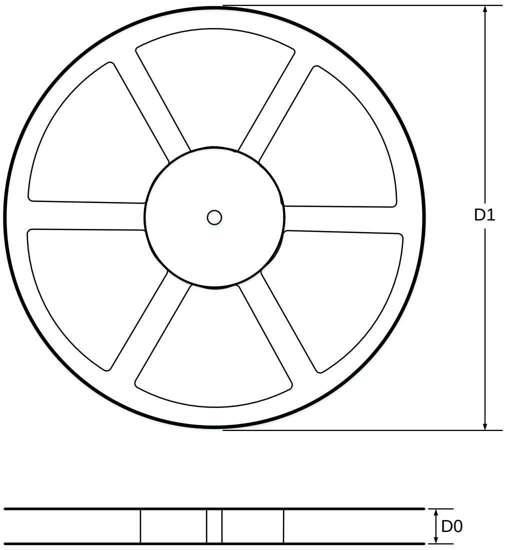
Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces, resulting in poor regulation or instability. To obtain the optimal performance, PCB layout should be considered carefully. Some guidelines:

1. The V_{IN} and GND traces are especially recommended to be as wide as possible. The important criterion is symmetry to ensure the solder leads reflow evenly.
2. Place the AW37416, the inductor, and filter capacitors close together and make the trace short. The traces between these components carry relatively high switching current and act as antennae. Following this rule reduces radiated noise.
3. Place the input filter capacitor close to the VIN and GND pads.
4. Arrange the components so that the switching current loops curl in the same direction. During the first half of each cycle, current flows from the input filter capacitor, through the AW37416 and inductor to the output filter capacitor and back through ground, forming a current loop. In the second of each cycle, current is pulled up from ground, forming a second current loop. Routing these loops so the current curls in the same direction prevents magnetic field reversal between the two half-cycles and reduces radiated noise.
5. Connect the ground pads of the AW37416 and filter capacitors together using generous component-side copper fill as a pseudo-ground plane. Then connect this to the ground-plane with several VIAs. This connection reduces ground-plane noise by preventing the switching currents from circulating through the ground plane. It also reduces ground bounce at the AW37416 by giving it a low impedance ground connection.

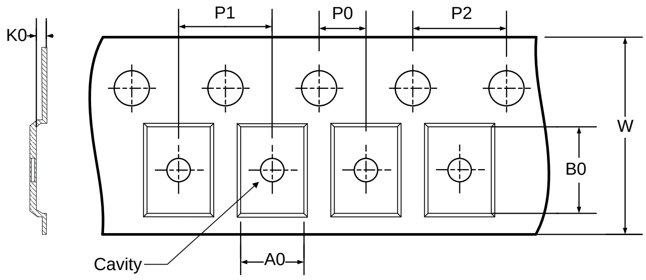
6. Use side traces between the power components and for power connections to the DC-DC converter circuit which reduces voltage errors caused resistive losses across the traces.
7. Route noise sensitive traces such as the voltage feedback path away from noisy traces between the power components. The output voltage feedback point should be taken approximately 1.5nH away from the output capacitor. The feedback trace also should be routed opposite to noise components. The voltage feedback trace must remain close to the AW37416 circuit and should be routed directly from OUT to VOUT at the inductor and should be routed opposite to noise components. This trace placement allows fast feedback and reduces EMI radiated onto the voltage feedback trace of the DC-DC converter.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

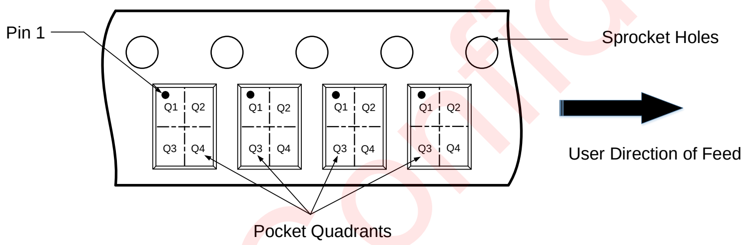


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

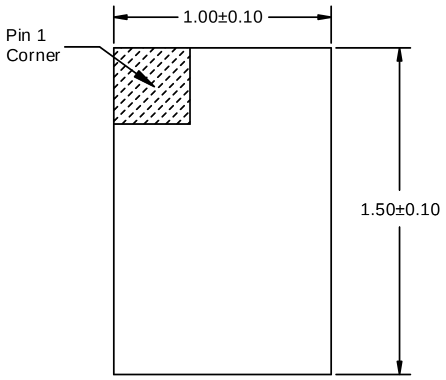
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



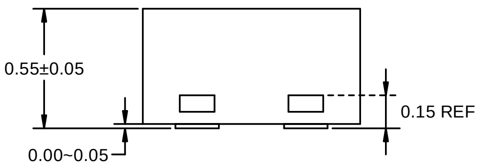
All Dimensions are nominal

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.4	1.12	1.72	0.7	2	4	4	8	Q1

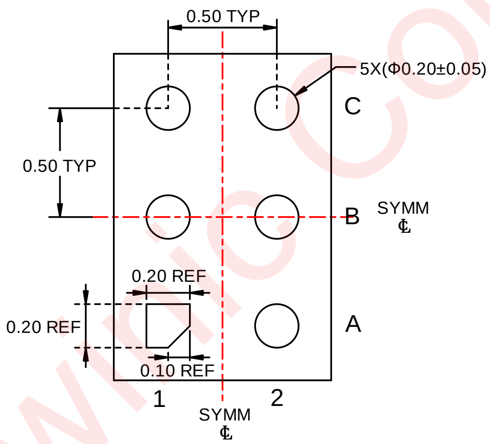
PACKAGE DESCRIPTION



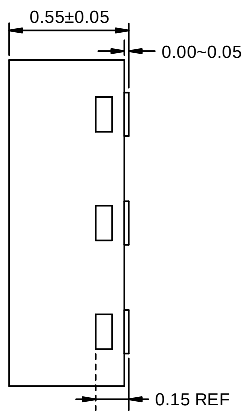
Top View



Side View



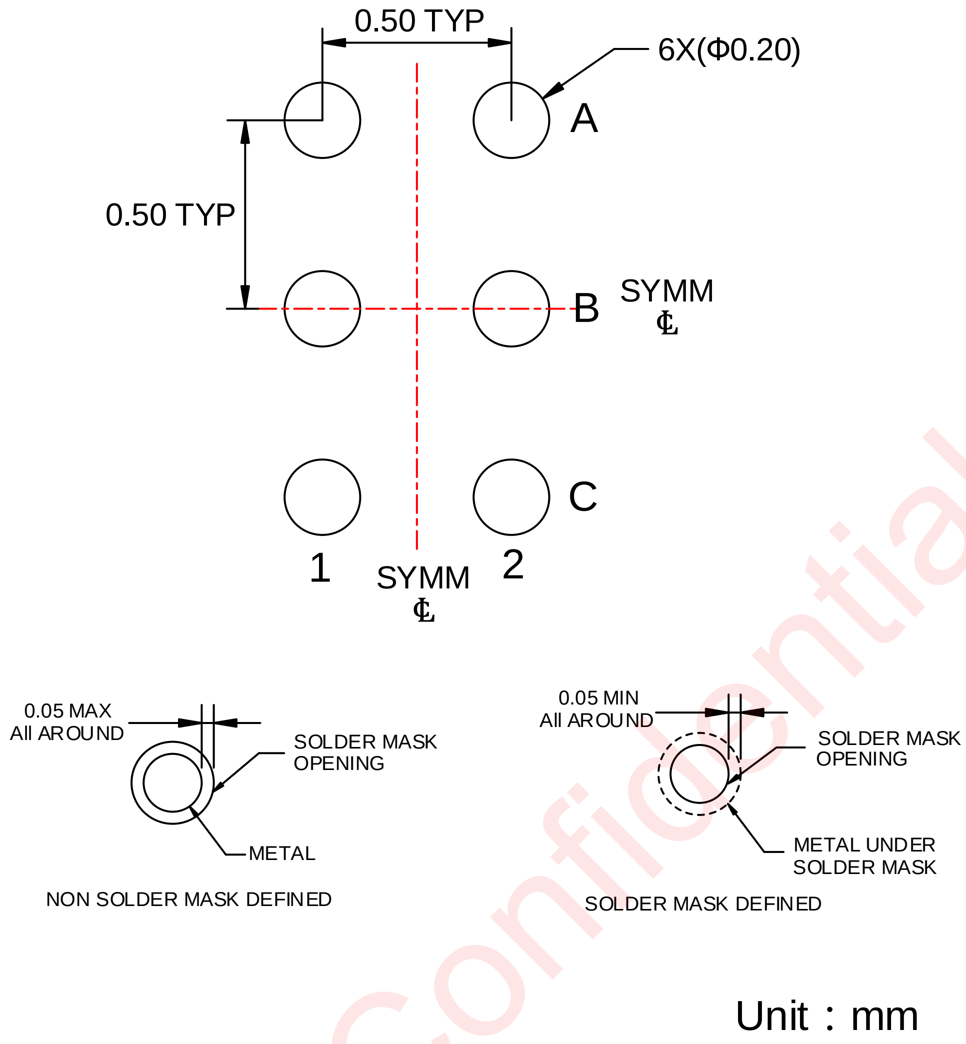
Bottom View



Side View

Unit：mm

LAND PATTERN DATA



REVISION HISTORY

Version	Date	Change Record
V1.0	Jan 2019	Officially Released
V1.1	Mar 2019	Add figure 17,18,19 and 20 in TYPICAL CHARACTERISTICS
V1.2	Jun 2019	1. Modify V_{OUT}=0.6V~3.4V to V_{OUT}=0.5V~3.4V in TYPICAL APPLICATION diagram 2. Modify fond type of Lead Temperature (Soldering 10 Seconds) to Arial in ABSOLUTE MAXIMUM RATINGS 3. Add descriptions in CAPACITORS SELECTION 4. Add more C_{IN} and C_{OUT} in RECOMMENDED COMPONENTS LIST
V1.3	Dec 2019	Modify the Junction-to-ambient Thermal Resistance θ_{JA}

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