Low-power Low-voltage and Rail-to-Rail Operational Amplifier

Features

- Wide Supply Voltage Range:1.8V ~ 5.5V
- Low Input Offset Voltage: ±0.4mV
- Slew Rate: 2V/μs
- Low Input Bias Current: 1pA
- Low Broadband Noise: 25nV/$\sqrt{\text{Hz}}$
- Low Quiescent Current: 66μA
- Rail-to-Rail Input and Output
- Bandwidth: 1MHz
- Small Package for Low-Cost Applications
- Sink and Source Current Capability: 44mA

Applications

- Smart Phones, Tablet PCs
- Mobile Internet Devices
- Headsets/Headphones/Earbuds
- Personal/Portable Electronics
- Motion Detectors/Smoke Detectors
- Active Filters
- Low-Side Current Sensing
- Pressure Transmitter
- Process Analytics(Gas, Force, Humidity & PH)

General Description

The AWS90001 is a high precision, micro-power, low-voltage (1.8V to 5.5V) operational amplifier with rail-to-rail input and output swing capabilities, which makes it ideal to general-purpose applications. This op amp features very good AC performance with a gain-bandwidth product of 1MHz, slew rate of 2V/μs and low input voltage noise of 2.2μVpp, while drawing 66μA (typical) of quiescent current. It has an input common-mode voltage range that extends to each supply rail, and its outputs swing to within 60mV of the supply rails with a 2kΩ load.

The AWS90001 provides an appropriate solution for space-constrained applications such as battery powered IoT devices, wearable electronics, and personal electronics where minimum PCB footprint is required. The AWS90001 is available in green small-size DFN - 5L package and SOT 23 - 5L package.

Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
AWS90001	DFN - 5L	0.8mm × 0.8mm
	SOT 23 - 5L	1.626mm × 2.926mm

Typical Application Circuit

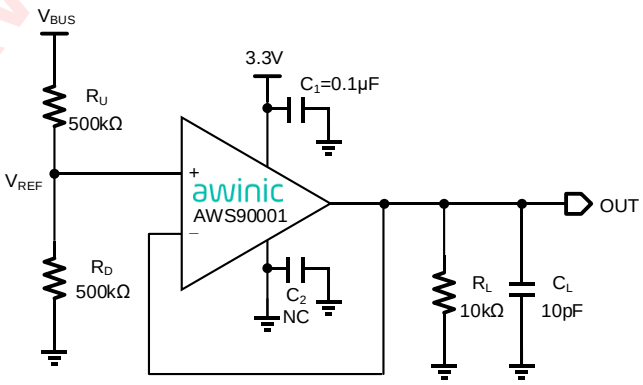
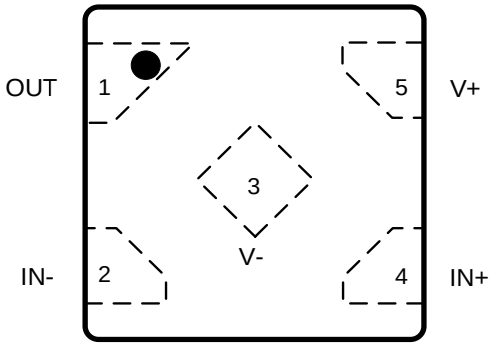


Figure 1 Typical Application of AWS90001

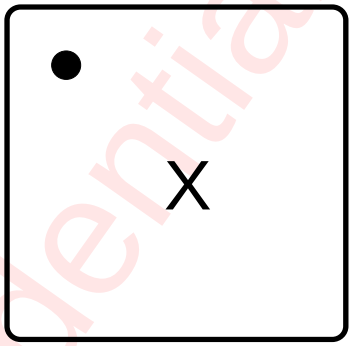
Pin Configuration And Top Mark

DFN - 5L

AWS90001DNR
(Top View)



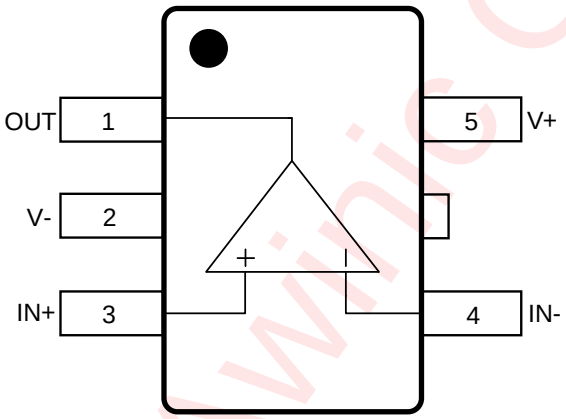
AWS90001DNR
Marking
(Top View)



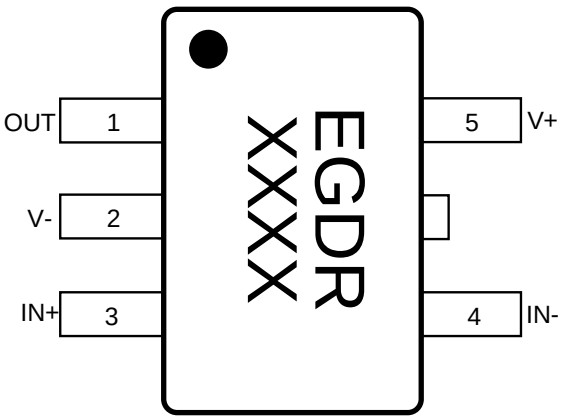
X – Production Tracing Code

SOT 23 - 5L

AWS90001STR
(Top View)

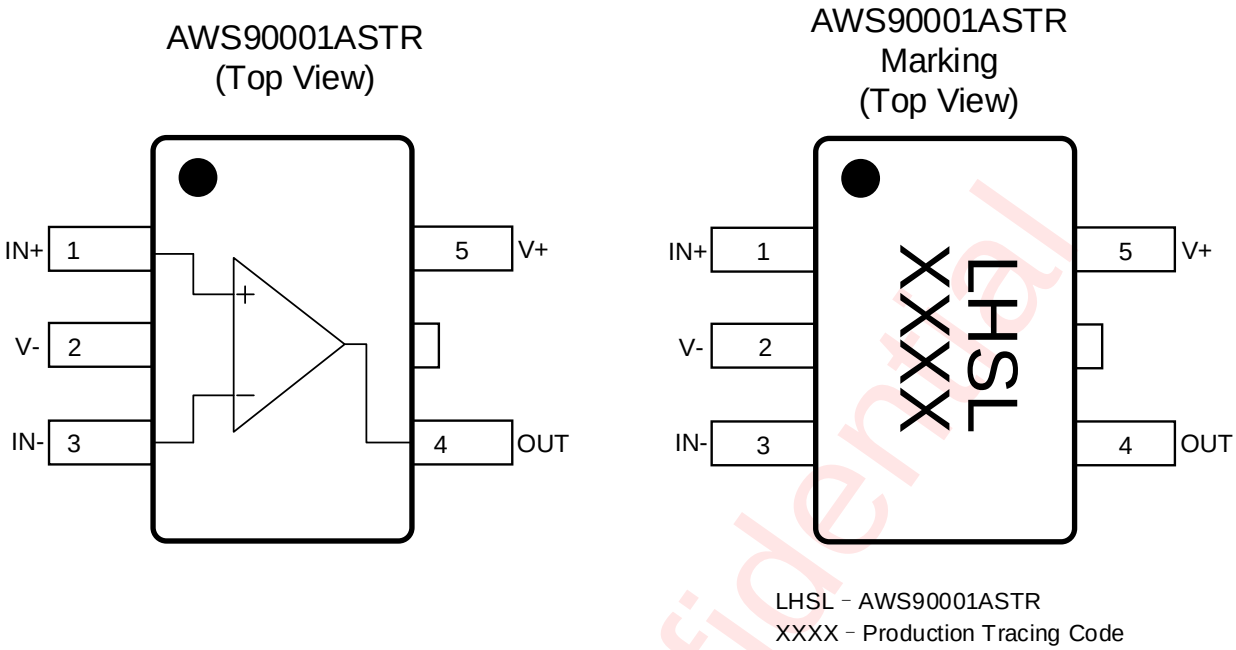


AWS90001STR
Marking
(Top View)



EGDR – AWS90001STR
XXXX – Production Tracing Code

SOT 23 - 5L



LHSL – AWS90001ASTR
XXXX – Production Tracing Code

Figure 2 Pin Configuration

Pin Definition

PIN				DESCRIPTION
NAME	DFN-5L DNR	SOT23-5L STR	SOT23-5L ASTR	
OUT	1	1	4	Output
IN-	2	4	3	Inverting input
V-	3	2	2	Negative (low) supply or ground (for single-supply operation)
IN+	4	3	1	Noninverting input
V+	5	5	5	Positive (high) supply

Functional Block Diagram

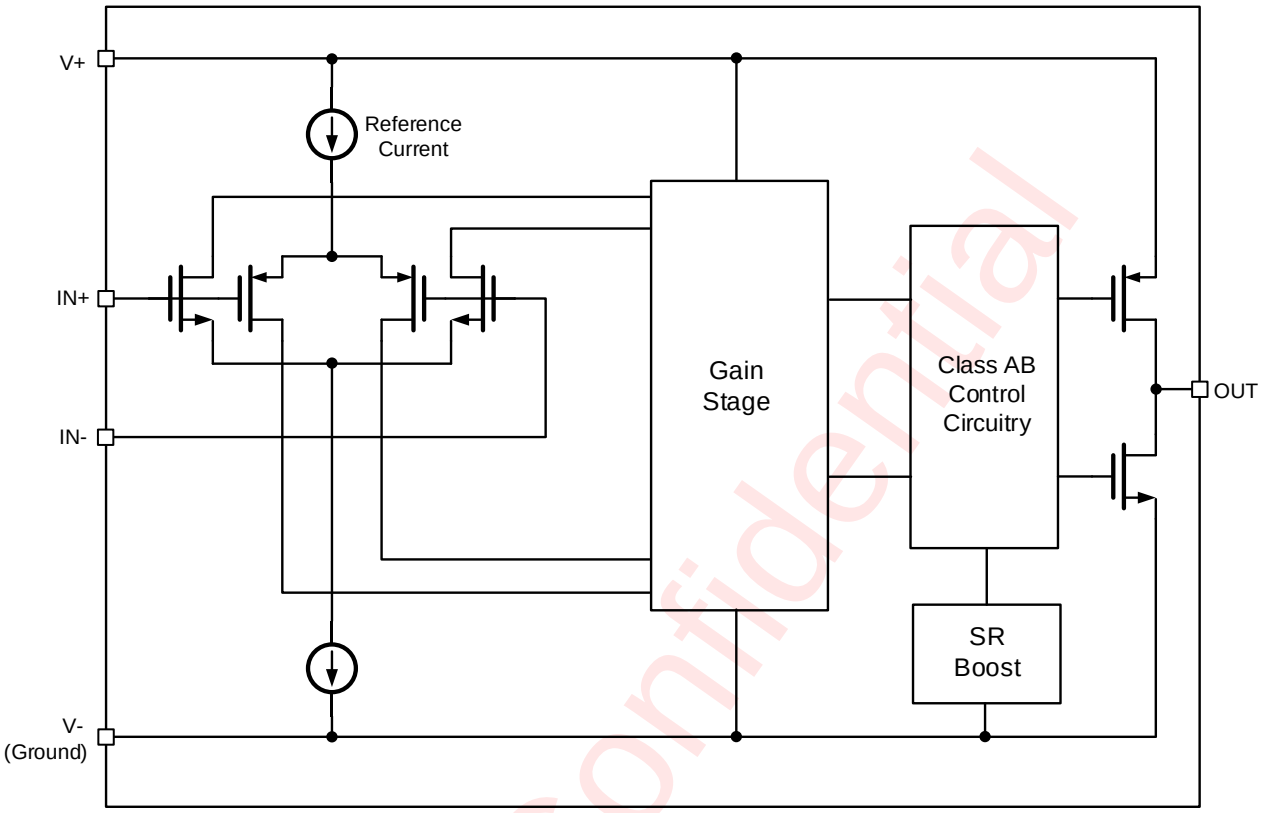


Figure 3 Functional Block Diagram

Typical Application Circuits

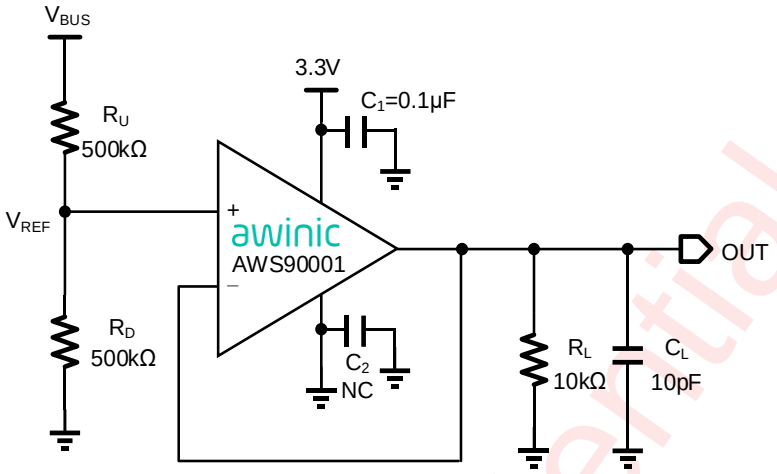


Figure 4 AWS90001 Application Circuit

Notice for typical application circuits:

1. Bypass capacitors C_1/C_2 are used to reduce the coupled noise by providing a low-impedance path to ground. So low-ESR, 0.1μF ceramic bypass capacitors are necessary between each supply pin and ground, placed close to the device, but far away from input traces. If negative supply is connected to GND, then negative supply to GND can be disconnected to bypass ceramic.

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AWS90001DNR	-40°C ~ 125°C	DFN - 5L		MSL1	RoHS+HF	9000 units/ Tape and Reel
AWS90001STR	-40°C ~ 125°C	SOT 23 - 5L	EGDR	MSL3	RoHS+HF	3000 units/ Tape and Reel
AWS90001ASTR	-40°C ~ 125°C	SOT 23 - 5L	LHSL	MSL3	RoHS+HF	3000 units/ Tape and Reel

Absolute Maximum Ratings (NOTE1)

PARAMETERS		RANGE
Supply voltage, V_S = (V+) - (V-)		-0.3V to 6.0V
Signal input pins	Common-mode voltage (NOTE 2)	(V-) - 0.5V to (V+) + 0.5V
	Differential voltage (NOTE 2)	-6.0V to 6.0V
	Current (NOTE 2)	-10mA to 10mA
Output short-circuit (NOTE 3)		Continuous
Operating free-air temperature range T_A		-40°C to 125°C
Maximum operating junction temperature T_{JMAX}		150°C
Storage temperature T_{STG}		-65°C to 150°C
Lead temperature (soldering 10 seconds)		260°C

NOTE1: *Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.*

NOTE2: *Input pins are diode-clamped to each power supply. Input signals that may extend more than 0.5V beyond the supply rails must be current limited to 10mA or less.*

NOTE3: *A heat sink may be required to keep the junction temperature below the absolute maximum.*

ESD Rating and Latch Up

PARAMETERS	VALUE	UNIT
HBM (Human Body Model) (NOTE 4)	±4	kV
CDM (NOTE 5)	±1.5	kV
Latch-Up (NOTE 6)	+IT: 400 -IT: -400	mA

NOTE4: *The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2017*

NOTE5: Test method: ESDA/JEDEC JS-002-2018

NOTE6: Test method: JESD78F

Thermal Information

THERMAL METRICS		AWS90001		UNIT
		DFN	SOT	
SYMBOL	PARAMETER	5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	421.2	228.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	90.5	86.4	°C/W
$R_{\theta JC}$	Junction-to-case (top) thermal resistance	146.5	160.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	89.3	51.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	96.9	72.3	°C/W

Electrical Characteristics

Unless otherwise noted, V_S = (V+) - (V-) = 1.8V to 5.5V (±0.9V to ±2.75V), R_L = 10kΩ connected to V_S/2, V_{CM} = V_S/2, and V_{OUT} = V_S/2, typical values are at V_S = 5V and T_A = 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_S = 5V	-1.6	±0.4	1.6	mV
		V_S = 5V, T_A = -40°C to 125°C	-2.5		2.5	
dV_{OS}/dT	Input offset voltage drift	T_A = -40°C to 125°C		±1		μV/°C
PSRR	Power-supply rejection ratio	V_S =1.8V to 5.5V, V_{CM} = V-	80	102		dB
INPUT BIAS CURRENT						
I_B	Input bias current	V_{CM} = V_S/2	-100	±1	100	pA
I_{OS}	Input offset current		-100	±1	100	pA
NOISE						
E_N	Input voltage noise (peak-to-peak)	f = 0.1Hz to 10Hz, V_S = 5V		2.2		μV_{PP}
e_N	Input voltage noise density	f = 1kHz, V_S = 5V		30		$nV/\sqrt{Hz}$
		f = 10kHz, V_S = 5V		25		
i_N (1)	Input current noise density	f = 1kHz, V_S = 5V		6		$fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range	No phase reversal, rail-to-rail input	(V-) -0.1		(V+) +0.1	V
CMRR	Common-mode rejection ratio	(V-) - 0.1V < V_{CM} < (V+) - 1.4V, V_S = 1.8V	75	97		dB
		(V-) - 0.1V < V_{CM} < (V+) - 1.4V, V_S = 5.5V	80	103		
		(V-) - 0.1V < V_{CM} < (V+) + 0.1V, V_S = 5.5V	63	84		
		(V-) - 0.1V < V_{CM} < (V+) + 0.1V, V_S = 1.8V	55	75		
INPUT CAPACITANCE						
C_{ID} (1)	Differential Mode			1		pF
C_{IC}	Common Mode			3		
POWER SUPPLY						
V_S	Specified voltage range		1.8 (±0.9)		5.5 (±2.75)	V

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
I_Q	Quiescent current	V_S = 5.5V	40	66	85	μA
		V_S = 5.5V, T_A = -40°C to 125°C			95	
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	V_S = 5.5V, R_L = 10kΩ, (V-) + 0.05 V < V_O < (V+) – 0.05V	85	126		dB
		V_S = 1.8 V, R_L = 10kΩ, (V-) + 0.06 V < V_O < (V+) – 0.06V	63	109		dB
		V_S = 1.8V, R_L = 2kΩ, (V-) + 0.1 V < V_O < (V+) – 0.1V	80	113		dB
		V_S = 5.5V, R_L = 2kΩ, (V-) + 0.15V < V_O < (V+) – 0.15V	85	130		dB
FREQUENCY RESPONSE CHARACTERISTICS						
GBP	Gain-bandwidth product	V_S = 5V		1		MHz
φ_m	Phase margin	V_S = 5V, G = +1		60		°
SR	Slew rate	V_S = 5.5V	1.3	2		V/μs
t_S	Settling time	To 0.1%, V_S = 5V, V_{STEP} = 2V, G = +1, C_L = 100pF		2		μs
		To 0.01%, V_S = 5V, V_{STEP} = 2V, G = +1, C_L = 100pF (1)		5		
THD+N	Total harmonic distortion + noise	V_S = 5.5V, V_{CM} = 2.5V, V_O = 1V_{RMS}, G = +1, f = 1kHz, 80kHz measurement BW		0.004		%
t_{OR}	Overload recovery time	V_S = 5V, V_{IN} × gain > V_S		0.65		μs
OUTPUT CHARACTERISTICS						
V_O	Voltage output swing from supply rails	V_S = 5.5V, R_L = 10kΩ		7	20	mV
		V_S = 5.5V, R_L = 2kΩ		35	60	
I_{SC}	Short-circuit current	V_S = 5.5V	28	44	53	mA

(1) The values are guaranteed by design.

Typical Characteristics

At T_A = 25°C, V+ = 2.75V, V- = -2.75V, V_{CM} = V_S/2, and V_{OUT} = V_S/2, R_L = 10kΩ connected to V_S/2 unless otherwise noted.

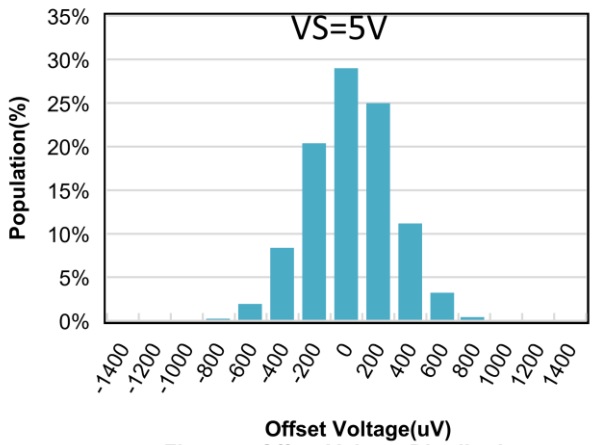


Figure 5 Offset Voltage Distribution

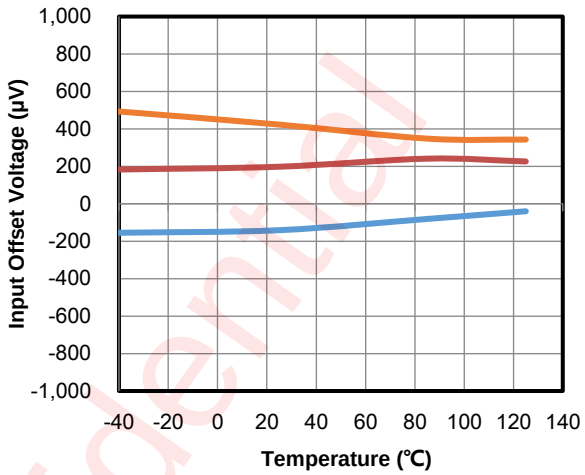


Figure 6 Input Offset Voltage vs. Temperature

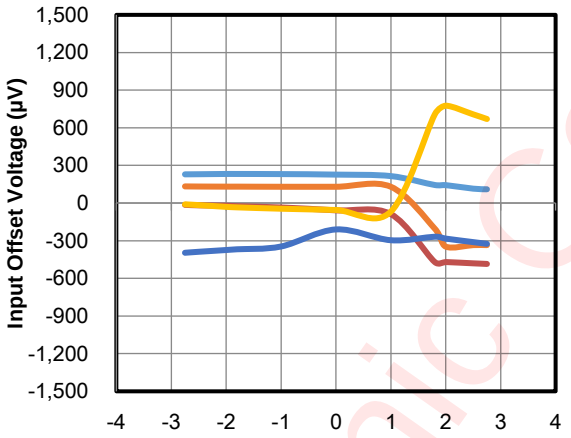


Figure 7 Input Offset Voltage vs. VCM

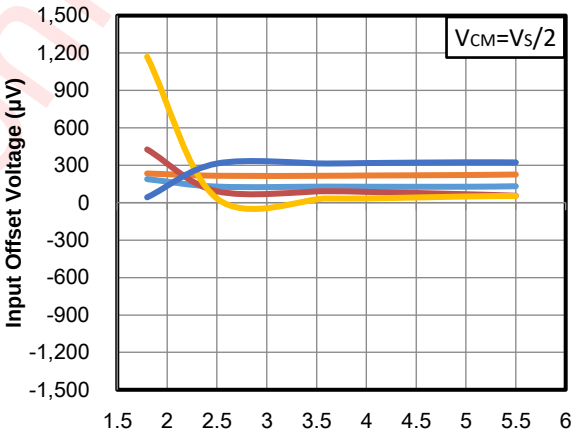


Figure 8 Offset Voltage vs. Supply Voltage

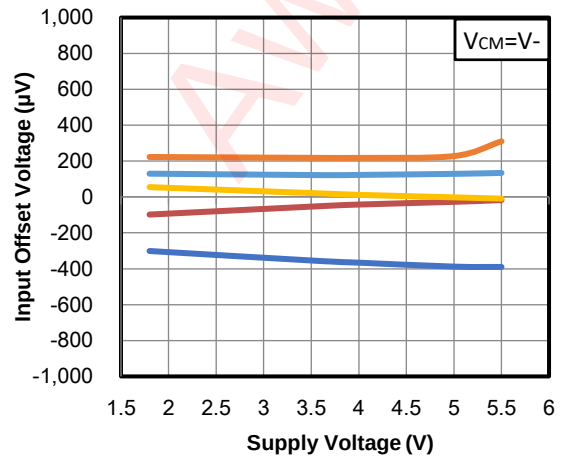


Figure 9 Offset Voltage vs. Supply Voltage

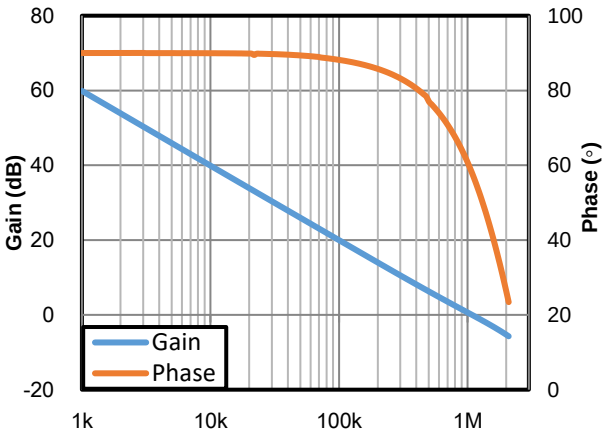


Figure 10 A_{OL} and Phase vs. Frequency

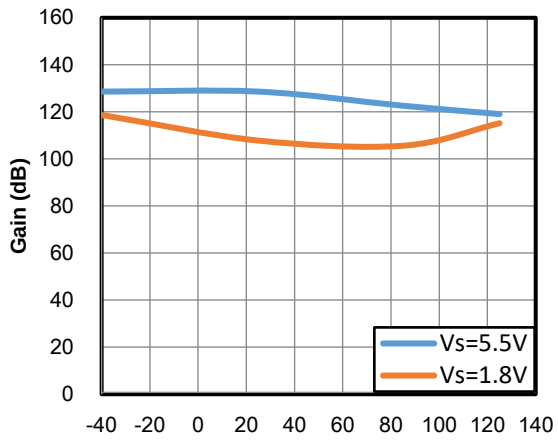


Figure 11 A_{OL} vs. Temperature

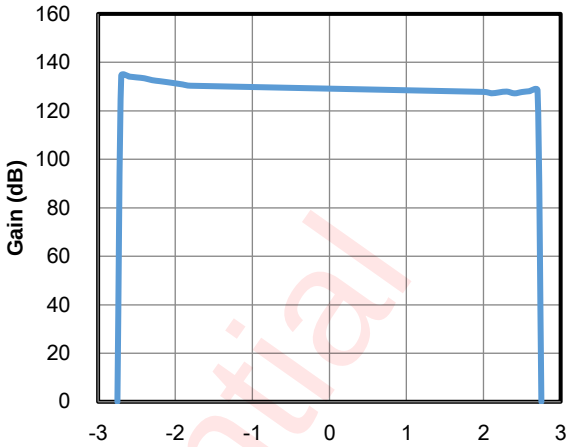


Figure 12 A_{OL} vs. Output Voltage

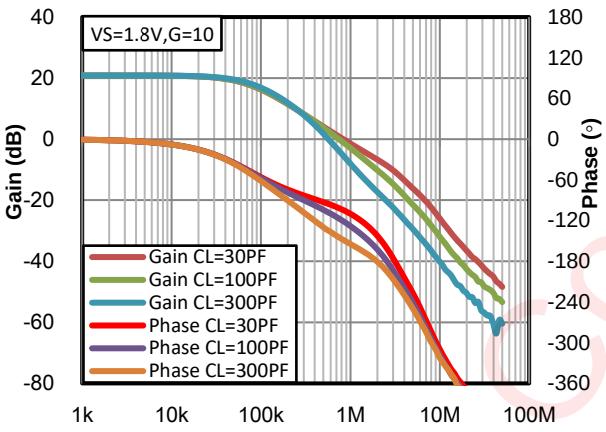


Figure 13 A_{CL} and Phase vs. Frequency

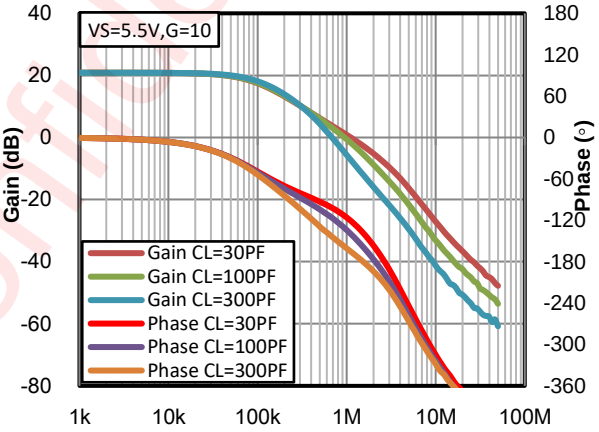


Figure 14 A_{CL} and Phase vs. Frequency

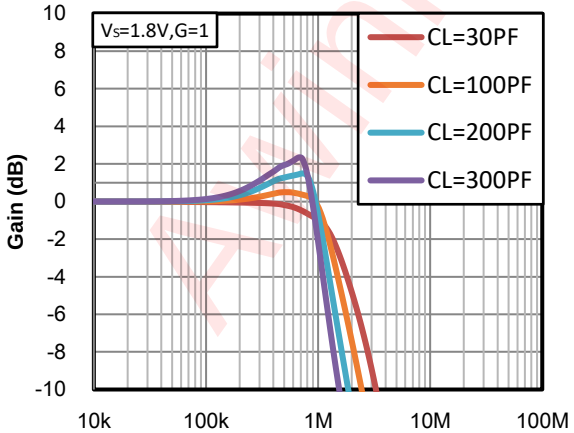


Figure 15 A_{CL} vs. Frequency

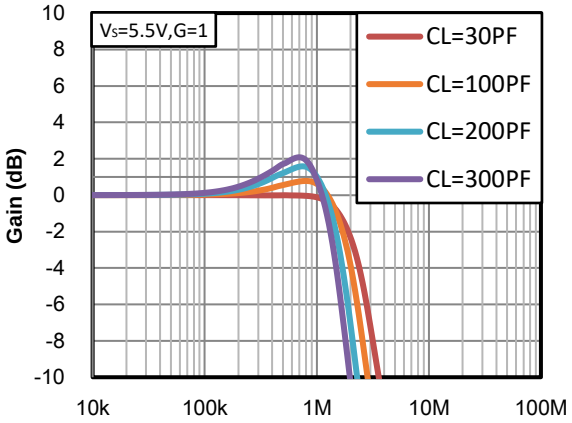


Figure 16 A_{CL} vs. Frequency

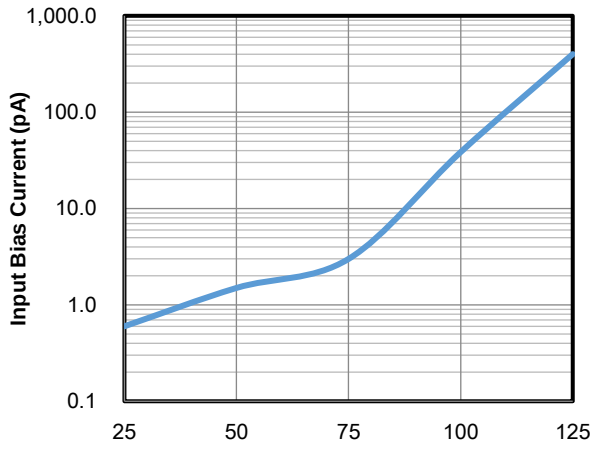


Figure 17 I_B vs. Temperature

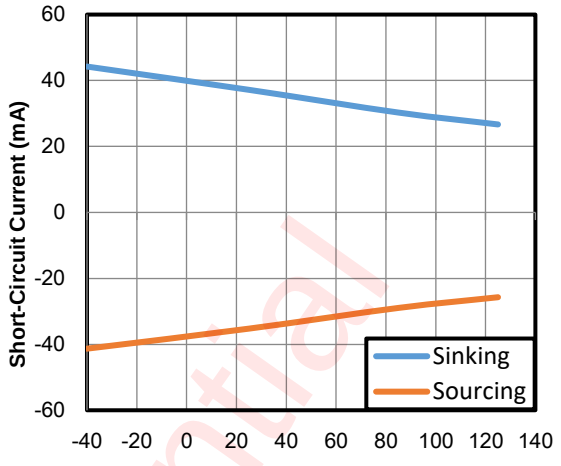


Figure 18 I_{SC} vs. Temperature

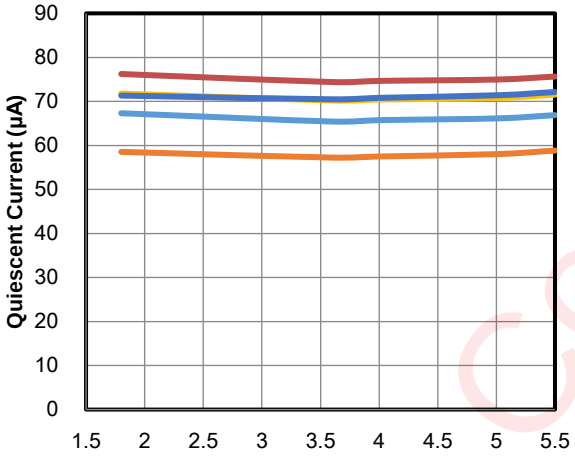


Figure 19 I_Q vs. Supply Voltage

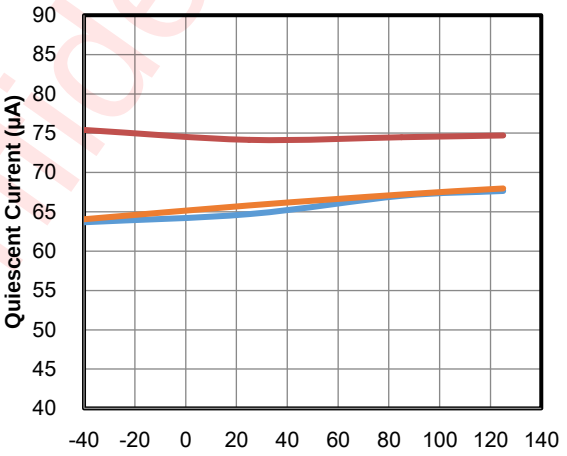


Figure 20 I_Q vs. Temperature

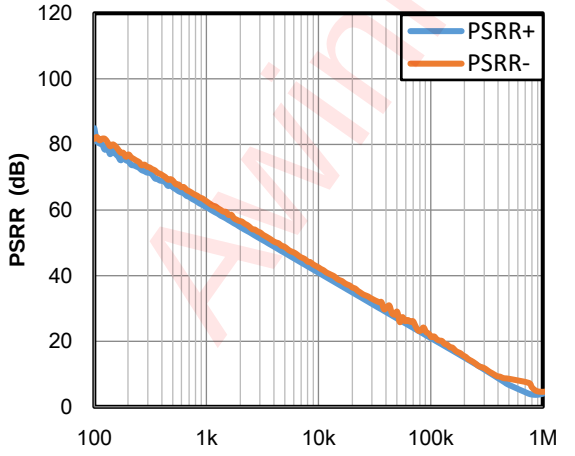


Figure 21 PSRR vs. Frequency

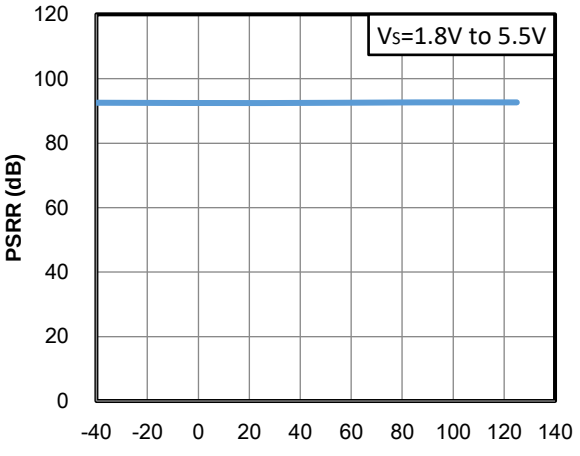


Figure 22 DC PSRR vs. Temperature

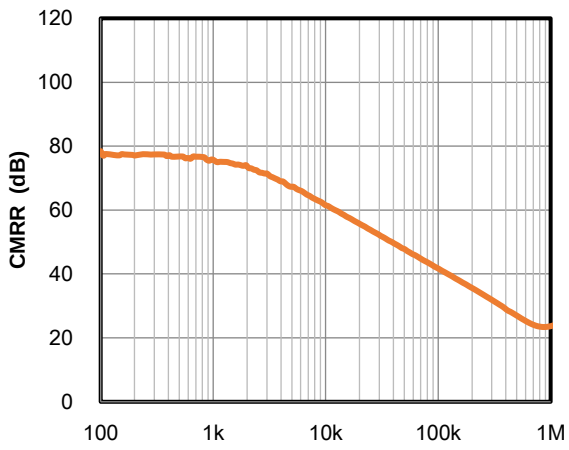


Figure 23 CMRR vs. Frequency

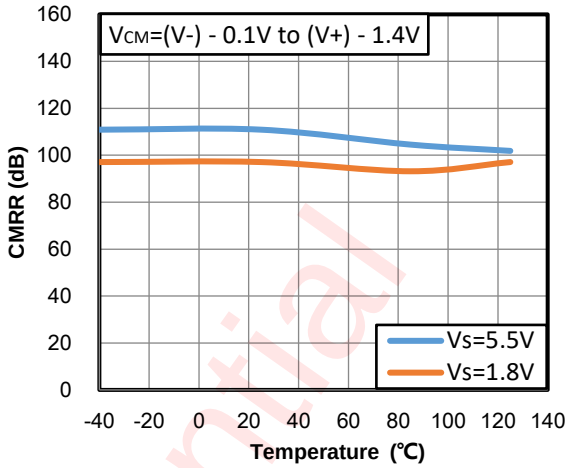


Figure 24 DC CMRR vs. Temperature

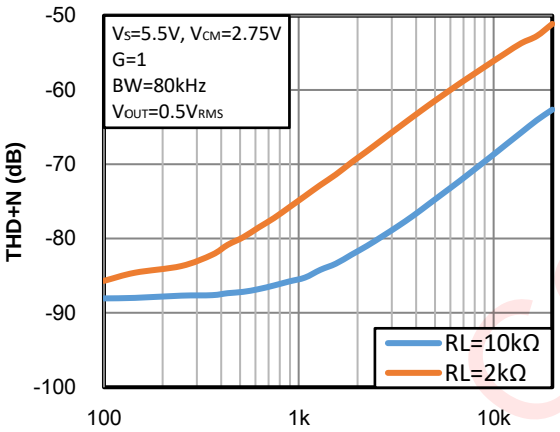


Figure 25 THD + N vs. Frequency

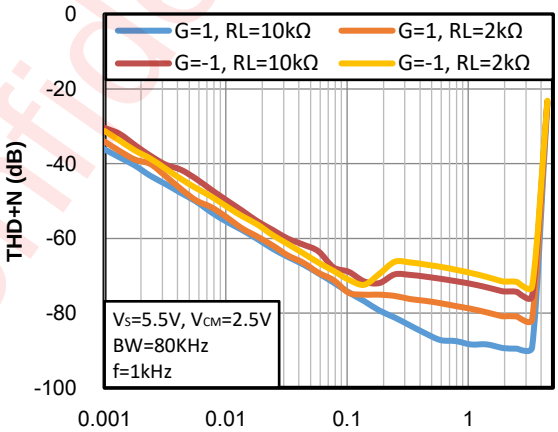


Figure 26 THD + N vs. Amplitude

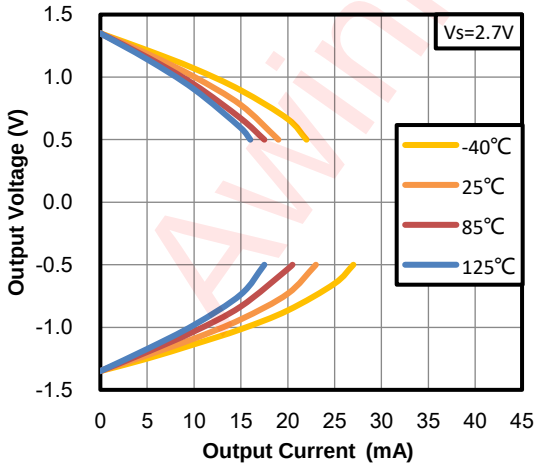


Figure 27 Output Voltage vs. Output Current

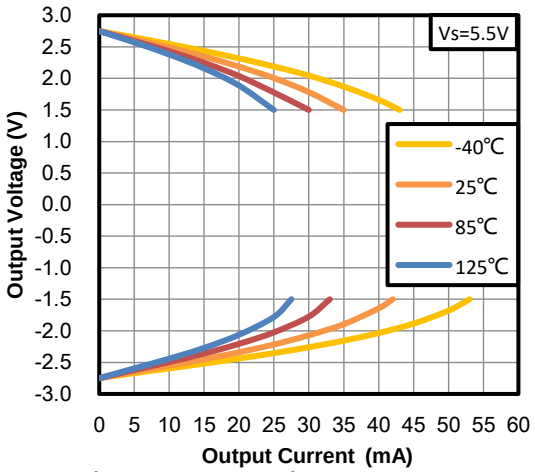


Figure 28 Output Voltage vs. Output Current

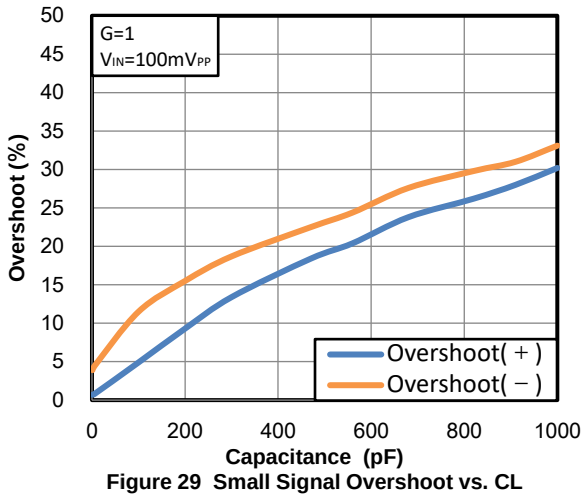


Figure 29 Small Signal Overshoot vs. CL

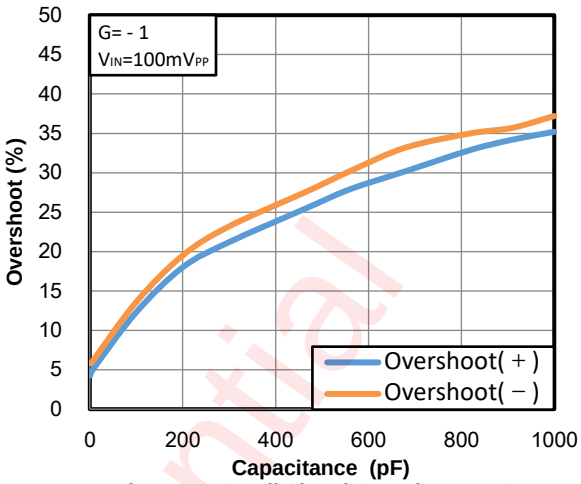


Figure 30 Small Signal Overshoot vs. CL

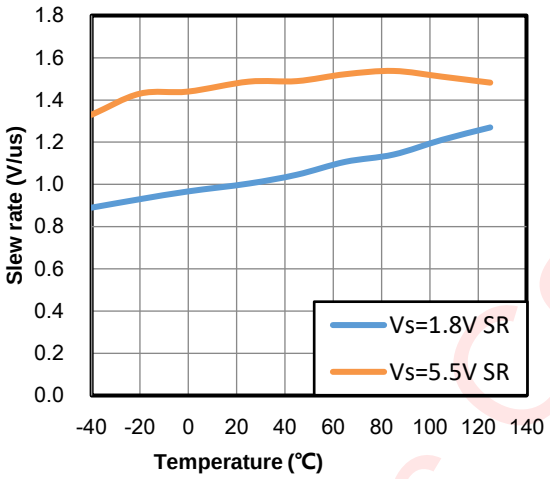


Figure 31 SR vs. Temperature

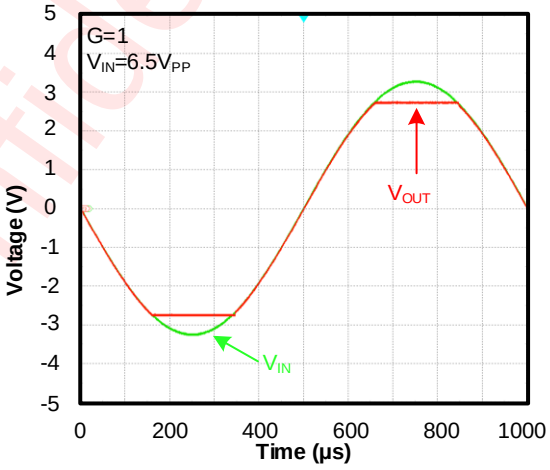


Figure 32 No Phase Reversal

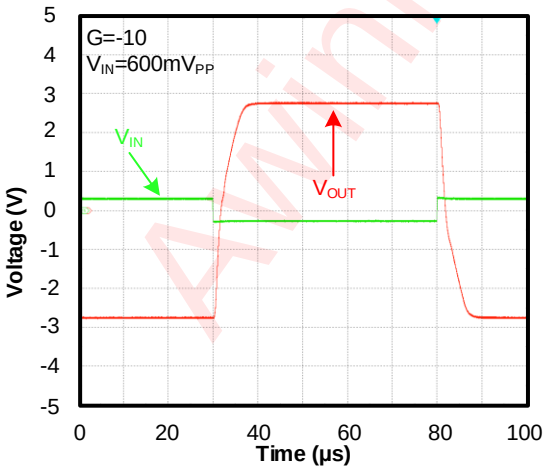


Figure 33 Overload Recovery

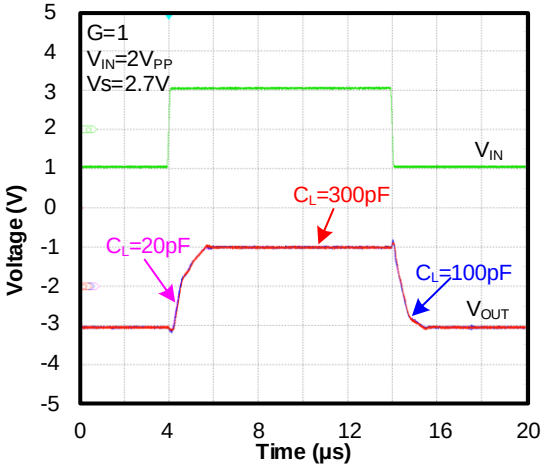


Figure 34 Large Signal Step Response

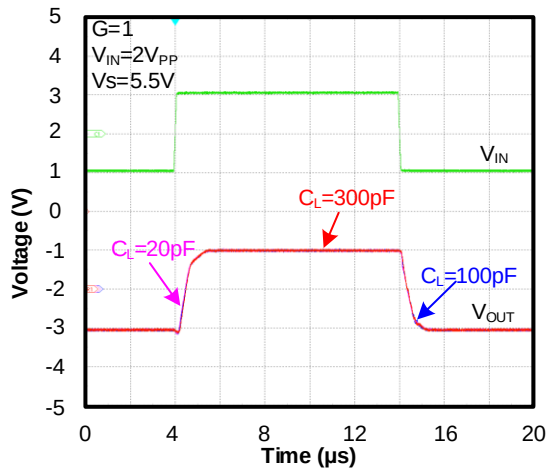


Figure 35 Large Signal Step Response

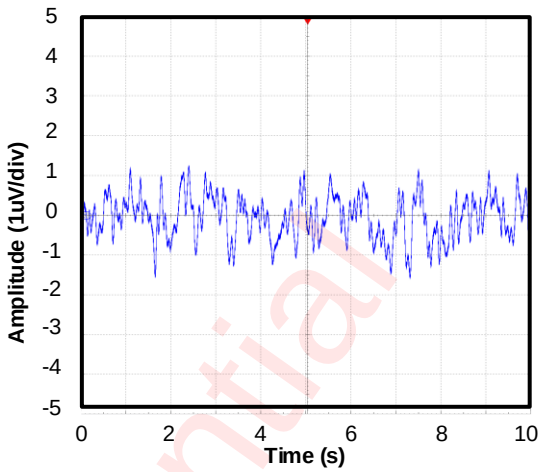


Figure 36 0.1-Hz to 10-Hz Integrated Voltage Noise

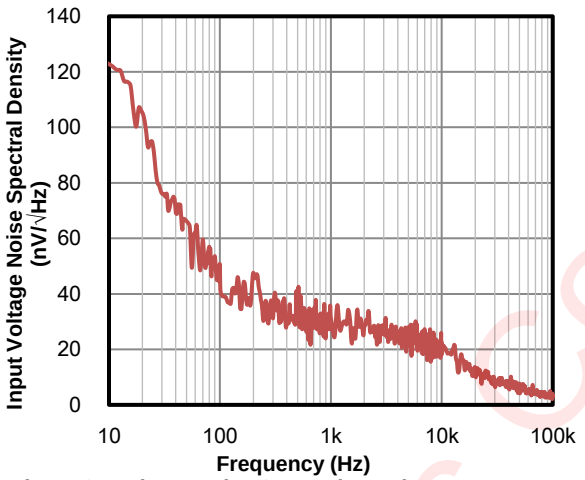


Figure 37 Voltage Noise Spectral Density vs. Frequency

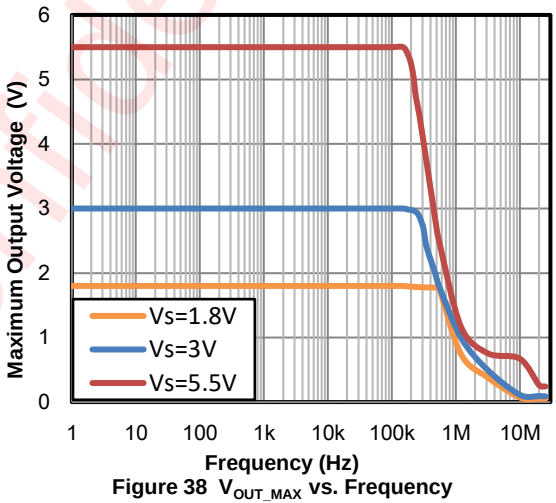


Figure 38 V_{OUT_MAX} vs. Frequency

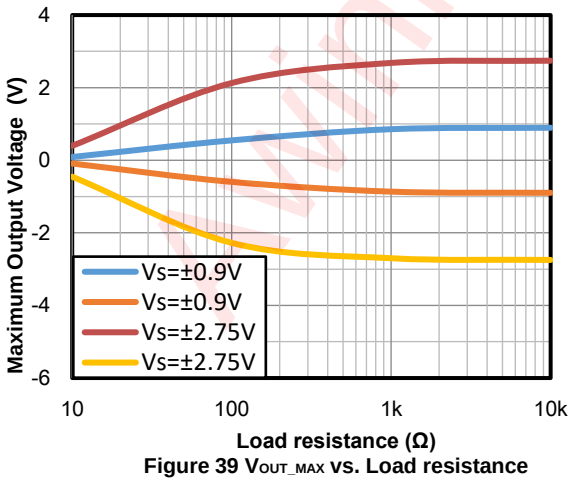


Figure 39 V_{OUT_MAX} vs. Load resistance

Detailed Functional Description

The AWS90001 is a high precision, low-voltage, low-power operational amplifier with rail-to-rail input and output swing capabilities, while drawing 66 μA (typical) of quiescent current. The device can be unity-gain stable with power supply voltages from 1.8 V to 5.5 V, which makes it ideal for a wide range of general-purpose applications.

Rail-to-Rail Input

When the input voltage is close to V+, op-amps with a differential input pair composed of P-channel MOSFETs do not provide a normal output, because a current source enters the linear region and gain is reduced. Similarly, op-amps with a differential input pair composed of N-channel MOSFETs do not provide a normal output when the input voltage is close to V-. The input voltage range of the AWS90001 can be as high as (V+) + 100 mV or as low as (V-) – 100mV within the full supply voltage range of 1.8 (±0.9) V to 5.5 (±2.75) V. This performance is achieved by using an N-channel input differential pair in parallel with a P-channel differential pair. When input voltage is close to the positive rail, typically (V+) – 1.4 V to (V+) + 100 mV, the N-channel pair is active, whereas the P-channel pair is active for inputs from (V-) – 100mV to approximately (V+) – 1.4 V. Both of the input pairs are on when the input voltage is between typically (V+) – 1.2 V to (V+) – 1 V, which is usually called the transition region. Within this transition region, PSRR, CMRR, offset voltage, and THD can degrade compared to device operation outside this region. Furthermore, the transition region can range from (V+) – 1.4 V to (V+) – 1.2 V on the low end, and up to (V+) – 1 V to (V+) – 0.8 V on the high end with process variations.

Rail-to-Rail Output

A class-AB output stage with common-source transistors achieves full rail-to-rail output swing capability. Different load conditions change the ability of the amplifier to swing close to the rails. The AWS90001 output stage can drive up to a 2kΩ load and still swing to within 60mV of the supply rails. The output of the amplifier has reverse-biased ESD diodes connected to each supply. The output should not be forced more than 0.3V beyond either supply, otherwise current will flow through these diodes.

The rail-to-rail output stage of the amplifier can be modeled as a current source when driving the load toward V+, and as a current sink when driving the load toward V-. The limit of this current source/sink varies with supply voltage. The maximum output current is a function of total supply voltage. The output current capability increases as the supply voltage to the amplifier increases. Attention must be paid to keep the junction temperature of the op-amp below 150°C when the output is in continuous short-circuit.

Driving Capacitive Loads

The AWS90001 is designed to drive large capacitive loads. The unity-gain follower (G = +1V/V) is the most sensitive configuration to capacitive loads. Thus, when driving large purely capacitive loads more than 500pF with the AWS90001 operated as unity-gain follower, it is always suggested to use a series resistor RSIS between the output and the capacitive load like the circuit in Figure 40, to improve the system's phase margin and stability. Though the bigger the resistance used, the better the phase margin will be, a loss of gain accuracy will be unavoidable because of the voltage consumption over R_{SIS} caused by output current.

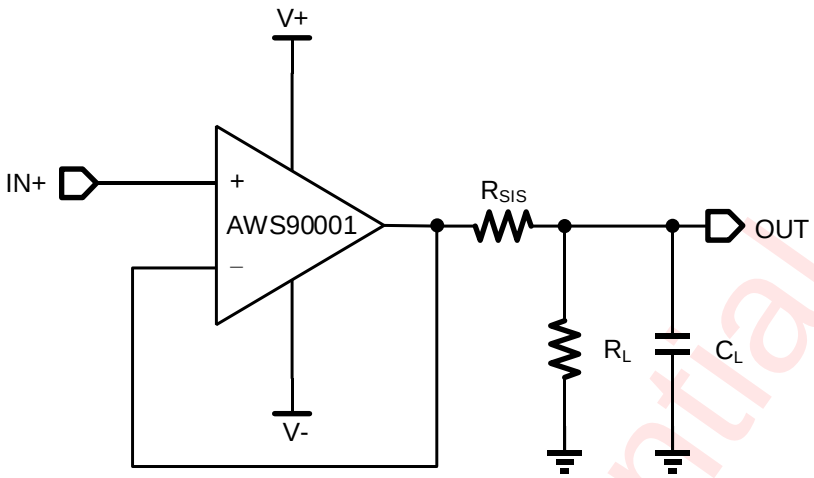


Figure 40 AWS90001 Indirectly Driving Heavy Capacitive Load

Phase Reversal Protection

Many op amps exhibit a phase reversal when the input is driven beyond its specified input common-mode range, causing the output to reverse into the opposite rail. This condition is most often encountered in noninverting circuits. The AWS90001 has internal phase-reversal protection, therefore, input signals beyond the rails do not cause phase reversal. This performance is shown in Figure 41.

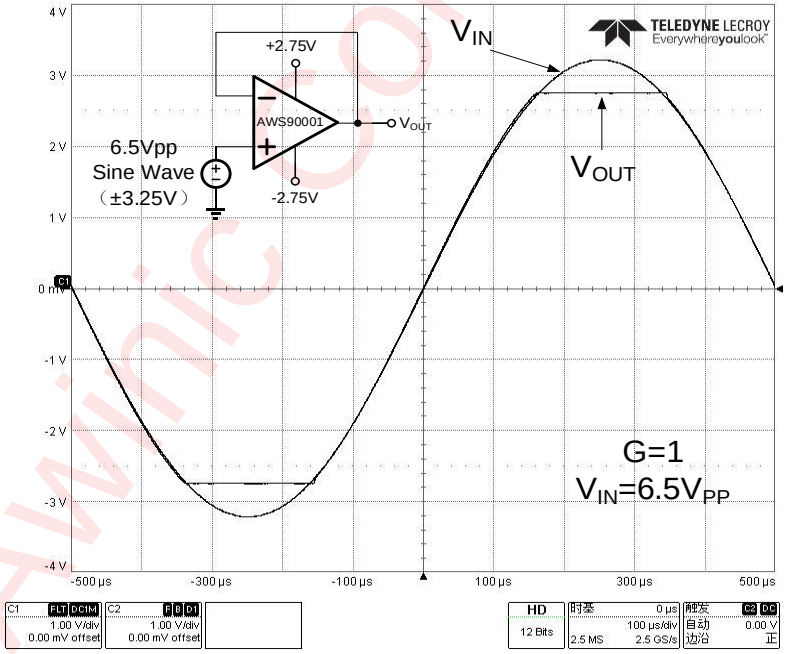


Figure 41 No Phase Reversal

PCB Layout Consideration

For the optimal performance of the device, good PCB layout practices are needed, here are some guidelines:

1. Bypass capacitors are used to reduce the coupled noise by providing a low-impedance path to ground. So low-ESR, 0.1 μF ceramic bypass capacitors are necessary between each supply pin and ground, placed close to the device, but far away from input traces.

2. R_I is a balance resistor equals to R_G || R_F to reduce the influence of the input bias current on R_G and R_F, which can be shorted when unnecessary.

3. Separate grounding for analog and digital portions of circuitry for better noise suppression. Devote one or more layers on multilayer PCBs to ground planes, which help distribute heat and reduces EMI noise.

4. Run the input traces far away from the Vs supply or output traces to reduce the parasitic coupling. If not, cross these sensitive traces at a 90 degree instead of being parallel with the noisy trace.

5. The input traces are the most sensitive part of the circuit, so keep the length of input traces as short as possible. Place the external resistors and capacitors as close to device as possible, especially the R_F and R_G should be close to the inverting input to minimize the parasitic capacitance.

6. In differential applications, the trace of the inverting input and the non-inverting input should be symmetrical including the same layer, same length, same width and same line spacing.

7. Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process.

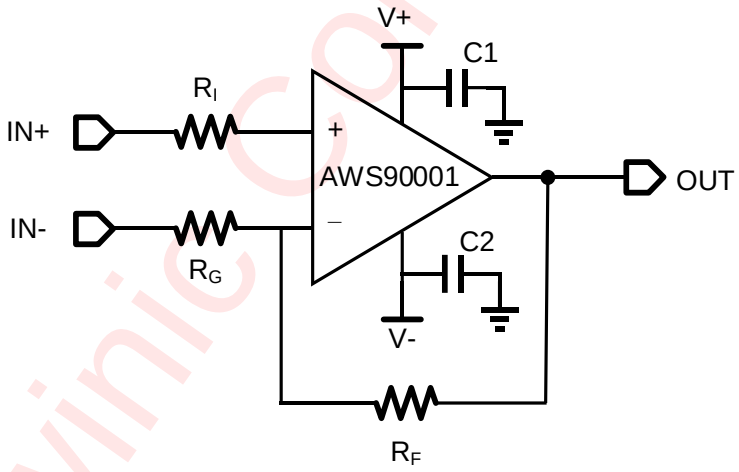
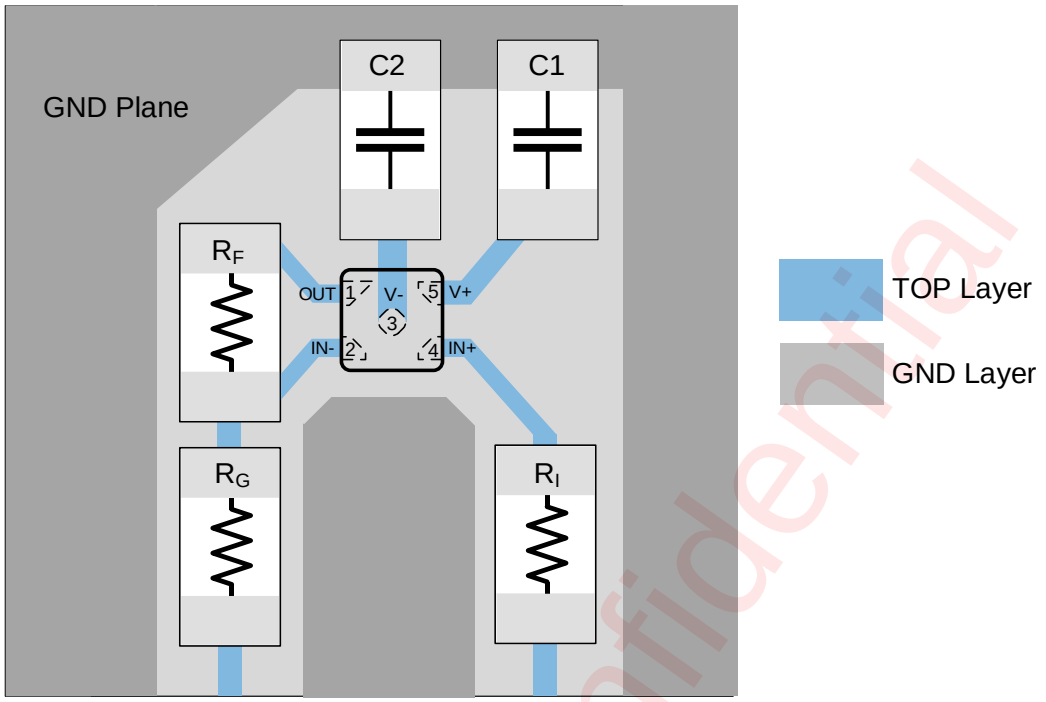
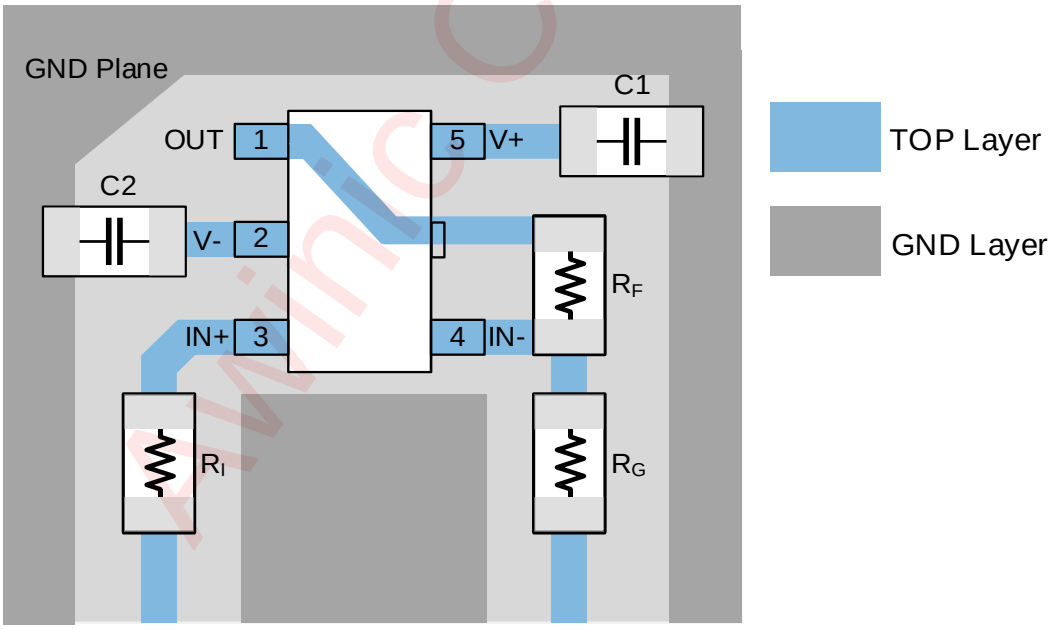


Figure 42 AWS90001 Schematic Example

DFN - 5L_AWS90001DNR



SOT 23 - 5L_AWS90001STR



SOT 23 - 5L_AWS90001ASTR

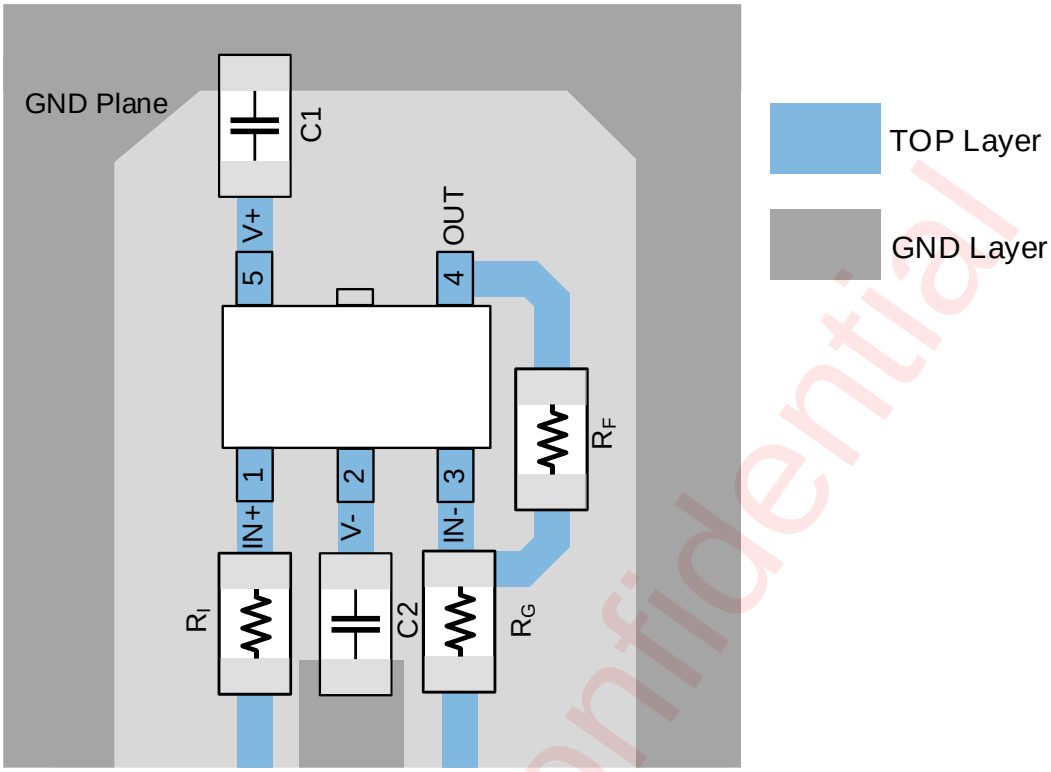


Figure 43 AWS90001 Layout Example

PCB Surface Leakage Current

In high precision applications where input bias current is critically concerned, the leakage current on PCB surface caused by dust or humidity may badly reduce the output accuracy. In this case, a multi-layer PCB is recommended for routing the input traces under the PCB surface. In addition, the usage of a guard ring can significantly reduce the leakage current to sensitive node. A conductive ring surrounding the inputs should be connected to a low impendence node with the same voltage as the inputs, so this ring will absorb the leakage current from high voltage nodes around the inputs.

For non-inverting gain application，connect the IN+ to the input with traces not touching the PCB surface, for example, routing in second layer in Figure 44. Then surround the IN+ pin with a guard ring which is connected to IN-, thus biasing the guard ring with the same voltage of the common mode input voltage.

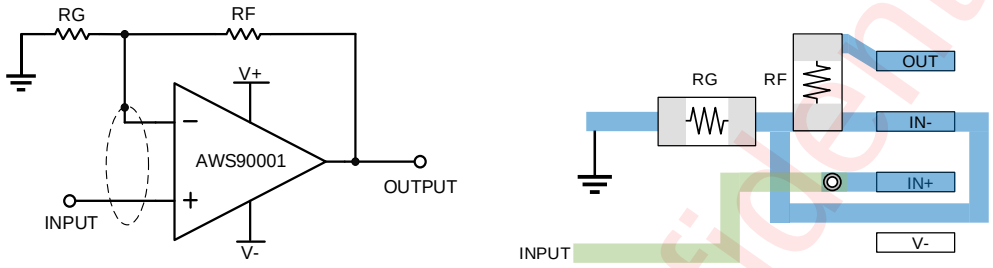


Figure 44　Non-inverting Gain Application Schematic and Layout Example

Similarly, for inverting gain application, connect the IN- to the input with traces not touching the PCB surface, for example, striding over with the input resistor in Figure 45. Then surround the IN- pin with a guard ring which is connected to IN+, thus biasing the guard ring with the reference voltage of AWS90001.

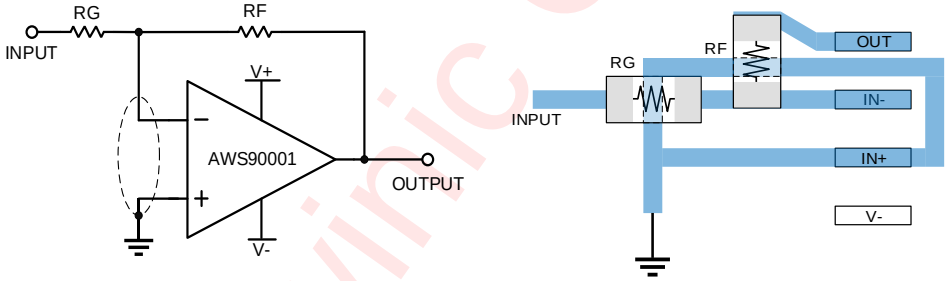
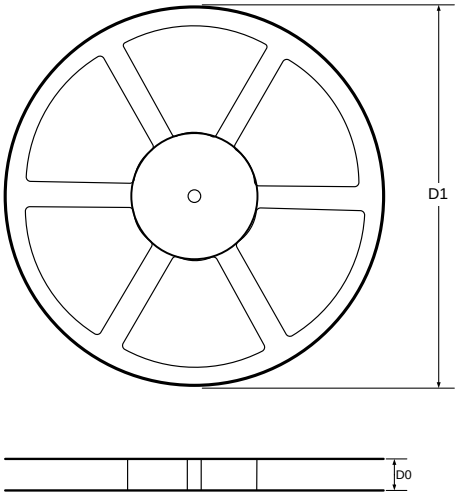


Figure 45　Inverting Gain Application Schematic and Layout Example

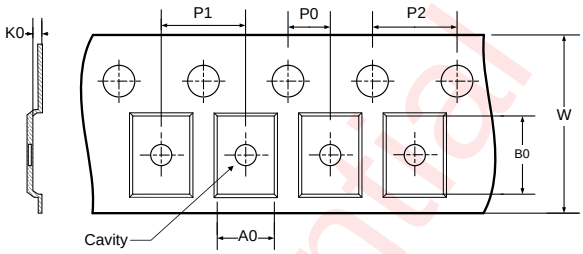
Tape And Reel Information

DFN 0.8mm × 0.8mm × 0.37mm - 5L

REEL DIMENSIONS

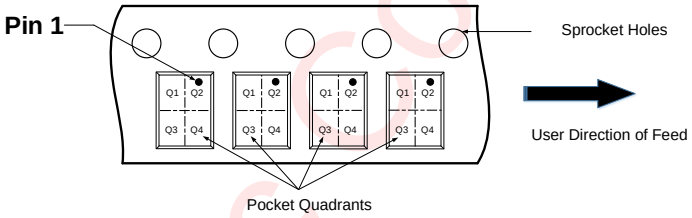


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

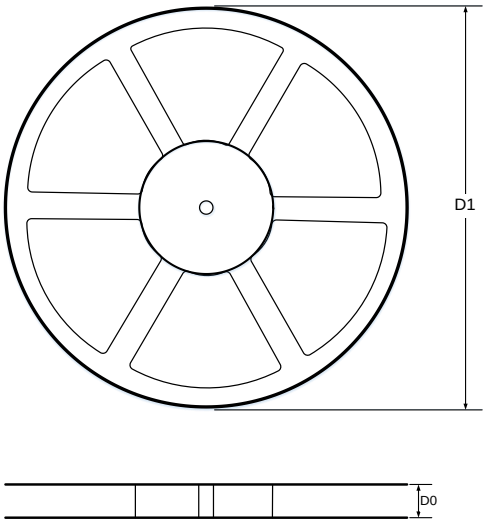
DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.4	0.91	0.91	0.5	2	2	4	8	Q2

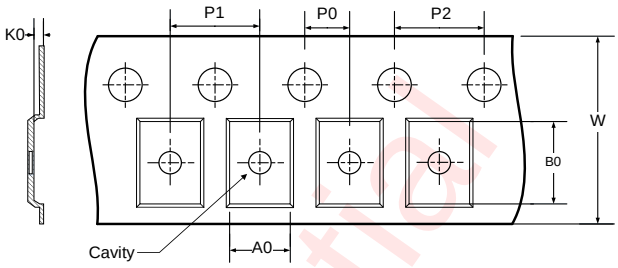
All dimensions are nominal

SOT 23 - 5L

REEL DIMENSIONS

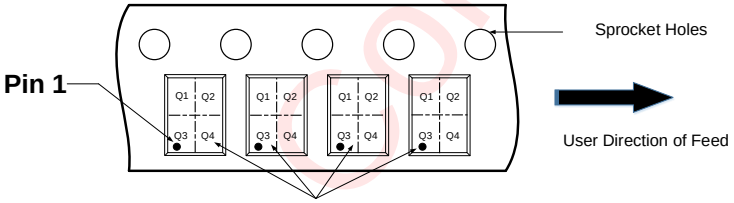


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

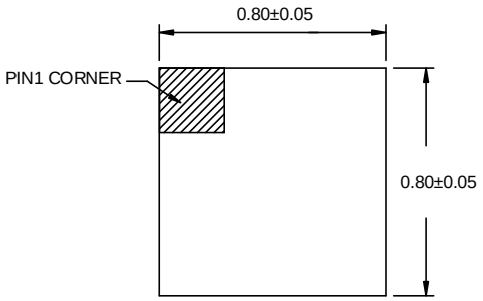
DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.4	3.3	3.2	1.4	2	4	4	8	Q3

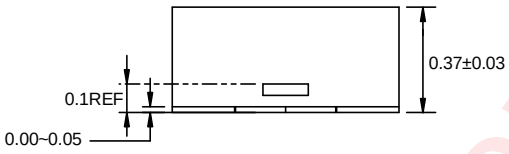
All dimensions are nominal

Package Description

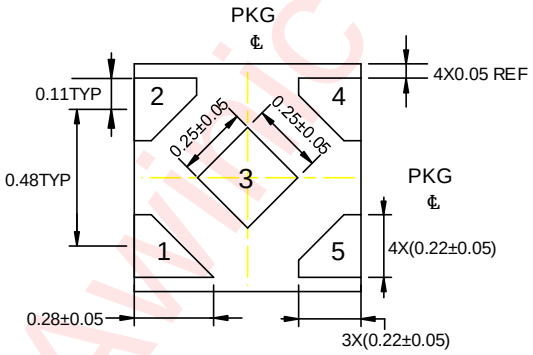
DFN 0.8mm × 0.8mm × 0.37mm - 5L



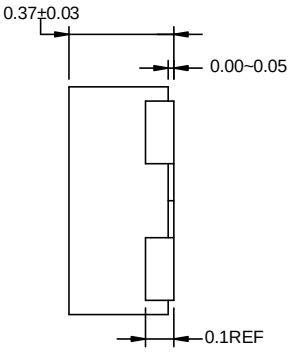
TOP VIEW



SIDE VIEW



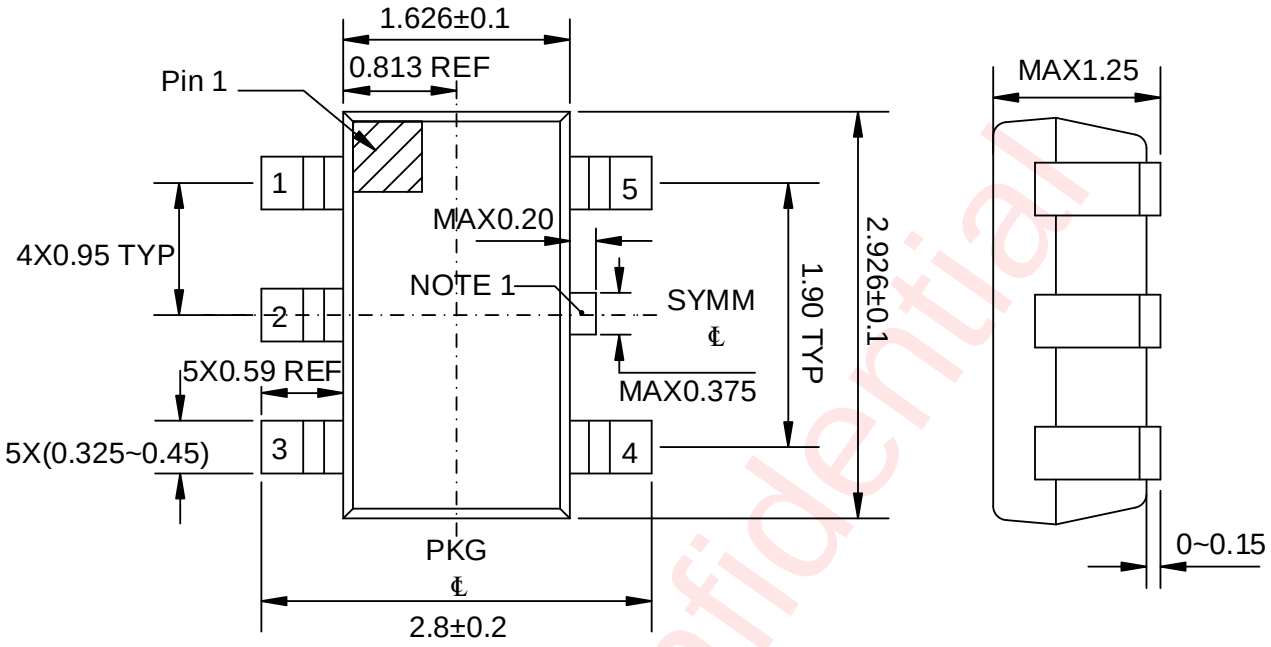
BOTTOM VIEW



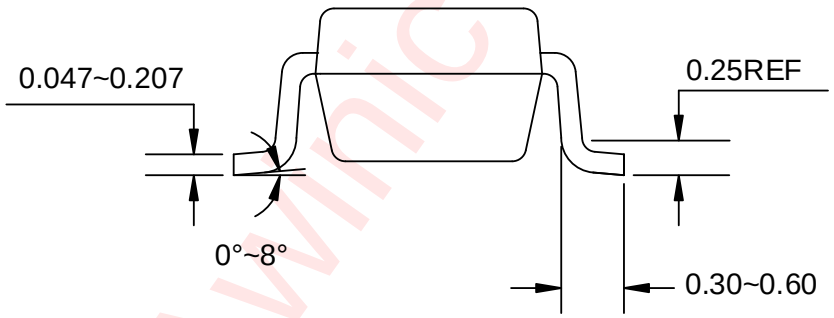
SIDE VIEW

Unit:mm

SOT 23 - 5L



Top View **Side View**



Side View

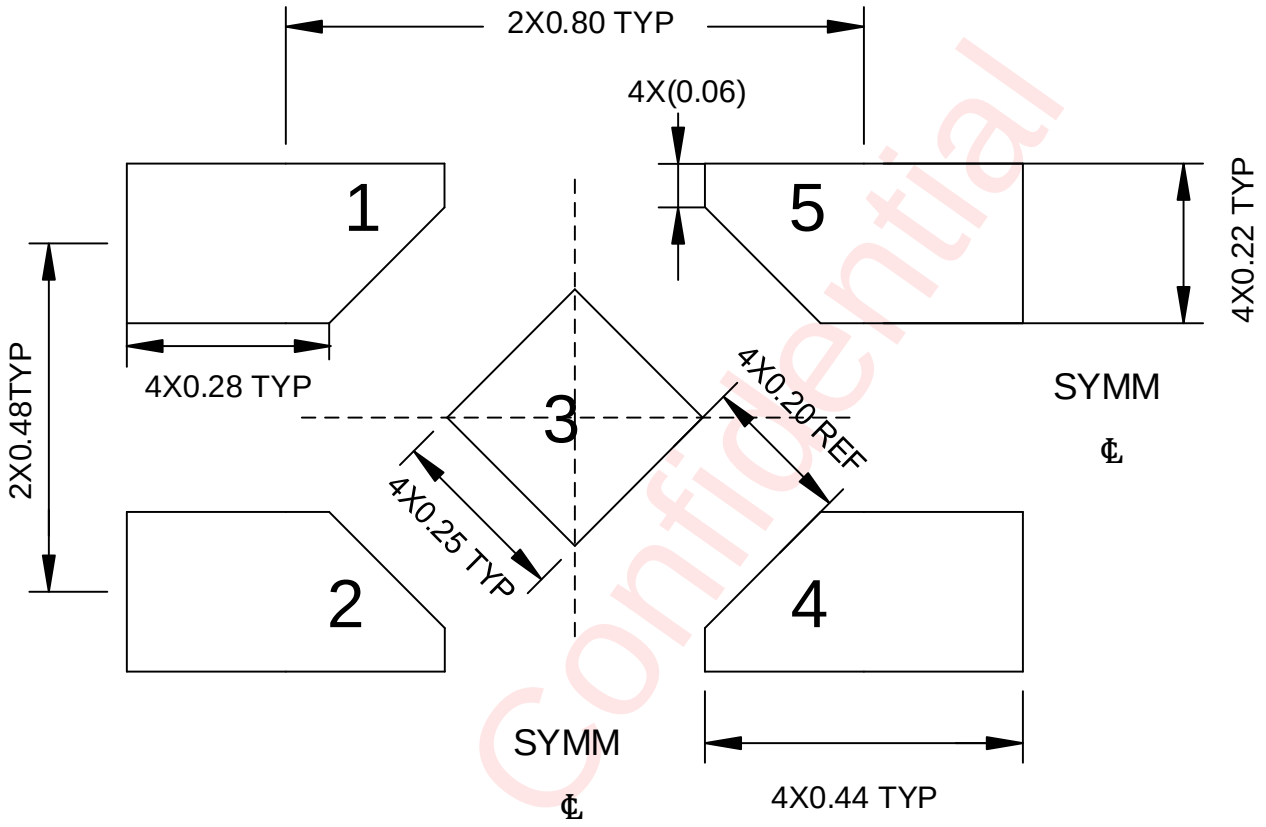
Unit: mm

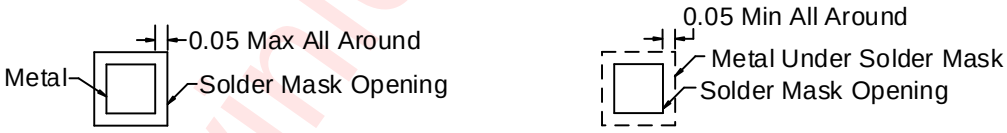
NOTE:

1.Support pin may differ or may not be present.

Land Pattern Data

DFN 0.8mm × 0.8mm × 0.37mm - 5L

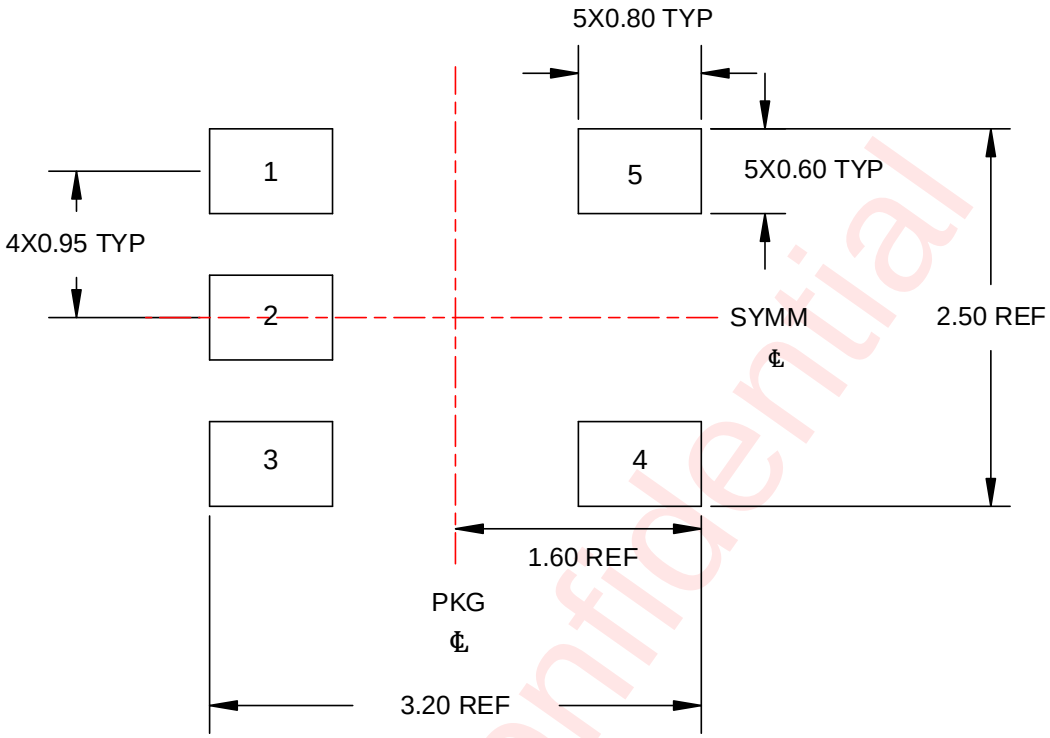


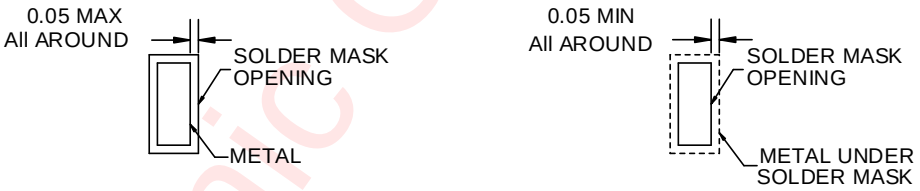


Non-solder Mask Defined Solder Mask Defined

Unit:mm

SOT 23 - 5L





NON SOLDER MASK DEFINED

SOLDER MASK DEFINED

Unit: mm

Revision History

Version	Date	Change Record
V1.0	Dec. 2021	Official released
V1.1	May. 2022	1. Added WBDFN package thermal information to the *Thermal Information* 2. Corrected typo in *Typical Characteristics* (Figure 19 horizontal axis title)
V1.2	Jun. 2022	1. Modified D1 from 179 to 178 in *Tape And Reel Information.* (P17) 2. Modified D0 from 9 to 8.4 in *Tape And Reel Information.* (P17) 3. Modified P1 from 4 to 2 in *Tape And Reel Information.* (P17) 4. Modified delivery form from 4500 to 9000 in *Ordering Information.* (P4)
V1.3	Jun. 2022	1. Added lower limit of PSRR in *Electrical Characteristics*. (P7) 2. Added upper and lower limits of both I_B and I_{OS} in *Electrical Characteristics.* (P7) 3. Added lower limits of CMRR in *Electrical Characteristics.* (P7) 4. Added upper and lower limits of I_Q in *Electrical Characteristics*. (P7) 5. Added lower limits of A_{OL} in *Electrical Characteristics.* (P8) 6. Added lower limit of SR in *Electrical Characteristics.* (P8) 7. Added upper limits of V_O in *Electrical Characteristics.* (P8) 8. Added upper and lower limits of I_{SC} in *Electrical Characteristics.* (P8)
V1.4	Aug. 2022	1. The upper limits of IQ changed from 100μA to 85μA in Electrical Characteristics. (P7)
V1.5	Sep. 2022	1. Added specs of V_{OS} over temperature from -40°C to 125°C in *Electrical Characteristics.* (P7) 2. Added specs of I_Q over temperature from -40°C to 125°C in *Electrical Characteristics.* (P8)
V1.6	Oct. 2022	1. Added WBSOT 23 - 5L package information to *General Description.* (P1) 2. Added WBSOT 23 - 5L pin configuration to *Pin Configuration And Top Mark.* (P2) 3. Added WBSOT 23 - 5L pin description table to *Pin Definition.* (P3) 4. Added WBSOT 23 - 5L information table to *Ordering Information.* (P5) 5. Added WBSOT 23 - 5L thermal metrics to *Thermal Information.* (P7) 6. Added WBSOT 23 - 5L information to *Tape And Reel Information.* (P19) 7. Added WBSOT 23 - 5L information to *Package Description.* (P21) 8. Added WBSOT 23 - 5L information to *Land Pattern Data.* (P23) 9. Added WBSOT 23 - 5L layout example of Figure 33 to *PCB Layout Consideration.* (P17)
V1.7	Nov. 2022	1. Modified WBSOT 23 - 5L layout example of Figure 33 in *PCB Layout Consideration.* (P17) 2. Modified highest temperature from 85°C to 125°C in *Ordering Information.* (P5) 3. Added PCB surface leakage current guidelines to *PCB Layout Consideration.* (P18) 4. Added 125°C test data of Figure 20 in *Typical Characteristics.* (P12) 5. Modified the legend of Figure 19 from "V_{OUT}=0.5V_{RMS}" to "f=1kHz" and deleted "G=1" in *Typical Characteristics.* (P12)
V1.8	Mar. 2023	1. Update WBSOT 23 - 5L information in *Package Description.* (P22) 2. Update WBSOT 23 - 5L information in *Land Pattern Data.* (P24)
V1.9	Aug.2023	1. Added *Device Information*. (P1) 2. Update AWS90001STR *Pin Configuration*. (P2) 3. Added AWS90001ASTR *Pin Configuration*. (P3) 4. Added AWS90001ASTR *Ordering Information*. (P6) 5. Added Figure 29. (P15) 6. Update SOT 23 - 5L_AWS90001STR *Layout Example*. (P19) 7. Added SOT 23 - 5L_AWS90001ASTR *Layout Example.* (P20)

V2.0	Dec.2023	1. Update *ESD Rating and Latch Up*. (P7)
V2.1	Jan.2024	1. Update *Device Information*. (P1) 2. Update *Pin Definition*. (P4) 3. Added Figure 5,13,14,15,16,17,27,31,34,35,39 in *Typical Characteristics.* (P11-16)
V2.2	Apr.2024	1. Update E_N , e_N and I_{SC} in *Electrical Characteristics.* (P9-10) 2. Update Figure 36. (P16)
V2.3	Apr.2024	1. Update Features and General Description. (P1)

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