3-Key Capacitive Touch Controller Integrated with 3-LED Driver

FEATURES

- 3 Capacitive key with sensitivity configurable
- RF Noise Filter
- Tap Gesture detection (Single/Double/Triple click and slide gesture)
- Automatic Calibration for Environmental Change
- Intrinsic Capacitance Compensation
- 8-level LED Maximum Current for each LED, max 24.5mA
- 256-level Linear/Logarithmic PWM Dimming,9 bits PWM resolution
- Capacitive Touch status trigger internal LED program to create complicated touch feedback
- Compatible I²C Interface, V_{IO}: 1.8V ~ 3.3V
- I2C address: 0x2C/0x2D
- Single Power Supply, Voltage Range: 3.0V ~ 4.5V
- CSP1.59mm×1.75mm×0.57mm-16L Package

APPLICATIONS

Mobile Phones, MID

Portable Media Player

Home Appliances

GENERAL DESCRIPTION

AW9233 integrates 3 capacitive sensor and a SRAM program-controlled 3 LED driver. By special programming and register configuring，the touch or gesture can trigger predefined lighting program to generate funny and complicated LED effect, without the aid of external MCU.

The capacitive sensor takes advantage of advanced Sigma-delta capacitance digital conversion technology to achieve high sensitivity and anti-noise capacitance detection. With internal DSP algorithm, the touch and gesture event can be detected and reported in status register and external interrupt pin.

3 LED driver uses common anode current source and PWM dimming. Each LED is 8-level driver current selectable with dimming independently controlled by external MCU or internal 256word*16bit SRAM program.

Compatible I²C interface of 400kHz fast mode is provided, the package is CSP1.59mm×1.75mm×0.57mm-16L. It requires only 3.0V-4.5V single power supply.

TYPICAL APPLICATION CIRCUIT

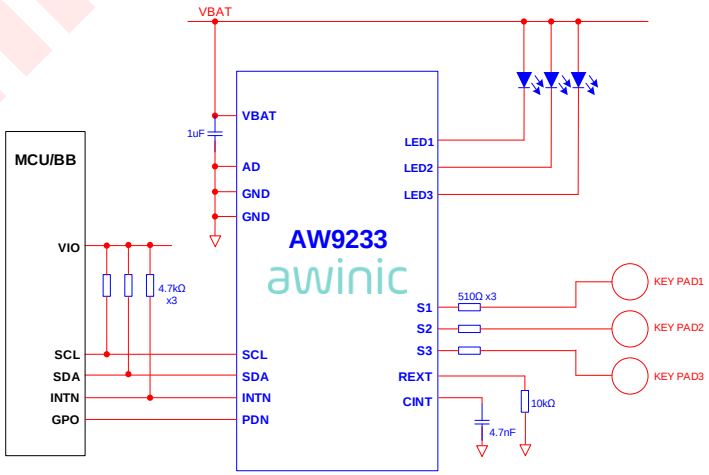
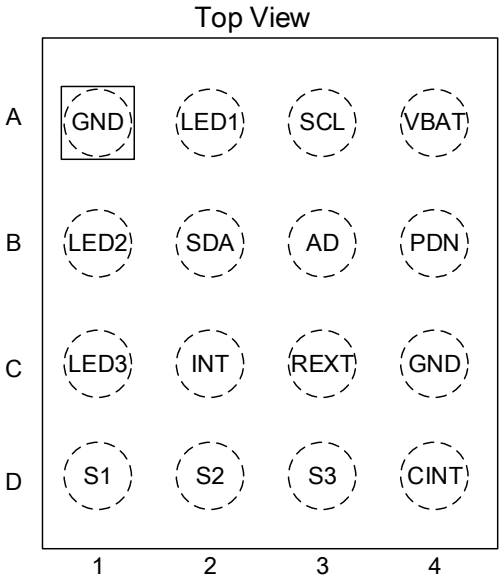
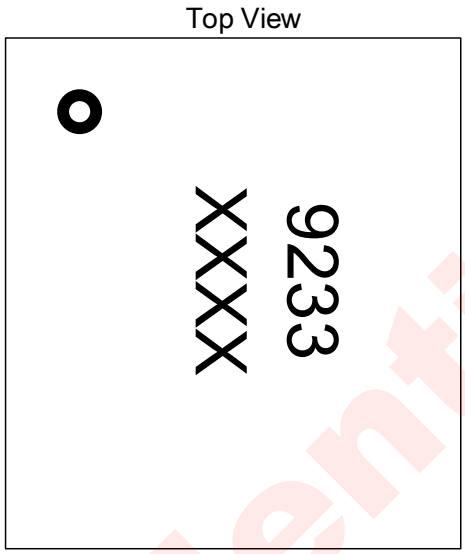


Figure 1 AW9233 Typical Application Circuit

1 PIN CONFIGURATION AND TOP MARK





9233-AW9233CSR
XXXX-Production Tracing Code

2 PIN DEFINITION

No.	NAME	DESCRIPTION
A1	GND	Ground
A2	LED1	LED1 cathode driver, anode connected to VBAT
A3	SCL	Clock input of I²C Interface
A4	VBAT	Power supply (3.0V to 4.5V)
B1	LED2	LED2 cathode driver, anode connected to VBAT
B2	SDA	Data I/O of I²C Interface
B3	AD	I²C Address Select
B4	PDN	Power-down input, low active, internal 1MΩ pull-down resistor
C1	LED3	LED3 cathode driver, anode connected to VBAT
C2	INTN	Open-drain Interrupt output, low active. Typically connected to VIO via a 4.7kΩ resistor
C3	REXT	External resistor for adjusting sensitivity (typical is 10kΩ)
C4	GND	Ground
D1	S1	Capacitive Touch Input S1
D2	S2	Capacitive Touch Input S2
D3	S3	Capacitive Touch Input S3
D4	CINT	External reference capacitor(typical is 4.7nF)

3 FUNCTIONAL BLOCK DIAGRAM

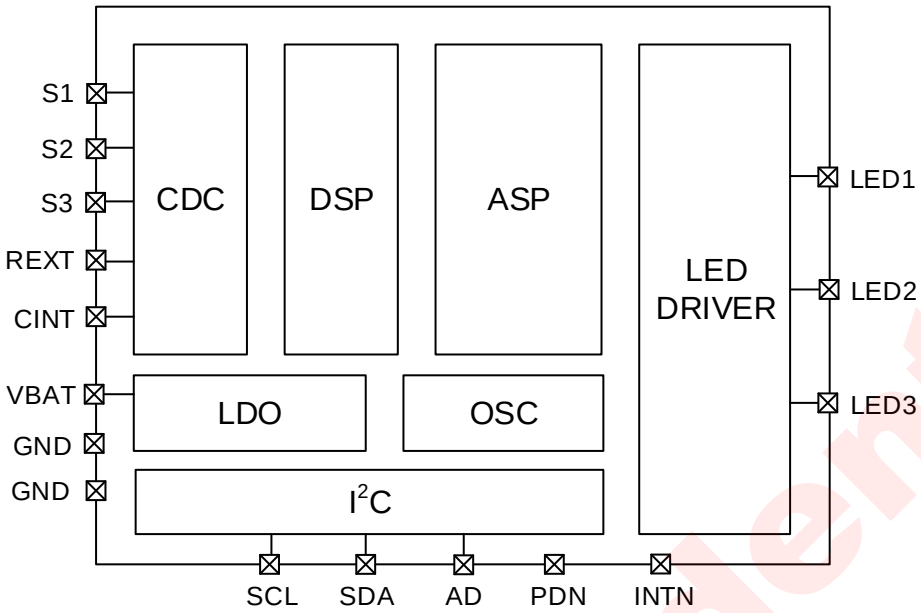


Figure 2 FUNCTIONAL BLOCK DIAGRAM

4 TYPICAL APPLICATION CIRCUITS

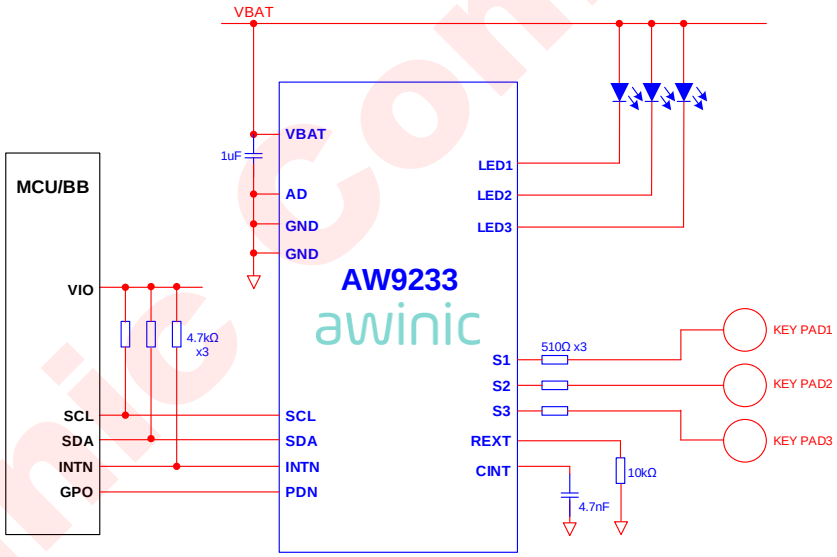


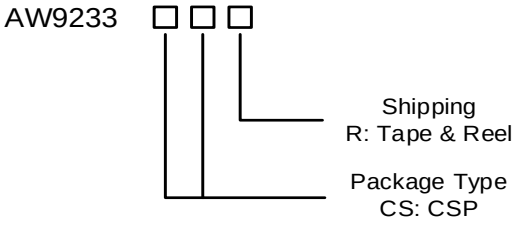
Figure 3 AW9233 Typical Application Circuit

NOTE1、Pin S1/S2/S3 must connect a 500Ω ~ 600Ω resistor.

NOTE2、C_{INT} and R_{EXT} should be placed as close as possible to the chip.

5 ORDERING INFORMATION

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW9233CSR	-40℃～85℃	CSP1.59 ×1.75-16L	9233	MSL1	ROHS+HF	3000 units/ Tape and Reel



6 ABSOLUTE MAXIMUM RATINGS(NOTE 3)

PARAMETERS		RANGE
Supply voltage range V_{BAT}		-0.3V to 5V
Input voltage range	SCL, SDA	-0.3V to 3.6V
	PDN, LED1~LED3	-0.3V to 4.5V
Output voltage range	SDA, INTN	-0.3V to 3.6V
Junction-to-ambient thermal resistance θ_{JA}		45℃/W
Operating free-air temperature range		-40℃ to 85℃
Maximum Junction temperature T_{JMAX}		150℃
Storage temperature T_{STG}		-65℃ to 150℃
Lead Temperature (Soldering 10 Seconds)		260℃
ESD(NOTE 4)		
HBM (human body model)		±5000V
CDM (charge device mode)		±2000V
Latch-up		
Test Condition: JEDEC STANDARD NO.78B DECEMBER 2008		+IT：450mA -IT：-450mA

NOTE3: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE4: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. HBM Test method: MIL-STD-883G Method 3015.7

CDM Test method: JESD22-C101

7 ELECTRICAL CHARACTERISTICS

V_{BAT}=3.8V, T_A=25℃ for typical values (unless otherwise noted)

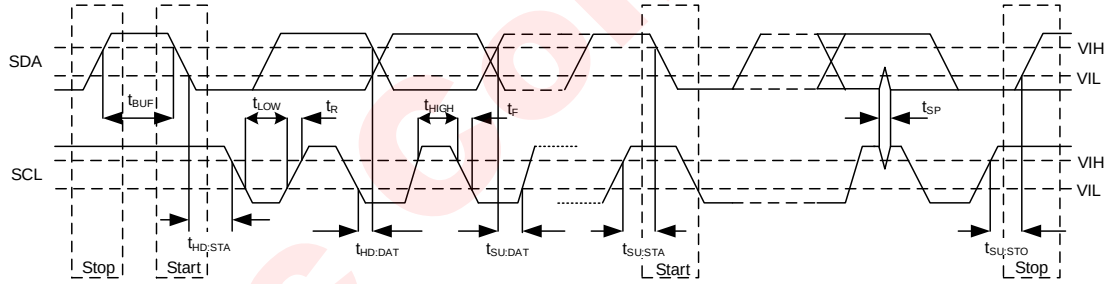
PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{BAT}	Power supply	-	3.0	3.8	4.5	V
$I_{SHUTDOWN}$	Current in Shutdown mode	PDN=GND		8	15	μA
$I_{STANDBY}$	Current in Standby mode	PDN=1.8V		130	160	μA
I_{ACTIVE}	Current in Touch Active Mode	PDN=1.8V, GCR=0x02		0.85	1.0	mA
	Current in LED Active Mode	PDN=1.8V, GCR=0x01		0.55	0.8	mA
	Current in Touch & LED Active Mode	PDN=1.8V, GCR=0x03		1.0	1.5	mA
F_{OSC}	Internal oscillator Frequency accuracy (16MHz)		14.8	16	17.2	MHz
Digital Logical Interface						
V_{IL}	Logic input low level	SDA,SCL,PDN			0.45	V
V_{IH}	Logic input high level	SDA,SCL,PDN	1.1			V
I_{IL}	Low level input current	SDA,SCL,PDN		5		nA
I_{IH}	High level input current	SDA,SCL,PDN		5		nA
V_{OL}	Logic output low level	SDA, INTN I_{OUT}=3mA			0.4	V
I_{OL}	Maximum output current	SDA, INTN			10	mA
I_L	Output leakage current	SDA,INTN open drain			1	μA
I²C Interface						
F_{SCL}	I²C-BUS clock frequency				400	kHz
$T_{Deglitch}$	SCL deglitch time			200		ns
	SDA deglitch time			250		ns
Capacitance Button						
SX_{range}	Range(NOTE5)	SX	0		80	pF
$SX_{resolution}$	Resolution(NOTE5)	SX	0.02			pF
F_{SCAN}	Scan frequency			30		Hz
T_{DET}	Response time			100		ms
LED Driver						
I_{MAX}	LED MAX Current	I_{LED}=24.5mA	18.5	24.5	30.5	mA
I_{MATCH}	Matching accuracy	I_{LED}=24.5mA			10	%
V_{DROP}	Drop-out voltage	I_{LED}=24.5mA			300	mV
F_{PWM}	PWM frequency	LCR.FREQ=1	110	122	135	Hz

		LCR.FREQ =0	220	244	270	Hz

NOTE5：the value is tested in default configuration.

8 I²C INTERFACE TIMING

Parameter Name			MIN	TYP	MAX	UNIT
F_{SCL}	Interface Clock frequency				400	kHz
$T_{DEGLITCH}$	Deglitch time	SCL		200		ns
		SDA		250		ns
$T_{HD:STA}$	(Repeat-start) Start condition hold time		0.6			μs
T_{LOW}	Low level width of SCL		1.3			μs
T_{HIGH}	High level width of SCL		0.6			μs
$T_{SU:STA}$	(Repeat-start) Start condition setup time		0.6			μs
$T_{HD:DAT}$	Data hold time		0			μs
$T_{SU:DAT}$	Data setup time		0.1			μs
T_R	Rising time of SDA and SCL				0.3	μs
T_F	Falling time of SDA and SCL				0.3	μs
$T_{SU:STO}$	Stop condition setup time		0.6			μs
T_{BUF}	Time between start and stop condition		1.3			μs



9 FUNCTIONAL DESCRIPTION

9.1 WORK MODE

9.1.1 Power On

After power-up, about 100μs delay is required before PDN set to high, otherwise, the device may work incorrectly. The minimal wait time for I²C communication is 5ms, during this period, some internal modules (such as LDO) start to work and reach a stable state.

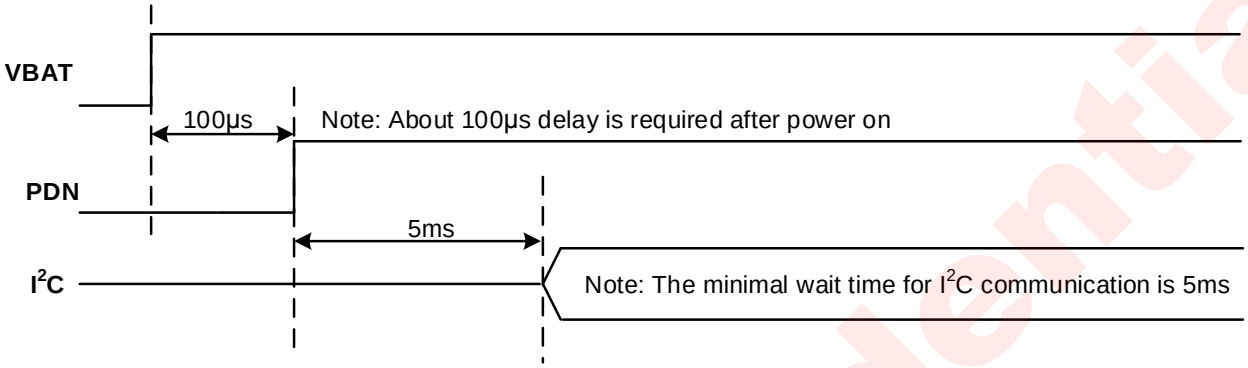


Figure 4 AW9233 Power On

9.1.2 Work Mode

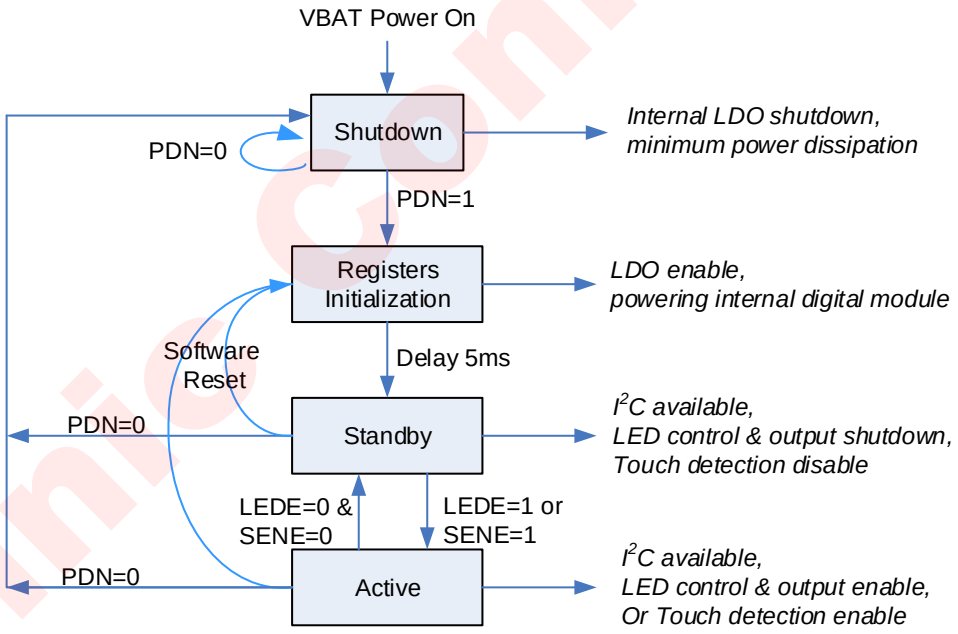


Figure 5 AW9233 Work Mode

After VBAT powered on, if PDN pin is low, the AW9233 is in shut-down mode, the current consumption is less than 15μA. When PDN pin becomes high, the internal LDO is activated, and a power-on reset (POR) signal is generated to initialize all internal registers, the device enters standby mode, this is a low power consumption mode, when all circuit functions are disabled. In standby mode, I²C interface is active, all internal configuration register can be written. If control bit GCR.SENE or/and GCR.LEDE is written high, the device enters the active mode.

9.2 RESET

9.2.1 Hardware Reset

When PDN pin changes from low to high, the power-up reset (POR) signal is generated, all internal registers are reset.

9.2.2 Software Reset

Writing 0x55AA to register RSTR via I²C interface will activate a software reset to reset all internal registers.

9.3 I²C INTERFACE

AW9233 supports the I²C serial bus and data transmission protocol in fast mode at 400kHz. It operates as a slave on the I²C bus. Connections to the bus are made via the open-drain I/O pins SCL and SDA. The pull-up resistor can be selected in the range of 1k~10kΩ and the typical value is 4.7kΩ. AW9233 can support different high level (1.8V~3.3V) of this I²C interface.

9.3.1 Device Address

The I²C device address (7-bit, followed by the R/W bit(Read=1/Write=0)) of AW9233 depends on the AD pin status. When AD level is low, the I²C address is 0x2C; when AD level is high, the I²C address is 0x2D.

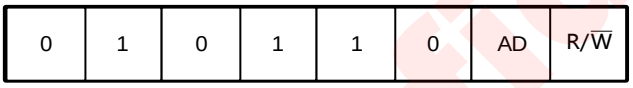


Figure 6 Device Address Configuration

9.3.2 Data Validation

When SCL is high level, SDA level must be constant. SDA can be changed only when SCL is low level.

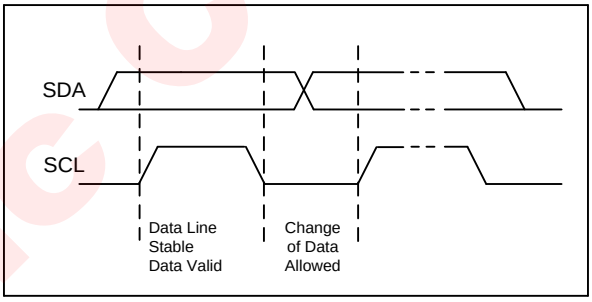


Figure 7 Data Validation Diagram

9.3.3 ACK(Acknowledgement)

ACK means the successful transfer of I2C bus data. After master sends 8bits data, SDA must be released; SDA is pulled to GND by slave device when slave acknowledges.

When master reads, AW9233 sends 8bit data, releases the SDA and waits for ACK from master. If ACK is send and I²C stop is not send by master, AW9233 sends the next data. If ACK is not send by master, AW9233 stops to send data and waits for I²C stop.

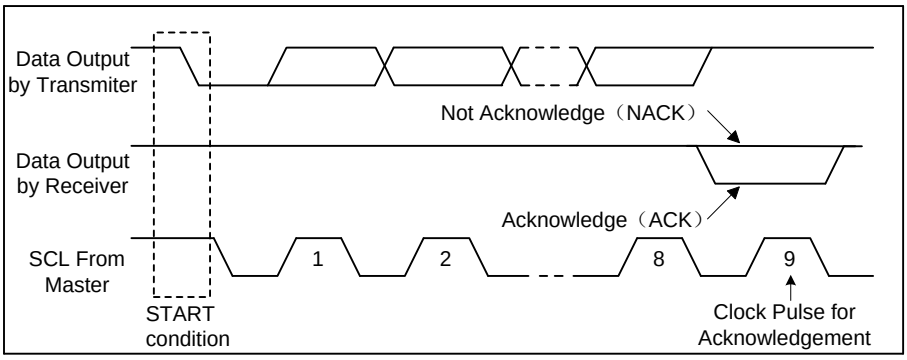


Figure 8 I²C ACK Timing

9.3.4 I²C Start/Stop

I2C start: SDA changes form high level to low level when SCL is high level.

I2C stop: SDA changes form low level to high level when SCL is high level.

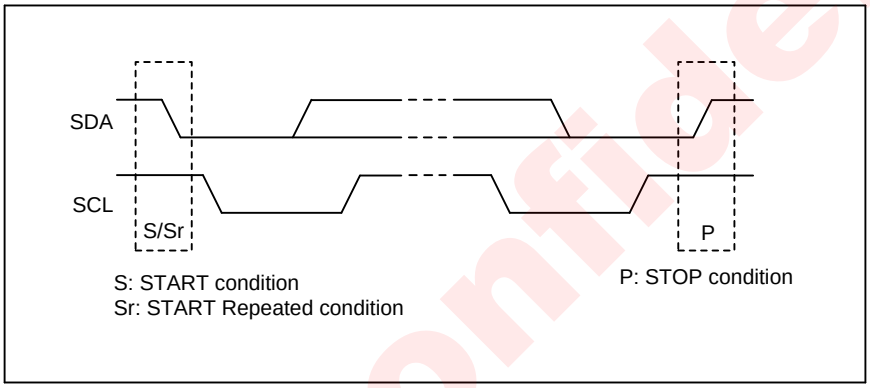


Figure 9 I²C Start/Stop Condition Timing

9.3.5 Write Cycle

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol permits a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a Start Condition, a number of byte transfers (set by the software) and a Stop Condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow.

In a write process, the following steps should be followed:

a) Master device generates START condition. The "START" signal is generated by lowering the SDA signal while the SCL signal is high.

b) Master device sends slave address (7-bit) and the data direction bit (W = 0).

c) Slave device sends acknowledge signal if the slave address is correct.

d) Master sends control register address (8-bit)

e) Slave sends acknowledge signal

f) Master sends data high 8Bit to be written to the addressed register

g) Slave sends acknowledge signal

h) Master sends data low 8Bit to be written to the addressed register

I) Slave sends acknowledge signal

j) Master generates STOP condition to indicate write cycle end

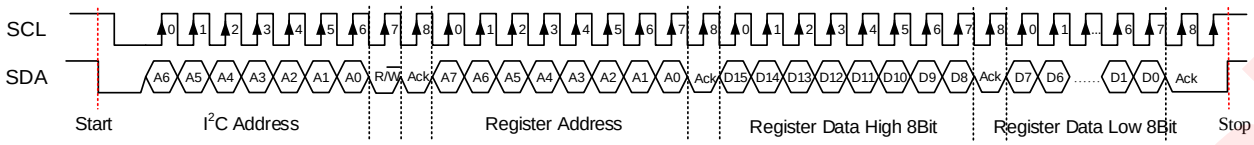


Figure 10 AW9233 I²C Write Timing

9.3.6 Read Cycle

In a read cycle, the following steps should be followed:

a) Master device generates START condition

b) Master device sends slave address (7-bit) and the data direction bit (W = 0).

c) Slave device sends acknowledge signal if the slave address is correct.

d) Master sends control register address (8-bit)

e) Slave sends acknowledge signal

f) Master generates STOP condition followed with START condition or REPEAT START condition

g) Master device sends slave address (7-bit) and the data direction bit (R = 1).

h) Slave device sends acknowledge signal if the slave address is correct.

i) Slave sends data high 8Bit from addressed register.

j) Master sends acknowledge signal

k) Slave sends data low 8Bit from addressed register.

l) If the master device sends acknowledge signal, the slave device will increase the control register address by one, then send the next data from the new addressed register. If master sends no acknowledge signal, the slave device stop to send data and wait for STOP condition.

m) If the master device generates STOP condition, the read cycle is ended.

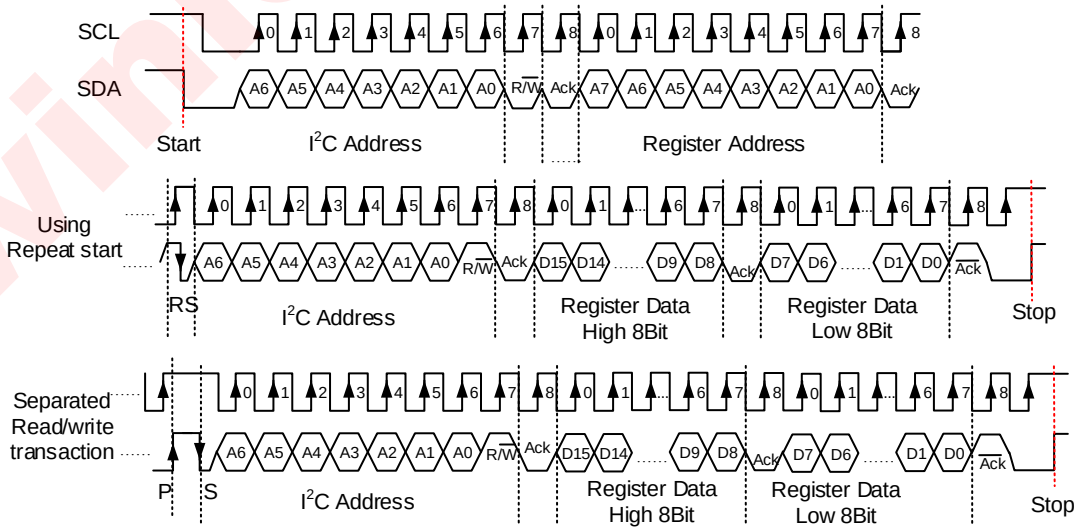


Figure 11 AW9233 I²C Read Timing

9.4 OSCILLATOR

An internal oscillator provides clock for both capacitive touch detecting and LED controlling circuit. If register bit GCR.SENE or GCR.LENE is high, the OSC starts to work, the start-up time is about 5 μs. When both the register bit GCR.SENE and GCR.LEDE are low, the internal OSC stops.

9.5 CAPACITIVE TOUCH DETECTION

With high performance sigma-delta capacitive digital conversion technology, the capacitance on SX pin is measured, the finger touch decision is made according to the increment of SX capacitance. Before finger touching, the key capacitance is only formed by the sensing electrode and surrounding ground, which is called intrinsic capacitance usually. When finger touching, an additional parallel plate capacitor capacitance (electrode-media-finger) is formed, resulting in the capacitance increment on pin SX. In general, because of the variation of different electrode size and dielectric characteristic of different media materials, the capacitance increment caused by finger touch is about 0.5pF～5pF.

In AW9233, the CDC resolution is 12Bit. the sampling period can be set by control register. The capacitive sample are send to DSP for further processing, including digital filtering, base-line compensation, touch and gesture judge, and so on.

The capacitive sensitivity can be adjusted by REXT resistance. The bigger the REXT value, the higher the sensitivity. By default, 10kΩ to GND resistor is recommended.

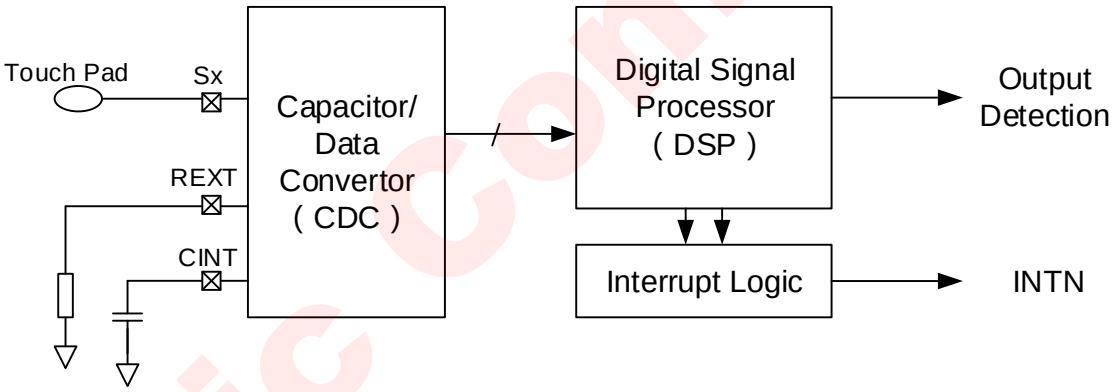


Figure 12 Functional Block of Capacitive Detection Circuit

When control bit GCR.SENE is 0, all capacitive touch detection circuit is reset. When control bit GCR.SENE is high, the SLPR register control the enable/disable touch detection. If control bit SLPR.SLPx is 0, channel x touch detection function is activated. If control bit SLPR.SLPx set to 1, channel x touch detection is disabled to save power consumption.

9.5.1 Touch Status and Interrupt

In AW9233 , the touch status can be read in register KEYST (0x31).

Touching status can generate the interrupt output on pin INTN, the interrupt enable control is defined by register KINTER (0x03). There are 4 interrupt mode selection defined by control bit KINTER.KIMD[1:0].

- KIMD[1:0] =00 interrupt generates when touch status changed
- KIMD[1:0] =01 interrupt generates when touch status changed from 1 to 0
- KIMD[1:0] =10 interrupt generates when touch status changed from 0 to 1
- KIMD[1:0] =11 interrupt generates when touch status is 1

The INTN pin will be pulled to GND when interrupt generates. The interrupt status can be clear by reading the register KISR (0x32) and INTN pin will be pulled up to V_{IO}.

9.5.2 Gesture Status

Besides for touch detection, AW9233 provides click gesture detection function, including slide gesture, single, double and triple click. Once the predefined gesture is detected，interrupt can be generated if corresponding interrupt enable bit is set in control register GIER. This function will help reduce programming on external MCU, and save the system power consumption, improve the usability.

The slide gesture detects the finger moving on the touchpad. When finger moves on the touchpad, the capacitive change can be detected one by one and the gesture module can identify the order of touch key and judge the slide gesture.

Register GSTR (0x20/0x21) defines the slide gesture.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	KCODE1			0	KCODE2			0	KCODE3			0	0	0	0

KCODE1~3 define 3bit key code. The code can be 3(s1), 4(s2), 5(s3), 0(no key).

The tap gesture is somewhat like the click on touchpad or touch screen. When finger clicks on the touchpad quickly, the single, double or triple click can be recognized. The continuously, fast finger click on touch area will make the touch detection status switching between ON and OFF quickly. By analyzing the characteristic of ON and OFF，pre-defined tap gesture can be detected. In practice application , the double tap gesture is now widely used.

Register TAPR(0x27) defines the click gesture.

Register TAPR:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	CSEL			0	0	TIMES	

TIMES defines the type of clicking, if TIMES =01, single click is enabled; if TIMES=10, double click is enabled; if TIMES=11, triple click is enabled, CSEL must set as 001 for AW9233.

The register GIER(0x2D) can enable/disable interrupt triggered by detected click gesture. When defined click gesture is detected, the TIS bit in register GISR will be set, if the TIE bit in register GIER is set, interrupt will occur. The TIS bit will be clear after register GISR is read via I^2C interface.

9.6 LED DRIVER

LED driver provide 3 current sources to drive LEDs, a dedicated Application-Specific-Processor（ASP）is designed to produce versatile lighting effect for mobile devices.

If the control bit GCR.LEDE is 0 , LED driver circuit is in reset state, all 3 LED outputs are disabled. If control bit GCR.LEDE is 1, the LED driver circuit is enabled, the control bit LER.LENx (x=1 to 3) configure the corresponding LED channel is active or not.

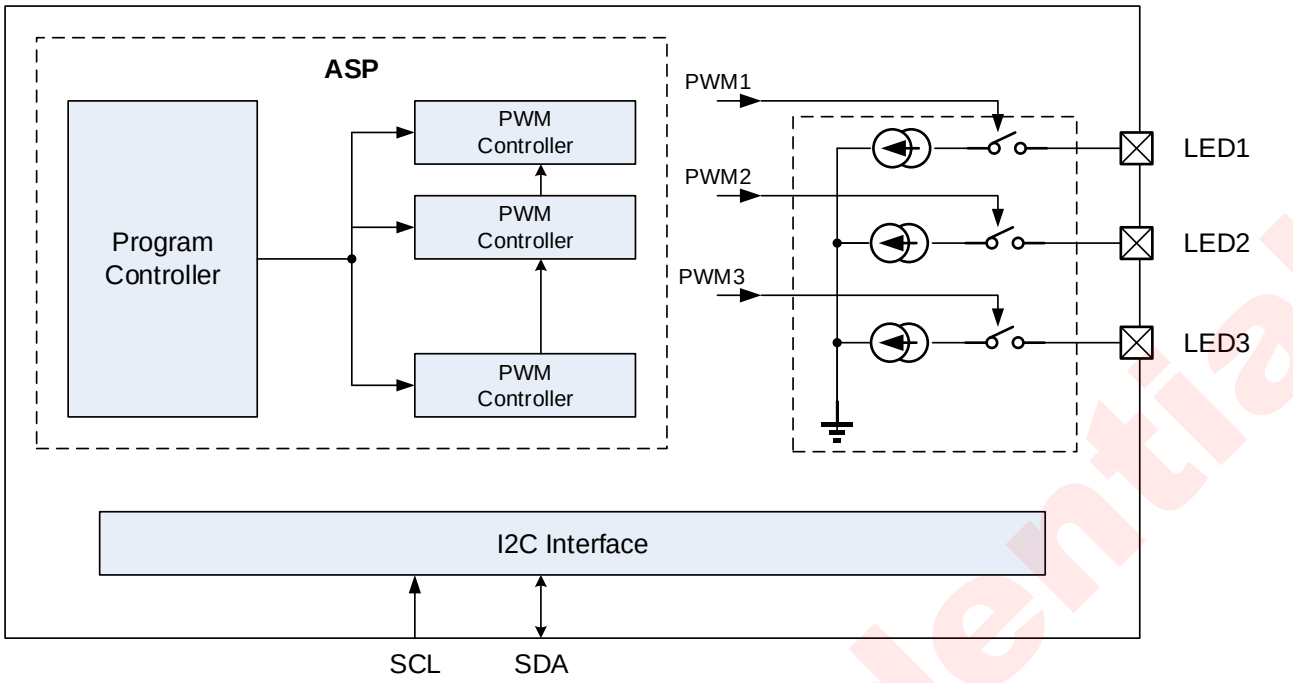


Figure 13 AW9233 LED Dimming Control Module Diagram

9.6.1 LED brightness controller

Pulse Width Modulation (PWM) is used to adjust the brightness of LED, 256 level brightness with 9bit resolution is adapted. The PWM frequency can be configured between 122Hz or 244Hz by control bit LCR.FREQ.

The ASP generates the PWM signal with dedicated and highly efficient dimming control instruction for all 9 independent LED constant current source. By programming, user-defined complicated lighting effect could be produced.

The LED control instruction executed by ASP could come from LED SRAM or external I^2C register. The register CTRS can choose every LED channel to be controlled by SRAM program or by I^2C register.

- CTRS[n] = 0, LED n controller is controlled by the internal SRAM instruction;
- CTRS[n] = 1, LED n controller is controlled by the external I^2C register.

9.6.2 LED Constant current driver

For each LED, the maximum output constant current is 24.5mA, with 8 level adjustable by register IMAXn (n=1~3).

9.6.3 ASP

ASP module is consist of one program controller and 3 PWM controllers.

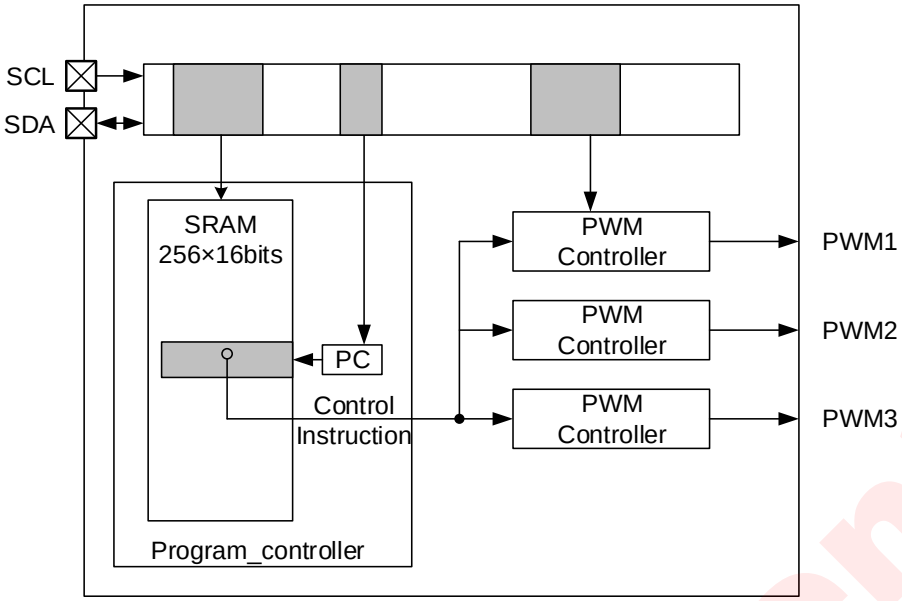


Figure 14 ASP Structure Diagram

9.6.3.1 Program Controller

The program controller is clocked by 32kHz internal clock, each instruction is executed in one clock cycle. The program controller is consist of a program SRAM, an algorithmic logic unit (ALU) and other internal registers. The 256x16bit internal SRAM is used to store LED lighting effect program loaded through I²C interface, the I²C interface also can start or stop the program execution. There are 4 internal registers RA/RB/RC/RD participating ALU operation so as to generate complicated program control such as repeating and looping. Except for that, there are 8 8bit temporary data registers(R1~R8) and 5 special function registers. Their internal address and function description is shown in the table below.

Table 1 Address allocation of internal data register in ASP

Register	Address(HEX)	Description
R1	00	R1 data temporary register，8bit，I²C readable
R2	01	R2 data temporary register，8bit，I²C readable
R3	02	R3 data temporary register，8bit，I²C readable
R4	03	R4 data temporary register，8bit，I²C readable
R5	04	R5 data temporary register，8bit，I²C readable
R6	05	R6 data temporary register，8bit，I²C readable
R7	06	R7 data temporary register，8bit，I²C readable
R8	07	R8 data temporary register，8bit，I²C reading
KST_AKS	08	Key AKS status register
KST	09	Key original status register
TISR1	0a	Key interrupt status register, clear by reading
TISR2	0b	Key interrupt status register, clear by reading
GMSK1	0d	Global control mask register(M3~M1)

Table 2 Special function registers definition

Register	B7	B6	B5	B4	B3	B2	B1	B0	Description
KST	-	-	-	KS3	KS2	KS1	-	-	Key status, KS= touched.

KST_AKS	-	-	-	AST3	AST2	AST1	-	-	Key AKS Status, Kx=1, Sx is touched
TISR1	-	-	-	KINT3	KINT2	KINT1	-	-	Touch interrupt status, cleared after read. KINTx=1 when touch interrupt active
TISR2	-	-	-	TAP	-	-	G2	G1	Gesture1/2 and TAP interrupt status register, cleared after reading.
GMSK1		M3		M2		M1	-	-	Mask control for global control instruction. When Mn=1, LEDn will not be affected by global control instruction.

9.6.3.2 PWM Controller

The PWM controller is execution unit of LED control instruction. There are 3 PWM controllers receiving the LED effect instruction from SRAM, and generate 8bit PWM code, which will be convert to 9bit duty cycle control code by logarithmic l transformation. If LCR.LOGLN=00, the transformation is natural logarithm($\log_e$). If LCR.LOGLN=01, the transformation is logarithm of 10 ($\log_{10}$), otherwise the 8b-to-9b transformation of PWM code is linear.

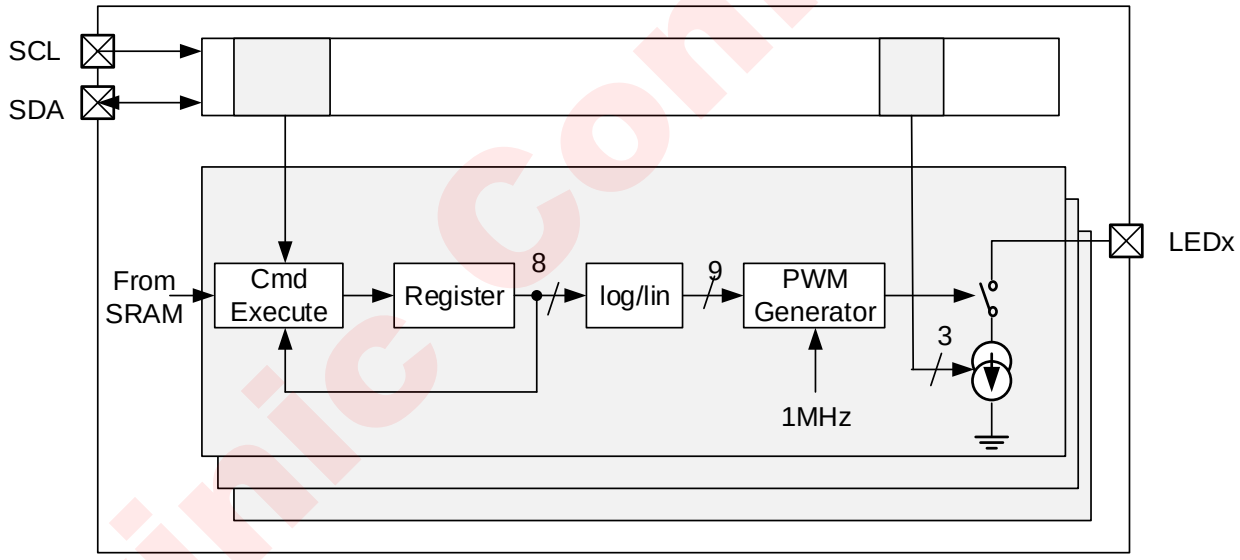


Figure 15 PWM Controller Schematic Diagram

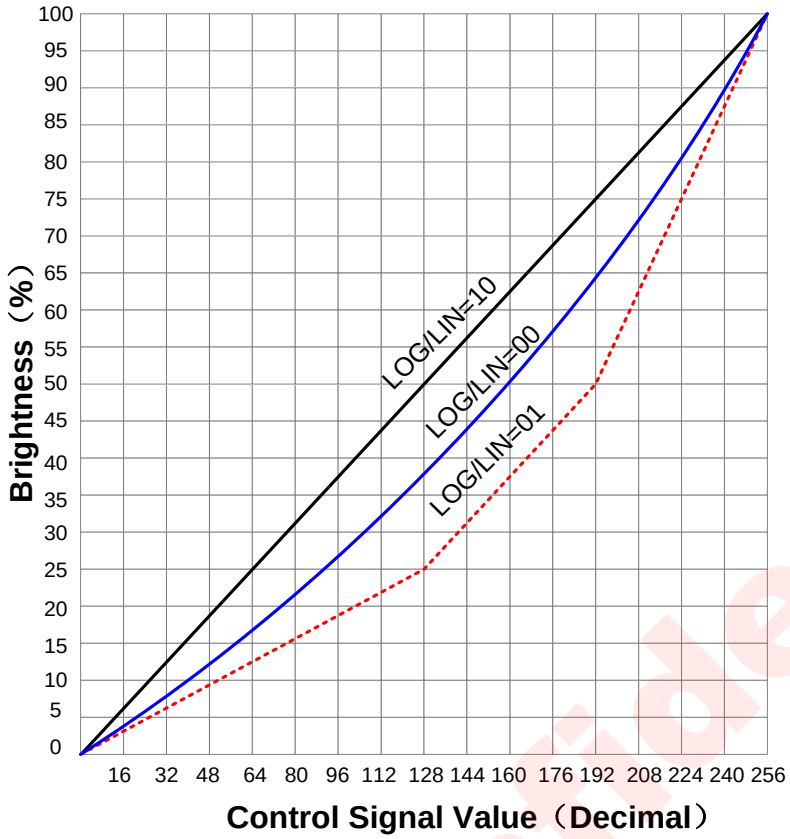


Figure 16 8bit-to-9bit PWM code transformation curve

9.6.3.3 Program Loading and execution

a) Program loading

It is recommended to load SRAM program only when control bit PMD.PROGMD is 00. In this state, the internal program can be read/write through I²C interface. When loading program, please write the SRAM loading address in register WADDR(0x7E) at first, and then write the 16bit LED effect instruction to register WDATA(0x7F). Continuously loading program is supported, after a 16b instruction is written through register WDATA, the value of WADDR will automatically plus by 1.

b) Program execution

Register bit PMD.PROGMD[1:0] controls the loading and execution mode of SRAM program.

When register bit IPMD.PROGMD[1:0]=00, program execution is shut down, SRAM program and program pointer(PC) are permitted to be loaded.

When IPMD.PROGMD[1:0] is written to be 01 from another value, current program will stop , and PC will be reload by register SADDR, and then executes the SRAM program starting from the address of PC

When Register bit PMD.PROGMD[1:0] =10, the SRAM program will be executed by the mode defined by register bit RMD.RUNMD[1:0]

Table 3 Program running mode control register

RMD.RUNMD	Function Description
0 0	Hold mode. program stop and PC hold after one instruction is finished.
0 1	Single step mode, only used for debugging. Once writing 01 to RUNMD, only one instruction will be executed with PC+1, and then RMD.RUMND is cleared (return to hold mode)

1 0	Continuously running mode, program starts from the address of PC.
1 1	Repeating mode, only used for debugging. Once writing 11 to RUNMD, current instruction will be executed without PC+1, and then RMD.RUMND is cleared (return to hold mode)

9.6.3.4 SRAM program Instruction

There are 27 commands in ASP instruction set, including LED control command, data operation and transfer command, wait and branch control command. The Rx,Ry and Rz in instruction list means the internal register RA, RB, RC and RD, each of them can participate the ALU operation as source or destination register.

Table 4 LED Effect Instruction

Command	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
JP	0	0	0	0	0	0	0	0	ADDR[7:0]							
NOP	0	0	0	0	0	0	0	1	-	-	-	-	-	-	-	-
-----	0	0	0	0	0	0	1	X								
JPZ Addr	0	0	0	0	0	1	0	0	ADDR[7:0]							
JPNZ Addr	0	0	0	0	0	1	0	1	ADDR[7:0]							
JPS Addr	0	0	0	0	0	1	1	0	ADDR[7:0]							
JPNS Addr	0	0	0	0	0	1	1	1	ADDR[7:0]							
LD Rz Im	0	0	0	0	1	0	Rz		Im[7:0]							
CMPI Rz Im	0	0	0	0	1	1	Rz		Im[7:0]							
ANDR Rz Im	0	0	0	1	0	0	Rz		Im[7:0]							
ORR Rz Im	0	0	0	1	0	1	Rz		Im[7:0]							
RDR Rz Addr	0	0	0	1	1	0	Rz		ADDR[7:0]							
WDR Rz Addr	0	0	0	1	1	1	Rz		ADDR[7:0]							
ADDI Rz Im	0	0	1	0	0	0	Rz		Im[7:0]							
AUBI Rz Im	0	0	1	0	0	1	Rz		Im[7:0]							
ADDR Rx Ry	0	0	1	0	1	0	Rz		-	-	-	-	Rx		Ry	
SUBR Rx Ry	0	0	1	0	1	1	Rz		-	-	-	-	Rx		Ry	
CMPR Rx Ry	0	0	1	1	0	0	0	0	-	-	-	-	Rx		Ry	
----	0	0	1	1	0	0	X	X								
END Int Rst	0	0	1	1	0	1	0	0	-	-	-	-	-	-	Int	Rst
INTN_MASKOFF	0	0	1	1	0	1	1	0	-	-	-	-	-	-	-	-
INTN_MASKON	0	0	1	1	0	1	1	1	-	-	-	-	-	-	-	-
WAITI Pre Time	0	0	1	1	1	Pre	T[9:0]									
SETPWMR Rx Ry	0	1	0	0	0	0	0	-	-	0	0	0	Rx		Ry	
RAMPR Dir Rx Ry	0	1	0	0	0	0	1	Dir	-	0	0	0	Rx		Ry	
SETSTEPTMRR Pre Rx Ry	0	1	0	0	0	1	0	-	Pre	0	0	0	Rx		Ry	
SETSTEPTMRI Pre Ch Im	1	0	0	Ch[4:0]					Pre	-	Im[5:0]					
SETPWMI Ch Im	1	0	1	Ch[4:0]					Im[7:0]							
RAMPI Dir Ch Im	1	1	Dir	Ch[4:0]					Im[7:0]							

a) Special LED Control Command

There are 3 types of LED control command.

- **SETPWM:** set the brightness level (0~255)for specified LED channel;
- **RAMP：** set the specified LED channel fade in or fade out for expected step(0~255)
- **SETSTEP：** set the fading slope for specified LED channel;

All control parameter in above commands can either come from specified register (RA~RD), or from immediate data contained in command..

All LED control command supports broadcast mode, one instruction may send to multiple or all LEDs

When SRAM program running, if Ch field or value of Rx in LED control command is '11111', the current command is active for all LED with setting of CTRSR.bitn=0. If Ch field or value of Rx in LED control command is '11110', the current command is only active for those channel with setting of GMSKx=0.

When LED instruction is come from I^2C interface directly, it is recommended to use only the command with immediate data. If the Ch field in command is "11111", the current command is only active for those LED with STRSR.bitn=1..

Table 5 LED Control Instruction explanation

Instruction	Description
Register Parameter	
SETPWMR Rx Ry	**Set the PWM brightness level with parameter in register** Rx: LED channel number, 2,4,6 for LED 1~ LED 3 respectively Ry: Brightness level, 0~255
RAMPR Dir Rx Ry	**Set the Fade-in/Fade-out for specified step with parameter in register** Dir: 1: Fade-in; 0: Fade-out Rx: LED channel number, 2,4,6 for LED 1~ LED 3 respectively Ry: the step number of Fade-in/Fade-out
SETSTEPTMRR Pre Rx Ry	**Set the RAMP slope with parameter in register** Pre: basic time unit, 0: 0.5ms; 1: 16ms Rx: LED channel number, 2,4,6 for LED 1~ LED 3 respectively Ry: RAMP step time = (Ry+1)*Pre, 0~255
Immediate Data	
SETPWMI Ch Im	**Set the PWM brightness level with immediate parameter** Ch: LED channel number, 2,4,6 for LED 1~ LED 3 respectively Im: Brightness level, 0~255
RAMPI Dir Ch Im	**Set the Fade-in/Fade-out for specified steps with immediate parameter** Dir: 1: Fade-in; 0: Fade-out Ch: LED channel number, 2,4,6 for LED 1~ LED 3 respectively Im: the steps of Fade-in/Fade-out
SETSTEPTMRI Pre Ch Im	**Set the RAMP step time with immediate parameter** Pre: basic unit of time, 0: 0.5ms; 1: 16ms Ch: LED channel number, 2,4,6 for LED 1~ LED 3respectively Im: RAMP step time = (Im +1)*Pre, 0~255

Table 6 Program Control and operation Instruction

Instruction	Encoding	Description
branch Instruction		
JP Addr	0x00xx	Immediate Jump, jump to PC = Addr
JPZ Addr	0x04xx	Conditional Jump, If Rz is 0, jump to PC = Addr
JPNZ Addr	0x05xx	Conditional Jump, If Rz is not 0, jump to PC = Addr
JPS Addr	0x06xx	Conditional Jump, If Rz < 0, jump to PC = Addr
JPNS Addr	0x07xx	Conditional Jump, If Rz >= 0, jump to PC = Addr
Data Transfer Instruction		
LD Rz Im	0x08xx - 0x0bxx	Rz = Im
RDR Rz Addr	0x18xx - 0x1bxx	Rz = *Addr
WDR Rz Addr	0x1cxx - 0x1fxx	*Addr = Rz
Computation Instruction		
CMPI Rz Im	0x0cxx - 0x0fxx	Rz – Im, only change S/Z flag
CMPR Rx Ry	0x30xx	Rx – Ry, only change S/Z flag
ANDR Rz Im	0x10xx - 0x13xx	Rz = Rz & Im, affect S/Z flag
ORR Rz Im	0x14xx - 0x17xx	Rz = Rz | Im, affect S/Z flag
ADDI Rz Im	0x20xx - 0x23xx	Rz = Rz + Im, affect S/Z flag
SUBI Rz Im	0x24xx - 0x27xx	Rz = Rz - Im, affect S/Z flag
ADDR Rz Rx Ry	0x28xx - 0x2bxx	Rz = Rx + Ry, affect S/Z flag
SUBR Rz Rx Ry	0x28xx - 0x2bxx	Rz = Rx - Ry, affect S/Z flag
Control Instruction		
END Int Rst	0x34xx	Program end with optionally reset register RMD and generate interrupt Int= 0: no interrupt after instruction executed;

		Int= 1: generate interrupt after instruction executed Rst=0: PC add 1 after instruction executed; Rst=1: Reload PC with SADDR after instruction executed
INTN_MASKOFF	0x36xx	Unmask internal interrupt
INTN_MASKON	0x37xx	Mask internal interrupt
WAITI Pre Time	0x38xx - 0x3fxx	Wait for specified time Pre: time of basic waiting cycle, 0: 0.5ms; 1: 16ms Time: number of waiting cycle, max value is 1023, wait time=Pre*Time

9.6.3.5 Example

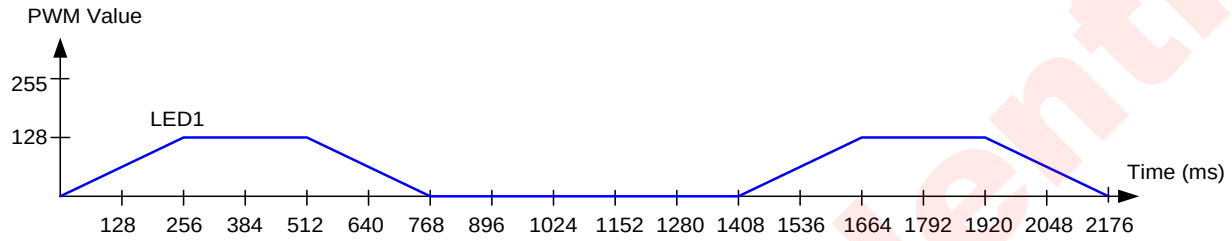


Figure 17 LED Effect Programming Diagram

Table 7 Reference Instruction of LED Effect Programming

PC	Assemble Instruction	Machine Code	explanation
0	SETSTEPTMRI 0x00 0x1F 0x03	0x9F03	RAMPI step time: 2ms
1	SETPWMI 0x1F 0x00	0xBF00	ALL LED turn off
	START:		Address Label “START” (02H)
2	RAMPI 0x01 0x02 0x80	0xE280	LED1 fade in, 128 steps breath
3	WAITI 0x01 0x20	0x3C20	Wait 512ms
4	RAMPI 0x00 0x02 0x80	0xC280	LED1 fade out, 128 steps breath
5	WAITI 0x01 0x38	0x3C38	Wait 896ms
6	JP START	0x0002	Jump to START, PC=2

Step1: Power On, configure register

- VBAT power on, 4.2V
- Pull PDN to 3V
- Wait 5ms
- GCR = 0x0001 // enable LED module
- LER = 0x0004 // enable LED1
- IMAX1 = 0x0100 // IMAX1 = 3.5mA
- PMD.PROGRMD = 00 //hold mode
- RMD.RUNMD = 00 //hold mode

Step2: Load Instruction to SRAM

- WADDR = 0x0000 // load program starting at address =0x0000
- WDATA = 0x9F03
- WDATA = 0xBF00
- WDATA = 0xE280
- WDATA = 0x3C20
- WDATA = 0xC280

- WDATA = 0x3C38
- WDATA = 0x0002

Step3: Run

- SADDR = 0x0000
- RMD.RUNMD = 10 // execution mode change to run mode,
- PMD.PROGMD = 01 // start program from 0x0000

9.7 Link touch status to LED lighting effect

There are two optional ways to connect touch status to LED lighting effect inside the device: direct output mode and program mode .

In direct output mode, the touch detection status directly turn on or off the specified LED. In program mode, user can adapt internal touch and gesture interrupt to start LED lighting effect program to generate complex touch feedback.

9.7.1 Direct output mode

If the OE bit in register OSR is 1, the touch status directly output to the LED defined by bit LSEL[3:0] in register OSR. When touch detected, the LED turn on, when touch released, the LED turns off.

The control bit OSR.LSEL[3:0] defines which LED display the touch status:

- OSR.LSEL[3:0]=0010, touch status sent to LED1
- OSR.LSEL[3:0]=0100, touch status sent to LED2
- OSR.LSEL[3:0]=0110, touch status sent to LED3

The control bit FON/ FOF in register OSR select the transition way between state on and off

- OSR.FON=1, turn on LED in smooth way (fade in) when touch detected;
- OSR.FON=0, turn on LED immediately (without fade-in) when touch detect;

- OSR.FOF=1, turn off LED in smooth way (fade out) when touch released
- OSR.FOF=0, turn off LED immediately (without fade-out) when touch released

When OSRx.FOF/FON=1, the speed of fade in/fade out is set by external MCU control command (SETSTEP) through I^2C interface.

9.7.2 Program mode

In general, ASP program can check touch and gesture status in internal register Key Status Register(KST), Touch Interrupt status register (TISR1,TISR2), As soon as touch or gesture is detected, program can jump to special subroutine to generate user-predefined lighting effect.

Besides status polling, Interrupt control is supported by ASP. When touch and gesture are detected, the register bit TISR1.KIS, and TISR2.TAP will be set, if control bit TIER.KIE and/or TIER.TIE is set (internal interrupt enabled), internal interrupt mechanism will trigger PC pointer jump to the address defined by interrupt vector register (TIVEC) to execute interrupt subroutine. The interrupt status register TISR1/TISR2 should be done at the beginning of interrupt subroutine, and after read out, TISR1/TISR2 well be cleared automatically.

Touch Interrupt Enable register (TIER) defines 2 interrupt sources. The first is KIE that enable key touch interrupt, which has 4 types of interrupt mode configured by control bit LCR.LINMD[1:0]. The second is TIE that enable TAP gesture interrupt. Both interrupts have the same priority.

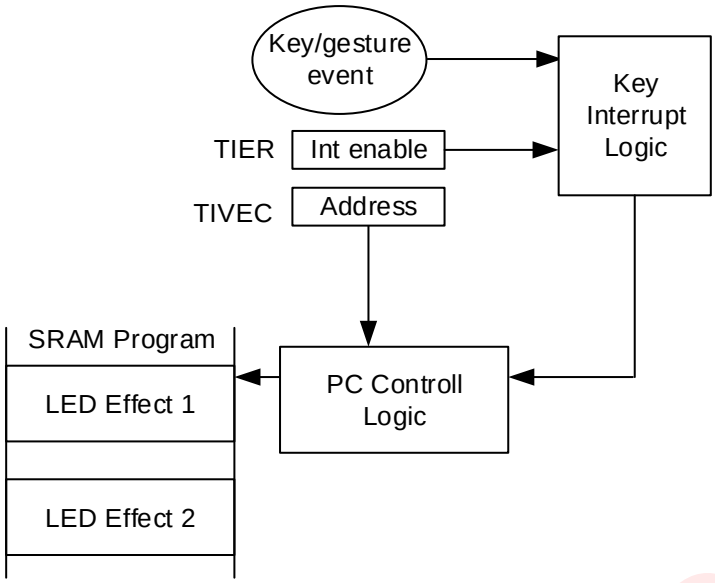


Figure 18 Key/gesture event trigger LED program interrupt

10 REGISTER DESCRIPTION

10.1 REGISTER CONFIGURATION

Address	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	IDRST	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0x01	GCR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SENE	LEDE
0x02	SLPR	0	0	0	0	0	0	0	0	0	0	0	SLP	SLP	SLP	0	0
0x03	KINTER	0	0	0	0	0	0	KIMD		FRME	0	0	IE3	IE2	IE1	0	0
0x04	-	RESERVED															
0x05	OSR1	OE2	FON2	FOF2	0	0	LSEL2			OE1	FON1	FOF1	0	0	LSEL1		
0x06	OSR2	0	0	0	0	0	0	0	0	OE3	FON3	FOF3	0	0	LSEL3		
0x07	AKSCR	0	0	0	0	0	0	0	0	0	0	0	ASEL			0	0
0x08	SLSR			SLID_INTERVAL						TT	0	0	SLIDSEL			0	0
0x09 0x0A 0x0B	-	RESERVED															
0x0C 0x0D 0x0E	JDGTHR	CLRTH								SETTH							
0x0F	-	RESERVED															
0x10	THR	0x08								NOISTH							
0x11	SCFG1	0	0	0	0	0	0	0	0	SCMD	0	NSMD	SCNUM				
0x12	SCFG2	0	0	0	0	0	SEED			RFFLTEN	0		SENS				
0x13	-	RESERVED															
0x14	OFSR1	0	0	0	EN2	OFFSET2				0	0	0	EN1	OFFSET1			
0x15	OFSR2	0	0	0	0	0	0	0	0	0	0	0	EN3	OFFSET3			
0x16	DOFCR1	DOF2				DOF1				0	0	0	0	0	0	0	0
0x17	DOFCR2													DOF3			
0x18	IDLECR	INCR[7:0]								0	IPER[6:0]						
0x19	MTOTR	0								MOT							
0x1A	DISMAX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0x1B	SETCNT	CCNT								SCNT							
0x1C	BLCTH	BLU								BLD							
0x1D	BLDTH	0	0	0	0	0	0	0	0	BLDTH							
0x1E	MCR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	DSEL	
0x1F	-	RESERVED															
0x20	GDCFGR	0	0	0	0	0	0	GSTMD		AKST	AKSG	0	S3	S2	S1	0	0

Address	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x21	GDTR	0	0	0	0	0	0	0	0	GOFFMAX							
0x22	TDTR	TONMAX								TOFFMAX							
0x23	GEST1	0	KEY1			0	KEY2			0	KEY3			0	0	0	0
0x24	GEST2	0	KEY1			0	KEY2			0	KEY3			0	0	0	0
0x25	-	RESERVED															
0x26	-	RESERVED															
0x27	TAPR	0	0	0	0	0	0	0	0	0	S3	S2	S1	0	0	TIMES	
0x28 - 0x2C	-	RESERVED															
0x2D	GIE	0	0	0	0	0	0	0	0	0	0	0	TIE1	0	0	GIE2	GIE1
0x2E	GIS	0	0	0	0	0	0	0	0	0	0	0	TIS1	0	0	GIS2	GIS1
0x2F	GTIMR	0	0	0	0	0	0	0	0	GTIMR							
0x30	KISR	0	0	0	0	0	0	0	IDST	0	-	0	INT3	INT2	INT1	0	0
0x31	RAWST	0	0	0	0	0	0	0	0	0	0	0	S3	S2	S1	0	0
0x32	KEYST	0	0	0	0	0	0	0	0	SBI	0	0	S3	S2	S1	0	0
0x33 0x34	-	RESERVED															
0x35	SMOVCNT	0								MOVCNT							
0x36 0x37	-	RESERVED															
0x38 0x39 0x3A	KDATA1 KDATA2 KDATA3	KDATA															
0x3B	-	RESERVED															
0x50	LER	0	0	0	0	0	0	0	0	0	LE3	0	LE2	0	LE1	0	0
0x51	-	RESERVED															
0x52	LCR	0	0	0	0	0	0	0	SRMINI	LIRMD		TIMD		LIE	FREQ	LOG/LIN	
0x53	PROGMD	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PROGMD	
0x54	RUNMD	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RUNMOD	
0x55	CTRS	0	0	0	0	0	0	0	0	0	CS3	0	CS2	0	CS1	0	0
0x56	-	RESERVED															
0x57	IMAX1	0				0	IMAX1			0				0			
0x58	IMAX2	0				0	IMAX3			0				0	IMAX2		
0x59 0x5A 0x5B	-	RESERVED															
0x5C	TIER	0	0	0	0	0	TIE	0	0	GIE2	GIE1	0	KIE3	KIE2	KIE1	0	0

Address	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x5D	TIVEC	0	0	0	0	0	0	0	0	TIVEC							
0x5E	ISR2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	LIS
0x5F	SADDR	0	0	0	0	0	0	0	0	SADDR							
0x60	PCR	0	0	0	0	0	0	0	0	PC							
0x61	CMDR	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0x62	RA	0	0	0	0	0	0	0	0	RA							
0x63	RB	0	0	0	0	0	0	0	0	RB							
0x64	RC	0	0	0	0	0	0	0	0	RC							
0x65	RD	0	0	0	0	0	0	0	0	RD							
0x66 ~ 0x6D	R1 ~ R8	0								R1 ~ R8							
6E	GRPR	0	0	0	0	0	0	0	0	0	GS3	0	GS2	0`	GS1	0	D0
7D	WP	WPW								0	0	0	0	0	0	0	0
7E	WADDR	0	0	0	0	0	0	0	0	ADDR							
7F	WDATA	CODE															

10.2 GLOBAL REGISTER DESCRIPTION

10.2.1 IDRST, Chip ID and Software Reset

Address: 0x00, R/W															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bit	Symbol		Description												
15:0	IDRST		Chip ID: 0xB223 Software Reset: write 0x55AA to IDRST, reset the whole device.												

10.2.2 GCR, Global Control Register

Address: 0x01, R/W, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	SENE	LEDE
Bit	Symbol		Description												
0	LEDE		LED driver function 0: disable LED driver (default) 1: enable LED driver												
1	SENE		Touch Key detection function 0: disable touch key detection (default) 1: enable touch key detection												

10.3 CAPACITIVE TOUCH DETECTION REGISTERS

10.3.1 SLPR, Sensor Sleep Control Register

Address: 0x02, R/W, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	SLP3	SLP2	SLP1	0	0
Bit	Symbol		Description												
0	SLP3~SLP1		Sensor sleep control 0: sensor work (default) 1: sensor sleep												

10.3.2 KINTER, Key Interrupt Enable Register

Address: 0x03, R/W, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	KIMD		FRME	0	0	IE3	IE2	IE1	0	0
Bit	Symbol		Description												
4:2	IE3~1		Key Interrupt enable, pull INTN to GND when triggering interrupt. 0: disable interrupt (default) 1: enable interrupt												
5:6	-		Reserved, must be 0												
7	FRME		Sensor Scan Frame interrupt enable 0: disable frame interrupt (default) 1: enable frame interrupt												
9:8	KIMD		Interrupt mode 00: interrupt occurs when touch status changed (default) 01: interrupt occurs when touch status changed from 1 to 0 10: interrupt occurs when touch status changed from 0 to 1 11: interrupt occurs when touch status is 1												

10.3.3 OSR1~2, Touch Status Connecting LED Control Register

Address: 0x05~0x06, R/W, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OE2	FON2	FOF2	0	0	LSEL2			OE1	FON1	FOF1	0	0	LSEL1		

0	0	0	0	0	0	0	0	OE3	FON3	FOF3	0	0	LSEL3
Bit	Symbol		Description										
	-		Reserved, must be 0										
15/7	OEx		Enable Touch status output to one of selected LED 0: disable (default) 1: enable										
14/6	FONx		Touch status related LED fade in control. 0: LED reach max brightness directly when touch occur (default) 1: LED fade in when touch occurs										
13/5	FOFx		Touch status related LED fade out control 0: LED turn off immediately when touch status changes from 1 to 0 (default) 1: LED fade out when touch status changes from 1 to 0										
10:8/2:0	LSELx		LED select for Touch status output directly LSEL=0, No LED is selected (default) LSEL=2, LED1 is selected LSEL=4, LED2 is selected LSEL=6, LED3 is selected Others, no LED is selected										

10.3.4 AKSCR, Adjacent Key Suppression Configuration Register

Address: 0x07, R/W, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	ASEL[3:1]			0	0
Bit	Symbol		Description												
4:2	ASEL		Adjacent Key Suppression Configuration, only one of ASEL=1 keys can be triggered.												

10.3.5 SLSR, Slide Configuration Register

Address: 0x08, R/W, default: 0x0200															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	SLID_INTERVAL						TT	0	0	SLIDSEL			0	0
Bit	Symbol		Description												
4:3	SLIDSEL		Slide Configuration 0: Unused for slide configuration 1: Used for slide configuration												
6	-		Reserved, must be 0												
7	TT		Sliders coordinate detection mode 0: Not end to end mode 1: End to end mode												
13:8	SLD_INTERVAL		Key interval time of slider detection effective, T=SLIDINTVAL*Tscan(one frame cycle)												

10.3.6 JDGTHRn, key status judge configuration register

Address: 0x0C~0x0E, R/W, default: 0x080F															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLRTH								SETTH							
Bit	Symbol		Description												
0:7	SETTH		Touch on threshold												
15:8	CLRTH		Touch off threshold												

10.3.7 NOISETHR, Noise Threshold Register

Address: 0x10, R/W, default: 0x080F															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x08								NOISETH							
Bit	Symbol		Description												
7:0	NOISETH		Noise gate threshold (default value is 0x0F)												
15:8	-		Reserved, must be 8												

10.3.8 SCFG1, Scan Configuration Register

Address: 0x11, R/W, default: 0x0004																
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0		0	0	0	0	SCNMD	0	0	SCNUM				

Bit	Symbol	Description
4:0	SCNUM	Scan cycle number, default value is 4. The bigger scan cycle number, the longer scan time, and the higher the detection sensitivity. SCNUM=0, 256 SCNUM!=0, SCNUM*512
7	SCNMD	Scan mode 0: scan all keys, the cycle time is constant 1: scan the selected keys
15~8	-	Reserved, must be 0

10.3.9 SCFG2, Scan Configuration Register

Address: 0x12, R/W, default: 0x0107															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	SEED			RFFLTEN		0		SENS			

Bit	Symbol	Description
3:0	SENS	Sensitivity configuration, there are 16 level available. The less the value of SENS, the higher the sensitivity. 0000 is the highest sensitivity, 1111 is the lowest sensitivity, the default value is 0111.
5:4	-	Reserved, must be 0
7:6	RFFLTEN	RF filter enable, when enable RF filter, SCFG1.SCNUM should be bigger than 4. 00: RF filter off (default) 01: RF filter mode 1 enable 10: RF filter mode2 enable 11: RF filter off
10:8	SEED	ADC output data length selection 000: ADC/16 001: ADC/8 (default) 010: ADC/4 011: ADC/2 100: ADC/1

10.3.10 OFSR1, Key Capacitance Offset Register

Address: 0x14, R/W, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	OFSEN2	OFFSET2				0	0	0	OFSEN1	OFFSET1			

Bit	Symbol	Description
3:0	OFFSET1	S1 capacitance offset value
4	OFSEN1	S1 capacitance offset enable
7:5	-	Reserved, must be 0
11:8	OFFSET2	S2 capacitance offset value
12	OFSEN2	S2 capacitance offset enable
15:13	-	Reserved, must be 0

10.3.11 OFSR2, Key Capacitance Offset Register

Address: 0x15, R/W, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	OFSEN3	OFFSET3			

Bit	Symbol	Description
3:0	OFFSET3	S3 capacitance offset value
4	OFSEN3	S3 capacitance offset enable
7:5	-	Reserved, must be 0
15:8	-	Reserved, must be 0

10.3.12 DOFCR1-2, ADC Digital Offset Register

Address: 0x16~0x17, R/W, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DOF2				DOF1				-							
-												DOF3			

Bit	Symbol	Description
11:8 15:12 3:0	DOFx	digital offset of ADC data. Since the ADC is 12bit, if the key parasitic capacitance is large enough , ADC data will be more than 12 bit and overflow. The digital offset can compensate partly the ADC data within acceptable range by minus a setting value. 0000 : offset= 0 (default) 0001: offset = 2000 0010: offset = 4000 0011: offset = 6000 0100: offset = 8000 0101: offset = 10000 0110: offset = 12000 0111: offset = 14000 1xxx: not used

10.3.13 IDLECR, IDLE Status Configuration Register

Address: 0x18, R/W, default: 0x1805															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INCR								0	IPER						

Bit	Symbol	Description
6:0	IPER	Scan period setting in IDLE mode, default is 05H Scan once every IPER normal scan periods
7	-	Reserved, must be 0
15:8	INCR	Time to enter IDLE mode, if no touch detected. The actual time can be calculated as : $T=INCR*T_{SCAN}*16$。

10.3.14 MTOTR, Maximum Touch On Time Register

Address: 0x19, R/W, default:0x0010															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0								MOT							

Bit	Symbol	Description
7:0	MOT	Maximum time of keeping touch on status, $T= MOT*T_{SCAN}*128$ T_{SCAN} is capacitance touch key scanning cycle. T_{SCAN} = Keys * SCNUM * 2us
15:8	-	Reserved, must be 0

10.3.15 DISMAX, Maximum Margin of Valid Data

Address: 0x1A, R/W, default: 0x0040															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DISMAX															

Bit	Symbol	Description
15:0	DISMAX	Maximum margin of valid data When the different of two consecutive raw data is larger than DISMAX, discard the raw data.

10.3.16 SETCNT, Touch Decision De-bounce Count

Address: 0x1B, R/W, default: 0x0404															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CCNT								SCNT							

Bit	Symbol	Description
7:0	SCNT	Touch on de-bounce threshold In no touch state, if delta over SETTHR for SCNT times continuously, touch status is set to1.
15:8	CCNT	Touch release de-bounce threshold In touch state, if delta below CLRTHR for CCNT times continuously, touch status is

		cleared.

10.3.17 BLCTH, Baseline Trace Configuration Register

Address: 0x1C, R/W, default: 0x1008															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BLU								BLD							

Bit	Symbol	Description
7:0	BLD	Baseline trace down speed, default value is 0x08 The bigger the BLD, the slower the trace down.
15:8	BLU	Baseline trace up speed, default value is 0x10 The bigger the BLU, the slower the trace up.

10.3.18 BLDTH, Baseline Reset Threshold

Address: 0x1D, R/W, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0								BLDTH							

Bit	Symbol	Description
7:0	BLDTH	Baseline abnormal threshold. If row data is less than the value of BLDTH, re-calibration of baseline will be activate. if BLDTH is 0x00, actual abnormal threshold is the same as SETTHR
15:8	-	Reserved, must be 0

10.3.19 MCR, Monitor Control Register

Address: 0x1E, R/W, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	DSEL	

Bit	Symbol	Description
1：0	DSEL	KDATA register output data type selection in DEBUG mode 00: Normal mode , KDATA =0 (default) 01: delta data 10: baseline data 11: raw data

10.3.20 GDCFGR, Gesture Detection Configuration Register

Address: 0x20, R/W, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	GSTMD		AKST	AKSG	0	S3	S2	S1	0	0

Bit	Symbol	Description
5:0	S3~S1	Gesture detection channel choice 0: disable gesture detection 1: enable gesture detection
6	AKSG	0: gesture detection without AKS key status 1: gesture detection with AKS key status
7	AKST	0: tap detection without AKS key status 1: tap detection with AKS key status
9:8	GSTMD	Gesture detection interrupt report mode 00: report after some time when finger leaving 01: report when finger leaving 1x: report when detecting gesture

10.3.21 GDTR, Gesture Detection Time Register

Address: 0x21, R/W, default: 0x07															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	GOFFMAX							

Bit	Symbol	Description
7:0	GOFFMAX	Maximum touch off time of gesture detection

		When finger moves, the touching cannot be detected some times. The gesture ends when the time of touch off over T_{OFFMAX}=GOFFMAX*T_{SCAN}.

10.3.22 TDTR, Tap Detection Register

Address: 0x22, R/W, default: 0x080F

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TONMAX								TOFFMAX							

Bit	Symbol	Description
15:8	TONMAX	Maximum touch on time of tap detection The tap is invalid when touch on time over T_{ONMAX}=TONMAX*T_{SCAN}.
7:0	TOFFMAX	Maximum touch off time of tap detection When finger taps, the touching cannot be off some times. The tap ends when the time of touch off over T_{OFFMAX}=TOFFMAX*T_{SCAN}.

10.3.23 GSTR1~2, Gesture Configuration Register

GSTR1: address: 0x23, R/W, default: 0x2340
GSTR2: address: 0x24, R/W, default: 0x4320

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	KCODE1			0	KCODE2			0	KCODE3			0	0	0	0

Bit	Symbol	Description
14:12	KCODE1	Gesture order of number 1 sensor channel 0: None 3: S1 4: S2 5: S3
10:8	KCODE2	Gesture order of number 2 sensor channel 0: None 3: S1 4: S2 5: S3
6:4	KCODE3	Gesture order of number 3 sensor channel 0: None 3: S1 4: S2 5: S3
3:0	-	Reserved, must be 0

The sensor channel is touched one by one when finger moves. AW9233 judges the touch order is the predefined order or not.

KCODE1 is the first touching sensor channel and then KCODE2/3 is detected.

Every gesture configuration must be more than 2 sensor channel and the other is set to 0.

The register is invalid if KCODE1 is 0.

10.3.24 TAPR, Tap Gesture Configuration Register

Address: 0x27, R/W, default: 0x12

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	CSEL			0	0	TIMES	

Bit	Symbol	Description
1:0	TIMES	Click times 1: single click 2: double click (default) 3: triple click
6:4	CSEL	Tap sensor channel selection 0: disabled 1: enable
15:8	-	Reserved, must be 0

10.3.25 GIER, Gesture Interrupt Enable Register

Address: 0x2D, R/W, default: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	TIE	0	0	GIE2	GIE1

Bit	Symbol	Description
1:0	GIE2~1	Gesture detection interrupt 0: disable interrupt 1: enable interrupt
4	TIE	Tap gesture detection interrupt enable 0: disable interrupt 1: enable interrupt
15:5	-	Reserved, must be 0

10.3.26 GISR, Gesture Interrupt Status Register

Address: 0x2E, R(cleared after reading), default: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	TIS	0	0	GIS2	GIS1

Bit	Symbol	Description
1:0	GIS2～1	Gesture detection interrupt status 0: no gesture interrupt 1: gesture interrupt
4	TIS	Tap interrupt status 0: no tap interrupt 1: tap interrupt
15:5	-	Reserved

10.3.27 GTIMR, Gesture Duration Register

Address: 0x2F, R, default: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	GTIMR							

Bit	Symbol	Description
7:0	GTIMR	Gesture duration timer, from touch on to touch off T_{GEST} = GTIMR*T_{SCAN}, 0: no limit

10.3.28 RAWST, Raw Key Status Register

Address: 0x30, R, default: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	IDLST	0	0	0	S3	S2	S1	0	0

Bit	Symbol	Description
4:2	S3～1	Touch status 0: no touch 1: touch on
8	IDLST	IDLE status indication 0: normal scan 1: IDLE mode status

10.3.29 KEYST, AKS Key Status Register

Address: 0x31, R, default: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	S3	S2	S1	0	0

Bit	Symbol	Description
4:2	S3～1	AKS key status 0: no touch 1: touch on

10.3.30 KISR, Key Interrupt Status Register

Address:0x32, R(clear by reading), default: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	SBI	-	-	IS3	IS2	IS1	-	-

Bit	Symbol	Description
4:2	IS3～1	Key interrupt status 0: no key interrupt 1: key interrupt
7	SBI	Set 1 every frame, clear by reading

10.3.31 MOVCNTR, Slider Move Counter Register

Address: 0x35, R(clear by reading), default: 0x00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	MOVCNTR							

Bit	Symbol	Description
7:0	MOVCNTR	Bit7 is sign bit, means the slide direction. Bit6-0 is the slide data.

10.3.32 KDATAn, Key Data Register

Address: 0x38~0x3A, R, default: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
KDATAn															

Bit	Symbol	Description
15:0	KDATAn	Sn channel key data (refer register MCR(0x1E))

10.3.33 DUM0, Reserved Register

Address: 0x3C, R/W, default: 0x0FFF

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DUM0															

Bit	Symbol	Description
15:0	DUM0	Reserved register, default is 0x0FFF

10.3.34 DUM1, Reserved Register

Address: 0x3D, R/W, default: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DUM1															

Bit	Symbol	Description
15:0	DUM1	Reserved register, default is 0x0000

10.4 LED Effect Control Register

10.4.1 LER, LED Driver Enable Register

Address: 0x50, R/W, default: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	LE3	0	LE2	0	LE1	0	0

Bit	Symbol	Description
1:0	-	Reserved, must be 0
6:2	LEx	LED output enable 0: disable 1: enable
15:11	-	Reserved, must be 0

10.4.2 LCR, LED Effect Configuration Register

Address: 0x52, R/W, default: 0x0080

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	SRMINI	LIRMD		TIMD		LIE	FREQ	LOGLIN	

Bit	Symbol	Description
1:0	Log/Lin	Log/Linear dimming mode selection 00: log dimming 1, log(e) （default） 01: log dimming 2, log10

		1x: linear dimming
2	FREQ	PWM frequency selection 0: 244Hz （default） 1: 122Hz
3	LIE	LED program end interrupt enable 0: disable interrupt（default） 1: enable interrupt
5:4	TIMD	Touch key interrupt mode for LED module 00: interrupt generate when key status change 01: interrupt generate when key released 10: interrupt generate when key pressed, 11: interrupt generate when key status is 1
7:6	LIRMD	LED effect code run mode after responding to interrupt request 00: hold mode, PC point can be changed, program hold and wait for RMD.RUNMD 01: step mode 10: run mode (default)
8	SRMINI	SRAM reset bit, write 1, reset SRAM; read SRAM status, default is 0.

10.4.3 PMD, Program Mode Register

Address: 0x53, R/W, default: 0x0000																
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	PROGMD	
Bit	Symbol		Description												
1:0	PROGMD		Program control mode 00: load program via I²C interface (default) 01: re-load program and execute. When write 01 to PROGMD[1:0], set PC pointer will be updated with SADDR, then start to run program, and finally PROGMD[1:0] is changed to 10 automatically 10: run program. Under this mode, the control bit RUNMD in register RMD can configure different program running mode for normal operation or debug. 11: undefined												

10.4.4 RMD, Program Run Mode Register

Address: 0x54, R/W, default: 0x0000																
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	RUNMD	
Bit	Symbol		Description												
1:0	RUNMD		SRAM program run mode, only active for these LED set with CTRSR.CSx=0 00: hold mode, program stop and hold PC pointer (default) 01: step mode, RUNMD reset, PC+1 after the current program executed 10: run mode, normal program run 11: repeat mode, RUNMD reset, PC hold after the current program executed												

10.4.5 CTRSR, LED Control Source Selection Register

Address: 0x55, R/W, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	CS3	0	CS2	0	CS1	0	0
Bit	Symbol		Description												
6:2	CSx		LED control source 0: LEDx controlled by SRAM program 1: LEDx controlled by external MCU via I²C interface												

10.4.6 IMAX1～IMAX3, LEDx Maximum Output Current Register

Address: 0x57~0x58, R/W, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0					IMAX1			0							
0					IMAX3			0					IMAX2		
Bit	Symbol		Description												

10:8 2:0 10:8	IMAX1 IMAX2 IMAX3	LEDx maximum output current selection 000: 0mA (default) 001: 3.5mA 010: 7.0mA 011: 10.5mA 100: 14.0mA 101: 17.5mA 110: 21.0mA 111: 24.5mA

10.4.7 TIER, Program Touch Interrupt Enable Register

Address: 0x5C, R/W, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	TIE	0	0	GIE2	GIE1	0	KIE3	KIE2	KIE1	0	0

Bit	Symbol	Description
4:2	KIE3~1	Touch key interrupt enable for ASP program 0: disable (default) 1: enable
7:6	GIE2~1	Gesture interrupt enable for ASP program 0: disable (default) 1: enable
10	TIE	Tap interrupt enable for ASP program 0: disable (default) 1: enable

10.4.8 TIVEC, Touch Interrupt Vector Register

Address: 0x5D, R/W, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	TIVEC							

Bit	Symbol	Description
7:0	TIVEC	Touch interrupt vector. When touch interrupt occurs, SRAM PC pointer jumps to the target address specified by TIVEC.

10.4.9 LISR, LED Interrupt Status Register

Address: 0x5E, R(clear by reading), default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	LIS

Bit	Symbol	Description
0	LIS	LED program end interrupt status, set by END instruction with parameter int=1, used for inform external MCU that program has finished. LCR.LIE is the enable bit for LIS. 0: no interrupt 1: interrupt request

10.4.10 SADDR, Program Start Address Register

Address: 0x5F, R/W, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	SADDR							

Bit	Symbol	Description
7:0	SADDR	SRAM program starting address. For reload and run mode, if setting PMD.PROGMD=10, program will jump to PC=SADDR and run again.

10.4.11 PCR, LED Program Control Pointer Register

Address: 0x60, R/W, default: 0x0000															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	PC							

Bit	Symbol	Description
7:0	PC	SRAM program pointer(PC), can be written by I^2C interface. For normal program execution, set the PC pointer at PMD.PROGMD= 00 mode at first,

		and then write PMD.PROGMD with 10.

10.4.12 CMDR, LED Command Register

Address: 0x61, R/W, default: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMD															

Bit	Symbol	Description
15:0	CMD	External controlled Command. used to send external LED command which is only active for those LED configured with control bit CTRSR.CSx=1. The external controlled command adapted the same instruction with internal ASP.

10.4.13 RA/RB/RC/RD,LED Internal Program Register

Address: 0x62~0x65, R, default: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	RA							
0	0	0	0	0	0	0	0	RB							
0	0	0	0	0	0	0	0	RC							
0	0	0	0	0	0	0	0	RD							

Bit	Symbol	Description
7:0	RA/RB/RC/RD	LED internal program register, read only, for debug usage.

10.4.14 R1~R8, LED Internal Data Register

Address: 0x66~0x6D, R, default: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	R1							
0	0	0	0	0	0	0	0	R2							
0	0	0	0	0	0	0	0	R3							
0	0	0	0	0	0	0	0	R4							
0	0	0	0	0	0	0	0	R5							
0	0	0	0	0	0	0	0	R6							
0	0	0	0	0	0	0	0	R7							
0	0	0	0	0	0	0	0	R8							

Bit	Symbol	Description
7:0	R1～R8	LED internal data register, for debug usage.

10.4.15 GRP, LED Group Operation Register

Address: 0x6E, R, default: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	GS3	0	GS2	0	GS1	0	0

Bit	Symbol	Description
6:2	GS3~1	LED channel selection for external group control command. GSx=0, LED_n is not included in external LED command with channel =0x1E; GSx=1, LED_n is included in external LED command with channel =0x1E;

10.4.16 WADDR, LED Program Loading Address Register

Address: 0x7E, R/W, default: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	ADDR							

Bit	Symbol	Description
7:0	ADDR	SRAM address for program access via I^2C interface

10.4.17 WDATA, LED Program Loading Data Register

Address: 0x7F, R/W, default: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CODE															

Bit	Symbol	Description

15:0	CODE	SARM data for program access via I²C interface

10.4.18 WPR, Writing Protection Register

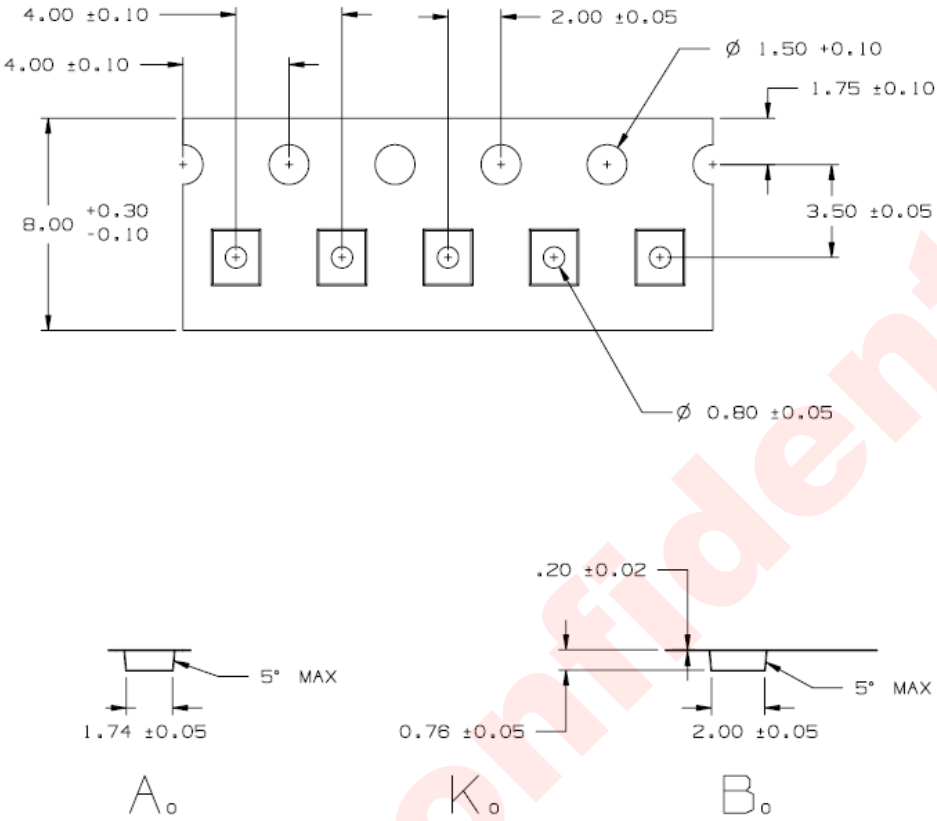
Address: 0x7D, R/W, default: 0x5500

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WPW								0	0	0	0	0	0	0	0

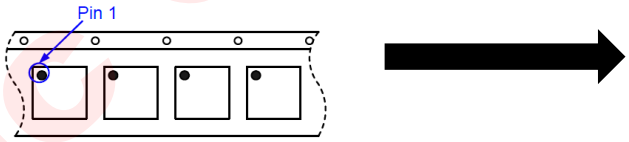
Bit	Symbol	Description
15:8	WPW	writing protection control, If WPW=0x55, all register is writable, otherwise all register except for WPR is not allowed to be written.

11 TAPE AND REEL INFORMATION

11.1 Carrier Tape

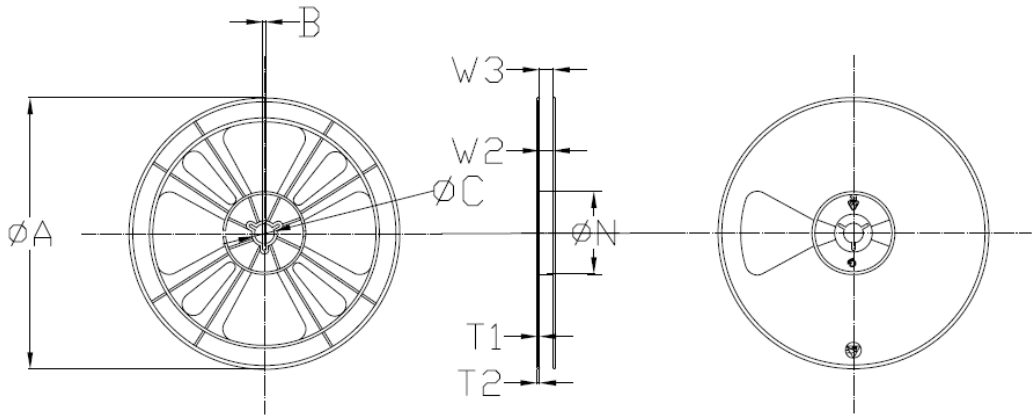


11.2 PIN1 Direction



User Direction of Feed

11.3 Reel

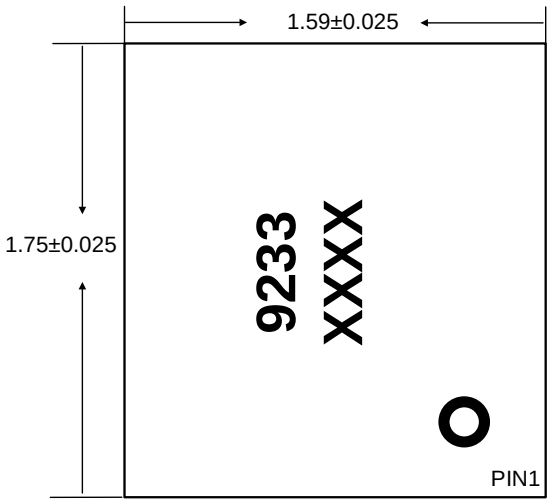


Item	Value&Tolerance
A	179±1.0
B	2.0±0.1
C	13.5±0.2
N	54.8±0.2
W2	9.0±0.2
W3	9.2+1.0
T1	1.2±0.2
T2	1.5±0.2

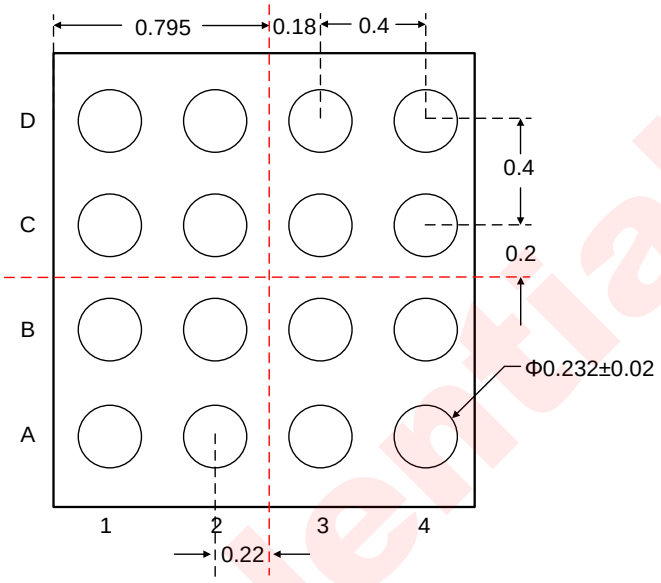
Note:

1. surface resistivity: 10^{5} to 10^{11} ohms/sq.
2. Restriction criterion of hazardous substance for packing material follow GP-M001.

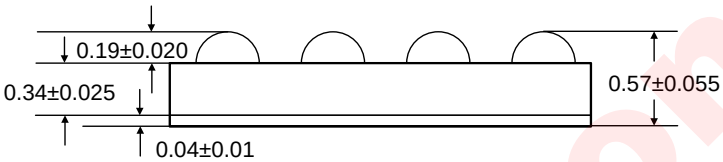
12 PACKAGE DESCRIPTION



Top View



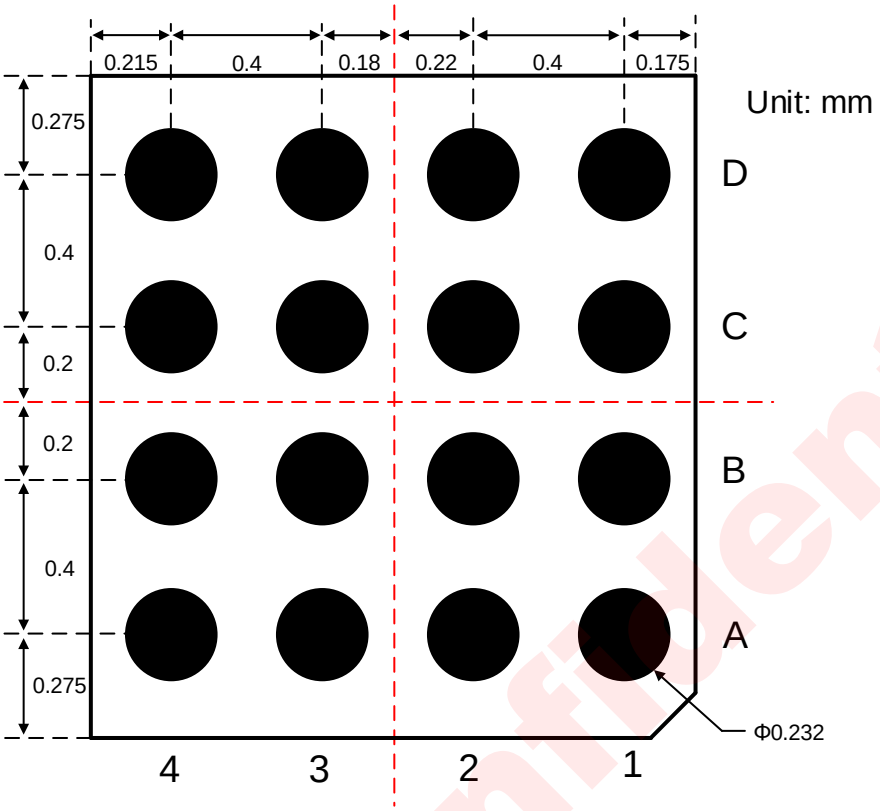
Bottom View



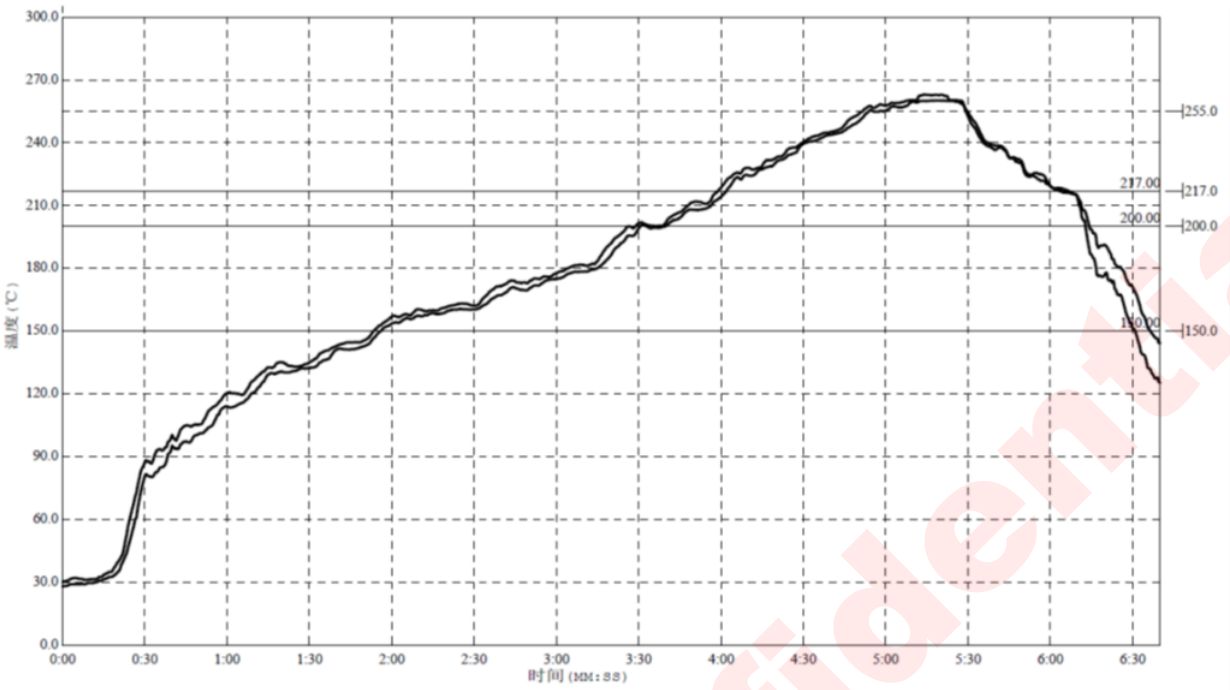
Side View

Unit: mm

13 RECOMMENDED LAND PATTERN



14 REFLOW



Reflow Note	Spec
Average ramp-up rate (217°C to peak)	Max. 3°C /sec
Time of Preheat temp. (from 150°C to 200°C)	60-120sec
Time to be maintained above 217°C	60-150sec
Peak Temperature	>260°C
Time within 5°C of actual peak temp	20-40sec
Ramp-down rate	Max. 6°C /sec
Time from 25°C to peak temp	Max. 8min

Package Reflow Standard Profile

NOTE 1: All data are compared with the package-top temperature, measured on the package surface;

NOTE 2: AW9233 adopted the Pb-Free assembly.

15 REVISION HISTORY

Vision	Date	Change Record
V1.0	Nov 2016	Officially Released
V1.1	Nov 2017	Add reflow information
V1.2	June 2018	Update ASP example Update the electrical characteristics
V1.3	Sep. 2018	Update the storage temperature
V1.4	Feb. 2019	Add power on procedure

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