300 mA High Performance Low-Dropout Linear Regulator

Features

- Input voltage range: 1.4V to 5.5V
- Fixed outputs of 1.1V, 1.2V, 1.5V, 1.8V, 2.5V, 2.8V, 2.85V, 2.9V, 2.95V, 3.0V, 3.1V, 3.3V
- Rated output current: 300mA
- Quiescent current: typical 50μA
- Typical 0.1μA shutdown current
- Typical 310mV dropout voltage (I_{OUT}=300mA, 1.8V output)
- Power supply rejection ratio: typical 90dB (I_{OUT}=30mA, freq=1kHz, 1.8V output)
- Noise: typical 33μVrms (I_{OUT}=30mA, BW=10Hz to 100kHz, 1.8V output)
- Built-in output short protection: typical 120mA when output short to ground
- DFN 1mmX1mmX0.37mm-4L package and SOT 23-5L package

General Description

AW37030YXXX is a low dropout voltage regulator featuring low ON resistance, high PSRR, low Noise, good load/line transient response and smooth soft-start.

AW37030YXXX integrates current limit, short circuit protection, thermal shutdown, sufficiently protecting IC from being damaged.

AW37030YXXX is designed to work with a 1μF or more input ceramic capacitor and a 1μF or more output ceramic capacitor. The low power dissipation and good dynamic response make AW37030YXXX very suitable for hand-held communication equipment. Tiny package makes high density mounting of the IC on boards possible.

Applications

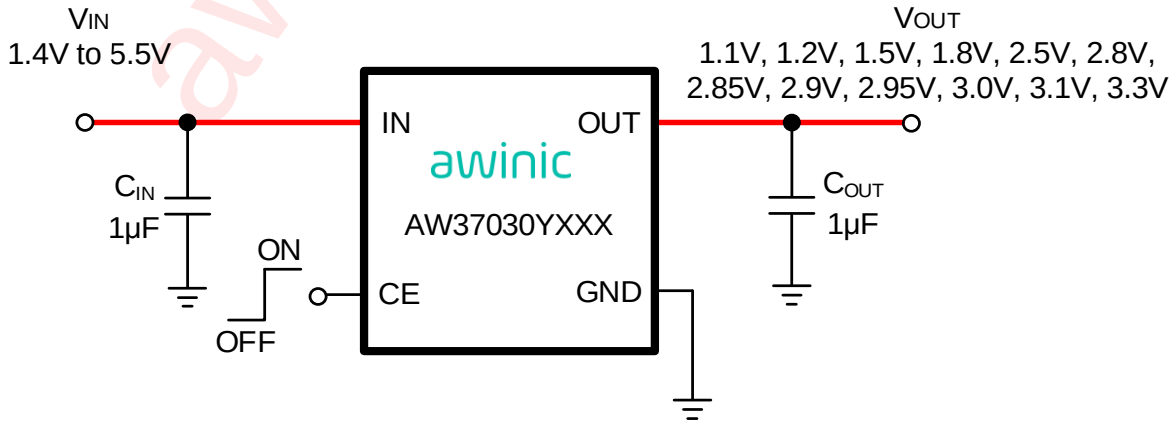
Battery-powered equipment

Smart phone

Digital camera

STB

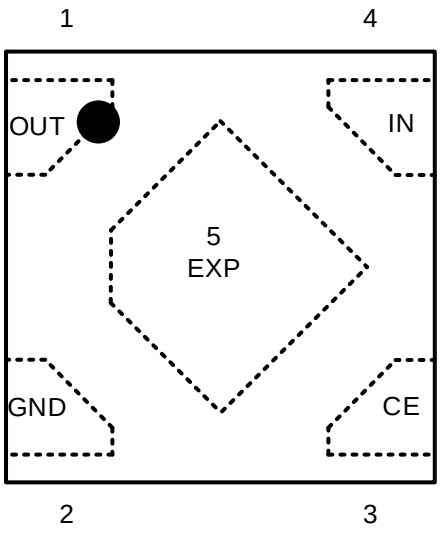
Typical Application Circuit



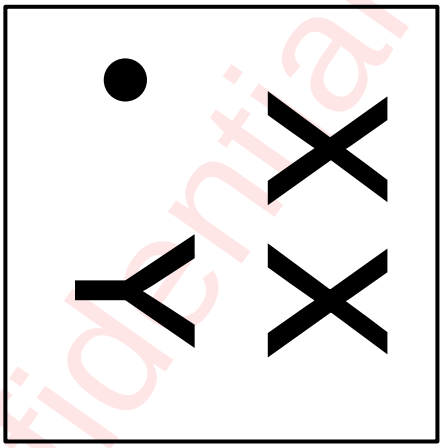
Pin Configuration And Top Mark

DFN 1mmX1mm-4L

AW37030YXXXDNR
(Top View)



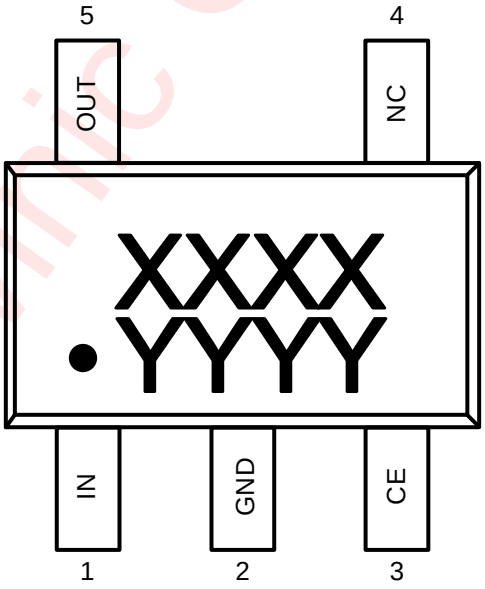
AW37030YXXXDNR Marking
(Top View)



XX – AW37030YXXXDNR
Y – Production Tracing Code

SOT 23-5L

AW37030YXXXSTR Marking
(Top View)



XXXX – AW37030YXXXSTR
YYYY – Production Tracing Code

Pin Definition

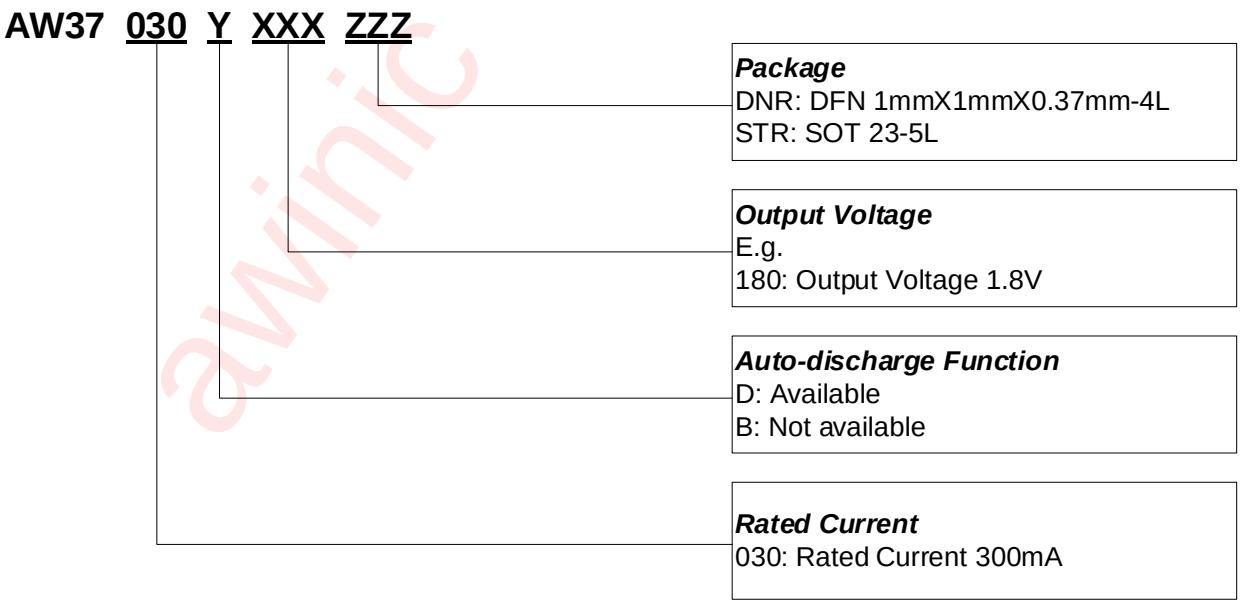
DFN 1mmX1mm-4L

No.	NAME	DESCRIPTION
1	OUT	Regulated output voltage pin. Put a 1μF or more ceramic capacitor at the output pin.
2	GND	Ground.
3	CE	Chip enable pin. Built-in 140nA pull-down current. (High Active)
4	IN	Input supply pin. Put a 1μF or more bypass capacitor at the power supply.
5	EXP	Expose pad should be tied to ground plane for better power dissipation.

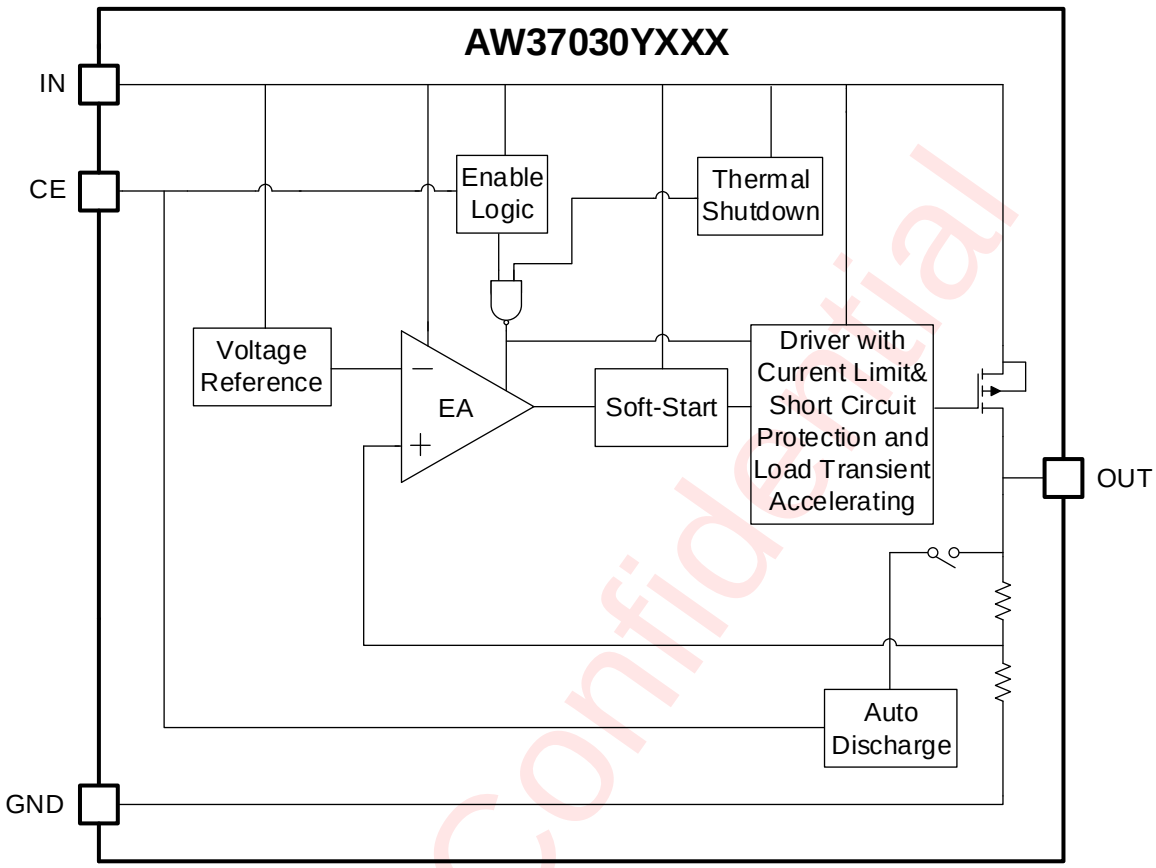
SOT 23-5L

No.	NAME	DESCRIPTION
1	IN	Input supply pin. Put a 1μF or more bypass capacitor at the power supply.
2	GND	Ground.
3	CE	Chip enable pin. Built-in 140nA pull-down current. (High Active)
4	NC	Not connected.
5	OUT	Regulated output voltage pin. Put a 1μF or more ceramic capacitor at the output pin.

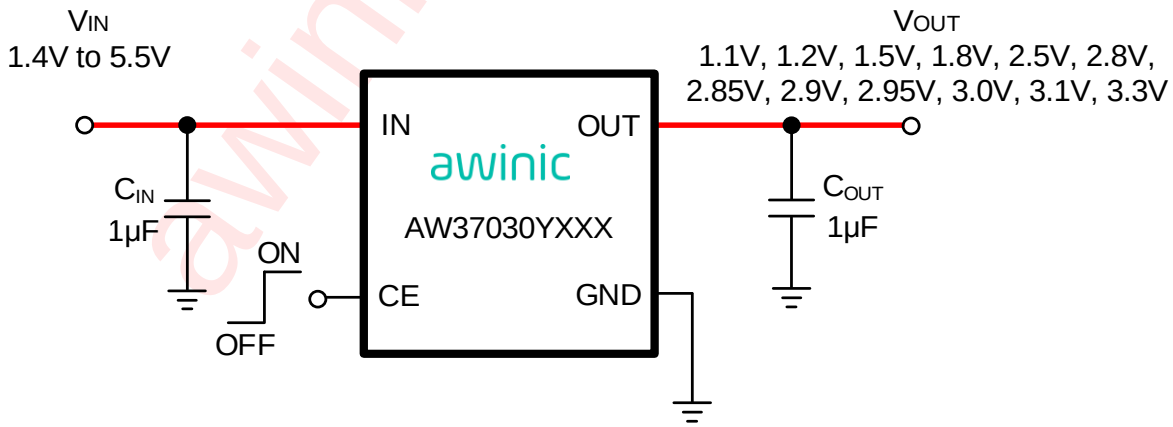
Name Rule



Functional Block Diagram



Typical Application Circuits



AW37030YXXX Application Circuit

Notice for typical application circuits:

Capacitance of C_{IN} and C_{OUT} should be 1μF or more.

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW37030D110DNR	-40°C～85°C	DFN 1mmX1mm-4L	VE	MSL1	ROHS+HF	3000 units/ Tape and Reel
AW37030D120DNR	-40°C～85°C	DFN 1mmX1mm-4L	SE	MSL1	ROHS+HF	3000 units/ Tape and Reel
AW37030D150DNR	-40°C～85°C	DFN 1mmX1mm-4L	CR	MSL1	ROHS+HF	3000 units/ Tape and Reel
AW37030D180DNR	-40°C～85°C	DFN 1mmX1mm-4L	HL	MSL1	ROHS+HF	3000 units/ Tape and Reel
AW37030D250DNR	-40°C～85°C	DFN 1mmX1mm-4L	J4	MSL1	ROHS+HF	3000 units/ Tape and Reel
AW37030D280DNR	-40°C～85°C	DFN 1mmX1mm-4L	ZJ	MSL1	ROHS+HF	3000 units/ Tape and Reel
AW37030D285DNR	-40°C～85°C	DFN 1mmX1mm-4L	2V	MSL1	ROHS+HF	3000 units/ Tape and Reel
AW37030D290DNR	-40°C～85°C	DFN 1mmX1mm-4L	HH	MSL1	ROHS+HF	3000 units/ Tape and Reel
AW37030D295DNR	-40°C～85°C	DFN 1mmX1mm-4L	C2	MSL1	ROHS+HF	3000 units/ Tape and Reel
AW37030D300DNR	-40°C～85°C	DFN 1mmX1mm-4L	VA	MSL1	ROHS+HF	3000 units/ Tape and Reel
AW37030D310DNR	-40°C～85°C	DFN 1mmX1mm-4L	RJ	MSL1	ROHS+HF	3000 units/ Tape and Reel
AW37030D330DNR	-40°C～85°C	DFN 1mmX1mm-4L	PP	MSL1	ROHS+HF	3000 units/ Tape and Reel
AW37030D110STR	-40°C～85°C	SOT 23-5L	75PY	MSL3	ROHS+HF	3000 units/ Tape and Reel
AW37030D120STR	-40°C ~ 85°C	SOT 23-5L	VGML	MSL3	ROHS+HF	3000 units/ Tape and Reel
AW37030D150STR	-40°C ~ 85°C	SOT 23-5L	ZUM4	MSL3	ROHS+HF	3000 units/ Tape and Reel

Ordering Information (Continued)

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW37030D180STR	-40°C～85°C	SOT 23-5L	5HGC	MSL3	ROHS+HF	3000 units/ Tape and Reel
AW37030D250STR	-40°C～85°C	SOT 23-5L	K2FA	MSL3	ROHS+HF	3000 units/ Tape and Reel
AW37030D280STR	-40°C～85°C	SOT 23-5L	JGLU	MSL3	ROHS+HF	3000 units/ Tape and Reel
AW37030D285STR	-40°C～85°C	SOT 23-5L	TKRW	MSL3	ROHS+HF	3000 units/ Tape and Reel
AW37030D290STR	-40°C～85°C	SOT 23-5L	6QN0	MSL3	ROHS+HF	3000 units/ Tape and Reel
AW37030D300STR	-40°C～85°C	SOT 23-5L	N02F	MSL3	ROHS+HF	3000 units/ Tape and Reel
AW37030D310STR	-40°C～85°C	SOT 23-5L	2JSX	MSL3	ROHS+HF	3000 units/ Tape and Reel
AW37030D330STR	-40°C～85°C	SOT 23-5L	BB3G	MSL3	ROHS+HF	3000 units/ Tape and Reel

Absolute Maximum Ratings(NOTE1)

PARAMETERS		RANGE
Input voltage range		-0.3V to 6.5V
Enable control voltage range		-0.3V to 6.5V
Output voltage range		-0.3V to VIN+0.3V, max. 6.5V
Maximum operating junction temperature T_{J_MAX}		150°C
Recommended operating junction temperature T_{J_REC}		-40°C to 125°C
Operating free-air temperature range		-40°C to 85°C
Storage temperature T_{STG}		-65°C to 150°C
Lead temperature (soldering 10 seconds)		260°C
Junction-to-ambient thermal resistance $R_{\theta JA}$ (NOTE2)	DFN 1mmX1mm-4L	215.4°C/W
	SOT 23-5L	177.4°C/W
Junction-to-case(top) thermal resistance $R_{\theta JC(top)}$ (NOTE2)	DFN 1mmX1mm-4L	161.85°C/W
	SOT 23-5L	102.1°C/W
Junction-to-board thermal resistance $R_{\theta JB}$ (NOTE2)	DFN 1mmX1mm-4L	156.4°C/W
	SOT 23-5L	42.7°C/W
Junction-to-top characterization parameter ψ_{JT} (NOTE2)	DFN 1mmX1mm-4L	17.3°C/W
	SOT 23-5L	13.5°C/W
Junction-to-board characterization parameter ψ_{JB} (NOTE2)	DFN 1mmX1mm-4L	170.4°C/W
	SOT 23-5L	39.4°C/W
Junction-to-case(bottom) thermal resistance $R_{\theta JC(bot)}$ (NOTE2)	DFN 1mmX1mm-4L	118°C/W
	SOT 23-5L	31.2°C/W
Maximum power consumption T_A=25°C, T_{J_REC}=125°C	DFN 1mmX1mm-4L	464mW
	SOT 23-5L	564mW
ESD	HBM (Human body model)(NOTE3)	±2kV
	CDM(Charged device model) (NOTE4)	±1.5kV
Latch-Up(NOTE5)		+IT：200mA - IT：-200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: Thermal resistances follow JEDEC 2S2P standards, and is usually highly dependent on PCB layout. Exceptionally, $R_{\theta JC(top)}$ of DFN 1mmX1mm-4L Package follows SEMI standard G43-87.

NOTE3: All pins. Test Condition: ESDA/JEDEC JS-001-2017.

NOTE4: All pins. Test Condition: ESDA/JEDEC JS-002-2018.

NOTE5: Test Condition: JESD78E.

Electrical Characteristics

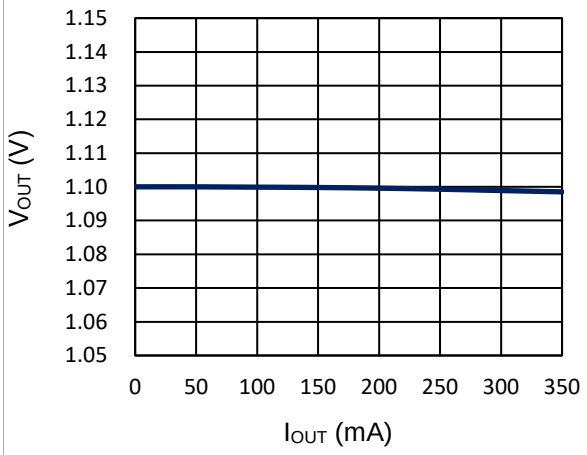
$V_{IN}=V_{OUT(SET)}+1V$, $V_{CE}>1V$, $I_{OUT}=1mA$, $C_{IN}=C_{OUT}=1\mu F$, $T_A=25°C$ (unless otherwise noted)

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
V_{IN}	Input Voltage Range			1.4		5.5	V
V_{OUT_ACC}	Output Voltage Accuracy	$T_A=25°C$		-1		1	%
		$-40°C \le T_A \le 85°C$		-2		2	
$LOAD_{Reg}$	Load Regulation	$1mA \le I_{OUT} \le 300mA$			1	20	mV
$LINE_{Reg}$	Line Regulation	$V_{OUT(SET)}+0.5V \le V_{IN} \le 5.5V$			1	5	mV
$V_{dropout}$	Dropout Voltage	I_{OUT}=300mA, When V_{OUT} falls 100mV below $V_{OUT(SET)}$	$V_{OUT(SET)}$=1.1V		680	884	mV
			$V_{OUT(SET)}$=1.2V		576	749	
			$V_{OUT(SET)}$=1.8V		310	403	
			$V_{OUT(SET)}$=2.5V		203	264	
			$V_{OUT(SET)}$=2.8V		184	239	
			$V_{OUT(SET)}$=3.0V		175	228	
			$V_{OUT(SET)}$=3.3V		158	205	
I_{SD}	Shutdown Current	$V_{CE}<0.4V$			0.1	1	μA
I_Q	Quiescent Current	I_{OUT}=0mA			50	100	μA
V_{CEH}	CE Input Voltage "H"	$-40°C \le T_A \le 85°C$		1			V
V_{CEL}	CE Input Voltage "L"	$-40°C \le T_A \le 85°C$				0.4	V
PSRR	Power Supply Ripple Rejection	I_{OUT}=30mA, f=1kHz $V_{OUT(SET)}$=1.8V			90		dB
V_N	Output Voltage Noise	I_{OUT}=30mA BW=10Hz to 100kHz	$V_{OUT(SET)}$=1.1V		21		μVrms
			$V_{OUT(SET)}$=1.8V		33		
			$V_{OUT(SET)}$=3.3V		46		
I_{CL}	Output Current Limit	$V_{OUT}=90\%*V_{OUT(SET)}$		300			mA
I_{SC}	Short Current Limit	$V_{OUT}<10\%*V_{OUT(SET)}$			120		mA
VTC	Output Voltage Temperature Coefficient	$-40°C \le T_A \le 85°C$			±40		ppm/°C
R_{DISC}	Auto Discharge Resistance	V_{IN}=4V, $V_{CE}<0.4V$, V_{OUT}=2.8V			130		Ω
I_{CE}	CE Pull Down Current				140		nA
T_{SDH}	Thermal Shutdown Threshold	Temperature Rising			160		°C
T_{SDL}	Thermal Shutdown Reset Threshold	Temperature Falling			130		°C

Typical Characteristics

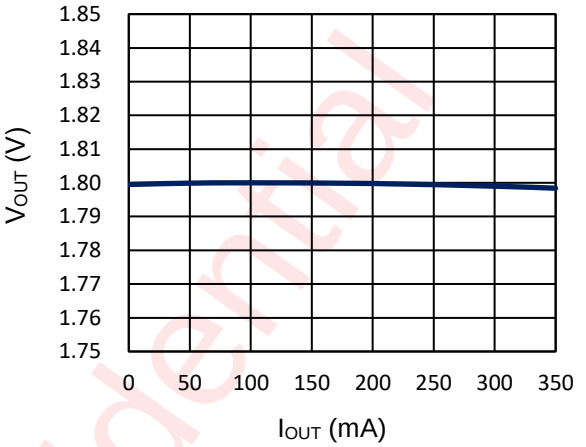
$V_{IN}=V_{OUT(SET)}+1V$, $V_{CE}>1V$, $I_{OUT}=1mA$, $C_{IN}=C_{OUT}=1\mu F$, $T_A=25°C$, In Typical Application Circuit, unless otherwise noted.

AW37030D110



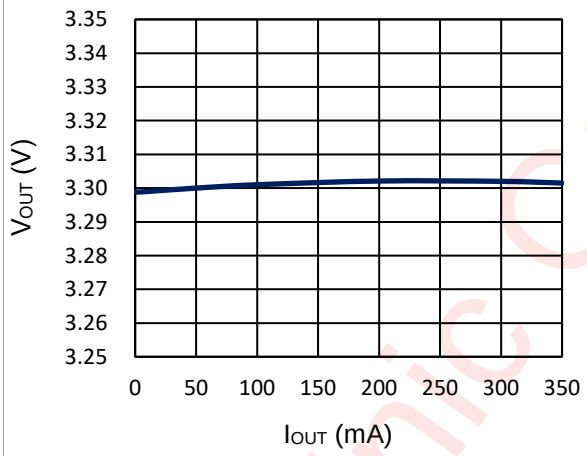
Output Voltage vs Output Current

AW37030D180



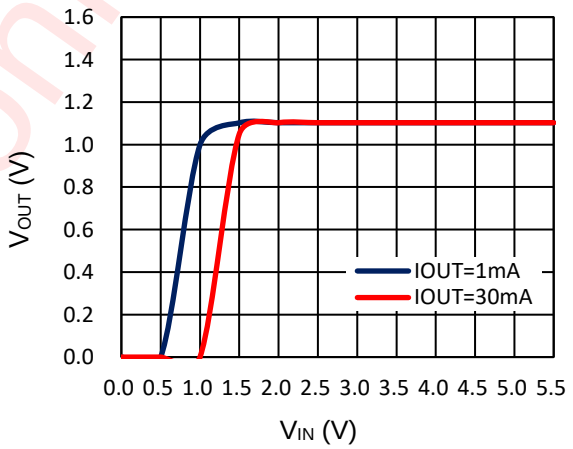
Output Voltage vs Output Current

AW37030D330



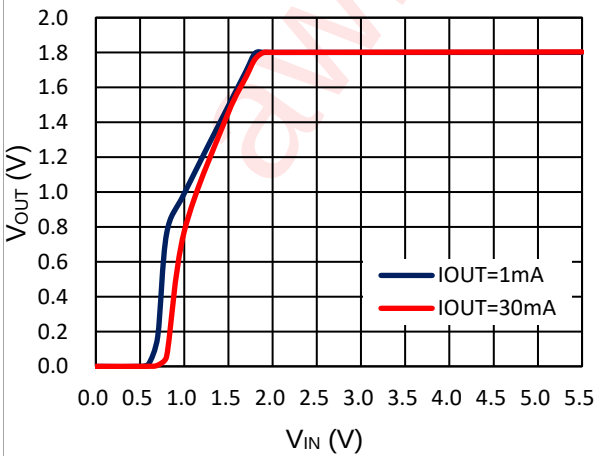
Output Voltage vs Output Current

AW37030D110



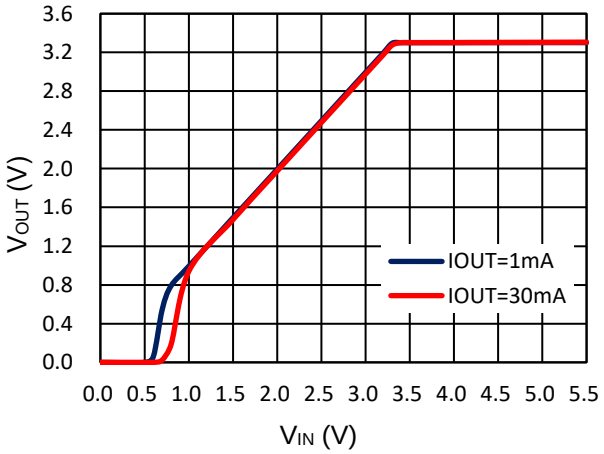
Output Voltage vs Input Voltage

AW37030D180



Output Voltage vs Input Voltage

AW37030D330

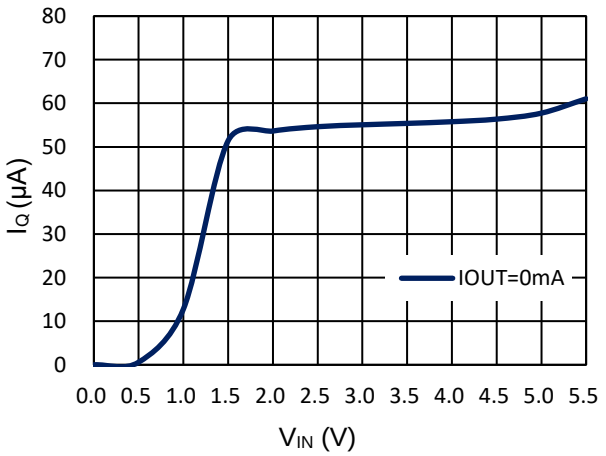


Output Voltage vs Input Voltage

Typical Characteristics (Continued)

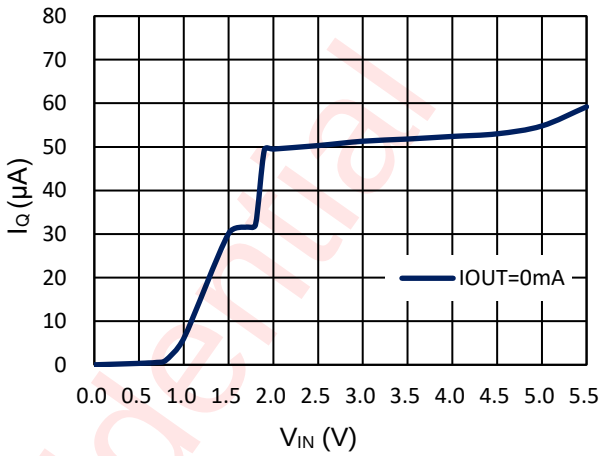
$V_{IN}=V_{OUT(SET)}$+1V, V_{CE}>1V, I_{OUT}=1mA, $C_{IN}=C_{OUT}$=1μF, T_A=25°C, In Typical Application Circuit, unless otherwise noted.

AW37030D110



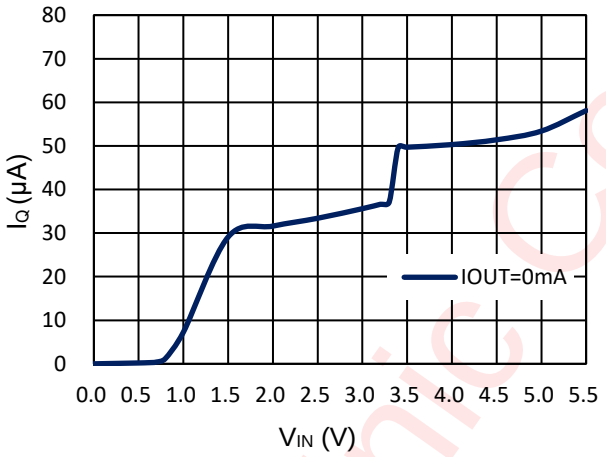
Quiescent Current vs Input Voltage

AW37030D180



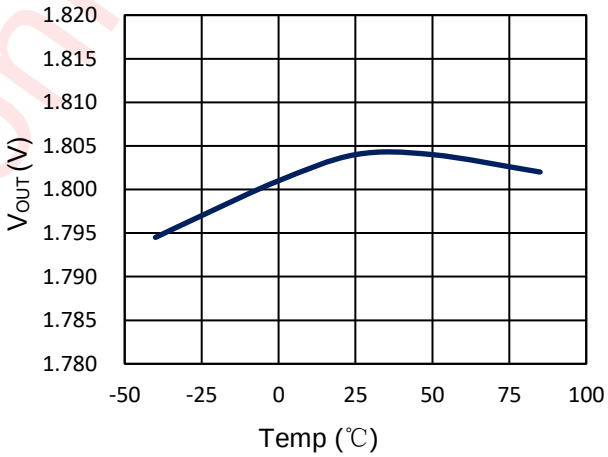
Quiescent Current vs Input Voltage

AW37030D330



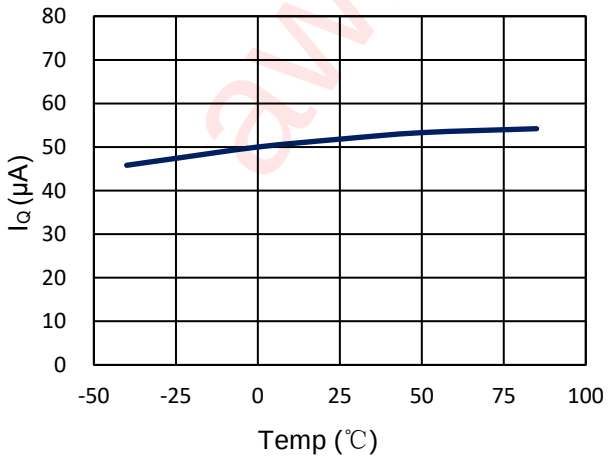
Quiescent Current vs Input Voltage

AW37030D180



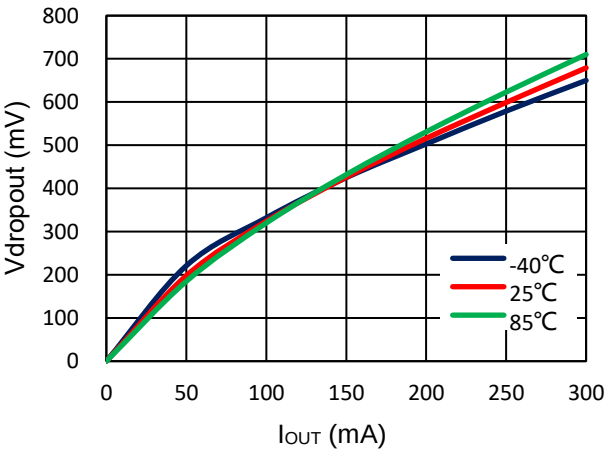
Output Voltage vs Temperature

AW37030D180



Quiescent Current vs Temperature

AW37030D110

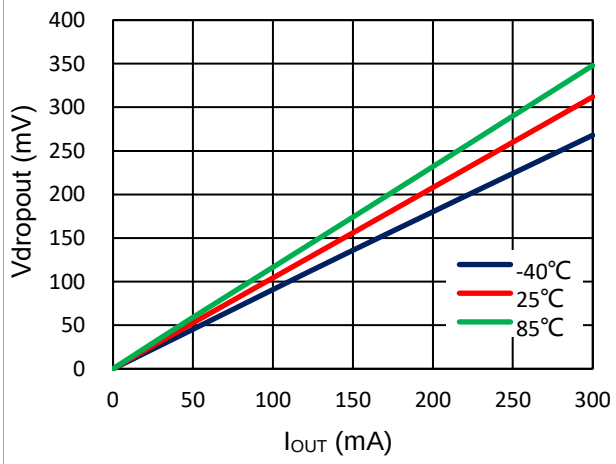


Dropout Voltage vs Output Current

Typical Characteristics (Continued)

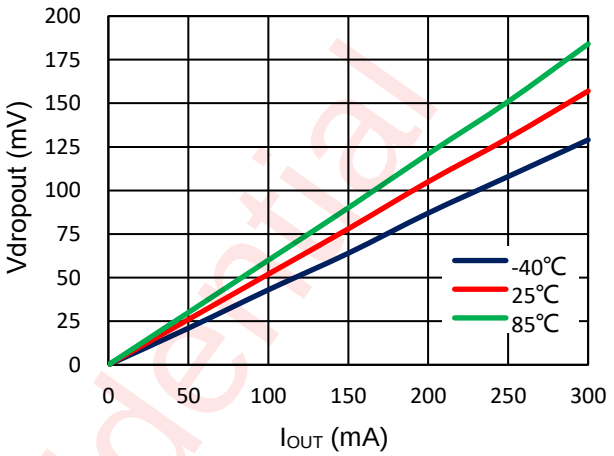
$V_{IN}=V_{OUT(SET)}+1V$, $V_{CE}>1V$, $I_{OUT}=1mA$, $C_{IN}=C_{OUT}=1\mu F$, $T_A=25°C$, In Typical Application Circuit, unless otherwise noted.

AW37030D180



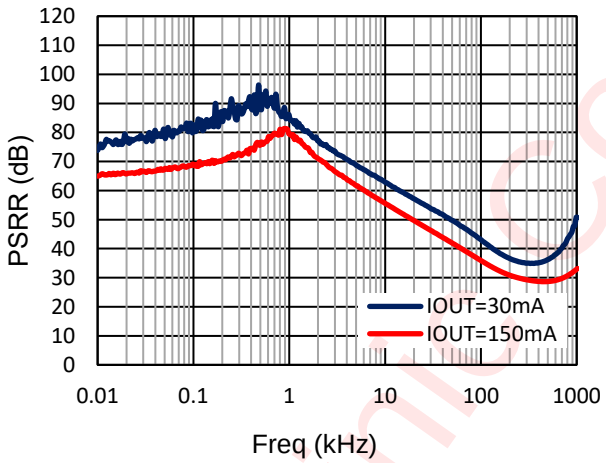
Dropout Voltage vs Output Current

AW37030D330



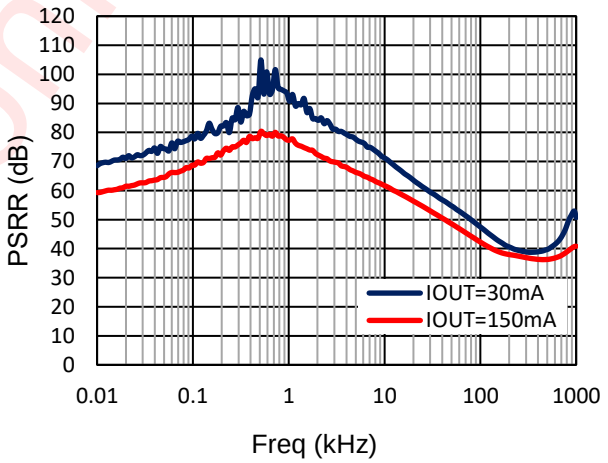
Dropout Voltage vs Output Current

AW37030D110



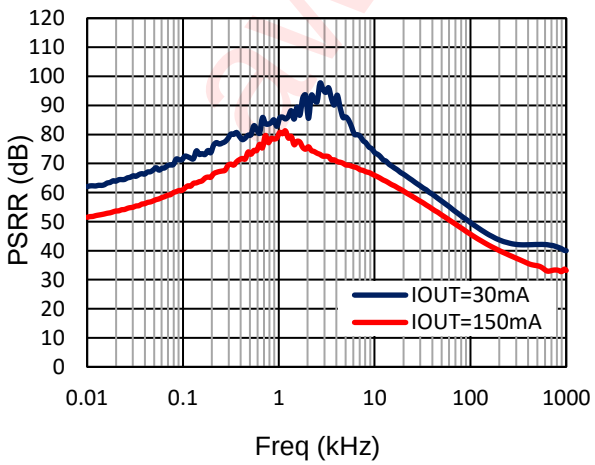
PSRR vs Frequency

AW37030D180



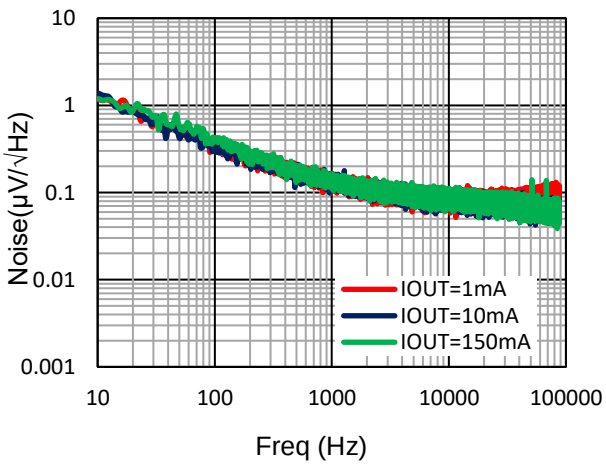
PSRR vs Frequency

AW37030D330



PSRR vs Frequency

AW37030D110

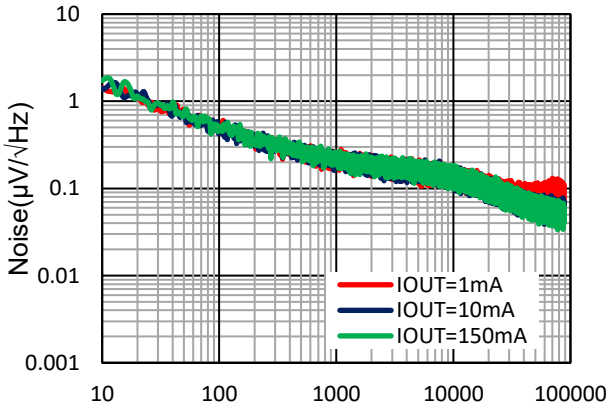


Output Spectral Noise Density

Typical Characteristics (Continued)

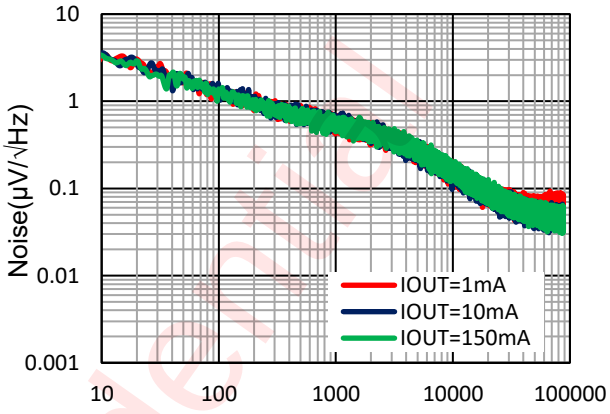
$V_{IN}=V_{OUT(SET)}$+1V, V_{CE}>1V, I_{OUT}=1mA, $C_{IN}=C_{OUT}$=1μF, T_A=25°C, In Typical Application Circuit, unless otherwise noted.

AW37030D180



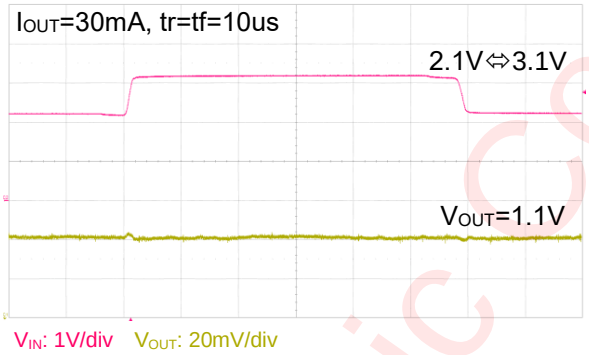
Output Spectral Noise Density

AW37030D330



Output Spectral Noise Density

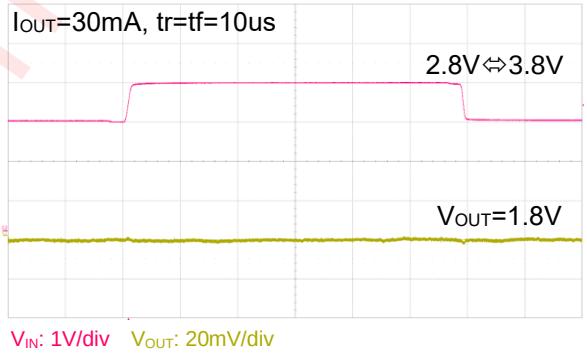
AW37030D110



Time(50us/div)

Input Transient Response

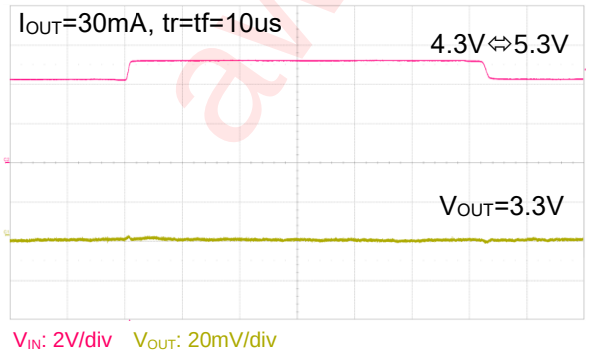
AW37030D180



Time(50us/div)

Input Transient Response

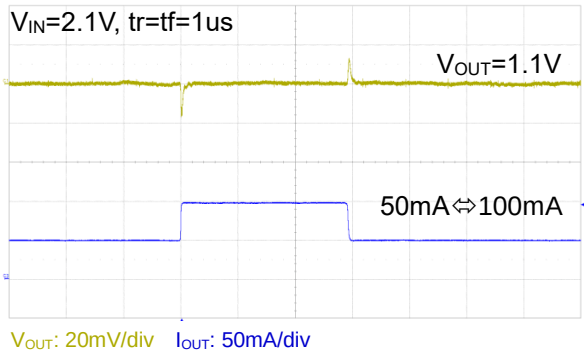
AW37030D330



Time(50us/div)

Input Transient Response

AW37030D110



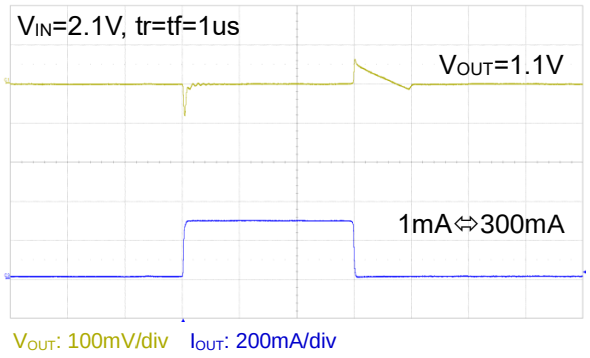
Time(50us/div)

Load Transient Response

Typical Characteristics (Continued)

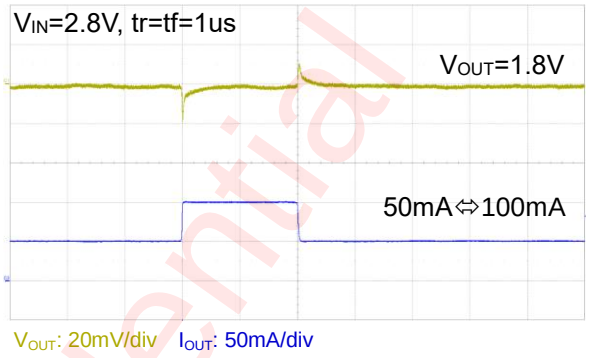
$V_{IN}=V_{OUT(SET)}+1V$, $V_{CE}>1V$, $I_{OUT}=1mA$, $C_{IN}=C_{OUT}=1\mu F$, $T_A=25°C$, In Typical Application Circuit, unless otherwise noted.

AW37030D110



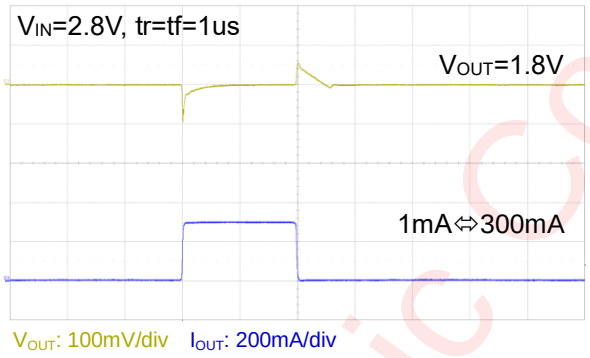
Load Transient Response

AW37030D180



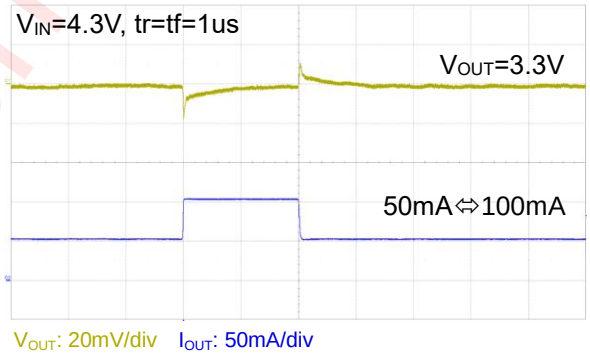
Load Transient Response

AW37030D180



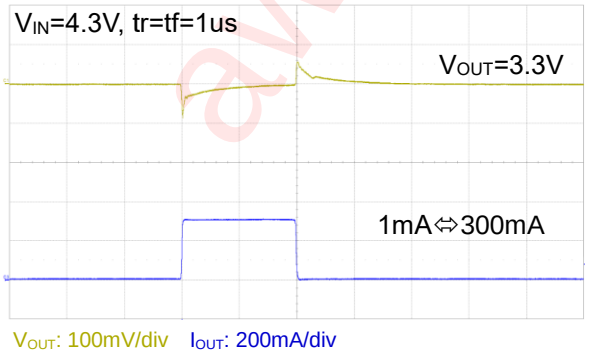
Load Transient Response

AW37030D330



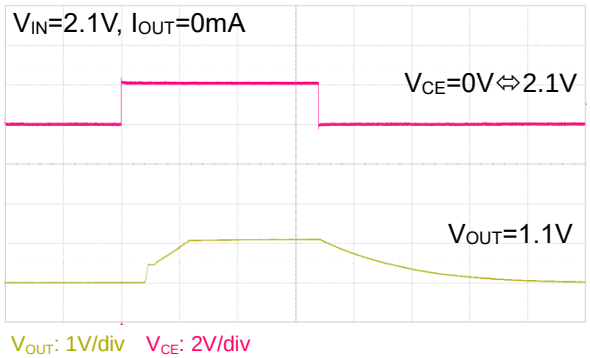
Load Transient Response

AW37030D330



Load Transient Response

AW37030D110

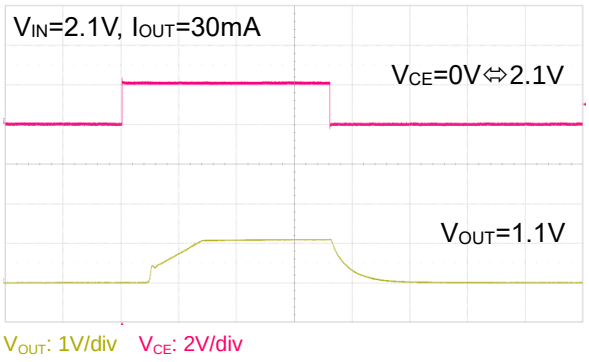


Turn On&Off Speed with CE pin

Typical Characteristics (Continued)

$V_{IN}=V_{OUT(SET)}+1V$, $V_{CE}>1V$, $I_{OUT}=1mA$, $C_{IN}=C_{OUT}=1\mu F$, $T_A=25°C$, In Typical Application Circuit, unless otherwise noted.

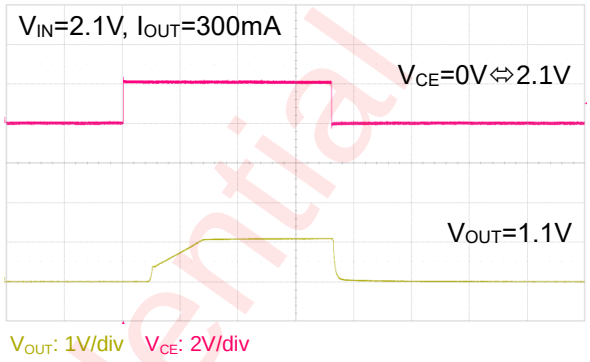
AW37030D110



Time(100us/div)

Turn On&Off Speed with CE pin

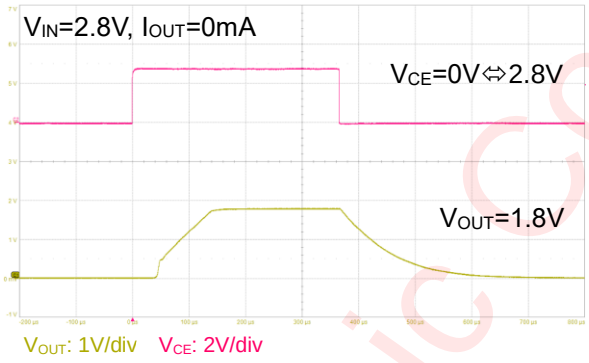
AW37030D110



Time(100us/div)

Turn On&Off Speed with CE pin

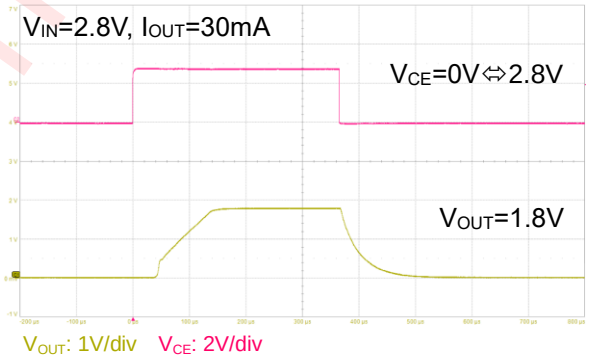
AW37030D180



Time(100us/div)

Turn On&Off Speed with CE pin

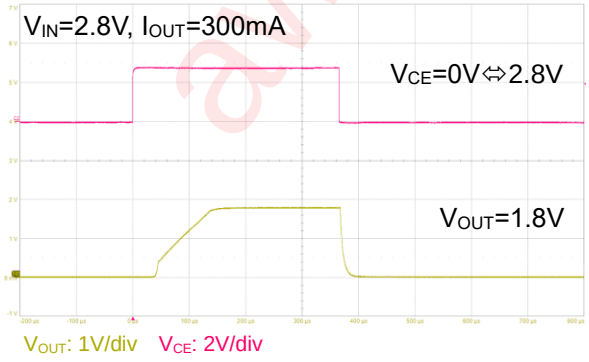
AW37030D180



Time(100us/div)

Turn On&Off Speed with CE pin

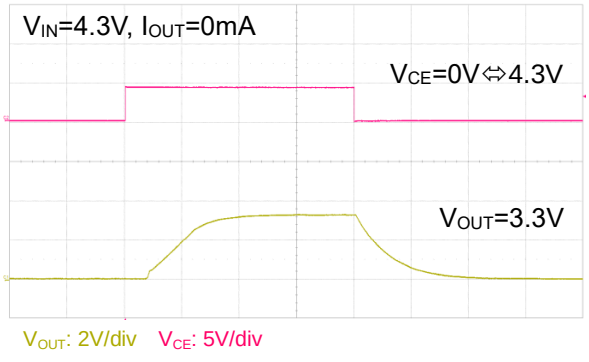
AW37030D180



Time(100us/div)

Turn On&Off Speed with CE pin

AW37030D330



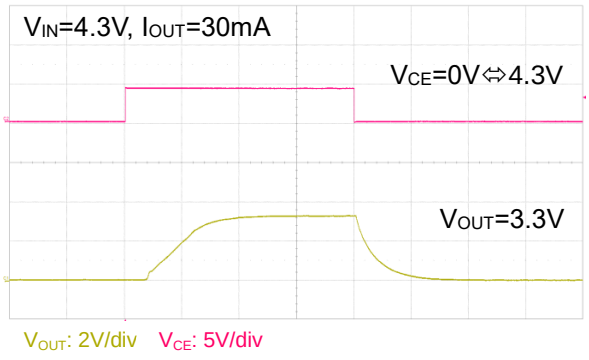
Time(100us/div)

Turn On&Off Speed with CE pin

Typical Characteristics (Continued)

$V_{IN}=V_{OUT(SET)}+1V$, $V_{CE}>1V$, $I_{OUT}=1mA$, $C_{IN}=C_{OUT}=1\mu F$, $T_A=25°C$, In Typical Application Circuit, unless otherwise noted.

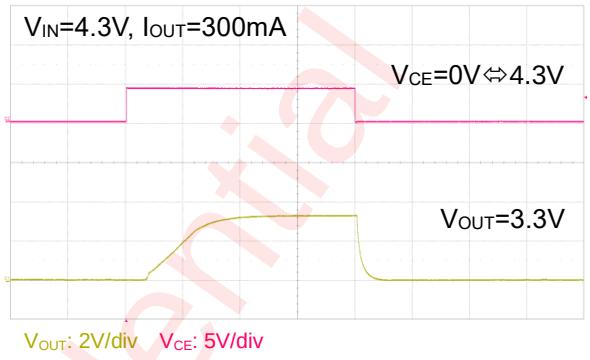
AW37030D330



Time(100us/div)

Turn On&Off Speed with CE pin

AW37030D330



Time(100us/div)

Turn On&Off Speed with CE pin

Detailed Functional Description

AW37030YXXX is a low dropout voltage regulator. After powered on, with CE pin assertion, feedback voltage signal from the integrated resistor network and a voltage related to the voltage reference are transmit to positive input terminal and negative input terminal of an error amplifier (EA) respectively. The output signal of EA is used to control the open-state of power MOSFET. After soft-start, feedback voltage signal compares with the established reference voltage, making output voltage stable and accurate. AW37030YXXX integrates function of load transient accelerating, making LDO obtain excellent dynamic load transient response performance.

Enable Operation

AW37030YXXX uses CE pin to realize enable operation. Applying proper value of voltage to CE pin can make IC enable/disable.

If the voltage of CE pin is less than 0.4V, AW37030YXXX is guaranteed to be disabled. In this state, function modules of IC and power MOSFET are turned off. And the auto discharge function is enabled making output discharge through a on-state NMOSFET to Ground. In disable state, AW37030YXXX only consumes a typical 10nA current.

If the voltage of CE pin is more than 1V, AW37030YXXX is guaranteed to be enabled. In this state, the auto discharge function is disabled, and AW37030YXXX regulates output voltage to the designed value of voltage.

A 140nA pull down current to Ground is built-in at CE pin, making sure that the IC is disabled when CE pin floats. If Enable function is not required, CE pin should be connected directly to IN pin.

Output Current Limit

AW37030YXXX integrates output current limit function, protecting IC from excessive current.

When the load is excessively heavy, AW37030YXXX limits the current flowing through the IC to a typical 500mA current. This value is specially designed, so that IC is protected properly and the output capability of 300mA is not influenced either.

Meanwhile, AW37030YXXX integrates a 120mA fold-back current limit function, lowering the system dissipation when output overload or short to Ground.

Thermal Shutdown

AW37030YXXX integrates thermal shutdown function, protect IC from excessively high temperature.

When the chip temperature exceeds 160°C, AW37030YXXX detects it as an over-temperature event, triggering thermal shutdown, which will turn off the main function module, including power MOSFET. This inhibits increase of chip's temperature. IC would keep the protection-state on until the chip's temperature falls below to 130°C. At this moment, the over-temperature protection-state is released, IC resumes to work again.The hysteresis avoids IC's turning off and on frequently around the the Thermal Shutdown threshold.

Auto Discharge

AW37030YXXX makes output voltage discharge quickly when in CE disable state or thermal shutdown state, benefit from integrating auto discharge function. Auto discharge function is implemented by integrated a NMOSFET of typical 130Ω Rdson route from Output to Ground, and the route is get through in CE disable state or thermal shutdown state. This feature prevents residual charge voltage on the output capacitor, which may impact proper power up of the system connected to the converter. It should be noted that auto discharge function is optional according to different specs.

Application Information

Power Dissipation and Device Operation

The permissible power dissipation is dependent on the ambient temperature T_A and the junction-to-ambient thermal resistance $R_{\theta JA}$.

The absolute maximum allowable power dissipation for the device in a given package can be calculated using Equation below, where T_{J_MAX} = 150°C :

$$PD_{MAX\_ABS} = (T_{J\_MAX} - T_A) / R_{\theta JA}$$

The recommended maximum allowable power dissipation for the device in a given package can be calculated using Equation below, where T_{J_REC} = 125°C :

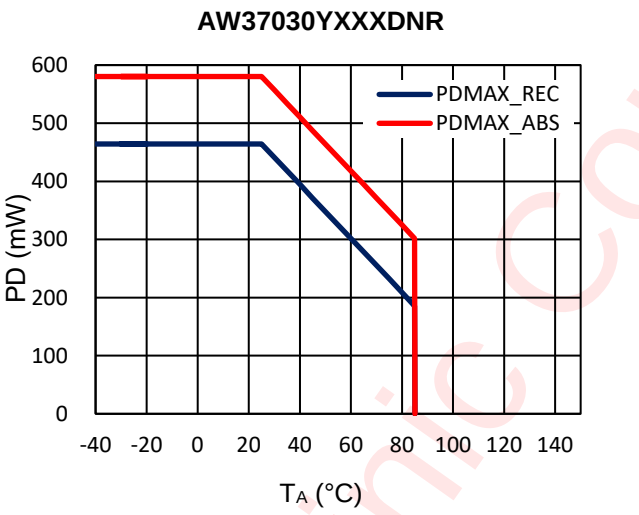
$$PD_{MAX\_REC} = (T_{J\_REC} - T_A) / R_{\theta JA}$$

The actual power being dissipated in the device can be represented by Equation below:

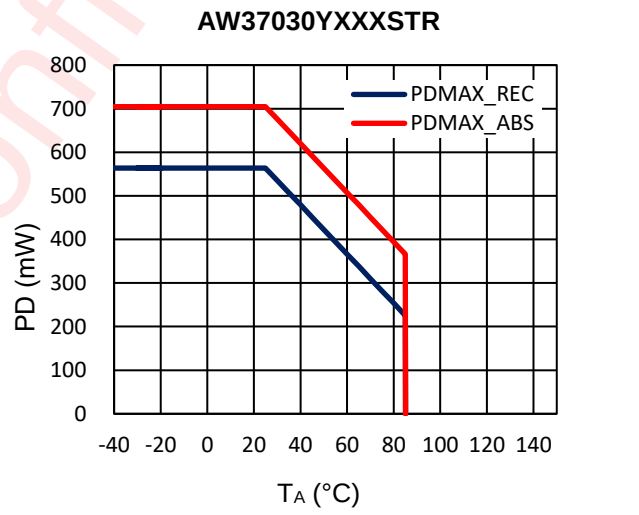
$$PD_{ACT} = (V_{IN} - V_{OUT}) \times I_{OUT}$$

These equations above establish the relationship between the maximum power dissipation allowed due to thermal consideration, the voltage drop across the device, and the continuous current capability of the device.

The graphs of Power Dissipation vs. Ambient Temperature are showed below :



Power Dissipation vs. Ambient Temperature



Power Dissipation vs. Ambient Temperature

The above graphs show the maximum power dissipation of the respective package at T_{J_REC} = 125°C and T_{J_MAX} = 150°C. Operating the device in the region between PD_{MAX_REC} and PD_{MAX_ABS} might have a negative influence on its lifetime.

Capacitors Selection

IN pin: Input Capacitor C_{IN}

AW37030YXXX advises to use a 1μF or more X5R or X7R ceramic capacitor at IN pin as shown in Typical Application Circuit.

OUT pin: Output Capacitor C_{OUT}

AW37030YXXX advises to use a 1μF or more X5R or X7R ceramic capacitor at OUT pin as shown in Typical Application Circuit.

Recommended Components List

Component	PART No.	DESCRIPTION	MFR	TYP.	UNIT
C_{IN}	GRM155R61A105KE15	10V, X5R, 0402	MURATA	1	μF
C_{OUT}	GRM155R61A105KE15	10V, X5R, 0402	MURATA	1	μF

PCB Layout Consideration

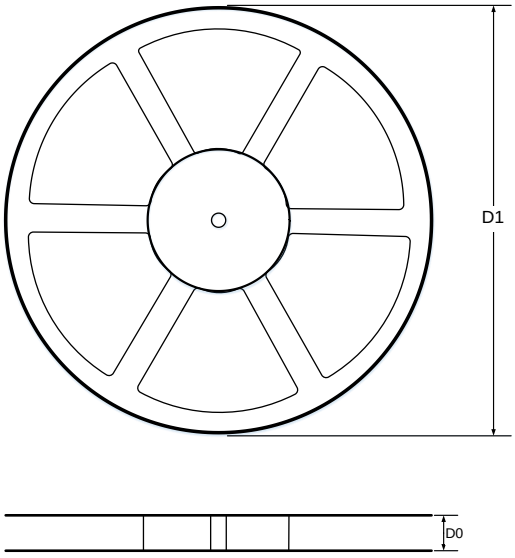
The performance of a power source circuit using this device is highly dependent on a peripheral circuit. To obtain the optimal performance, a peripheral component or the device mounted on PCB should not exceed its rated voltage, rated current or rated power. When designing a peripheral circuit, guidelines below for PCB layout of AW37030YXXX should be obeyed:

1. All peripheral components should be placed as close to the chip as possible. C_{IN} and C_{OUT} should be close to IN and OUT pins respectively. Avoid connecting device and chip pins with two different layers of copper, use the same layer of copper instead.
2. IN and OUT pin are the large current input and output of the chip, make IN, OUT, and meanwhile GND lines sufficient.
3. The connection lines between the planes of C_{IN} or C_{OUT} and respective chip pin should be as short and wide as possible, to reduce noise and EMI interference, or it may cause noise pickup or unstable operation.
4. The exposed plane of chip and GND pins must be connected to the large-area ground layer of PCB directly, meanwhile place sufficient vias below the exposed plane. Thus we can decrease the thermal resistor on the board to optimize heat-diffusion performance.

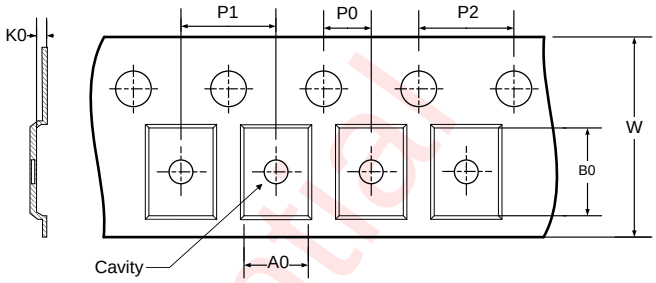
Tape And Reel Information

DFN 1mmX1mm-4L

REEL DIMENSIONS

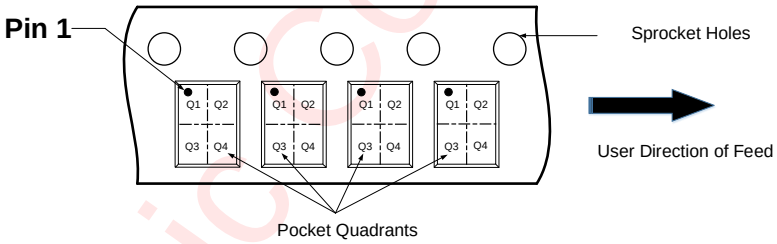


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

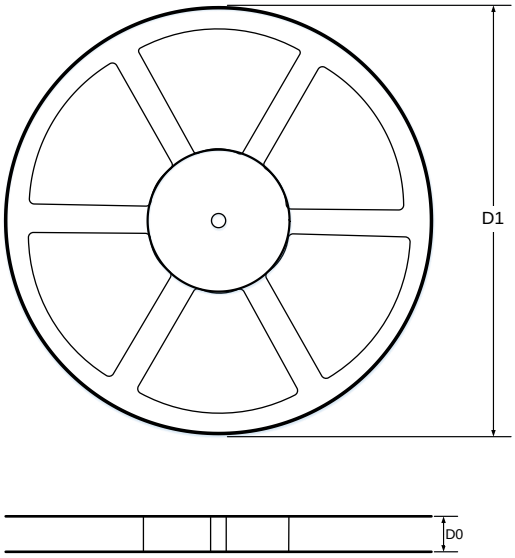
DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.4	1.14	1.17	0.56	2	4	4	8	Q1

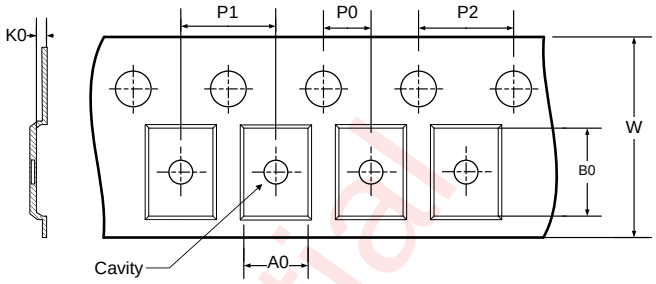
All dimensions are nominal

SOT 23-5L

REEL DIMENSIONS

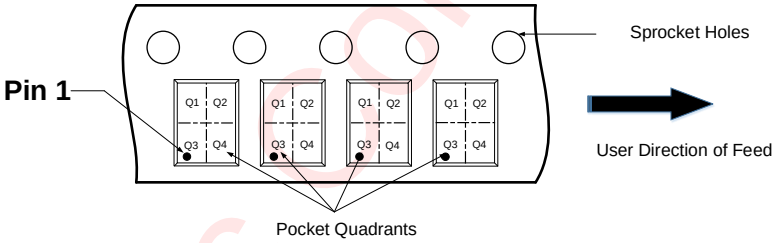


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

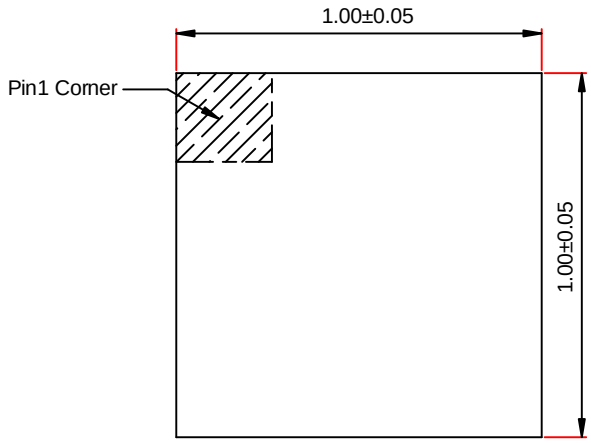
DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.4	3.3	3.2	1.4	2	4	4	8	Q3

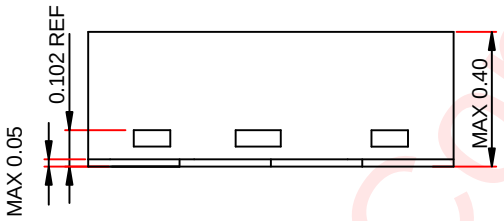
All dimensions are nominal

Package Description

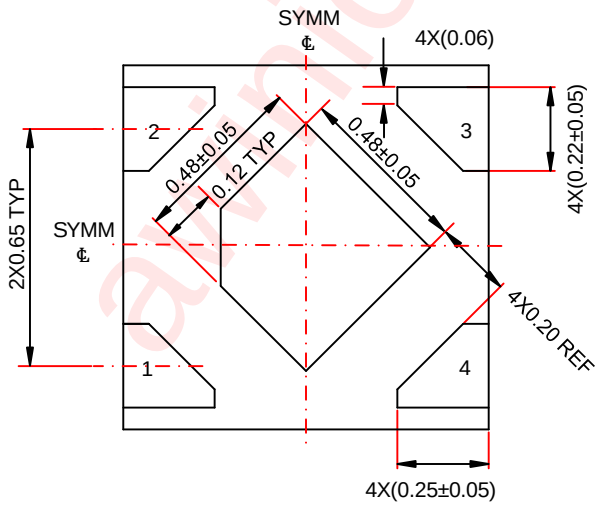
DFN 1mmX1mm-4L



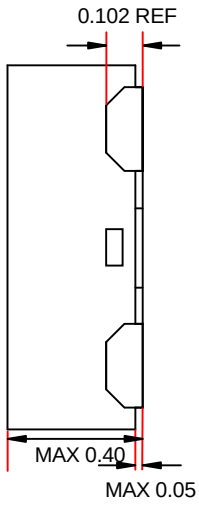
Top View



Side View



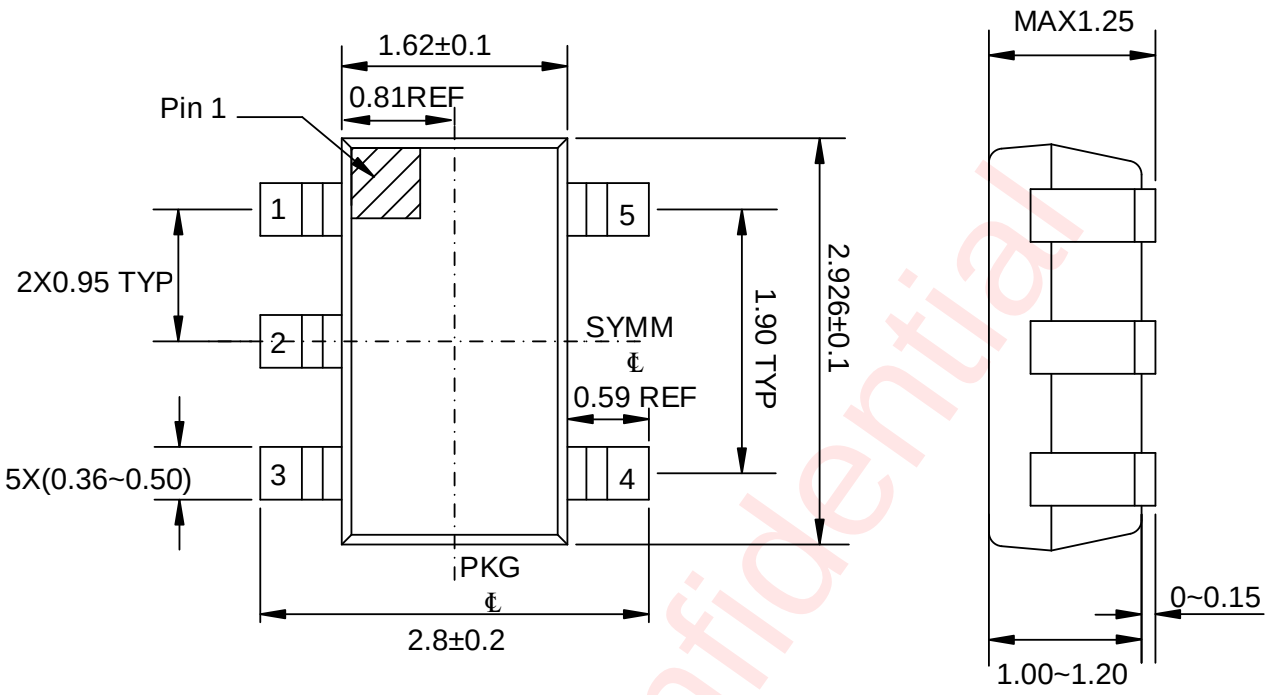
Bottom View



Side View

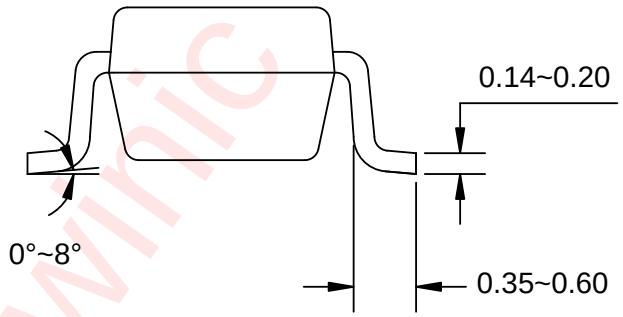
Unit:mm

SOT 23-5L



Top View

Side View

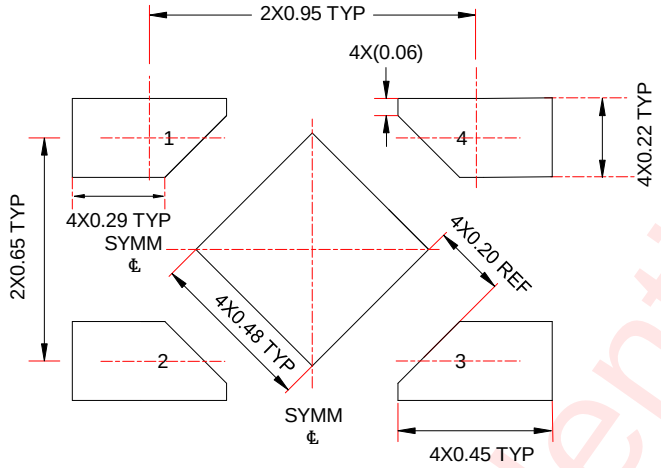


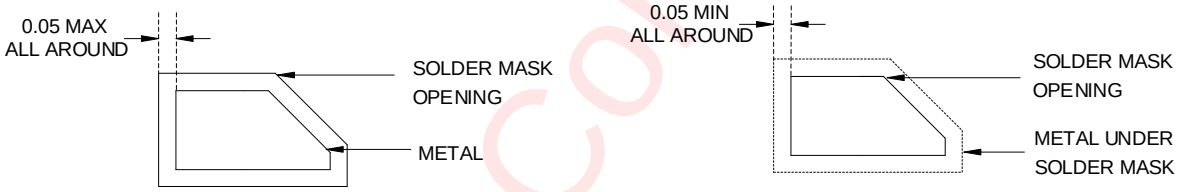
Side View

Unit: mm

Land Pattern Data

DFN 1mmX1mm-4L



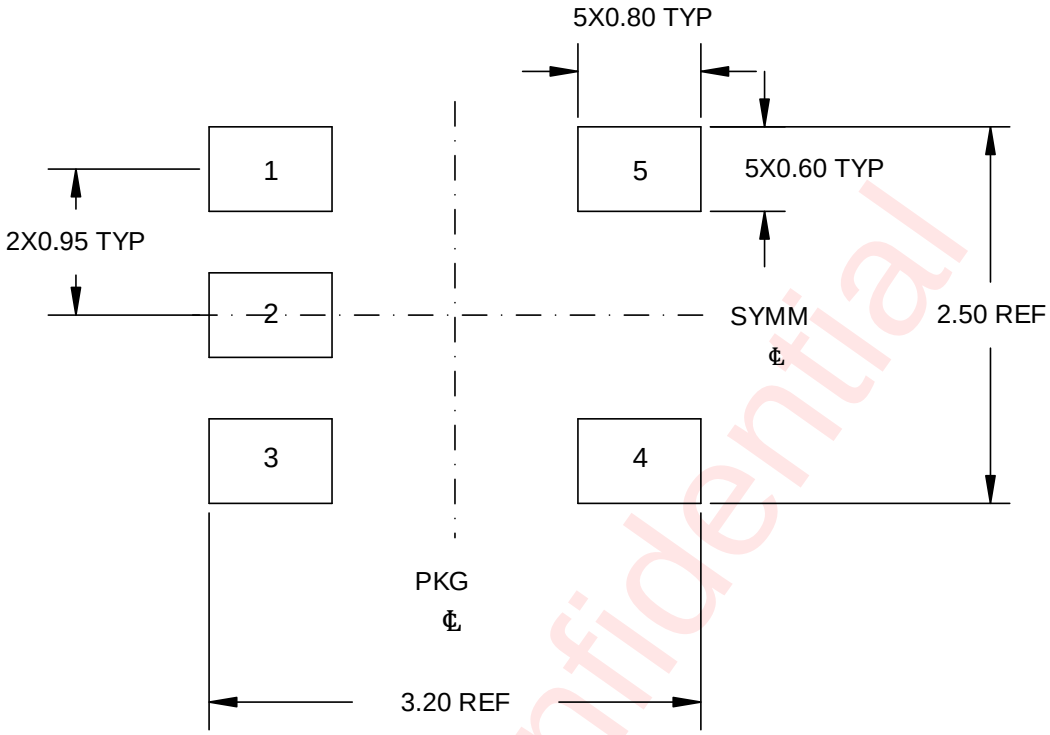


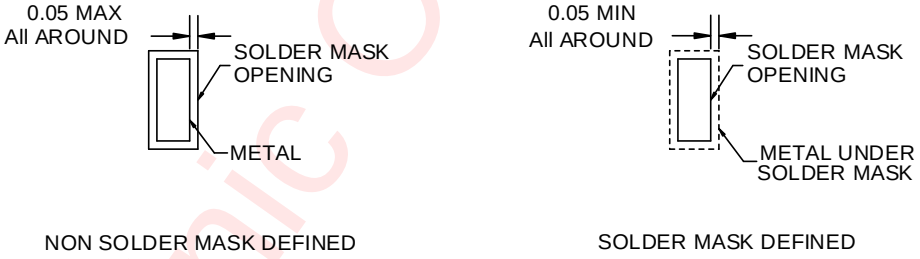
NON SOLDER MASK DEFINED

SOLDER MASK DEFINED

UNIT : mm

SOT 23-5L



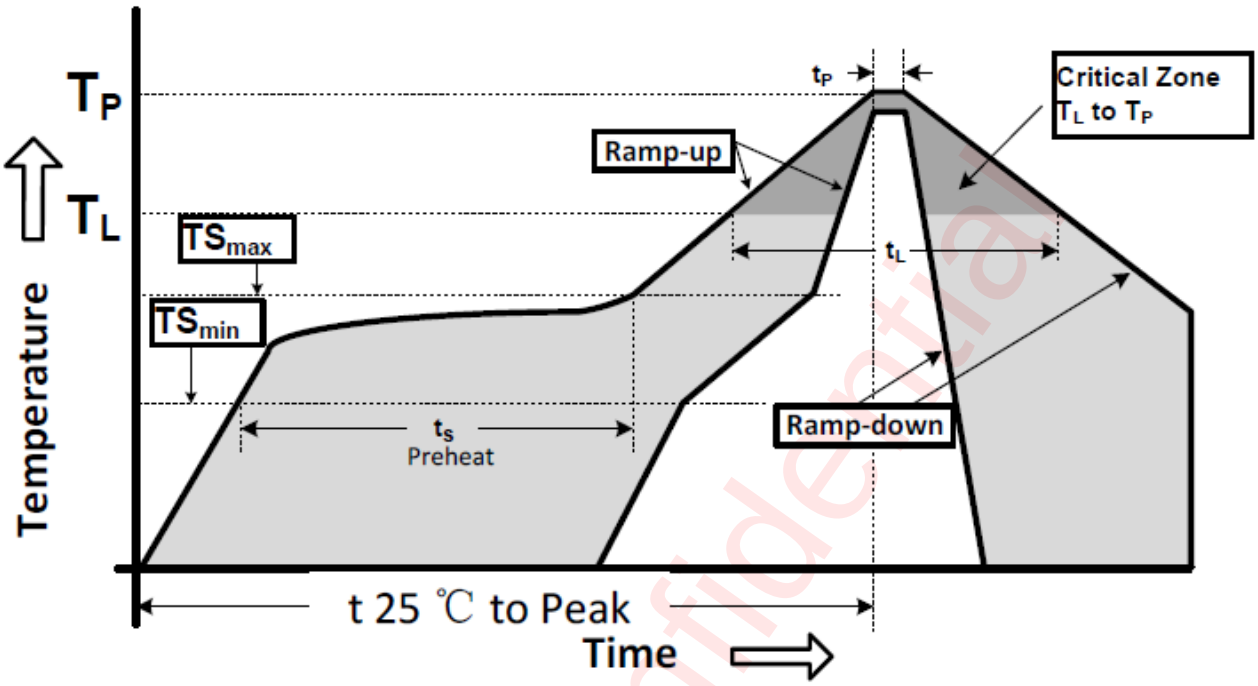


NON SOLDER MASK DEFINED

SOLDER MASK DEFINED

Unit: mm

Reflow



Reflow Note	Spec
Ramp-up rate（TSmax to T_P）	3°C/second max.
Preheat temperature（TSmin to TSmax）	150°C to 200°C
Preheat time（t_s）	60 - 180 seconds
Time above T_L , 217°C（t_L）	60 - 150 seconds
Peak temperature（T_P）	260°C
Time within 5°C of peak temperature(t_P)	20 - 40 seconds
Ramp-down rate	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

Revision History

Version	Date	Change Record
V1.0	Jan. 2020	Officially released
V1.1	Nov. 2020	V_{OUT_ACC} at T_A=25℃ change to ±1%; $LOAD_{REG}$ MAX change to 20mV; I_Q MAX change to 100μA
V1.2	Jan. 2021	Add V_{OUT} of 1.2V and 2.5V
V1.3	Jan. 2021	Add Maximum power consumption and Inrush Current
V1.4	Mar. 2021	Add test waves of 1.2V; Add name rule; Add V_{OUT} of 1.1V and 1.5V; Add wave of Output Spectral Noise Density
V1.5	Apr. 2021	Add SOT 23-5L package
V1.6	Jul. 2021	Add V_{OUT} of 2.85V and 3.1V; Remove test waves of 1.2V and add electical characteristics of 1.1V
V1.7	Oct. 2021	Replenish Thermal Metric parameters; Add V_{OUT} of 2.9V 2.95V; Add graphs of Power Dissipation vs. Ambient Temperature; Add reflow curve; Add max of $V_{dropout}$
V1.8	Aug. 2022	Update Tape And Reel Information of DFN 1mmX1mm-4L and SOT 23-5L packages; Update Package Description of SOT 23-5L package

Disclaimer

All trademarks are the property of their respective owners. Information in this document is believed to be accurate and reliable. However, Shanghai AWINIC Technology Co., Ltd (AWINIC Technology) does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

AWINIC Technology reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. Customers shall obtain the latest relevant information before placing orders and shall verify that such information is current and complete. This document supersedes and replaces all information supplied prior to the publication hereof.

AWINIC Technology products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an AWINIC Technology product can reasonably be expected to result in personal injury, death or severe property or environmental damage. AWINIC Technology accepts no liability for inclusion and/or use of AWINIC Technology products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications that are described herein for any of these products are for illustrative purposes only. AWINIC Technology makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

All products are sold subject to the general terms and conditions of commercial sale supplied at the time of order acknowledgement.

Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Reproduction of AWINIC information in AWINIC data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. AWINIC is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of AWINIC components or services with statements different from or beyond the parameters stated by AWINIC for that component or service voids all express and any implied warranties for the associated AWINIC component or service and is an unfair and deceptive business practice. AWINIC is not responsible or liable for any such statements.

单击下面可查看定价，库存，交付和生命周期等信息

>>AWINIC(艾为)