Low Noise Amplifier for Global Navigation Satellite Systems (GNSS)

Features

- Reduce RF environment Interference with patented Smart-Linearity-Technology (SLT)
- Ultra low current=1.2 mA
- Low noise figure(NF)=0.7 dB
- High power gain=18.2 dB
- High input 1dB-compression point=-7 dBm
- GPS L1 requires only one input matching inductor
- RF output internally matched to 50 ohm for GPS L1
- Supply voltage: 1.5 V to 3.1 V
- Operating frequencies: 1550~1615 MHz, 1164~1215 MHz
- DFN 1.1 mmX0.7 mmX0.37 mm-6L package
- ±2 kV HBM ESD protection (including RFIN and RFOUT pin)

Applications

- Smart phones, feature phones
- Tablet PCs
- Personal Navigation Devices
- Digital Still Cameras, Digital Video Cameras
- RF Front End modules
- Complete GPS chipset modules
- Theft protection(laptop, ATM)

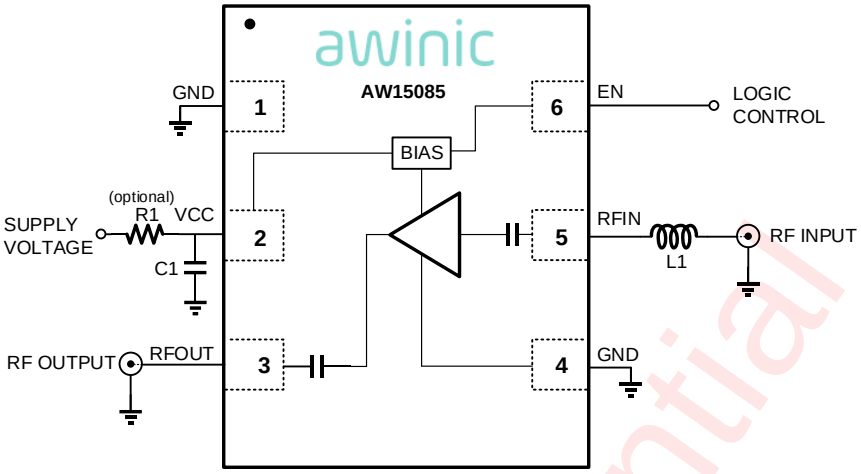
General Description

The AW15085 is a Low Noise Amplifier designed for Global Navigation Satellite Systems (GNSS) as GPS, Beidou, GLONASS, Galileo and Compass. With on-chip DC blocking capacitors at RFIN and RFOUT, the AW15085 can be close to the antenna. The AW15085 requires only one external input matching inductor for GPS L1, which can reduce assembly complexity and the PCB area, enabling a cost-effective solution.

The AW15085 with patented Smart Linearity Technology (SLT) achieves low noise figure, high linearity, high gain, over a wide range of supply voltages from 1.5 V up to 3.1 V. All these features make AW15085 an excellent choice for GNSS LNA as it improves sensitivity with low noise figure and high gain, provides better immunity against out-of-band jammer signals with high linearity, reduces filtering requirement of preceding stage and hence reduces the overall cost of the GNSS receiver.

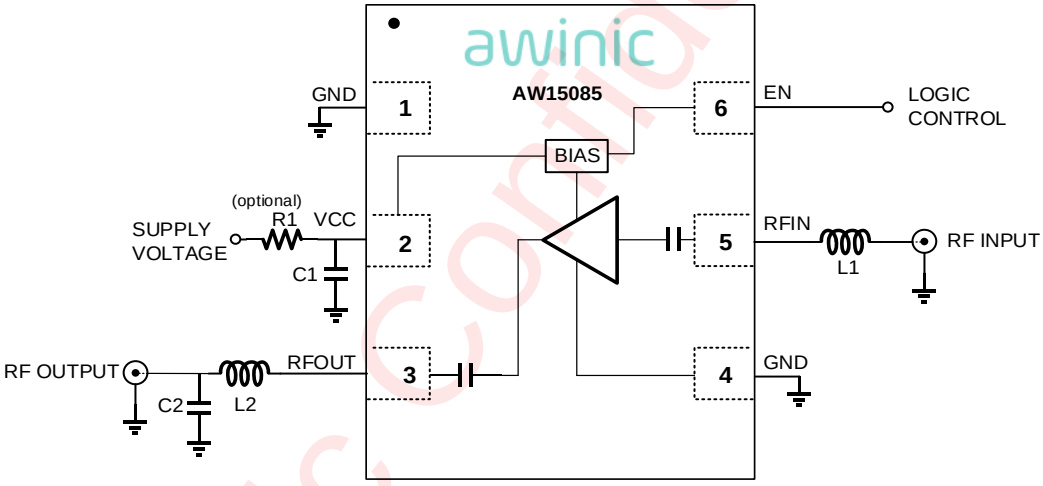
The AW15085 is available in a small lead-free, RoHS-Compliant, DFN 1.1 mm X 0.7 mm X 0.37 mm-6L package.

Typical Application Circuit



C1, R1, L1 Closed to LNA

Typical Application Circuit of AW15085 for GNSS L1



C1, R1, L1, C2, L2 Closed to LNA

Typical Application Circuit of AW15085 for GNSS L5

Recommended Components List

Table1 and Table2 list the recommended components types and values.

Table1: list of components for GNSS L1

Component	Part Number	Inductance	Q(min)	Q Test Frequency	Supplier	Size
L1	LQW15A	12nH	30	250MHz	Murata	0402
L1	SDWL1005C	12nH	28	250MHz	Sunlord	0402

Component	Part Number	Capacitance	Rated Voltage	Supplier	Size
C1	GRM155	1nF	50V	Murata	0402

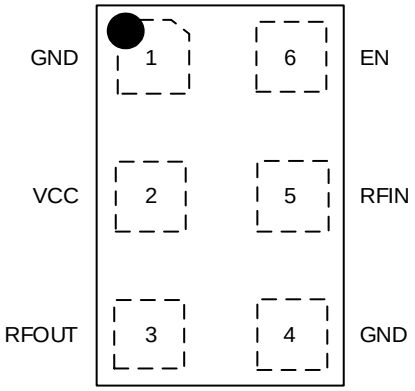
Table2: list of components for GNSS L5

Component	Part Number	Inductance	Q(min)	Q Test Frequency	Supplier	Size
L1	LQW15A	20nH	30	250MHz	Murata	0402
L2	LQW15A	12nH	30	250MHz	Murata	0402

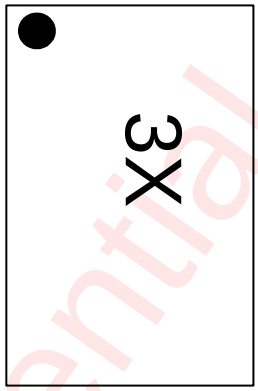
Component	Part Number	Capacitance	Rated Voltage	Supplier	Size
C1	GRM155	1nF	50V	Murata	0402
C2	GRM155	3.3pF	50V	Murata	0402

Pin Configuration And Top Mark

AW15085DNR
(Top View)



AW15085DNR Marking
(Top View)



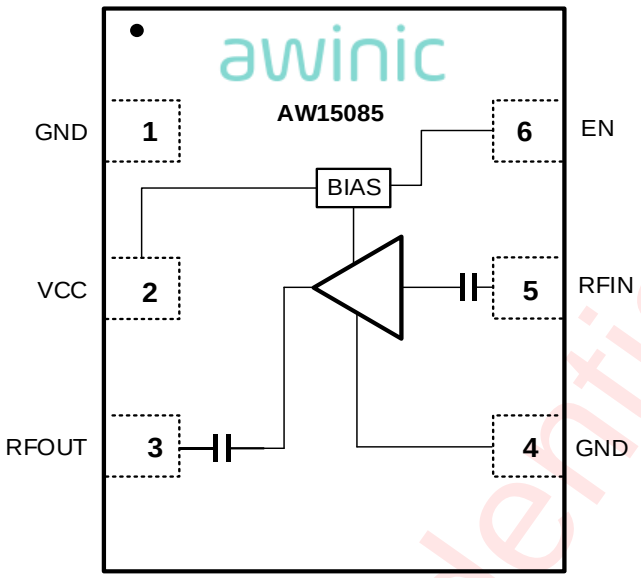
3 – AW15085DNR
X – Production Tracing Code

Pin Configuration and Top Mark

Pin Definition

No.	NAME	DESCRIPTION
1	GND	Ground
2	VCC	DC Supply
3	RFOUT	LNA output
4	GND	Ground
5	RFIN	LNA input
6	EN	Logic control

Functional Block Diagram



Functional Block Diagram

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW15085DNR	-40°C ~ 85°C	DFN 1.1mmX0.7mm-6L	3	MSL1	ROHS+HF	3000 units/ Tape and Reel

Absolute Maximum Ratings[1]

PARAMETERS	Symbol	Values			Unit
		Min.	Typ.	Max.	
Supply Voltage at pin VCC	VCC	-0.3	-	3.3	V
Voltage at pin EN [2]	V_{EN}	-0.3	-	3.3	V
Current into pin VCC	I_{CC}	-	-	10	mA
RF input power [3]	P_{IN}	-	-	0	dBm
Junction temperature	T_J	-	-	150	°C
Storage temperature range	T_{STG}	-65	-	150	°C
Ambient temperature range	T_{amb}	-40	-	85	°C
Solder temperature(10s)		-	260	-	°C
ESD range					
HBM [4]		±2			kV
CDM [5]		±1			kV
Latch-up					
Test condition: JESD78E		+IT: +200 -IT: -200			mA mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: Warning: due to internal ESD diode protection, the applied DC voltage should not exceed 3.3V in order to avoid excess current.

NOTE3: The RF input and RF output are AC coupled through internal DC blocking capacitor.

NOTE4: HBM standard: ESDA/JEDEC JS-001.

NOTE5: CDM standard: ESDA/JEDEC JS-002.

Electrical Characteristics

AW15085 EVB[1]; V_{CC}=V_{EN}=2.8 V and TA=+25 °C, f=1575.42 MHz; unless otherwise noted

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
DC ELECTRICAL CHARACTERISTICS						
V_{CC}	Supply Voltage		1.5	-	3.1	V
I_{SD}	Shut-Down Current	EN=Low	-	-	2	μA
I_{CC}	Supply Current	EN=High	-	1.2	1.85	mA
V_{EN}	Digital Input-Logic High		1.0	-	Vcc	V
V_{EN}	Digital Input-Logic Low		0	-	0.3	V
AC ELECTRICAL CHARACTERISTICS						
Gp	Power Gain		15	18.2	20.5	dB
RL_{in}	Input Return Loss		6	10	-	dB
RL_{out}	Output Return Loss		6	15	-	dB
ISL	Reverse Isolation		20	30	-	dB
NF	Noise Figure[2]	Zs=50 ohm; No jammer	-	0.7	1.2	dB
Kf	Stability factor	f=0.1-10GHz	1	-	-	
IP1dB	Inband input 1dB-compression point	f=1575.42MHz	-12	-7	-	dBm
$IIP3_{ib}$	Inband input 3^{rd}-order intercept point[3]	f1=1574.42MHz; f2=1575.42MHz;	-10	-5	-	dBm
$IIP3_{oob}$	Out-of-band input 3^{rd}-order intercept point[4]	f1=1712.7MHz; f2=1850MHz;	-14	-7	-	dBm
t_{on}	turn-on time	time from V_{EN} ON to 90% of the final gain	-	-	2	μs
t_{off}	turn-off time	time from V_{EN} OFF to 10% of the gain	-	-	1	μs

NOTE1: input matched to 50 ohm using a high quality factor 12 nH inductor.
NOTE2: PCB losses are subtracted.
NOTE3: Input power = -20 dBm for each tone.
NOTE4: Input power = -20 dBm at f1 and -65 dBm at f2.

AW15085 EVB[1]; V_{CC}=V_{EN}=1.8 V and TA=+25 °C, f=1575.42 MHz; unless otherwise noted

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
DC ELECTRICAL CHARACTERISTICS						
V_{CC}	Supply Voltage		1.5	-	3.1	V
I_{SD}	Shut-Down Current	EN=Low	-	-	2	μA
I_{CC}	Supply Current	EN=High	-	1.2	1.8	mA
V_{EN}	Digital Input-Logic High		1.0	-	Vcc	V
V_{EN}	Digital Input-Logic Low		0	-	0.3	V
AC ELECTRICAL CHARACTERISTICS						
Gp	Power Gain		15	17.7	20	dB
RL_{in}	Input Return Loss		6	10	-	dB
RL_{out}	Output Return Loss		6	15	-	dB
ISL	Reverse Isolation		20	30	-	dB
NF	Noise Figure[2]	Zs=50 ohm; No jammer	-	0.75	1.25	dB
Kf	Stability factor	f=0.1-10GHz	1	-	-	
IP1dB	Inband input 1dB-compression point	f=1575.42MHz	-15	-10	-	dBm
$IIP3_{ib}$	Inband input 3^{rd}-order intercept point[3]	f1=1574.42MHz; f2=1575.42MHz;	-10	-5	-	dBm
$IIP3_{oob}$	Out-of-band input 3^{rd}-order intercept point[4]	f1=1712.7MHz; f2=1850MHz;	-14	-7	-	dBm
t_{on}	turn-on time	time from V_{EN} ON to 90% of the final gain	-	-	2	μs
t_{off}	turn-off time	time from V_{EN} OFF to 10% of the gain	-	-	1	μs

NOTE1: input matched to 50 ohm using a high quality factor 12 nH inductor.
NOTE2: PCB losses are subtracted.
NOTE3: Input power = -20 dBm for each tone.
NOTE4: Input power = -20 dBm at f1 and -65 dBm at f2.

AW15085 EVB[1]; V_{CC}=V_{EN}=2.8 V and TA=+25 °C, f=1176.45 MHz; unless otherwise noted

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
DC ELECTRICAL CHARACTERISTICS						
V_{CC}	Supply Voltage		1.5	-	3.1	V
I_{SD}	Shut-Down Current	EN=Low	-	-	2	μA
I_{CC}	Supply Current	EN=High	-	1.2	1.85	mA
V_{EN}	Digital Input-Logic High		1.0	-	Vcc	V
V_{EN}	Digital Input-Logic Low		0	-	0.3	V
AC ELECTRICAL CHARACTERISTICS						
Gp	Power Gain		14	17.5	19.5	dB
RL_{in}	Input Return Loss		6	10	-	dB
RL_{out}	Output Return Loss		6	15	-	dB
ISL	Reverse Isolation		25	35	-	dB
NF	Noise Figure[2]	Zs=50 ohm; No jammer	-	0.7	1.2	dB
Kf	Stability factor	f=0.1-10GHz	1	-	-	
IP1dB	Inband input 1dB-compression point	f=1176.45MHz	-15	-10	-	dBm
$IIP3_{ib}$	Inband input 3^{rd}-order intercept point[3]	f1=1175.45MHz; f2=1176.45MHz;	-12	-7	-	dBm
$IIP3_{oob}$	Out-of-band input 3^{rd}-order intercept point[4]	f1=1800MHz; f2=2400MHz;	-3	3.5	-	dBm
t_{on}	turn-on time	time from V_{EN} ON to 90% of the final gain	-	-	2	μs
t_{off}	turn-off time	time from V_{EN} OFF to 10% of the gain	-	-	1	μs

NOTE1: input matched to 50 ohm using a high quality factor 20 nH inductor. Output matching using 12nH inductor and 3.3pF capacitor.

NOTE2: PCB losses are subtracted.

NOTE3: Input power = -20 dBm for each tone.

NOTE4: Input power = -25 dBm for each tone.

AW15085 EVB[1]; V_{CC}=V_{EN}=1.8 V and TA=+25 °C, f=1176.45 MHz; unless otherwise noted

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
DC ELECTRICAL CHARACTERISTICS						
V_{CC}	Supply Voltage		1.5	-	3.1	V
I_{SD}	Shut-Down Current	EN=Low	-	-	2	μA
I_{CC}	Supply Current	EN=High	-	1.2	1.8	mA
V_{EN}	Digital Input-Logic High		1.0	-	Vcc	V
V_{EN}	Digital Input-Logic Low		0	-	0.3	V
AC ELECTRICAL CHARACTERISTICS						
Gp	Power Gain		13.5	17	19	dB
RL_{in}	Input Return Loss		6	10	-	dB
RL_{out}	Output Return Loss		6	15	-	dB
ISL	Reverse Isolation		25	35	-	dB
NF	Noise Figure[2]	Zs=50 ohm; No jammer	-	0.75	1.25	dB
Kf	Stability factor	f=0.1-10GHz	1	-	-	
IP1dB	Inband input 1dB-compression point	f=1176.45MHz	-19	-14	-	dBm
$IIP3_{ib}$	Inband input 3^{rd}-order intercept point[3]	f1=1175.45MHz; f2=1176.45MHz;	-15	-10	-	dBm
$IIP3_{oob}$	Out-of-band input 3^{rd}-order intercept point[4]	f1=1800MHz; f2=2400MHz;	-3	3.5	-	dBm
t_{on}	turn-on time	time from V_{EN} ON to 90% of the final gain	-	-	2	μs
t_{off}	turn-off time	time from V_{EN} OFF to 10% of the gain	-	-	1	μs

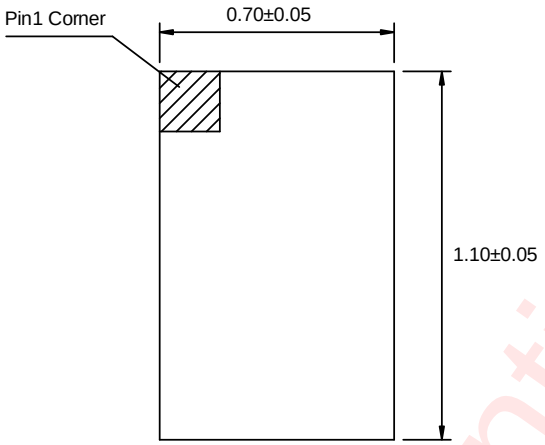
NOTE1: input matched to 50 ohm using a high quality factor 20 nH inductor. Output matching using 12nH inductor and 3.3pF capacitor.

NOTE2: PCB losses are subtracted.

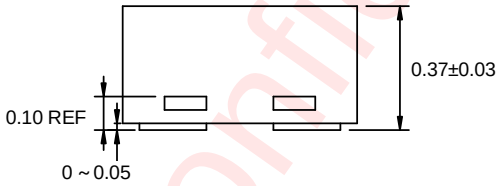
NOTE3: Input power = -20 dBm for each tone.

NOTE4: Input power = -25 dBm for each tone.

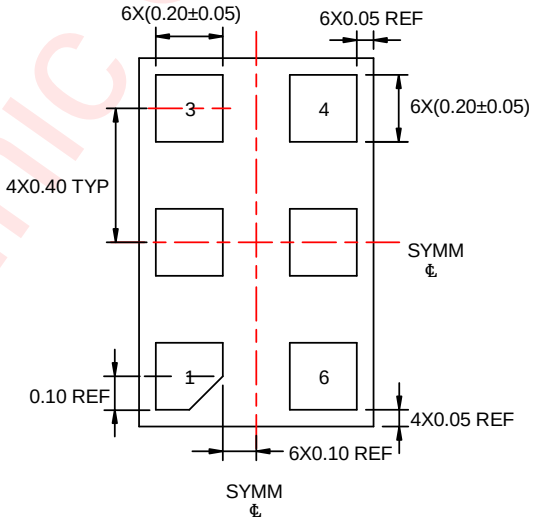
Package Description



TOP VIEW



SIDE VIEW

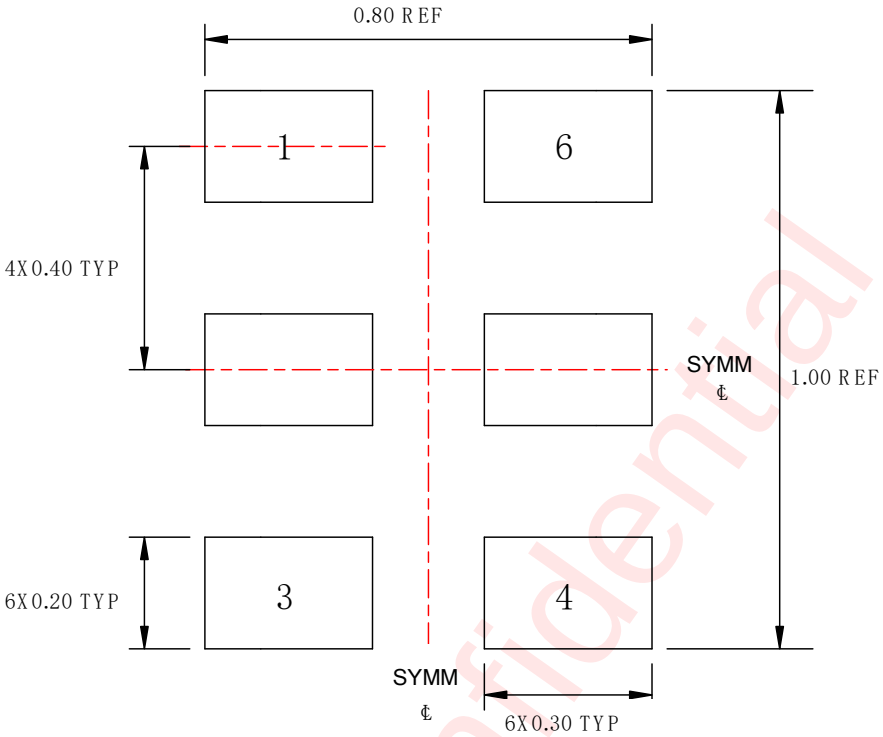


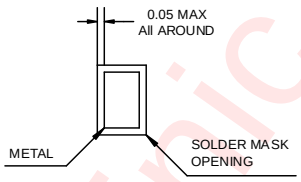
BOTTOM VIEW

Unit: mm

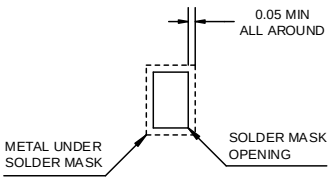
Package Outline

Land Pattern





NON-SOLDER MASK DEFINED



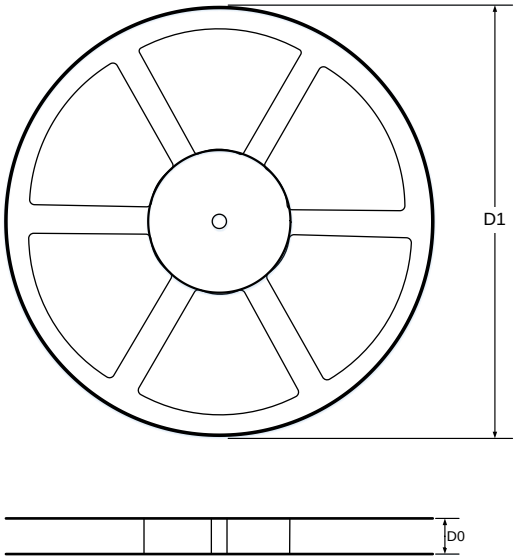
SOLDER MASK DEFINED

Unit: mm

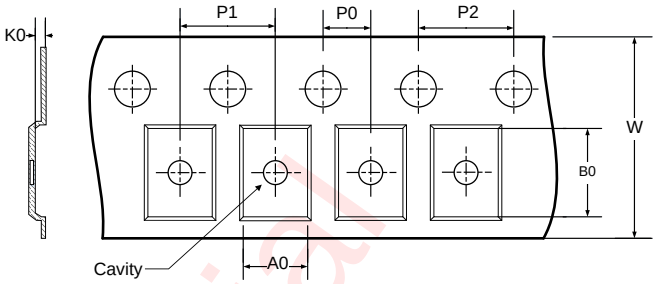
Land Pattern

Tape & Reel Description

REEL DIMENSIONS

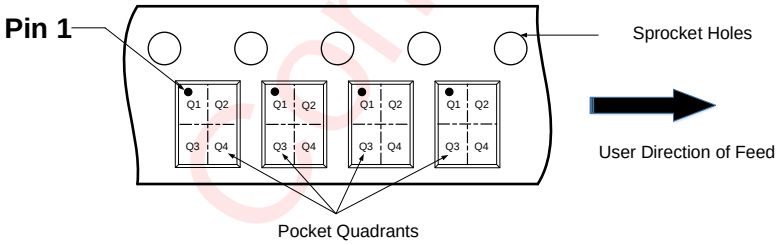


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.4	0.82	1.22	0.46	2	2	4	8	Q1

All dimensions are nominal

Tape & Reel Description

Revision History

Version	Date	Change Record
V1.0	Mar. 2020	Officially Released
V1.1	May. 2020	Add GPS L5
V1.2	May. 2021	Add Spec
V1.3	Nov. 2022	Updated DC electrical characteristics of V_{EN}

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