AW8646 Dual H-Bridge Stepper Motor Driver

FEATURES

- 3V to 12V Supply Voltage Range
- 1.4A Full Scale current per H-Bridge
- Rdson HS + LS: Typical 0.8Ω
- Support up to 1/32th Microstepping
- Decay Modes supported:
  - Adaptive Decay Technology
  - Mixed Decay
  - Slow Decay
  - Fast Decay
- Support 1.8V Logic Level
- Programmable off-time

  10,20, or 30µs off-time
- Programmable Motor Torque Current
- Short-Circuit Protection, Over-Temperature Protection, Under-Voltage Protection
- Fault Condition Indication
- QFN 4mm X4mm X0.85mm-24L package

APPLICATIONS

- Mobile phones
- Tablets
- Printer
- Video Security Cameras

GENERAL DESCRIPTION

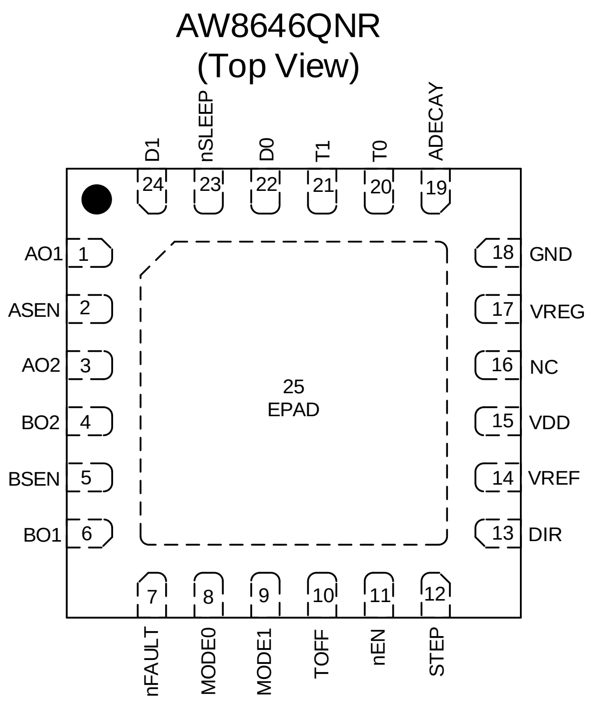
The AW8646 is a flexible microstepping stepper motor driver. It is designed to operate bipolar stepper motor with up to 1/32th step mode for mobile phones, tablets, and other automated equipment applications. The device can be controlled by simple STEP/DIR interface allowing easy interfacing to controller circuits. The output block of each H-bridge driver consists of N-channel and P-channel power MOSFETS configured as full H-bridges to drive the motor windings.

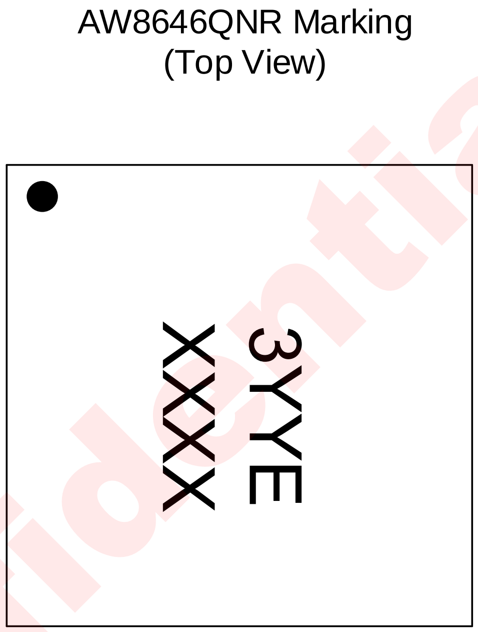
Pins allow configuration of the motor in full-step up to 1/32th step modes. Decay mode is configurable so that adaptive decay, slow decay, fast decay, and mixed decay can be used. A low power sleep mode is provided to achieve very-low quiescent current draw.

AW8646 is capable of driving up to 1.4A (Full Scale) or 1A (RMS) current per H-Bridge

The device offers a complete set of protection features including UVLO, overcurrent protection, short circuit protection, and over temperature. Fault conditions are indicated via the nFAULT pin.

PIN CONFIGURATION AND TOP MARK





3YYE - AW8646QNR
XXXX - Production Tracing Code

Figure 1 Pin Configuration And Top Mark

PIN DEFINITION

No.	NAME	DESCRIPTION
1	AO1	H-bridge A output
2	ASEN	Sense output of bridge A, If current regulation is not required it must connect to GND
3	AO2	H-bridge A output
4	BO2	H-bridge B output
5	BSEN	Sense output of bridge B, If current regulation is not required it must connect to GND
6	BO1	H-bridge B output
7	nFAULT	Pulled low when a failure occurs, open-drain output requires external pull up
8	MODE0	Tri-level pin, low bit of step mode setting pins, controls step mode (full, half, up to 1/32th step) , see description section
9	MODE1	Tri-level pin, high bit of step mode setting pins, controls step mode (full, half, up to 1/32th step) , see description section
10	TOFF	Tri-level pin, decay mode off time set, sets the off-time during current control
11	nEN	Driver enable control input pin. Logic low to enable device outputs, logic high to disable device outputs
12	STEP	Step input, A rising or falling edge increases one step
13	DIR	Direction input, sets the direction of stepping
14	VREF	Full scale current reference input, Voltage on this pin sets the full scale current; short to VREG if not supplying an external reference voltage
15	VDD	Power supply, Connect to motor power supply
16	NC	No connect, Unused pin
17	VREG	Internal regulator, Internal supply voltage
18	GND	Ground pin, both the GND pin and device thermal pad must be connected to ground
19	ADECAY	Adaptive Decay mode control pin, when set to logic low, decay modes controlled by D0 and D1 pins; when set to logic high, Adaptive Decay mode is enabled, must be set prior to coming out of sleep
20	T0	Tri-level pin, Scales the torque current from 100% to 12.5% in 12.5% steps, see description section
21	T1	Tri-level pin, Scales the torque current from 100% to 12.5% in 12.5% steps, see description section
22	D0	Tri-level pin, Decay mode setting pins, see description section
23	nSLEEP	Sleep mode input, Logic high to enable device; logic low to enter low-power sleep mode; internal pull down
24	D1	Tri-level pin, Decay mode setting pins, see description section
25	EPAD	Thermal pad, must be connected to GND

FUNCTIONAL BLOCK DIAGRAM

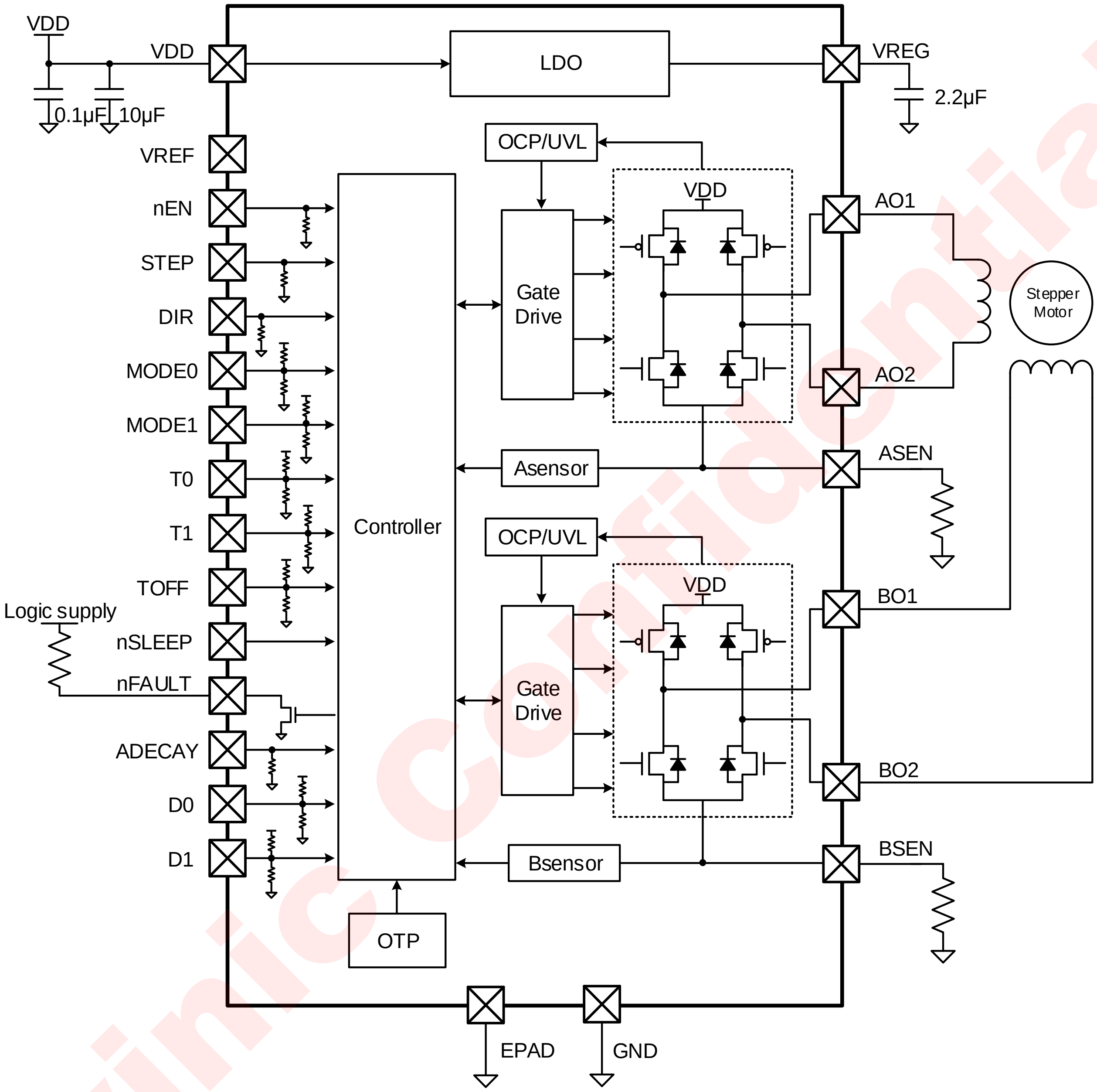
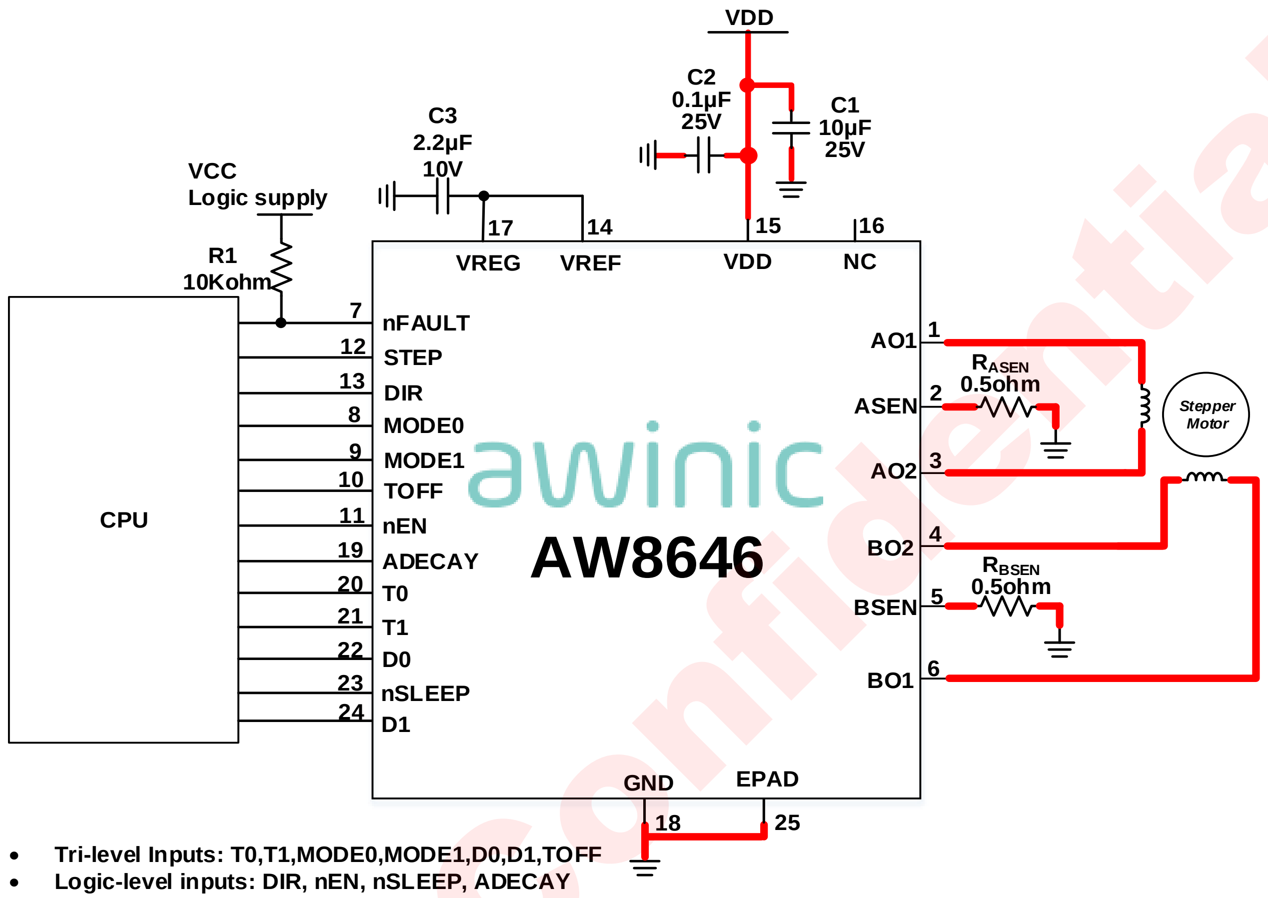


Figure 2 Functional Block Diagram

TYPICAL APPLICATION CIRCUITS



- Tri-level Inputs: T0,T1,MODE0,MODE1,D0,D1,TOFF
- Logic-level inputs: DIR, nEN, nSLEEP, ADECAY
- PWM signal: STEP
- The current of RxSEN is equal to the current of motor, refer to the application maxium motor current when calculate the power of RxSEN

Figure 3 Typical Application Circuit of AW8646

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Notice for Typical Application Circuits:

1：Please place C1，C2，C3 as close to the chip as possible. The capacitors should be placed in the same layer with the AW8646 chip.

2：For the sake of driving capability, the power lines (especially the one to Pin C2) and output lines should be short and wide as possible.

3：Table 1 lists the recommended external components for the device.

Table 1 External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C_1	VDD	GND	25V, 10μF (minimum) ceramic capacitor rated for VDD
C_2	VDD	GND	25V, 0.1μF ceramic capacitor rated for VDD
C_3	VREG	GND	10V, 2.2μF ceramic capacitor
R1	VCC	nFAULT	>5kΩ
R_{ASEN}	ASEN	GND	Sense resistor, see applications section for sizing
R_{BSEN}	BSEN	GND	Sense resistor, see applications section for sizing

ORDERING INFORMATION

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW8646 QNR	-40℃~85℃	QFN 4mmX4mm-24L	3YYE	MSL3	ROHS+HF	6000 units/Tape and Reel

ABSOLUTE MAXIMUM RATINGS(NOTE1)

PARAMETERS	RANGE
Power supply voltage (VDD)	-0.3V to 16V
Power supply voltage ramp rate (VDD)	0V/µs to 2 V/µs
Internal regulator voltage (VREG)	-0.3V to 3.6V
Analog input pin voltage (VREF)	-0.3V to 3.6V
Control pin voltage (nEN, STEP, DIR, T0, T1, MODE0, MODE1, D0, D1, TOFF, nSLEEP,nFAULT, ADECAY)	-0.3V to 7V
Continuous phase node pin voltage (AO1, AO2, BO1, BO2)	-0.3V to (VDD+0.6)V
Continuous shunt amplifier input pin voltage (ASEN, BSEN)	-0.6V to 0.6V
Peak drive current (AO1, AO2, BO1, BO2, ASEN, BSEN)	Internally limited
Junction-to-ambient thermal resistance θ_{JA}	60°C /W
Operating free-air temperature range	-40°C to 85°C
Maximum operating junction temperature T_{JMAX}	165°C
Storage temperature T_{STG}	-65°C to 150°C
Lead temperature (soldering 10 seconds)	260°C
ESD(Including CDM HBM MM)(NOTE 2)	
HBM(Human Body Model)	±4kV
CDM(Charge Device Model)	±1.5kV
Latch-Up	
Test Condition: JEDEC STANDARD NO.78E	+IT：200mA -IT：-200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ANSI/ESDA/JEDEC JS-001

ELECTRICAL CHARACTERISTICS

VDD=5V, T_A=25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (VDD, VREG)						
VDD	VDD operating voltage		3	5	12	V
I_{VDD}	VDD operating supply current	VDD = 5 V, excluding winding current, nSLEEP = 1, nEN = 0 or 1	1.0	2.5	4.0	mA
I_{VDDQ}	VDD sleep mode supply current	VDD = 5 V, nSLEEP = 0, nEN = 0 or 1		0.1	1	μA
t_{SLEEP}	Sleep time	nSLEEP = 0 to sleep mode		0.7		ms
t_{WAKE}	Wake time	nSLEEP = 1 to output transition		0.5		ms
t_{ON}	Power-on time	VDD > V_{UVLO} rising to output transition		0.5		ms
VREG	VREG voltage	VDD > 4 V, I_{OUT} = 0 A to 1 mA	3.13	3.3	3.47	V
LOGIC-LEVEL INPUTS (STEP, DIR, nEN, nSLEEP, ADECAY)						
V_{IL}	Input logic low voltage		0		0.45	V
V_{IH}	Input logic high voltage		1.3		5.5	V
V_{HYS}	Input logic hysteresis			100		mV
I_{IL}	Input logic low current	VIN = 0 V	–1		1	μA
I_{IH}	Input logic high current	VIN = 5 V	1		40	μA
R_{PD}	Pulldown resistance	nEN, STEP, DIR, ADECAY		200		kΩ
		nSLEEP		500		kΩ
t_{DEG}	Input deglitch time			200		ns
t_{PROP}	Propagation delay	STEP edge to current change		600		ns
TRI-LEVEL INPUTS (T0, T1, MODE0, MODE1, D0, D1, TOFF)						
V_{IL}	Tri-level input logic low voltage		0		0.45	V
V_{IZ}	Tri-level input Hi-Z voltage			0.9		V
V_{IH}	Tri-level input logic high voltage		1.3		5.5	V
V_{HYS}	Tri-level input hysteresis			100		mV
I_{IL}	Tri-level input logic low current	V_{IN} = 0 V	–22		–1	μA
I_{IH}	Tri-level input logic high current	V_{IN} = 5 V	1		40	μA
R_{PD}	Tri-level pulldown resistance	To GND		180		kΩ
R_{PU}	Tri-level pullup resistance	To VREG		480		kΩ
CONTROL OUTPUTS (nFAULT)						
V_{OL}	Output logic low voltage	I_O = 5 mA			0.5	V
I_{OH}	Output logic high leakage	V_O = 3.3 V	–1		1	μA
MOTOR DRIVER OUTPUTS (AO1, AO2, BO1, BO2)						
$R_{DS(ON)}$	High-side FET on resistance	VDD = 5 V, I = 0.5 A, T_J = 25°C		430		mΩ
$R_{DS(ON)}$	Low-side FET on resistance	VDD = 5 V, I = 0.5 A, T_J = 25°C		300		mΩ
t_{RISE}	Output rise time			50		ns
t_{FALL}	Output fall time			50		ns
t_{DEAD}	Output dead time	Internal dead time		150		ns
PWM CURRENT CONTROL (VREF, ASEN, BSEN)						
I_{REF}	Externally applied VREF input current	VREF = 1 to 3.3 V		2		μA
V_{TRIP}	xSEN trip voltage	For 100% current step with VREF = 3.3 V		500		mV

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
K	Current sense amplifier gain	Reference Only		6.6		V/V
t_{OFF}	Current control constant off time	TOFF = GND		20		µs
		TOFF = Hi-Z		10		
		TOFF = VREG		30		
PROTECTION CIRCUITS						
V_{UVLO}	VDD under voltage lockout	VDD falling; UVLO Report		2.7		V
		VDD rising; UVLO Recovery		2.8		
I_{OCP}	Overcurrent Protection Trip Level		2			A
t_{OCP}	Overcurrent Deglitch Time			0.1		µs
t_{RETRY}	Overcurrent Protection Period			1.6		ms
T_{TSD}	Thermal shutdown temperature	Die Temperature T_J		160		°C
T_{HYS}	Thermal shutdown hysteresis	Die Temperature T_J		30		°C

TIMING REQUIREMENTS

VDD=5V, T_A=25°C for typical values (unless otherwise noted)

NO.	NAME	DESCRIPTION	MIN	MAX	UNIT
1	f_{STEP}	Step Frequency		250	KHz
2	$t_{WH(STEP)}$	Pulse Duration, STEP High	1.9		µs
3	$t_{WL(STEP)}$	Pulse Duration, STEP Low	1.9		µs
4	$t_{SU(STEP)}$	Setup Time, DIR or Mx to STEP Rising	200		ns
5	$t_{H(STEP)}$	Hold Time, DIR or Mx to STEP Rising	600		ns

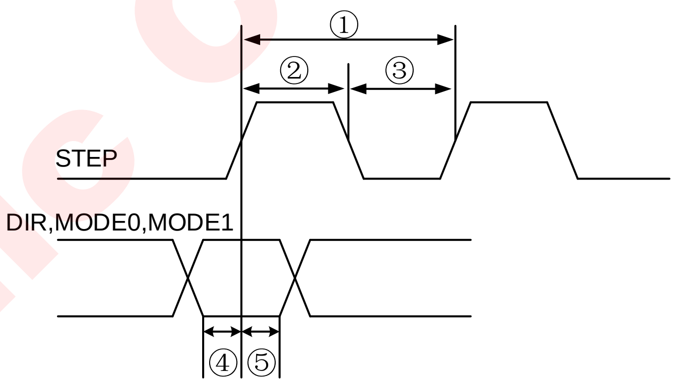


Figure 4 Timing Diagram

DETAILED FUNCTIONAL DESCRIPTION

OVERVIEW

The AW8646 is a bipolar stepper motors driver integrating 2 H-bridges that use NMOS low-side drivers and PMOS high-side drivers, two PWM current controller, and a microstepping sequencer. The AW8646 can be powered with a supply range between 3 to 12V. The AW8646 is capable of driving up to 1.4A (Full Scale) or 1A (RMS) current per H-Bridge.

At each STEP rising edge or falling edge(some step mode), the sequencer of the device increased or decreased as step mode configuration.

The internal sequencer is able to execute high-accuracy microstepping setting the reference value of the PWM current controller and the direction of the current for both of the H-bridge.

The total PWM off-time, t_{OFF} can be adjusted to 10, 20, or 30μs.

The AW8646 has Adaptive Decay Technology that automatically adjusts the decay setting to minimize current ripple. This feature allows the device to quickly be integrated into a system.

The torque current can be adjusted using digital input pins. This allows the controller to save power by decreasing the current consumption when not required.

A low-power sleep mode is included, which allows the system to save power when not driving the motor.

FEATURE DESCRIPTION

PWM MOTOR DRIVERS

AW8646 contains two identical H-bridge motor drivers with current-control PWM circuitry. Figure 2 shows a block diagram of the circuitry.

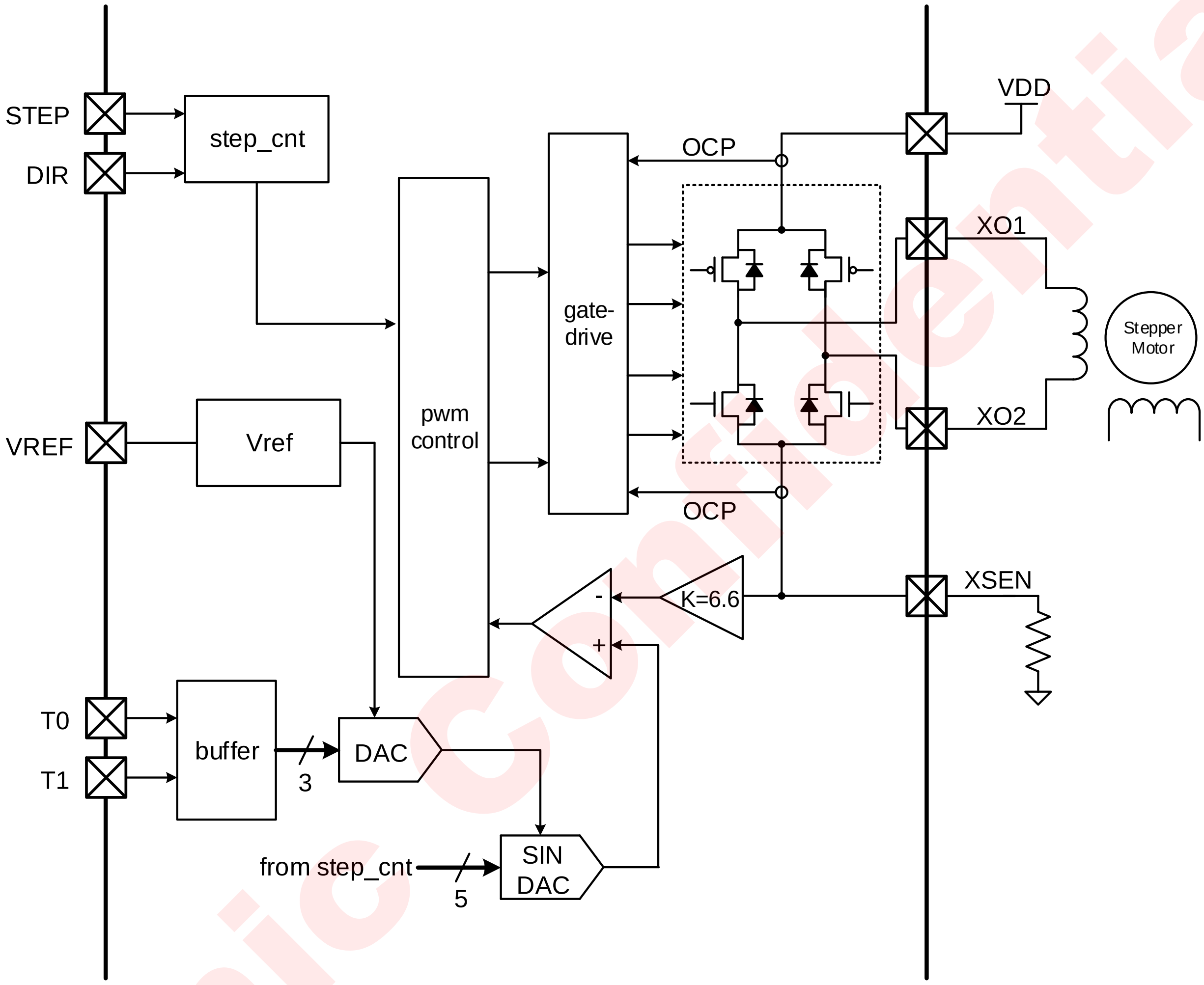


Figure 5 PWM Motor Driver Circuitry

MICRO-STEPPING SEQUENCER

Through step and direction interface the device contains a microstepping sequencer to control the state of the H-bridges automatically. When the correct transition is applied at the STEP input, thesequencer moves to the next step, according to the direction set by the DIR pin. In 1/8th, 1/16th,and 1/32th step modes, both the rising and falling edges of the STEP input may be used to advance the sequencer, depending on the MODE0/MODE1 setting.

The nEN pin can disable the output stage. When nEN = 1, the sequencer inputs are still active and respond to the STEP and DIR input pins; only the output stage is disabled.

The sequencer logic in the AW8646 allows a number of different stepping configurations. The MODE0 and MODE1 pins configure the stepping format (see Table 2).

Table 2 Step Mode Settings

MODE1	MODE0	STEP MODE
0	0	Full step, rising-edge only
0	Z	1/2 step, rising-edge only
0	1	1/4 step, rising-edge only
Z	0	8 microsteps/step, rising-edge only
Z	Z	8 microsteps/step, rising and falling edges
Z	1	16 microsteps/step, rising-edge only
1	0	16 microsteps/step, rising and falling edges
1	Z	32 microsteps/step, rising-edge only
1	1	32 microsteps/step, rising and falling edges

For 1/8, 1/16, and 1/32-step modes, selections are available to advance the sequencer only on the rising edge of the STEP input, or on both the rising and falling edges.

The step mode may be changed on-the-fly while the motor is moving. The sequencer advances to the next valid state for the new MODE0 / MODE1 setting at the next rising edge of STEP.

The home state is 45°. The sequencer enters the home state after power-up, after exiting UVLO, or after exiting sleep mode.

CURRENT REGULATION

The current through the motor windings is regulated by an adjustable fixed-off-time PWM current regulation circuit. When an H-bridge is enabled, current rises through the winding at a rate dependent on the DC voltage, inductance of the winding, and the magnitude of the back EMF present. After the current reaches the current control threshold, the bridge enters a decay mode for a fixed period of time to decrease the current, which is configurable between 10 to 30 µs through the tri-level input TOFF. After the time expires, the bridge is re-enabled, starting another PWM cycle.

Table 3 Fixed Off-Time Selection

TOFF	TOFF Duration
Z	10 µs
0	20 µs
1	30 µs

The PWM current control is set by a comparator which compares the voltage across a current sense resistor connected to the xSEN pin, with a reference voltage. The reference voltage can be supplied by an internal reference of 3.3 V (which requires VREG to be connected to VREF), or externally supplied to the VREF pin. The reference voltage is then scaled first by the 3-bit torque DAC, then by the output of a sine lookup table that is applied to a sine-weighted DAC (sine DAC). The voltage is attenuated by a factor of 6.6.

The full-scale (100%) control current is calculated as follows:

$$I_{FS} = \frac{VREF}{6.6 x R_{XSEN}} x TORQUE$$

where

- I_{FS} is the full scale regulated current
- VREF is the voltage on the VREF pin
- R_{XSEN} is the resistance of the sense resistor
- TORQUE is the scaling percentage from the torque DAC.

Example: Using VREF is 3.3 V, torque DAC = 100%, and a 500 mΩ sense resistor, the full-scale control current is 3.3 V / (6.6 × 500 mΩ) × 100% = 1 A.

The current for both motor windings is scaled depending on the T0 and T1 pins as in Table 4.

Table 4 Torque DAC Settings

T1	T0	CURRENT SCALING (TORQUE)
0	0	100.0%
0	Z	87.5%
0	1	75.0%
Z	0	62.5%
Z	Z	50.0%
Z	1	37.5%
1	0	25.0%
1	Z	12.5%
1	1	0% (outputs disabled)

DECAY MODE

After the control current threshold is reached, the drive current is interrupted, but due to the inductive nature of the motor, current must continue to flow for some period of time (called recirculation current). To handle this recirculation current, the H-bridge can operate in two different states, fast decay or slow decay (or a mixture of fast and slow decay).

In fast-decay mode, after the PWM control current level is reached, the H-bridge reverses state to allow winding current to flow through the opposing FETs. As the winding current approaches 0, the bridge is disabled to prevent any reverse current flow. For fast-decay mode, see number 2 in Figure 3.

In slow-decay mode, winding current is recirculated by enabling both of the low-side FETs in the bridge. For slow-decay mode, see number 3 in Figure 3.

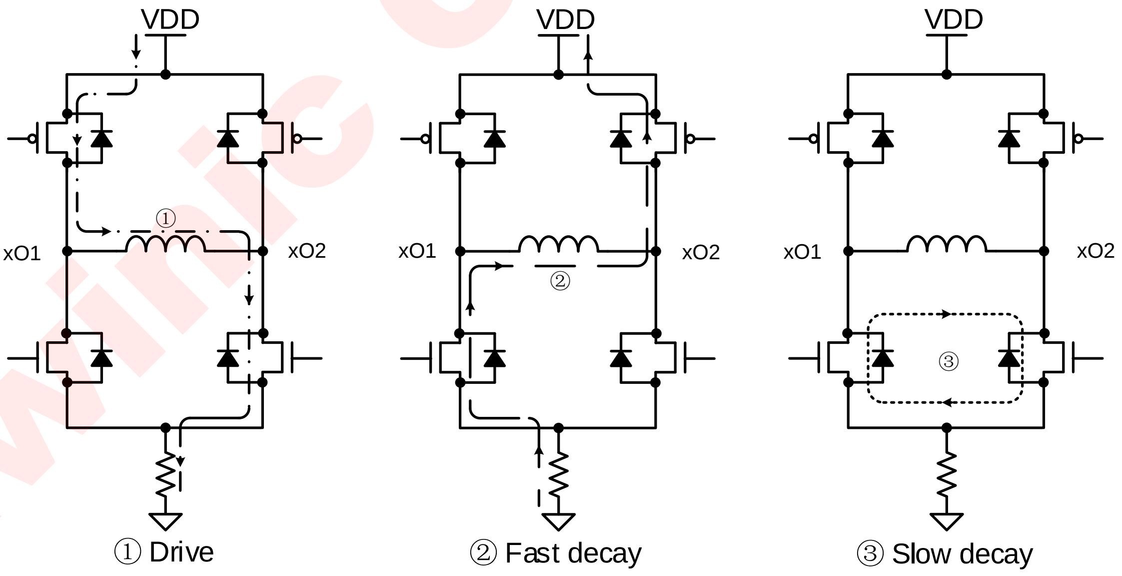


Figure 6 Decay Modes

The AW8646 supports fast, slow, mixed, and Adaptive Decay modes. With stepper motors, the decay mode is chosen for a given stepper motor and operating conditions to minimize mechanical noise and vibration.

In mixed decay mode, the current recirculation begins as fast decay, but at a fixed period of time (determined by the state of the D1 and D0 pins shown in Table 5) the current recirculation switches to slow decay mode for the remainder of the fixed PWM period. Note that the D1 and D0 pins are tri-level inputs; these pins can be driven logic low, logic high, or high-impedance (Z).

Table 5 Decay Pins Configuration

D1	D0	Decay Mode (Increasing Current)	Decay Mode (Decreasing Current)
0	0	Slow decay	Slow decay
0	Z	Slow decay	Mixed decay: 25% fast
0	1	Slow decay	Mixed decay: 1 t_{BLANK}
Z	0	Mixed decay: 1 t_{BLANK}	Mixed decay: 1 t_{BLANK}
Z	Z	Mixed decay: 50% fast	Mixed decay: 50% fast
Z	1	Mixed decay: 25% fast	Mixed decay: 25% fast
1	0	Slow decay	Mixed decay: 50% fast
1	Z	Slow decay	Mixed decay: 12.5% fast
1	1	Slow decay	Fast decay

Figure 4 shows increasing and decreasing current. When current is decreasing, the decay mode used is fast, slow, or mixed as commanded by the D1 and D0 pins. Three DEC pin selections allow for mixed decay during increasing current.

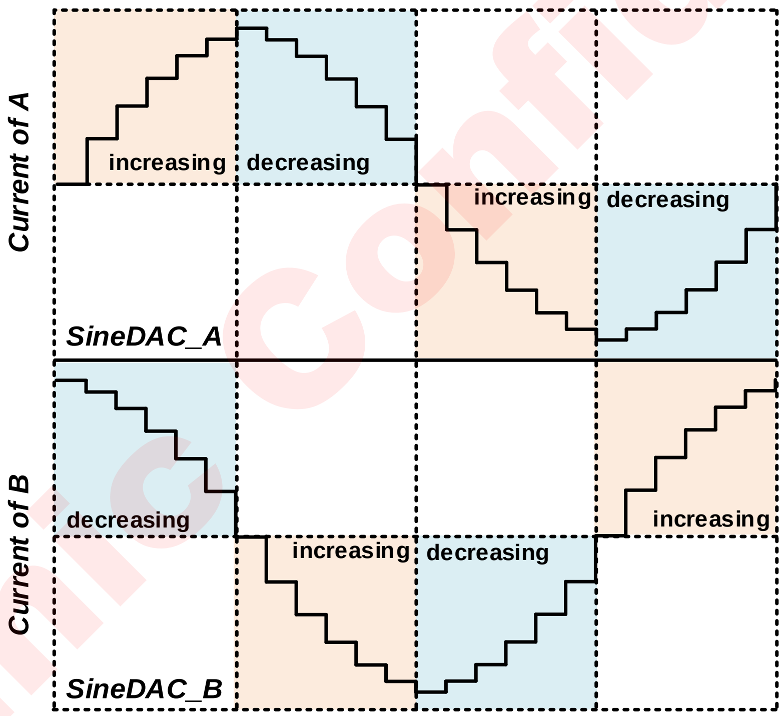


Figure 7 Increasing and Decreasing Current

Adaptive Decay Technology simplifies the decay mode selection by dynamically changing to adjust for current level, step change, supply variation, BEMF, and load. To enable Adaptive Decay mode, pull the ADECAY pin to logic high. The state of the ADECAY pin is only evaluated when exiting sleep mode. (ADECAY pin must be high before exiting sleep to enable Adaptive Decay mode.)

Figure 5 shows Adaptive Decay mode adjusts the time spent in fast decay to minimize current ripple and quickly adjust to current-step changes. If the drive time is longer than the minimum (t_{BLANK}), in order to reach the current trip point, the decay mode applied is slow decay. When the minimum drive time (t_{BLANK}) provides more current than the regulation point, fast decay of 1 t_{BLANK} is applied. If the second drive period also provides more current than the regulation point, fast decay of 2 t_{BLANK} is applied. If a third (or more) consecutive period provides more current than the regulation point, fast decay using 25% of t_{OFF} time is applied. When the minimum drive time is insufficient to reach the current regulation level, slow decay is applied until the current exceeds the current reference level.

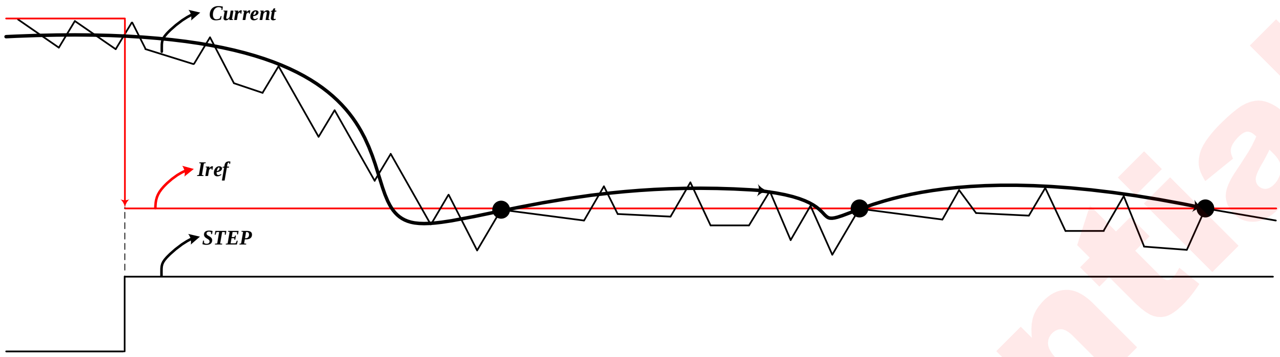


Figure 8 Adaptive Decay mode

OVERCURRENT PROTECTION (OCP)

An analog current limit circuit on each FET limits the current through the FET by limiting the gate drive. If this analog current limit persists for longer than the OCP deglitch time t_{OCP}, all FETs in the H-bridge are disabled and the nFAULT pin is driven low. The device remains disabled until the retry time, t_{RETRY}, occurs. The OCP is independent for each H-bridge.

Overcurrent conditions are detected independently on both high-side and low-side devices; that is, a short to ground, supply, or across the motor winding all result in an OCP event. Note that OCP does not use the current sense circuitry used for PWM current control, so OCP functions without the presence of the xSEN resistors.

THERMAL SHUTDOWN (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge are disabled and the nFAULT pin is driven low. After the die temperature falls to a safe level, operation automatically resumes. The nFAULT pin is released after operation has resumed.

UNDERVOLTAGE LOCKOUT (UVLO)

If at any time the voltage on the VDD pin falls below the UVLO falling threshold voltage, V_{UVLO}, all circuitry in the device is disabled, and all internal logic is reset. Operation resumes when VDD rises above the UVLO rising threshold. The nFAULT pin is driven low during an under voltage condition and is released after operation has resumed.

Table 6 Fault Behavior

Fault	Error Report	H-Bridge	Internal Circuits	Recovery
VDD UVLO	nFAULT unlatched	Disabled	Shut down	System and fault clears on recovery
OCP	nFAULT unlatched	Disabled	Operating	System and fault clears on recovery and motor is driven after time, T_{RETRY}
TSD	nFAULT unlatched	Disabled	Operating	System and fault clears on recovery

DEVICE FUNCTIONAL MODES

The AW8646 device is active unless the nSLEEP pin is driven low. In sleep mode, the VREG regulator is disabled and the H-bridge FETs are disabled (Hi-Z). The time T_{SLEEP} must elapse after a falling edge on the nSLEEP pin before the device enters sleep mode. The AW8646 is brought out of sleep mode by bringing the nSLEEP pin high. The time T_{WAKE} must elapse, after nSLEEP is brought high, before the outputs change state.

If the nEN pin is brought high, the H-bridge outputs are disabled, but the internal logic is still active. An appropriate edge on STEP (depending on the step mode) advances the sequencer, but the outputs do not change state until nEN is driven low.

Table 7 Operating Modes

Mode	Condition	H-Bridge	VREG	Sequencer
Operating	3V<VDD<12V nSLEEP pin=1 nEN=0	Operating	Operating	Operating
Disabled	3V<VDD<12V nSLEEP pin=1 nEN=1	Disabled	Operating	Operating
Sleep	3V<VDD<12V nSLEEP pin=0	Disabled	Disabled	Disabled
Fault	Any fault condition met	Disabled	Depends on fault	Depends on fault

APPLICATION INFORMATION

TYPICAL APPLICATION

DESIGN REQUIREMENTS

Table 8 System Design Input Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Nominal supply voltage	VDD	12 V
Supply voltage range		3 to 12V
Motor winding resistance	R_L	3.0Ω/phase
Motor winding inductance	L_L	330 μH/phase
Motor full step angle	θ_{step}	1.8°/step
Target stepping level	nm	1/8 step
Target motor speed	v	400 rpm
Target control current	ICTRL	500 mA
Control current reference voltage	VREF	3.3 V
Current scaling	TORQUE	100%

STEPPER MOTOR SPEED

The first step in configuring the AW8646 requires the desired motor speed and stepping level. The AW8646 can support from full step to 1/32 step mode. If the target motor speed is too high, the motor will not spin. Make sure that the motor can support the target speed.

For a desired motor speed (v), microstepping level (nm), and motor full step angle (θ_{step}),

$$f_{step} = (steps/s) = \frac{v(rpm) \times n_m(steps) \times 6}{\theta_{step}(°/step)}$$

θ_{step} can be found in the stepper motor data sheet or often written on the motor itself. For AW8646, the microstepping levels are set by the MODE0/MODE1 pins and can be any of the settings in Table 2.

Higher microstepping means a smoother motor motion and less audible noise requires a higher f_{step} to achieve the same motor speed.

CURRENT REGULATION

The control current (I_{CTRL}) is the maximum current driven through either winding. This quantity will depend on the sense resistor value (R_{XSEN}).

$$I_{CHOP} = \frac{VREF}{6.6 \times R_{XSEN}} \times TORQUE$$

I_{CTRL} is set by a comparator which compares the voltage across R_{XSEN} to a reference voltage. Note that I_{CTRL} must follow the Equation to avoid saturating the motor.

$$I_{CHOP}(A) < \frac{VDD(V)}{R_L(\Omega) + 2 \times R_{DS(ON)}(\Omega) + R_{XSEN}(\Omega)}$$

where R_L is the motor winding resistance.

DECAY MODES

The AW8646 supports four different decay modes: slow decay, fast decay, mixed decay, and Adaptive Decay. The first selection to try is the Adaptive Decay mode, which adjusts the decay mode automatically to improve current regulation. The current through the motor windings is regulated using a fixed-off-time PWM scheme. This means that after any drive phase, when a motor has reached the current control threshold (I_{CHOP}), the AW8646 places the motor in one of the four decay modes until the PWM cycle has expired. Afterward, a new drive phase starts.

The blanking time, t_{BLANK}, defines the minimum drive time for the current control. I_{CTRL} is ignored during t_{BLANK}, so the winding current may overshoot the trip level during this blanking period.

APPLICATION CURVES

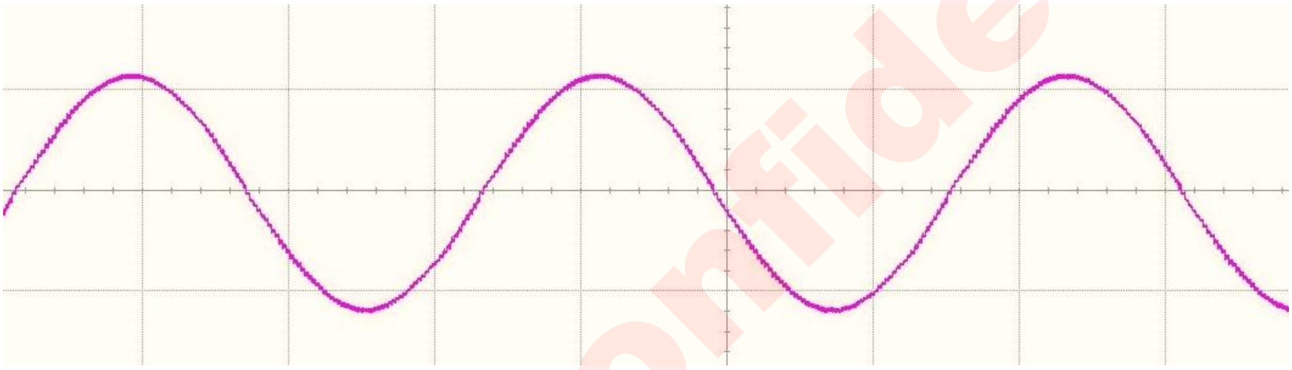


Figure 9 Microstepping Waveform, Phase A, Adaptive Decay

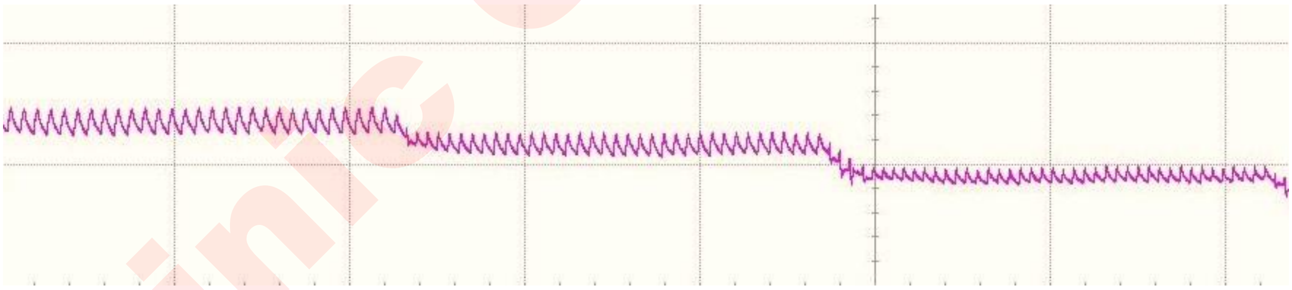


Figure 10 Microstepping Waveform, Adaptive Decay, Step Current Regulation

POWER SUPPLY RECOMMENDATIONS

The AW8646 is designed to operate from an input voltage supply (VDD) range between 3 to 12V. A 0.1µF ceramic capacitor rated for VDD must be placed as close to the AW8646 as possible. In addition, a bulk 10µF capacitor must be included on VDD.

PCB LAYOUT CONSIDERATION

EXTERNAL COMPONENTS PLACEMENT

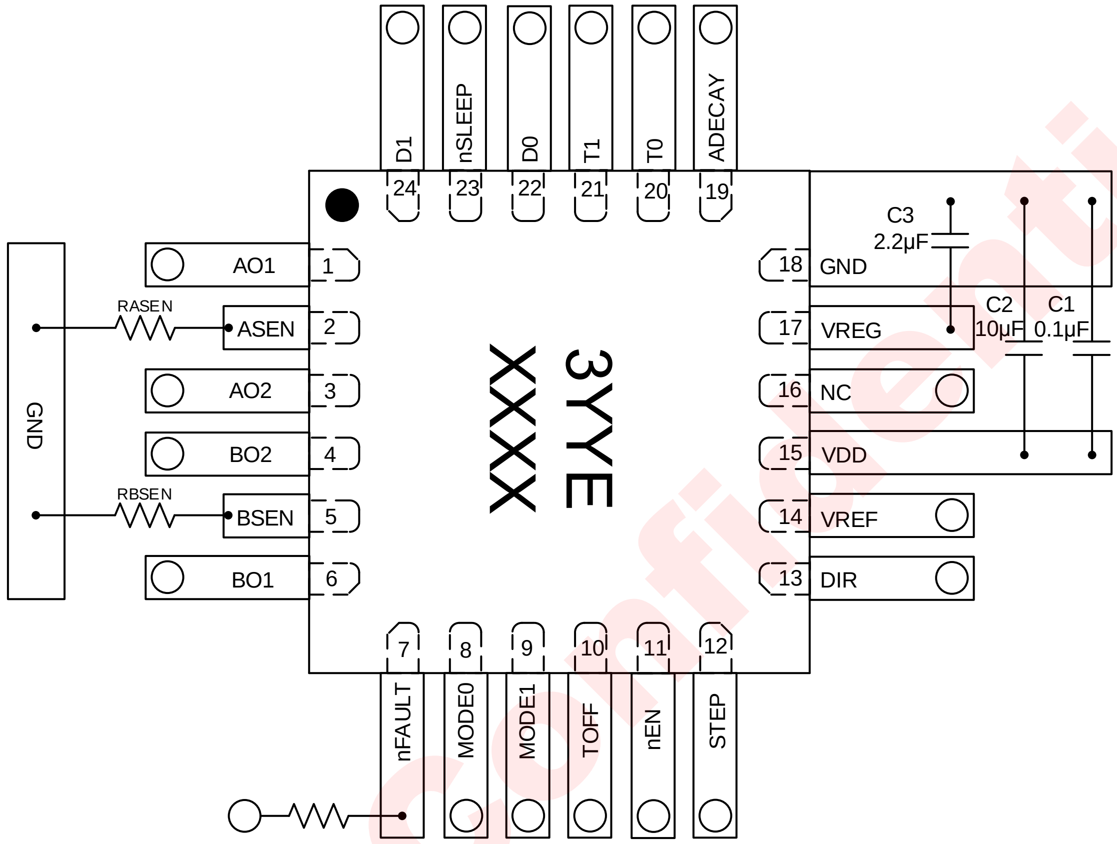


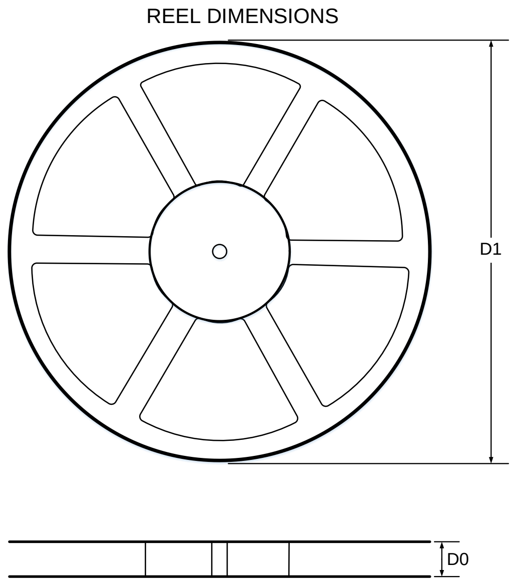
Figure 11 AW8646 External Components Placement

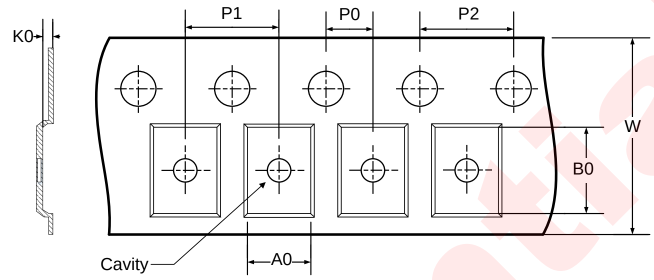
LAYOUT CONSIDERATIONS

This device is a high voltage driver chip. To obtain the optimal performance, PCB layout should be considered carefully. The suggested Layout is illustrated in the following diagram:

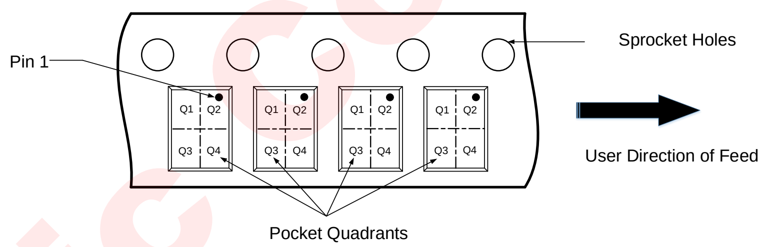
1. All of the external components close to IC in top layer PCB;
2. Create solid GND plane near and around the IC;
3. No via in traces from IC pin VREG through C3 to IC pin GND, keep the trace as short as possible;
4. No via in traces from IC pin VDD through C2/C1 to IC pin GND, keep the trace as short as possible;
5. Try to provide a separate short and thick power line to the device, the copper width is recommended to be larger than 0.75mm. The decoupling capacitors should be placed as close as possible to boost power supply pin;
6. The output line from the device to load should be as short and thick as possible. The width is recommended to be larger than 0.5mm;

TAPE AND REEL INFORMATION





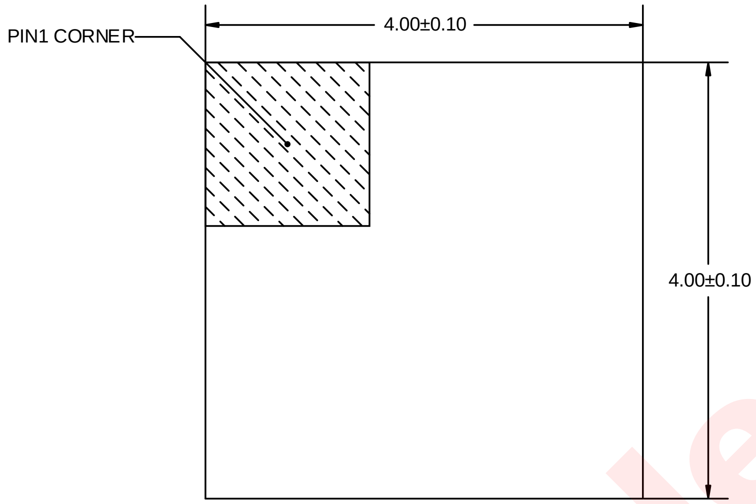
A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width



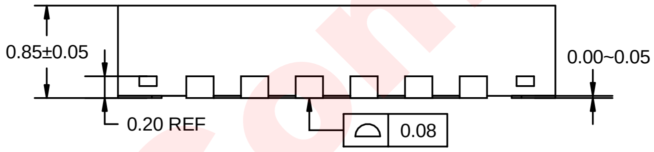
All Dimensions are nominal

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330	12.4	4.3	4.3	1.1	2.0	8.0	4.0	12.0	Q2

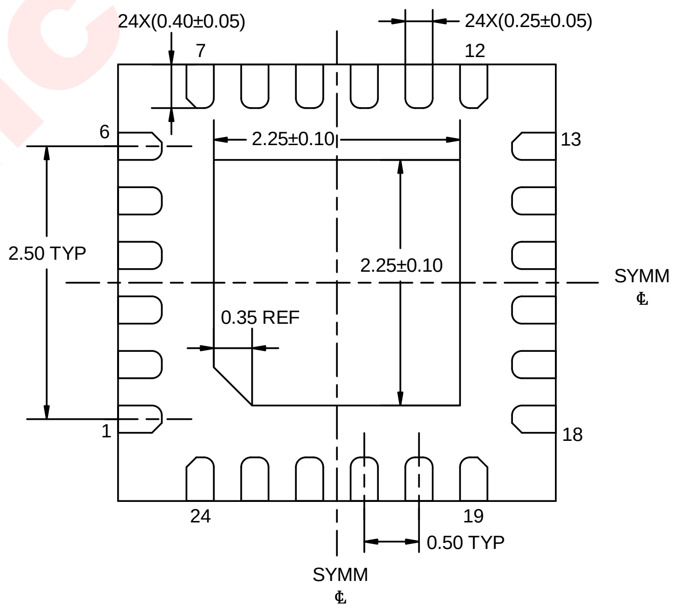
PACKAGE DESCRIPTION



Top View



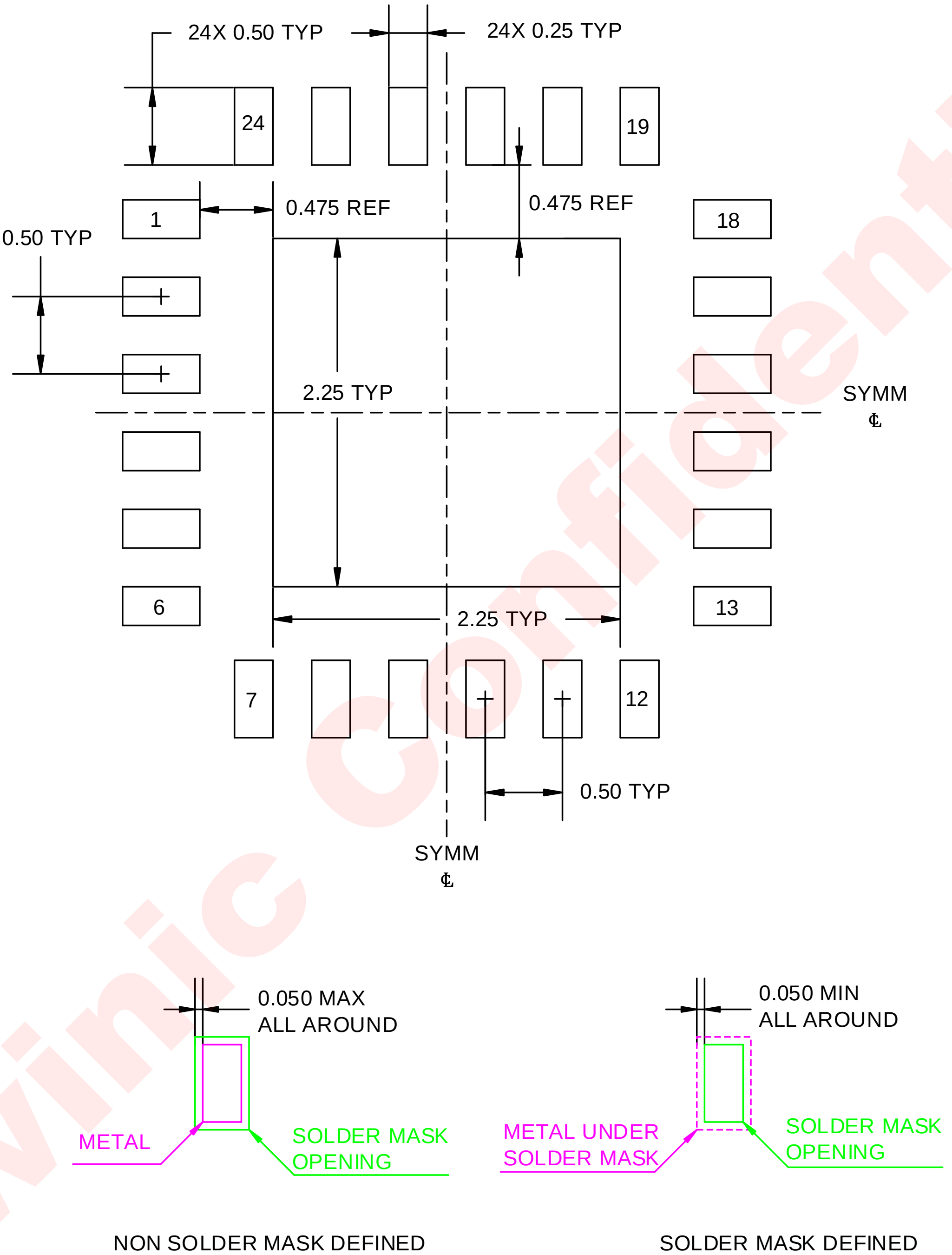
Side View



Bottom View

Unit: mm

LAND PATTERN DATA



Unit: mm

REVISION HISTORY

Version	Date	Change Record
V1.0	Dec 2018	Officially released
V1.1	Jan 2019	Change the description for max drive current and Overcurrent protection trip level
V1.2	Feb 2019	Change PCB layout considerations

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