High Efficiency, Low Noise, Ultra-Low Distortion, Constant Large Volume, Upgrade 7th-Generation Class K Audio Amplifier with Ultra-Low Distortion Audio Analog Switch

FEATURES

- **Speaker and Receiver two-in-one application**
  - **Analog Switch Direct Mode: Vn<1uV, THD+N=0.001%**
  - **Class AB Receiver Mode: 1V/V, Vn=11μV, THD+N=0.15%**
  - **Class K Speaker Mode: 8V/V, Vn=53μV, THD+N=0.008%**
- **Power Amplifier's Overall Efficiency: 80%**
- **High PSRR: -100dB@217Hz**
- **Selectable Speaker-Guard Power Level: 0.6W, 0.8W, 1.0W, 1.2W**
- **Within Lithium Battery Voltage Range, Outputs Constant Large Volume**
- Upgrade for AW87317, AW87327
- No-Crack-Noise (NCN) Technology
- Super TDD-Noise Suppression
- Excellent Pop-Click Suppression
- One-Wire Pulse Control
- ESD Protection: ±6kV (HBM)
- Small 1.575mm×1.575mm, 0.4mm Pitch CSP-16 Package

APPLICATIONS

- **Smart Phones**

DESCRIPTION

AW87337 is specifically designed to enhance overall sound quality. It is an upgrading 7th-generation class K audio amplifier with high efficiency, low noise, ultra-low distortion and capability of outputting constant large volume.

With integrated AWINIC proprietary NCN output AGC audio algorithm, AW87337 can eliminate noise in playback and improve sound quality and effect. Using a novel K-Chargepump technology, its integrated charge pump efficiency can reach 93%, and power amplifier's overall efficiency can reach 80%. With high efficiency, AW87337 can greatly prolong smart phone usage time.

AW87337 noise floor is as low as 53μV, with 97dB high signal-to-noise-ratio (SNR). The ultra-low distortion 0.008% brings high-quality musical enjoyment.

AW87337 has a setting of 4-step selectable speaker-guard output power level from 0.6W to 1.2W, suitable for different rated power speakers. Within lithium battery voltage range, it keeps output power constant, preventing voice from degrading.

AW87337 supports speaker and receiver two-in-one application. The Class AB Receiver Mode has an ultra-low output noise of 11μV and an ultra-high power supply noise suppression of -100dB@217Hz. The Direct Mode using audio analog switch can realize ultra-low THD of 0.001% and ultra-high suppression of power supply of -100dB@217Hz.

AW87337 has built-in over-current protection, over-temperature protection and short-circuit protection. AW87337 is available in a 1.575mm×1.575mm, 0.4mm pitch CSP-16 package.

APPLICATION DIAGRAM

Speaker Mode (MD7)			
Cin (nF)	Rin (kΩ)	Av (V/V)	Fin (Hz)
47	3	16.3	173
33	10	12	181

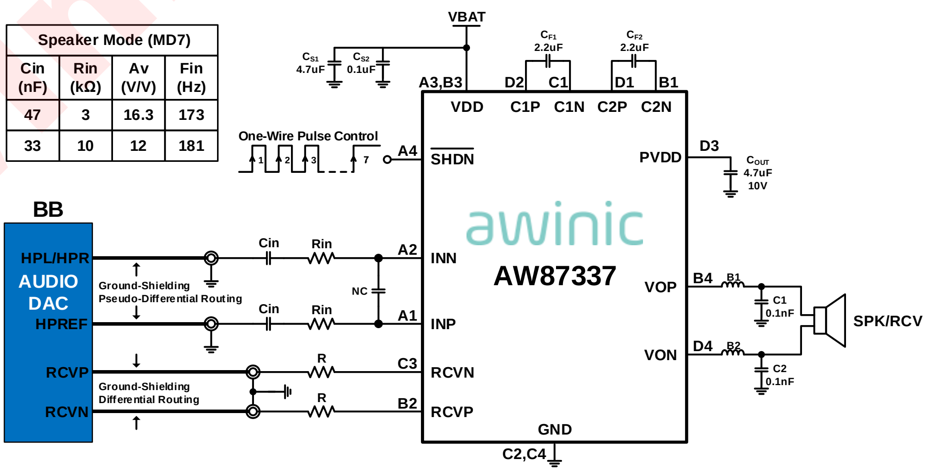

Figure 1 AW87337 Application Diagram

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PIN DIAGRAM AND DEVICE MARKING

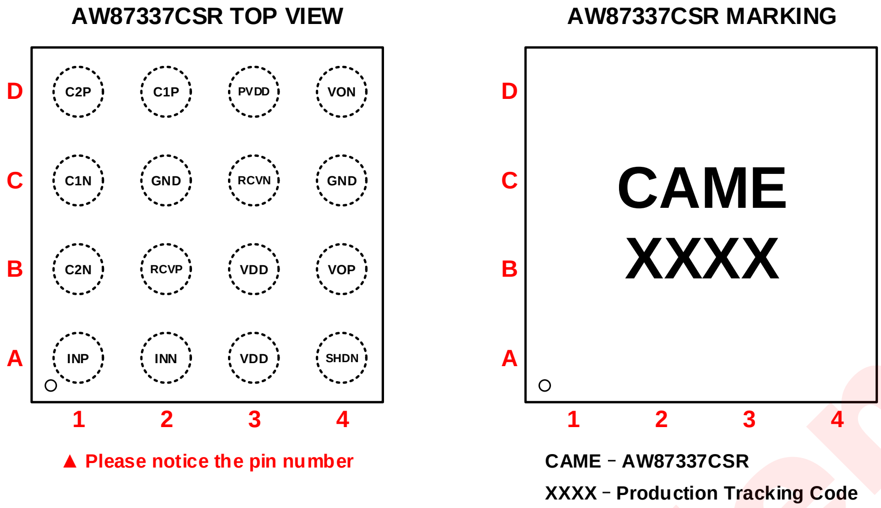


Figure 2 AW87337 Pin Diagram Top View and Device Marking

PIN DESCRIPTION

Number	Symbol	Description
A1	INP	Positive audio input
A2	INN	Negative audio input
A3, B3	VDD	Power supply
A4	SHDN	Chip power down pin, active low: one wire pulse control
B1	C2N	Negative terminal of the charge pump flying capacitor C_{F2}
B2	RCVP	Analog switch positive input
B4	VOP	Positive audio output
C1	C1N	Negative terminal of the charge pump flying capacitor C_{F1}
C2, C4	GND	Ground
C3	RCVN	Analog switch negative input
D1	C2P	Positive terminal of the charge pump flying capacitor C_{F2}
D2	C1P	Positive terminal of the charge pump flying capacitor C_{F1}
D3	PVDD	Charge pump output
D4	VON	Negative audio output

AWINIC CLASS K FAMILY

ITEM	TEST CONDITION	AW87327	AW87337	AW87347
PVDD (V)	VDD=4.2V	6.05	6.05	6.05
Ouput Noise (μV)	VDD=4.2V, f=20Hz to 20kHz Input ac grounded, 8V/V, A-weighting	53	53	53
Efficiency (%)	VDD=3.6V, Po=1.0W, R_L=8Ω+33μH	80	80	80

FUNCTIONAL DIAGRAM

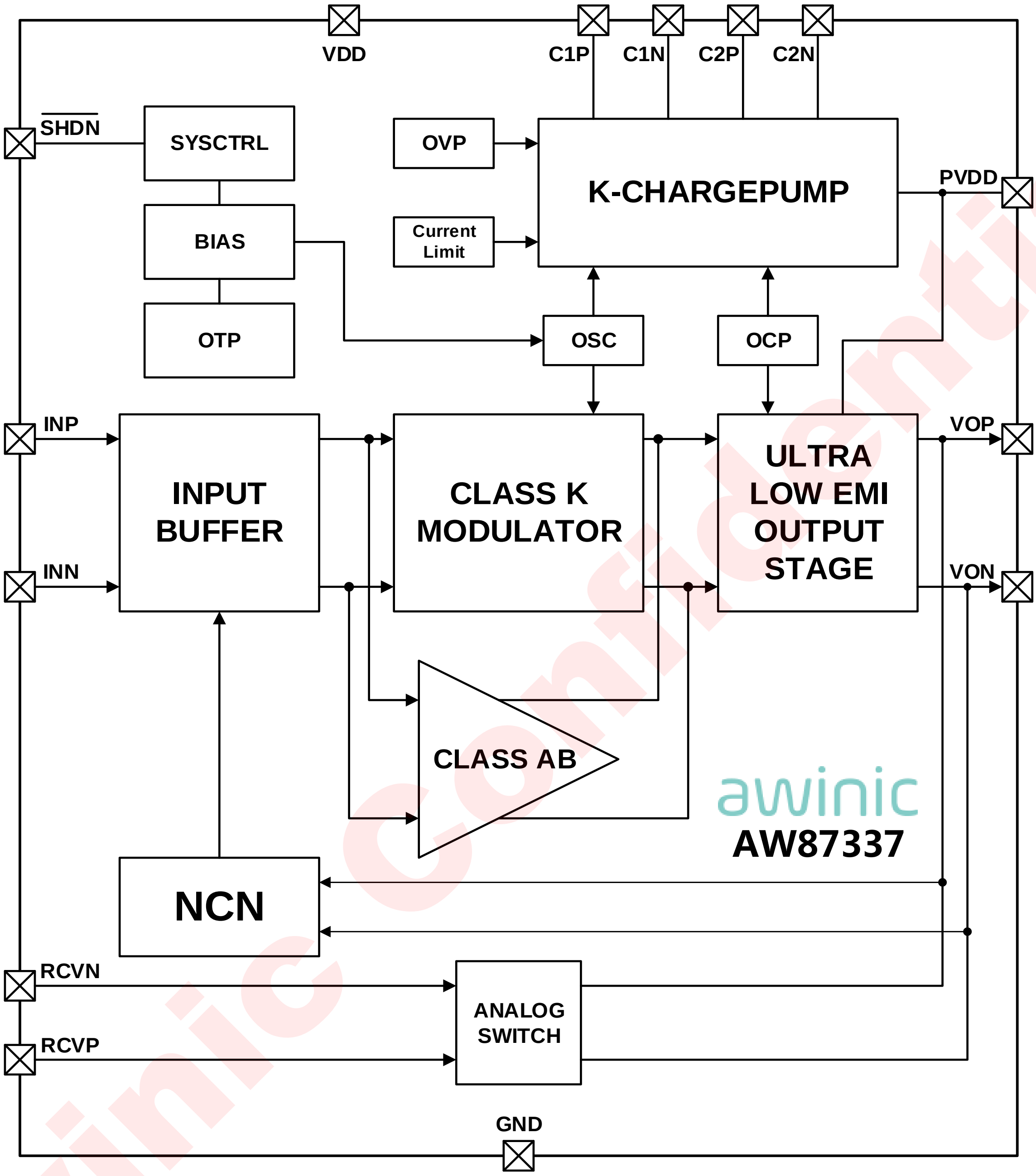


Figure 3 AW87337 Functional Diagram

APPLICATION DIAGRAM

Speaker Mode (MD7)			
Cin (nF)	Rin (kΩ)	Av (V/V)	Fin (Hz)
47	3	16.3	173
33	10	12	181

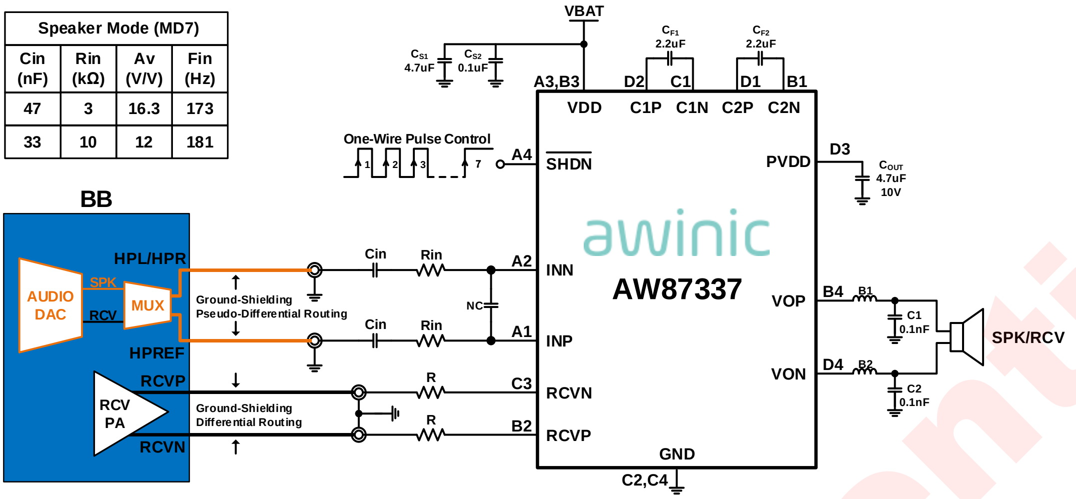


Figure 4 AW87337 Speaker Mode and FM Mode Application Diagram(Note 1)

***Note1*：** *When single-ended input, audio signal line from audio DAC (HPL or HPR) can arbitrarily connected to either of INN or INP input terminal. The other terminal must be connected to reference ground (HPREF) through input capacitor and resistor.*

Receiver Mode (MD5)			
Cin (nF)	Rin (kΩ)	Av (V/V)	Fin (Hz)
47	3	1	71
33	10	0.87	88

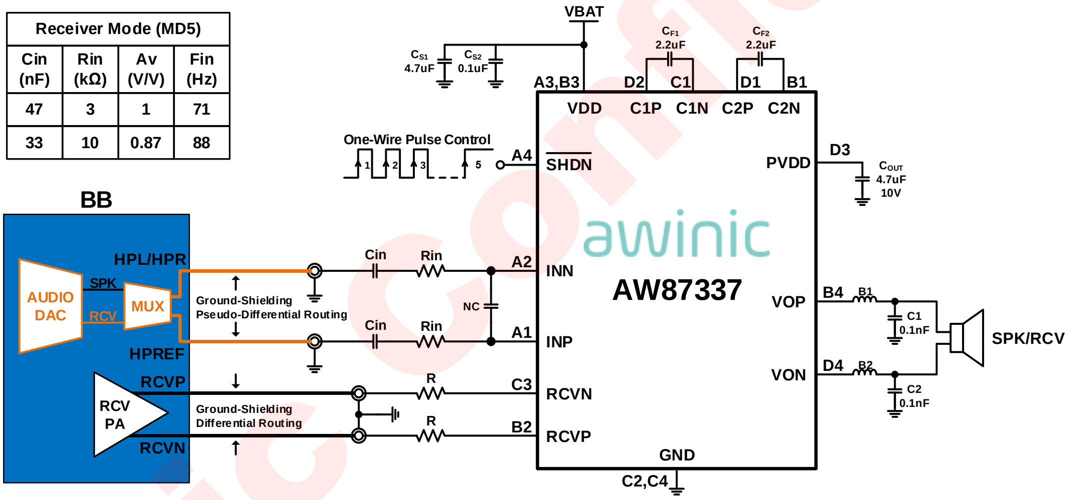


Figure 5 AW87337 Receiver Mode Application Diagram

Direct Mode (MD8)			
Cin (nF)	R (Ω)	Av (V/V)	Fin (Hz)
--	12	0.25	--

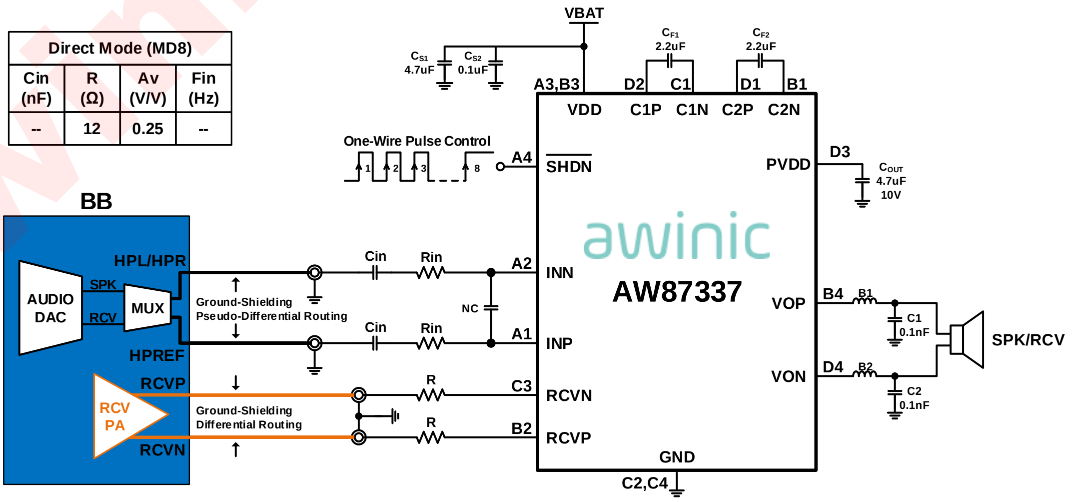
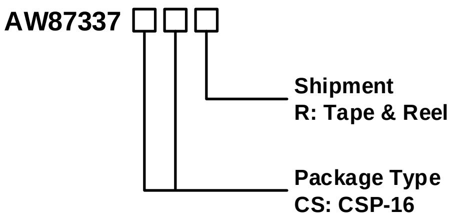


Figure 6 AW87337 Direct Mode Application Diagram

ORDERING INFORMATION

Product Type	Operation Temperature Range	Package	Device Marking	Moisture Sensitivity Level (MSL)	Environmental Information	Delivery Form
AW87337CSR	-40°C to 85°C	CSP-16	CAME	MSL1	ROHS+HF	Tape & Reel 3000 pcs



ABSOLUTE MAXIMUM RATINGS(NOTE2)

Parameter	Range
Power Supply VDD Voltage	-0.3V to 6V
Charge Pump Output PVDD Voltage	-0.3V to 7V
VOP, VON, C1P, C2P	-0.3V to PVDD+0.3V
C1N, C2N	-0.3V to VDD+0.3V
Input Pin INP, INN Voltage	-0.3V to VDD+0.3V
Input Pin RCVP, RCVN Voltage	-0.3V to 3V
Junction-to-Ambient Thermal Resistance θ_{JA}	84.9°C/W
Operating Free-Air Temperature T_A	-40°C to 85°C
Maximum Junction Temperature T_{JMAX}	165°C
Storage Temperature T_{STG}	-40°C to 150°C
Lead Temperature (Soldering 10 Seconds)	260°C
ESD Rating	
Human Body Model (HBM) (Note 3)	±6kV
Charged Device Model (CDM) (Note 4)	±2kV
Latch-up	
Test Condition: JEDEC STANDARD NO.78D SEPTEMBER 2010	+IT: 450mA -IT: -450mA

Note 2: *Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.*

Note 3: *The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: MIL-STD-883J Method 3015.9.*

Note 4: *Test Method: ESDA/JEDEC JS-002-2014.*

MODE DESCRIPTIONS (T_A=25°C, VDD=4.2V)

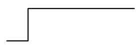
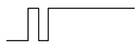
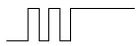
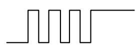
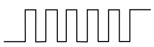
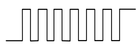
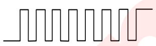
Under Speaker Mode (Mode 1 to Mode 4, and Mode 7) or Receiver Mode (Class AB Receiver Mode, Mode 5 and Mode 6), audio signal is inserted through INP & INN pins. The AW87337 external input capacitor is Cin and the external input resistor is Rin.

1) Under Speaker Mode, the internal input resister is 16.6kΩ. The gain of AW87337 (Av) can be calculated by 319.5k/(Rin+16.6k) (Rin unit: Ω). Recommended operating external setting is: Cin=47nF, Rin=3kΩ, Av=16.3V/V or Rin=10kΩ, Av=12V/V.

2) Under Class AB Receiver Mode, the internal input resistor is 45kΩ under both Mode 5 and Mode 6. The gain of AW87337 (Av) can be calculated by 48k/(Rin+45k) (Rin unit: Ω) under Mode 5 and 144k/(Rin+45k) (Rin unit: Ω) under Mode 6, respectively. Recommended operating external setting is: Cin=47nF, Rin=3kΩ, Av=1V/V (Mode 5) and Av=3V/V (Mode 6).

Under Direct Mode (Mode 8), the external input resistor is R. If the resistor of load is RL, the signal gain under this mode can be calculated by RL/(2R+RL). Recommended operating external setting is: R=12Ω, Av=0.25V/V@RL=8Ω.

The operating modes of AW87337 are listed below:

MODE	Enable Signal (SHDN)	Gain (V/V)	NCN Power Level (W)		NCN Function	Class AB Receiver Mode	Analog Switch Direct Mode	FM Mode
		Rin=3kΩ	R_L=8Ω +33μH	R_L=6Ω +33μH				
1		16.3	1.2	1.6	√			
2		16.3	1.0	1.3	√			
3		16.3	0.8	1.0	√			
4		16.3	0.6	0.8	√			
5		1				√		
6		3				√		
7		16.3	1.75W@ THD=1%	2.05W@ THD=1%				
8		1					√	

ELECTRICAL CHARACTERISTICS

Test condition: T_A=25°C, VDD=3.6V, R_L=8Ω+33μH, f=1kHz (unless otherwise noted)

Parameter		Test Conditions	Min	Typ	Max	Unit
V_{DD}	Power supply voltage		3.0		5.5	V
V_{IH}	$\overline{SHDN}$ high input voltage		1.3		V_{DD}	V
V_{IL}	$\overline{SHDN}$ low input voltage		0		0.45	V
$\lvert V_{OS}\rvert$	Output offset voltage	V_{IN}=0V, V_{DD}=3.0V to 5.5V	-30	0	30	mV
I_{SD}	Shutdown current	V_{DD}=3.6V, $\overline{SHDN}$=0V			2	μA
T_{TG}	Thermal AGC start temperature threshold			150		°C
T_{TGR}	Thermal AGC exit temperature threshold			130		°C
T_{SD}	Over temperature protection threshold			160		°C
T_{SDR}	Over temperature protection recovery threshold			120		°C
T_{ON}	Start-up time			40		ms
K-Chargepump						
PVDD	Output voltage	V_{DD}=3.0V to 4V		1.5×VDD		V
		V_{DD}>4V		6.05		V
Vhys	OVP hysteresis voltage	V_{DD}>4V		50		mV
F_{CP}	Charge pump frequency	V_{DD}=3.0V to 5.5V	0.79	1.06	1.33	MHz
η_{CP}	Charge pump efficiency	V_{DD}=3.6V, I_{load}=200mA		93		%
T_{ST}	Soft-start time	No load, C_{OUT}=4.7μF	1.0	1.2	1.4	ms
I_L	Current limit when PVDD short to ground		200	300	400	mA
Class K power amplifier (Mode1 to Mode4, and Mode7)						
I_q	Quiescent current	V_{DD}=4.2V, Vin=0, no load		10	15	mA
η	Efficiency	V_{DD}=3.6V, Po=1.0W, R_L=8Ω+33μH		80		%
Fosc	Modulation frequency	V_{DD}=3.0V to 5.5V	600	800	1000	kHz
Av	Gain	External input resistance=3kΩ		16.3		V/V
Vin	Recommended max input voltage	V_{DD}=3.0V to 5.5V			1	Vp
Rini	Internal input resistor	Mode1 to Mode4, and Mode7		16.6		kΩ
Fhin	Input high pass filter corner frequency	Cin=47nF, external input resistor=3kΩ		173		Hz
Pagc	Mode1 NCN output AGC power	V_{DD}=4.2V, R_L=8Ω+33μH	1.08	1.2	1.32	W
		V_{DD}=4.2V, R_L=6Ω+33μH	1.44	1.6	1.76	W
	Mode2 NCN output AGC power	V_{DD}=4.2V, R_L=8Ω+33μH	0.9	1	1.1	W
		V_{DD}=4.2V, R_L=6Ω+33μH	1.17	1.3	1.43	W
	Mode3 NCN output AGC power	V_{DD}=4.2V, R_L=8Ω+33μH	0.72	0.8	0.88	W
		V_{DD}=4.2V, R_L=6Ω+33μH	0.9	1	1.1	W
	Mode4 NCN output AGC power	V_{DD}=4.2V, R_L=8Ω+33μH	0.54	0.6	0.66	W
		V_{DD}=4.2V, R_L=6Ω+33μH	0.72	0.8	0.88	W

Parameter		Test Conditions		Min	Typ	Max	Unit
PSRR	Power supply rejection ratio	V_{DD}=4.2V, Vp-p_sin=200mV	217Hz		-68		dB
			1kHz		-68		dB
SNR	Signal-to-noise ratio	V_{DD}=4.2V, Po=1.75W, THD+N=1%, R_L=8Ω+33μH Av=8V/V			97		dB
Vn	Output noise voltage	V_{DD}=4.2V, f=20Hz to 20kHz, input ac grounded, A-weighting	Av=8V/V		53		μVrms
			Av=12V/V		58		μVrms
			Av=16V/V		68		μVrms
THD+N	Total harmonic distortion+noise	V_{DD}=3.6V, Po=1W, R_L=8Ω+33μH, f=1kHz, Mode1			0.008		%
		V_{DD}=3.6V, Po=1W, R_L=6Ω+33μH, f=1kHz, Mode10			0.008		%
P_O	Mode7 output power	THD+N=10%, f=1kHz, R_L=8Ω+33μH, V_{DD}=4.2V			2.15		W
		THD+N=1%, f=1kHz, R_L=8Ω+33μH, V_{DD}=4.2V			1.75		W
		THD+N=10%, f=1kHz, R_L=8Ω+33μH, V_{DD}=3.6V			1.6		W
		THD+N=1%, f=1kHz, R_L=8Ω+33μH, V_{DD}=3.6V			1.28		W
		THD+N=10%, f=1kHz, R_L=6Ω+33μH, V_{DD}=4.2V			2.52		W
		THD+N=1%, f=1kHz, R_L=6Ω+33μH, V_{DD}=4.2V			2.05		W
		THD+N=10%, f=1kHz, R_L=6Ω+33μH, V_{DD}=3.6V			1.82		W
		THD+N=1%, f=1kHz, R_L=6Ω+33μH, V_{DD}=3.6V			1.5		W
Class AB Receiver (Mode5 and Mode6)							
I_q	Quiescent current	V_{DD}=4.2V, V_{IN}=0, no load			7		mA
η	Efficiency	V_{DD}=3.6V, Po=0.4W, R_L=8Ω+33μH, Mode6			69		%
Av	Gain	External input resistor=3kΩ, Mode5			1		V/V
		External input resistor=3kΩ, Mode6			3		V/V
Rini	Internal input resistor	Mode5 & Mode6			45		kΩ
Po	Mode 5, single-ended input	THD+N=1%, f=1kHz, R_L=8Ω+33μH, V_{DD}=3.6V			250		mW
	Mode 5, differential input	THD+N=1%, f=1kHz, R_L=8Ω+33μH, V_{DD}=3.6V			450		mW
	Mode 6	THD+N=1%, f=1kHz, R_L=8Ω+33μH, V_{DD}=3.6V			450		mW
Fhin	Input high pass filter corner frequency	Cin=47nF, external input resistor=3kΩ, Mode5			71		Hz
		Cin=47nF, external input resistor=3kΩ, Mode6			71		Hz
PSRR	Power supply rejection ratio	V_{DD}=4.2V, Vp-p_sin=800mV, Mode5	217Hz		-100		dB
			1kHz		-100		dB
Vn	Output noise voltage	VDD=4.2V, f=20Hz to 20kHz,	Av=1V/V		11		μVrms
		input ac grounded, A-weighting	Av=3V/V		26		μVrms
THD+N	Total harmonic distortion+noise	V_{DD}=4.2V, R_L=8Ω+33μH, f=1kHz	Po=0.1W, Mode5		0.15		%
			Po=0.3W, Mode6		0.15		%
Analog Switch Direct Mode (Mode8)							
RCVX	RCVP/RCVN Input Voltage			-0.3		3	V
I_q	Quiescent current	V_{DD}=4.2V, V_{IN}=0, no load			0.6		mA
R_{ON}	Switch On Resistance	I_{ON} =100mA, V_{RCVP}, V_{RCVN}=-0.3V to 3V			1		Ω
R_{FLAT}	On Resistance Flatness	I_{ON} =100mA, V_{RCVP}, V_{RCVN}=-0.3V to 3V			10		mΩ
PSRR	Power supply rejection ratio	V_{DD}=4.2V, Vp-p_sin=200mV	217Hz		-100		dB
			1kHz		-116		dB
THD+N	Total harmonic distortion+noise	V_{DD}=4.2V, R_L=32Ω, f=1kHz, V_{IN}=1Vrms			0.001		%

Parameter		Test Conditions	Min	Typ	Max	Unit
THD+N	Total harmonic distortion+noise	V_{DD}=4.2V, No Load, f=1kHz, V_{IN}=1Vrms		0.0005		%
One Wire Pulse Control						
T_H	$\overline{SHDN}$ high level duration time	V_{DD}=3.0V to 5.5V	0.75	2	10	μs
T_L	$\overline{SHDN}$ low level duration time	V_{DD}=3.0V to 5.5V	0.75	2	10	μs
T_{LATCH}	$\overline{SHDN}$ turn on delay time	V_{DD}=3.0V to 5.5V	150		500	μs
T_{OFF}	$\overline{SHDN}$ turn off delay time	V_{DD}=3.0V to 5.5V	150		500	μs
NCN (Note 5)						
T_{AT}	Attack time	-13.5dB gain attenuation completed		40		ms
T_{RL}	Release time	13.5dB gain release completed		1.2		s
A_{MAX}	Maximum attenuation			-13.5		dB

***Note 5**：Attack Time refers to the duration of gain attenuation by 13.5dB. Similarly, Release Time refers to the duration of gain recovery by 13.5dB.*

MEASUREMENT SETUP

AW87337 features switching digital output, as shown in Figure 7. It is crucial to connect a low pass filter after VOP/VON outputs, respectively, to filter out switch modulation frequency, then measure the differential output of filter to obtain audio analog output signal.

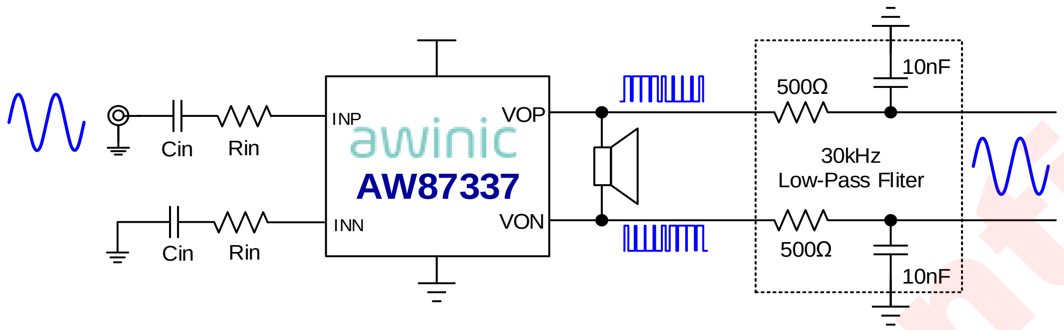


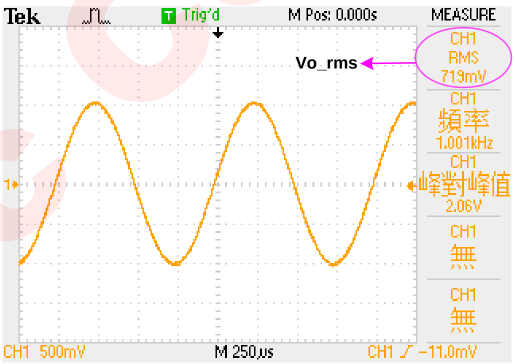
Figure 7 AW87337 Test Setup

The values of resistor and capacitor used by low pass filter are listed below:

R_{filter}	C_{filter}	Low-pass cutoff frequency
500Ω	10nF	32kHz
1kΩ	4.7nF	34kHz

Output Power Calculation

According to the above test method, the differential audio analog output signal is obtained at the output of the low pass filter. The valid value Vo_rms of the differential signal is as shown below:



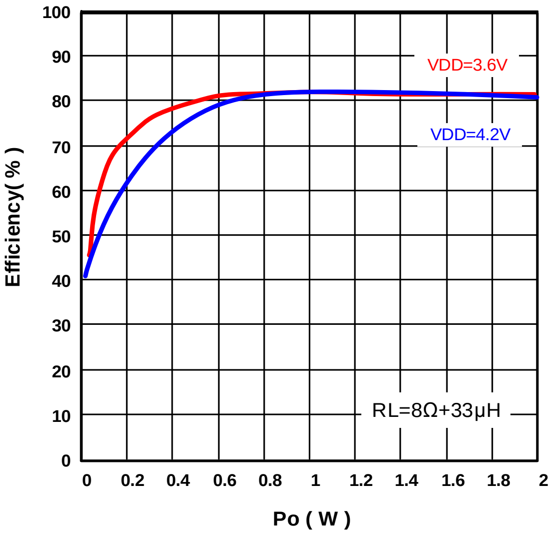
The power calculation of Speaker is as follows：

$$P_L = \frac{V_{O\_RMS}^2}{R_L}$$

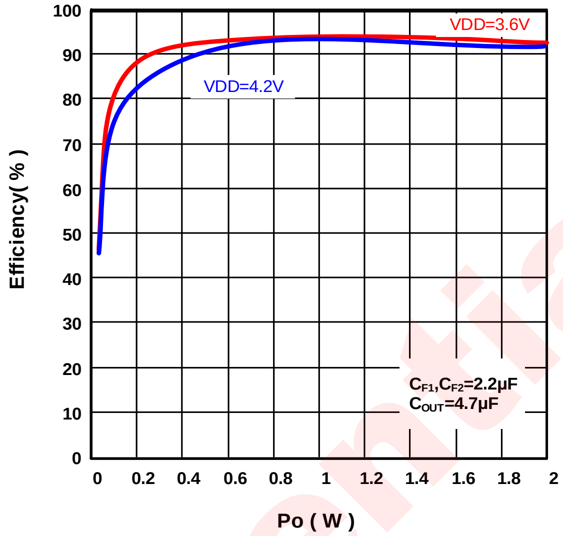
(R_L: Load Impedance of the speaker or receiver)

TYPICAL CHARACTERISTICS

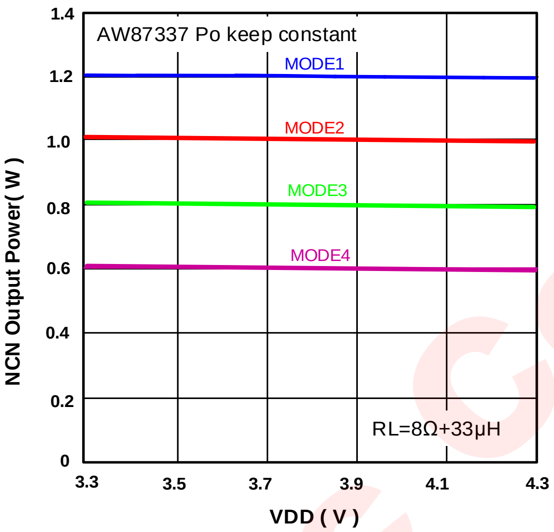
Efficiency vs Po



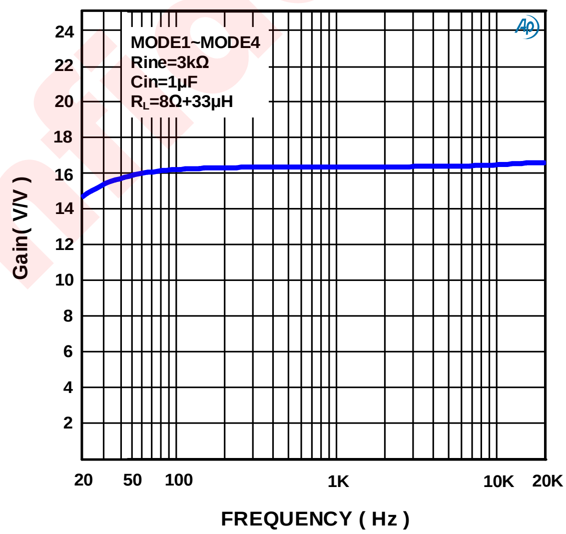
K-chargepump Efficiency



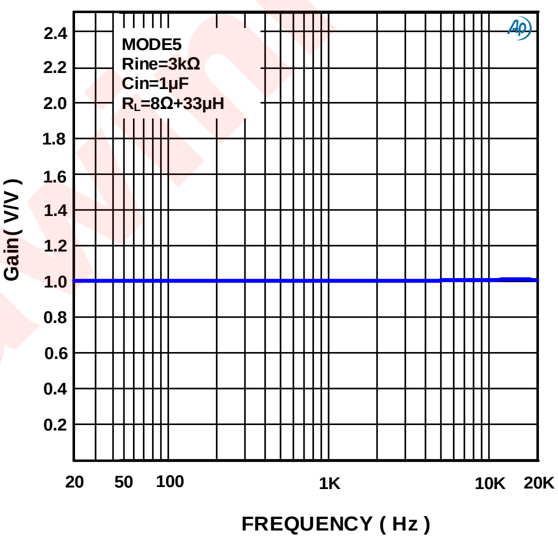
OUTPUT POWER vs VDD



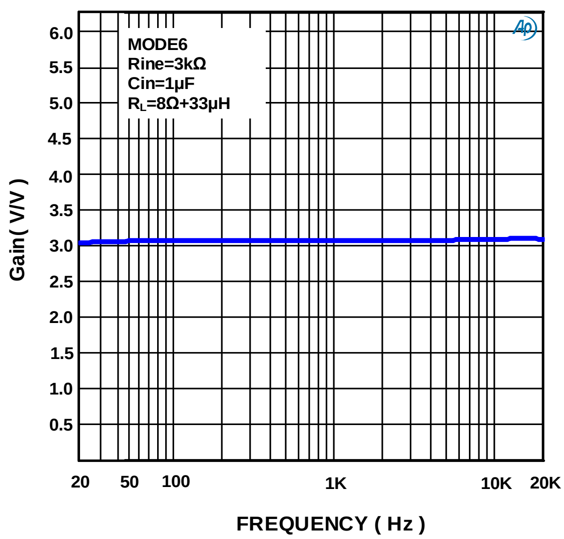
GAIN vs FREQUENCY



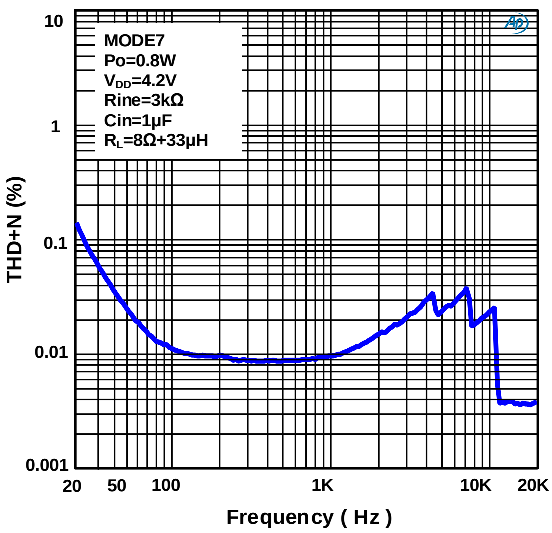
GAIN vs FREQUENCY



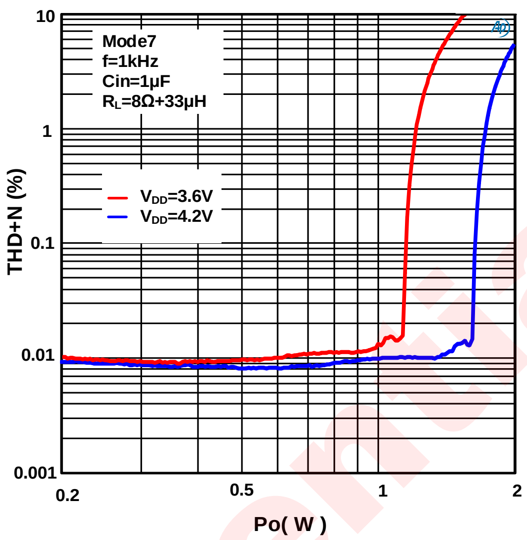
GAIN vs FREQUENCY



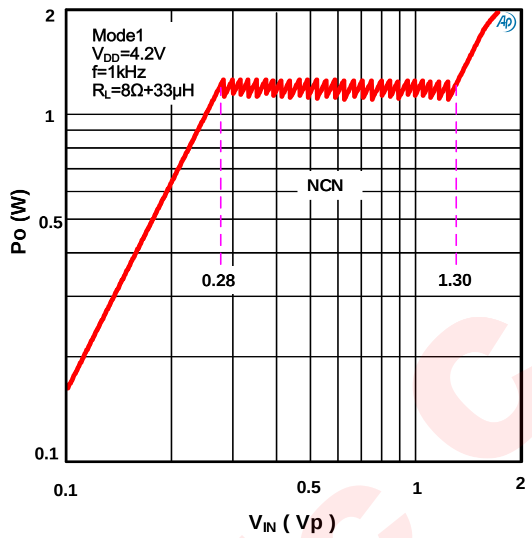
THD+N vs FREQUENCY



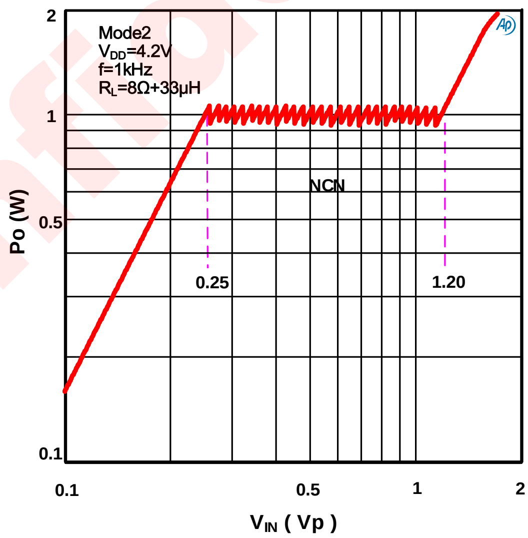
THD+N vs Po



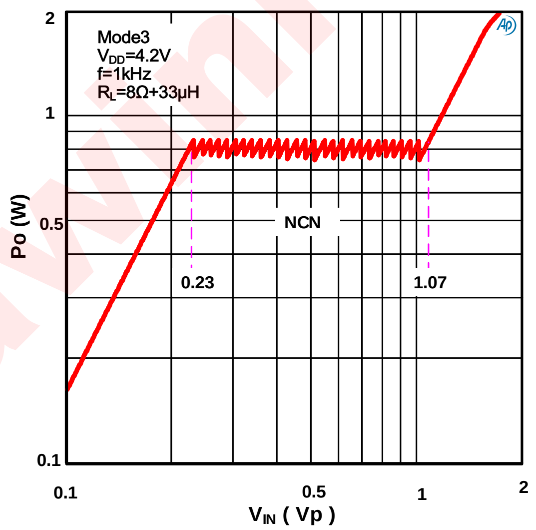
Po vs V_{IN}



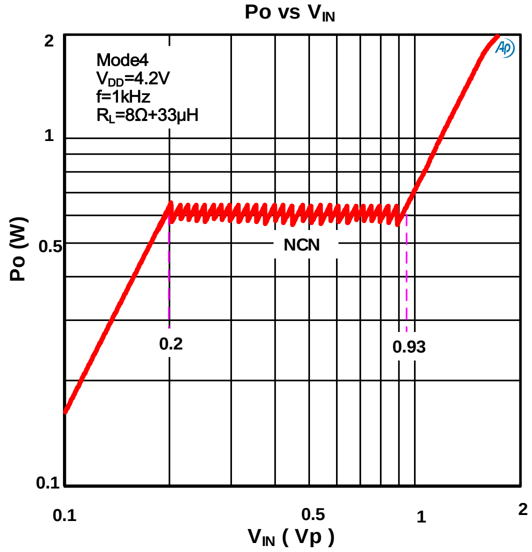
Po vs V_{IN}



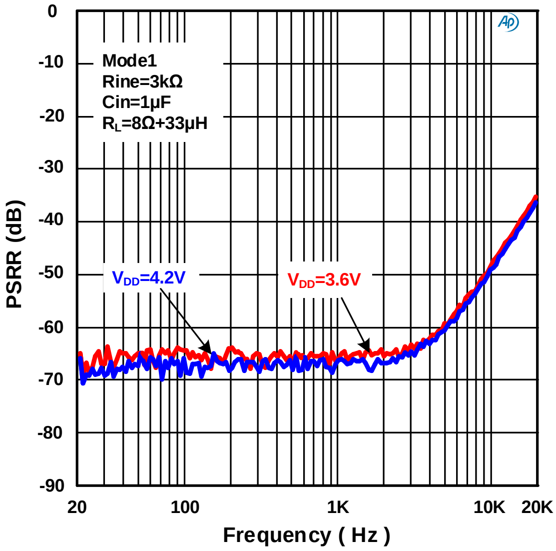
Po vs V_{IN}



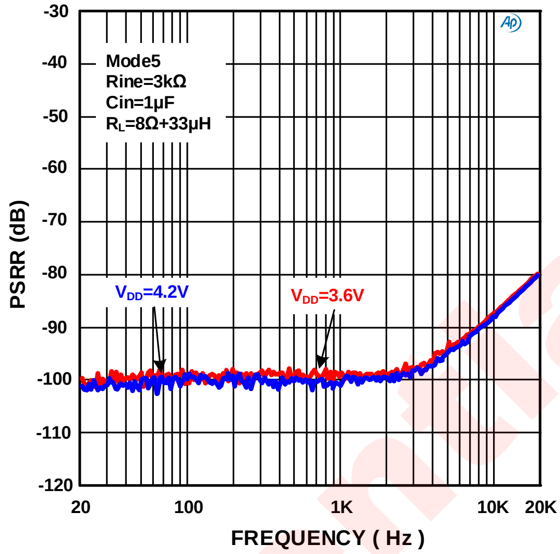
Po vs V_{IN}



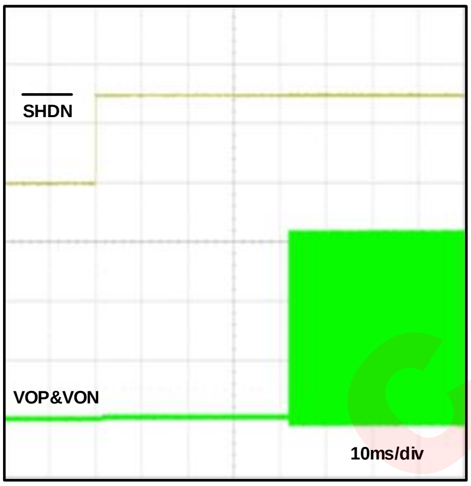
PSRR vs FREQUENCY



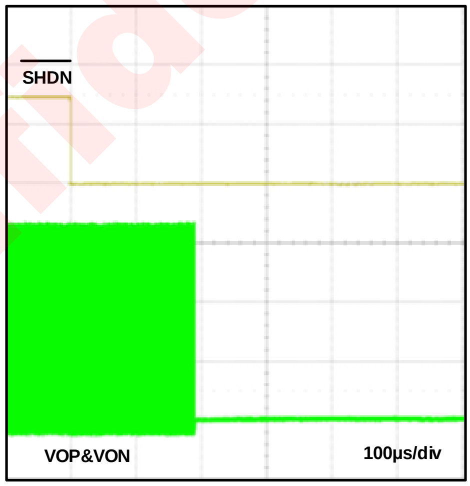
PSRR vs FREQUENCY



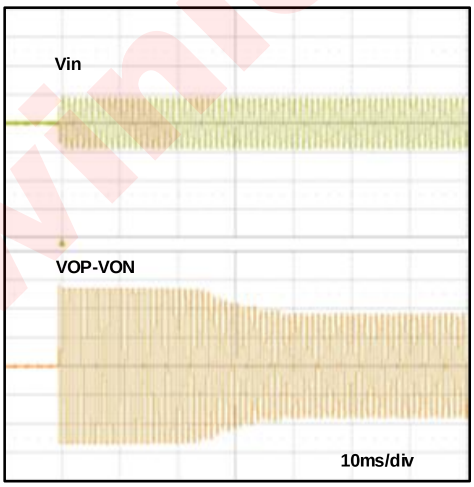
STARTUP SEQUENCE



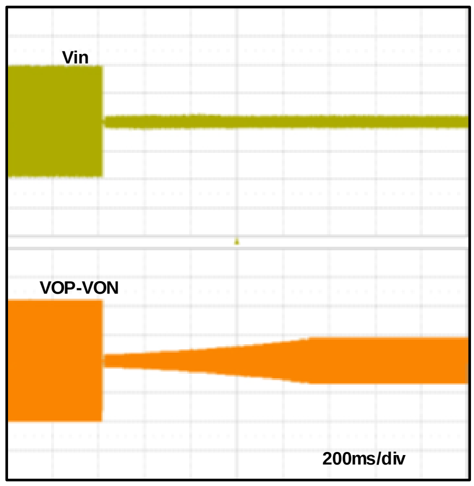
SHUTDOWN SEQUENCE



NCN ATTACK SEQUENCE



NCN RELEASE SEQUENCE



DETAILED FUNCTIONAL DESCRIPTION

AW87337 is specifically designed to enhance overall sound quality. It is an upgrading 7th-generation class K audio amplifier with high efficiency, low noise, ultra-low distortion and capability of outputting constant large volume.

With integrated AWINIC proprietary NCN output AGC audio algorithm, AW87337 can eliminate noise in playback and improve sound quality and effect. Using a novel K-Chargepump technology, its integrated charge pump efficiency can reach 93%, and power amplifier's overall efficiency can reach 80%. With high efficiency, AW87337 can greatly prolong smart phone usage time.

AW87337 noise floor is as low as 53μV, with 97dB high signal-to-noise-ratio (SNR). The ultra-low distortion 0.008% brings high-quality musical enjoyment.

AW87337 has a setting of 4-step selectable speaker-guard output power level from 0.6W to 1.2W, suitable for different rated power speakers. Within lithium battery voltage range, it keeps output power constant, preventing voice from degrading.

AW87337 supports speaker and receiver two-in-one application. The Class AB Receiver Mode has an ultra-low output noise of 11μV and an ultra-high power supply noise suppression of -100dB@217Hz. The Direct Mode using audio analog switch can realize ultra-low THD of 0.001% and ultra-high suppression of power supply of -100dB@217Hz.

AW87337 has built-in over-current protection, over-temperature protection and short-circuit protection. AW87337 is available in a 1.575mm×1.575mm, 0.4mm pitch CSP-16 package.

Constant Output Power

In the smart phone audio applications, the AGC function which can promote music volume and audio quality is very attractive, but as the lithium battery voltage drops, the driver capability of ordinary audio power amplifiers will reduce gradually, leading to degrading audio effect. Therefore, it is hard to provide high-quality music within the battery voltage range.

With integrated AWINIC proprietary NCN output AGC audio algorithm and within lithium battery voltage range (3.3V to 4.35V), AW87337 can keep output power constant and never decreasing during lithium battery voltage dropping down. As a result, even if the battery voltage drops, AW87337 can still provide high-quality large-volume music enjoyment.

AW87337 has 8 operating modes. The first 4 modes have NCN output AGC function and their output AGC power levels are 1.2W, 1W, 0.8W, 0.6W, respectively.

2nd Generation NCN Technology

In audio application, there is undesirable distortion in a clipping output signal, because of a too large input signal along with a drop of supply voltage powered by lithium battery. To prevent a speaker load from permanent damage by a clipping output signal, adoption of traditional NCN technology can adjust gain of power amplifier automatically by detecting "Crack" distortion in a output signal, and keep the output signal smooth without clipping. NCN function can effectively prevent a power amplifier overloading, protect a speaker load, and bring high quality music enjoyment at the same time. A traditional NCN function is shown in Figure 8 below.

By adopting AWINIC unique 2nd generation NCN technology, AW87337's output signal is not limited by lithium battery voltage. When battery voltage drops, output signal keeps unchanged and free from distortion, realizing constant output power as shown in figure 9. Therefore, even if battery voltage drops, AW87337 can still provide high quality large volume music enjoyment.

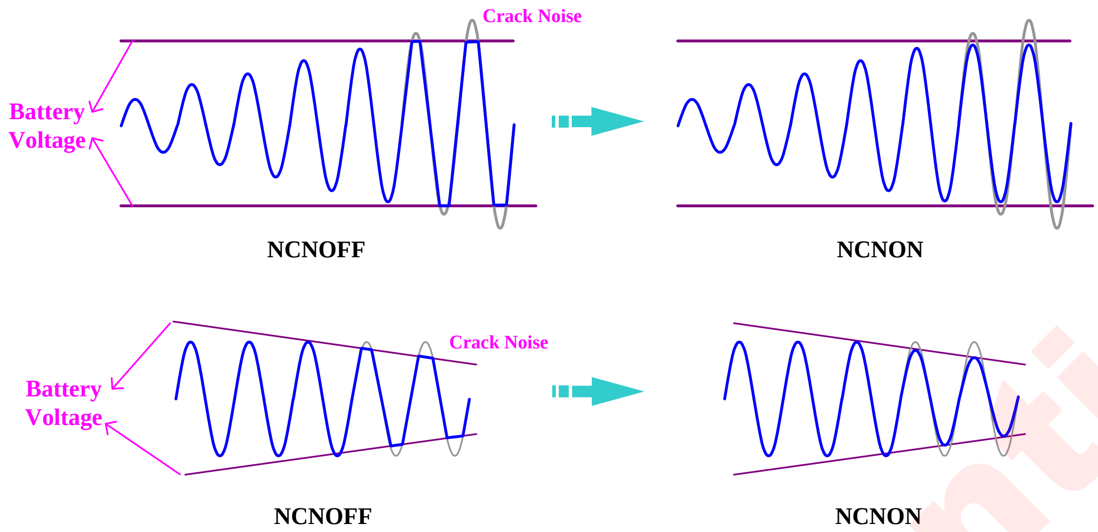


Figure 8 Traditional NCN Operating Principle

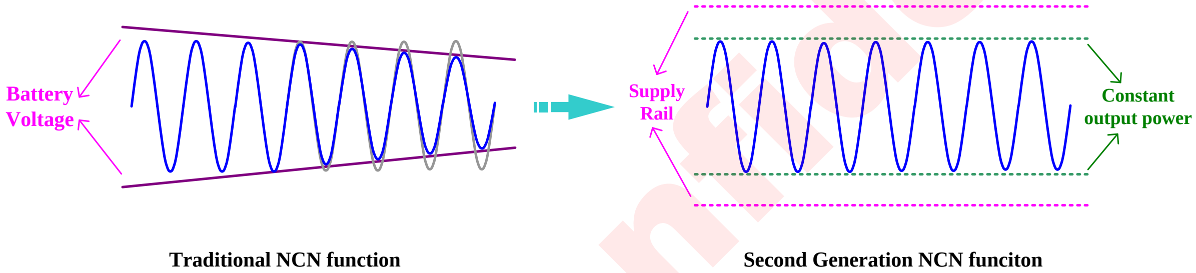


Figure 9 2nd Generation NCN Operating Principle

Attack Time

Attack time is the time which NCN output AGC takes for the gain to be attenuated by 13.5dB when audio signal exceeds the constant output power threshold level. Short attack time (fast attack) allows NCN function to react quickly and suppress harmful transients. However, it can lead to volume pumped and make process of gain reduction noticeable. While long attack time (slow attack) makes NCN function ignore fast transients and act upon longer passages instead, resulting in an increase of distortion. According to audio features in portable equipment, attack time in AW87337 is set to be 40ms, improving the music rhythm, eliminating crack distortion, and protecting the speaker at the same time.

Release time

Release time is the time which NCN output AGC takes for the gain to return to its setting value when audio signal is smaller than clipping level or constant output power threshold level. According to features of music noise in smart phone application and demands for better music quality and volume, release time of AW87337 is designed to be 1.2s, which can effectively eliminate the noise, and make sound smoother.

K-Chargepump

AW87337 adopts a new generation of charge pump technology: K-Chargepump structure. It has higher efficiency and larger driving capability. Its operating frequency is 1.06MHz. With built-in soft-start circuit, current-limit control loop and over-voltage-protection (OVP) loop, charge pump of this configuration can provide more stable and reliable power supply.

High Efficiency

The output voltage PVDD is 1.5 times of supply voltage VDD in K-Chargepump, of which the ideal efficiency can reach 100%. Actually, the K-Chargepump efficiency can be calculated as the ratio of output power to input power, that is

$$\eta = \frac{P_{OUT}}{P_{IN}} \times 100\%$$

For example, in an ideal M-times charge pump, the input current I_{IN} is M times of the output current I_{OUT}, the efficiency formula can be written as:

$$\eta = \frac{P_{OUT}}{P_{IN}} \times 100\% = \frac{V_{OUT} \cdot I_{OUT}}{V_{IN} \cdot M \cdot I_{OUT}} \times 100\% = \frac{V_{OUT}}{M \cdot V_{IN}} \times 100\%$$

Also, M is a parameter depending on the operating mode of a charge pump; VOUT is the output voltage of a charge pump; VIN is the input voltage (generally is also the power supply voltage) of a charge pump; I_{OUT} is also the load current. For K-Chargepump structure, the output voltage is 1.5 times of the input voltage. Due to the switch loss and quiescent current loss inside the charge pump, the actual efficiency can still be up to 93%. As a result, the power booster technology of K-Chargepump can greatly improve the power efficiency.

K-Chargepump Structure

As shown in Figure 10 is a K-Chargepump fundamental functional diagram: K-Chargepump integrated in AW87337 has seven switches, of which the output voltage PVDD is boosted to 1.5 times as input voltage VDD through seven switches operating timing.

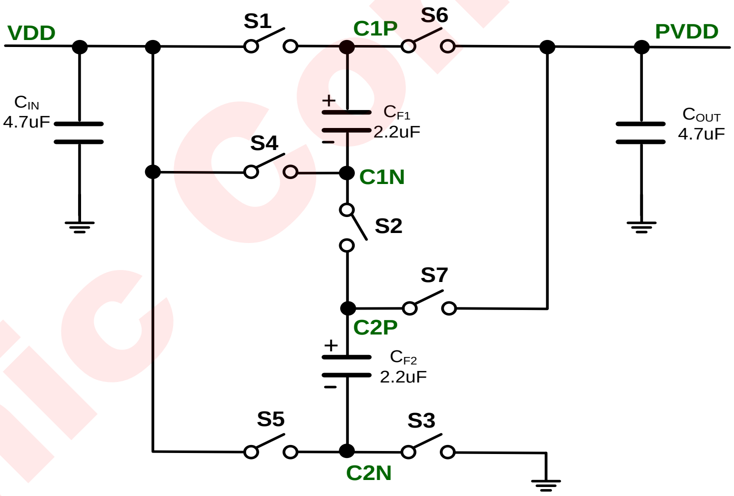


Figure 10 K-Chargepump Functional Diagram

The operation of the charge pump has two phases. In Φ1, as shown in Figure 11, when switches S1, S2 and S3 are closed, VDD charges to the flying capacitor C_{F1} and C_{F2}.

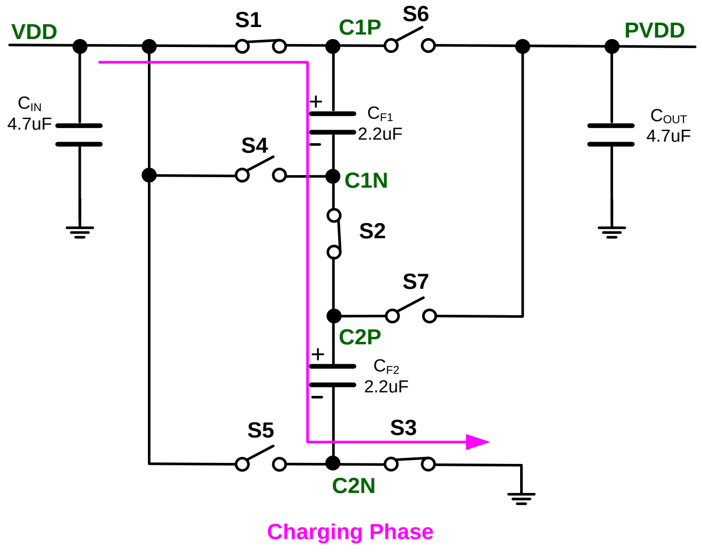


Figure 11 Φ_1: Charge Flying Capacitors C_{F1} and C_{F2}

In Φ_2, as shown in Figure 12, switches S1, S2 and S3 are opened, and switches S4, S5, S6 and S7 are closed. Because the voltage across the capacitor can't change instantaneously, so either the voltage on flying capacitors C_{F1} or C_{F2}, is added to the VDD, realizing a PVDD boosted to a higher voltage.

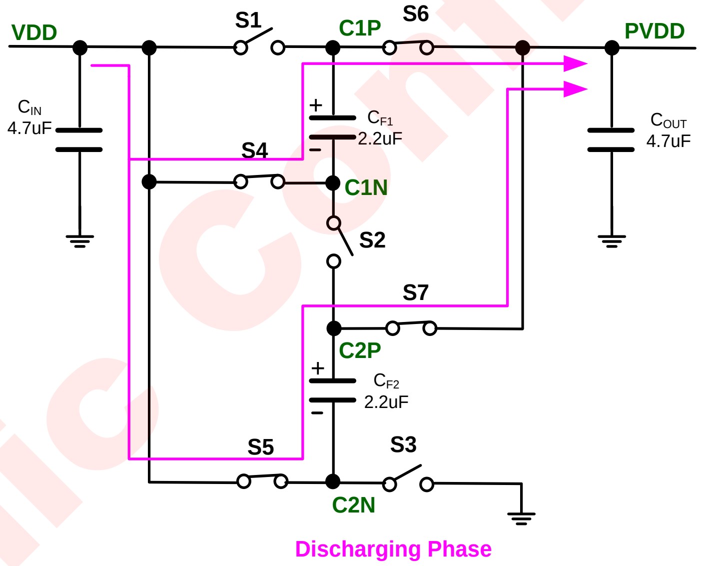


Figure 12 Φ_2: Flying Capacitor Charges Transfer to the Output Capacitor C_{OUT}

Soft Start

K-chargepump has integrated soft start function in order to limit inrush current from power supply during start-up. The current from power supply can be limited to 300mA, and the start-up time is about 1.2ms.

Peak Current Control

K-chargepump has integrated a peak current control circuit. In normal operation, when a heavy load or a situation that makes the charge pump extracts very large current from power supply, the peak current control circuit can limit the maximum output load current, which is typically 2A.

Over-Voltage Protection (OVP)

K-Chargepump keeps the output voltage PVDD a multiple of the input voltage VDD. It provides a high voltage power rail for internal power amplifier circuits, allowing the amplifiers provide greater output dynamic range in the lithium battery voltage range, realizing much larger volume, higher audio quality. K-Chargepump has integrated a over-voltage protection circuit. When the input voltage VDD is greater than 4V, the output voltage PVDD is no longer a multiple of VDD, but a controlled voltage by over-voltage protection (OVP) circuit and kept in 6.05V. The hysteresis voltage of OVP is about 50mV.

Speaker & Receiver Two-in-One Application

Both Mode5 and Mode6 of AW87337 are Class AB Receiver Modes. Their gain are selectable, 1V/V and 3V/V, respectively, for the application flexibility. By multiplexing the speaker's signal path, AW87337 Receiver Modes have ultra-low distortion and strong driving capability. Therefore, it is suitable for high-resolution voice calls. Another advantage is that there is no need to use additional external components, reducing system cost and saving PCB layout space.

In typical applications as Figure 4 shown, with input capacitor Cin=47nF and input resister Rine=3kΩ, the gain at Speaker Mode is about 16.3V/V, and the corner frequency of the input high-pass RC filter is about 173Hz. At Receiver Mode (Mode5) as Figure 5 shown, the gain is changed to 1V/V, with ultra-low output noise of 11μV, and the corner frequency of the input high-pass RC filter is about 71Hz. AW87337 can realize a speaker & receiver two-in-one application without changing any hardware.

Direct Mode Application

Mode8 of AW87337 is a special mode using audio analog switch to realize ultra-low THD and strong suppression of power supply. The audio analog switch integrated in AW87337 is a high-performance, Double-Pole Single-Throw (DPST) switch. It features excellent flatness of Ron (ΔRon≤10mΩ, typically), strong rejection to power supply variation (PSRR=-100dB@217Hz, typically) and ultra-low THD+N (0.001%@R_L=32Ω, typically). This ultra-low power mode takes full advantage of outputs (RCVP&RCVN) from an audio power amplifier for receiver applications (Receiver Power Amplifier, RCV PA) in CODEC of Baseband and can make an ultra-low distortion and strong suppression of interference for receiver applications, as Figure 6 shown.

In typical application as Figure 6 shown, with input resistor R=12Ω and a speaker load of R_L=8Ω, a 32Ω overall load is realized for the receiver power amplifier driving. Therefore, one can just use the RCV PA to drive an 8Ω speaker load as if use the RCV PA to drive a 32Ω receiver load. It should be noticed that actual signals received by the speaker load is only 1/4 output from the RCV PA.

One-Wire Pulse Control: Principle

One-wire pulse control technology only needs a single GPIO port to turn on the chip and select a variety of functions. It is very popular in an environment lack of GPIO ports, such as portable systems.

Considering the problems of signal integrity or RF interference, there is narrow glitch in signal line when the PCB routine is too long. AWINIC one-wire pulse control technology integrated a deglitch circuit along with the internal control pin. The deglitch-module can completely eliminate the harmful glitch interference, as shown in Figure 13.

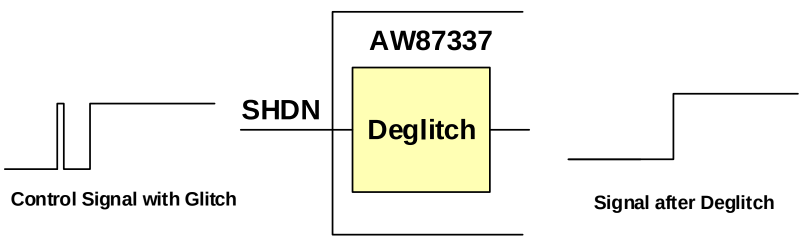


Figure 13 AWINIC Deglitch Working Principle

The traditional one-wire pulse control technology keeps working after the slave chip is powered up. Therefore, when the master chip (such as Baseband in a smart phone) sends other control signal through the same control port, the slave chip will probably enter into a wrong state. AW87337 uses one-wire pulse technology with a latch circuit, by which the right working state will be stored after the master chip sending order and AW87337 will no longer receive successive signals (except shutting down the chip firstly), as shown in Figure 14.

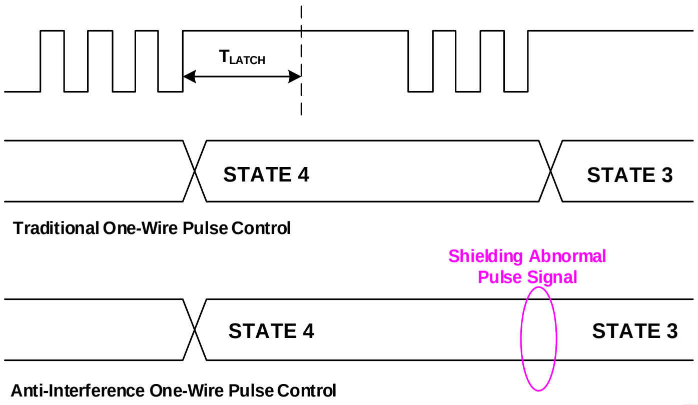


Figure 14 Anti-Interference One-Wire Pulse Control Functional Diagram

One-Wire Pulse Control: Working Mode

Each mode of AW87337 can be set by the on-wire pulse control circuit, which can detect the number of pulses sent by master chip through SHDN pin. When SHDN pulls to high level from shutdown state (low level), i.e. only a rising edge, AW87337 will enter into Mode1, and the constant output power level of Multi-Level AGC is 1.2W (with 8Ω speaker load). When SHDN shows a high-to-low-to-high logic signal, i.e. a rising edge after a pulse, or two rising edges, AW87337 will enter into Mode2, and the level is 1.0W. Similarly, N rising edges means Mode"N", as shown in Figure 15. After all, AW87337 has 8 operating modes, more than 8 rising edges is forbidden.

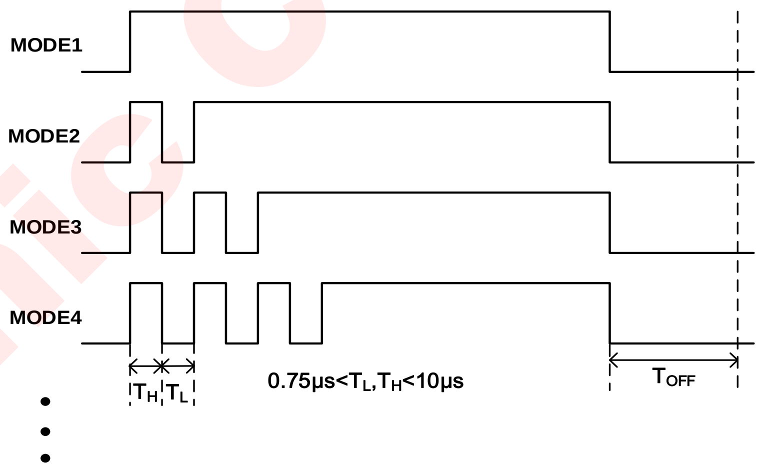


Figure 15 Working Mode Setting through One-Wire Pulse Control

To change the working mode of AW87337, one needs to keep SHDN low longer than T_{OFF} firstly (1ms is recommended), to shut down the chip. Then, send pulses to bring the chip into a right mode, as shown in Figure 16.

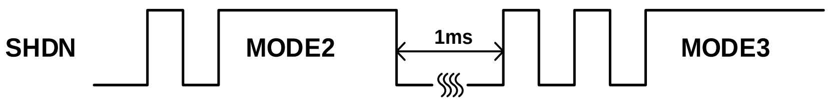


Figure 16 Mode Switch through One-Wire Pulse Control

RNS (RF Noise Suppression)

GSM transmission adopts TDMA (Time Division Multiple Access) Technology which results in frame burst at frequency of 217Hz, also called TDD (Time Division Duplexing), leading to a strong RF interference (RF Noise) and the 217Hz energy along with its harmonics (TDD Noise) can be easily interacted with audio power amplifiers.

In applications, optimization of both layout and selection of peripheral components may decrease the AW87337's susceptibility to RF noise and prevent TDD Noise from being demodulated into audible noise. Minimization of length of routings prevents them from functioning as antennas and coupling RF noise into an AW87337. Further RF immunity can also be realized by using capacitors of which feature of frequency response is like a notch filter. Depending on manufacturers, self-resonance frequency of 10pF to 20pF capacitors typically located at RF band. Such capacitors placed in front of input pins of AW87337 can effectively suppress RF noise. Also, such capacitors must have a low-impedance, low-inductance path to the ground plane.

Even if part of RF energy is injected into AW87337 by traces connected to the chip, regardless of efforts of TDD Noise Reduction. AW87337 features a unique RNS technology, which effectively reduces RF energy and attenuates RF TDD-noise to an acceptable audible level for customers.

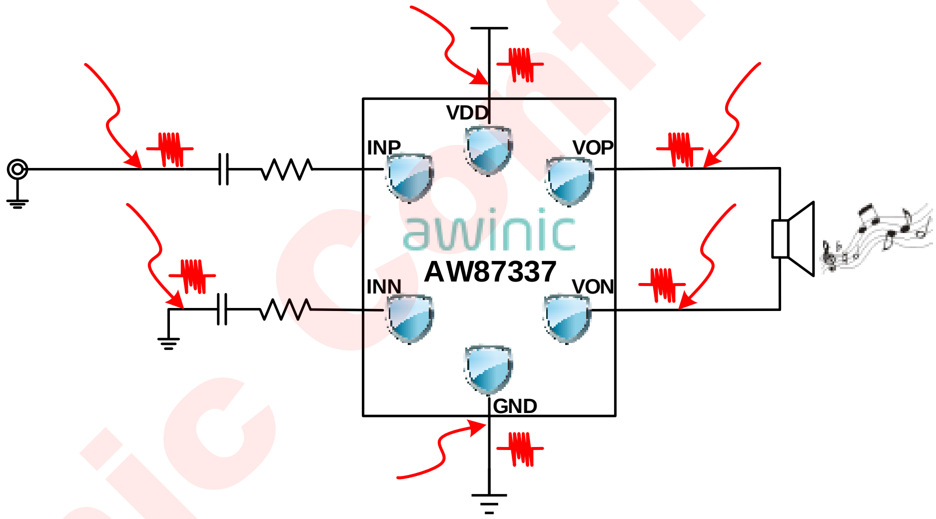


Figure 17 AW87337 Rejection of RF Noise

Filter-Free Pulse Width Modulation (Filter-Free PWM)

AW87337 features a filter-free PWM architecture which removes a LC filter behind the output stage of a traditional Class D power amplifier, resulting in improvement of overall efficiency, decrease of PCB area and reduction of system cost.

Enhanced Emission Elimination (EEE)

AW87337 features a unique Enhanced Emission Elimination (EEE) technology, which adjusts the speed of waveform transition of PWM output signal, and effectively reduces EMI over FM/AM bandwidth.

Pop-Click Suppression

AW87337 integrates a unique timing-control circuit, which fundamentally suppresses pop-click noise, and eliminates audible crack at shut-down, wake-up, and power-up/down.

Protection

When a short-circuit occurs among output pins (VOP, VON) and power pins (VDD, GND, PVDD) of AW87337, an over-current protection (OCP) circuit will be trigged and shut down the chip immediately, preventing the device from being damaged. When abnormal condition is removed, AW87337 can restart automatically without wake-up.

When junction temperature in AW87337 is too high, an over-temperature protection (OTP) circuit will be triggered and shut down the chip immediately. The circuit will turn the device on once the temperature decrease into a safe scope.

APPLICATION INFORMATION

Gain Setting -- Selection of External Input Resistor (R_{ine})

AW87337 is a differential-input audio power amplifier. It integrates two internal input resistors (R_{ini}), which are both 6.6kΩ. Take external input resistors R_{ine}=3kΩ for instance, overall gain (A_V) can be set as below:

AW87337 Mode	Calculation of Overall Gain (V/V)
Class K Speaker Mode (Mode1~4, and Mode7)	$A_V = \frac{319.5k\Omega}{R_{ine}+R_{ini}} = \frac{319.5k\Omega}{3k\Omega+16.6k\Omega} = 16.3V/V$
Class AB Receiver Mode with 1V/V gain (Mode5)	$A_V = \frac{48k\Omega}{R_{ine}+R_{ini}} = \frac{48k\Omega}{3k\Omega+45k\Omega} = 1V/V$
Class AB Receiver Mode with 3V/V gain (Mode6)	$A_V = \frac{144k\Omega}{R_{ine}+R_{ini}} = \frac{144k\Omega}{3k\Omega+45k\Omega} = 3V/V$

Input High-Pass Cutoff Frequency Setting -- Selection of Input Capacitor (C_{in})

Input capacitors in front of external input resistors can block DC component of input audio signals. An input capacitor (C_{in}) along with input resistors (R_{ine}+R_{ini}) forms an input high-pass filter with a corner frequency (f_H) calculated as below:

$$f_H(-3dB) = \frac{1}{2\pi(R_{ine}+R_{ini})C_{in}}$$

A higher f_H results in a better suppression of 217Hz GSM input noise. A better matching of input capacitors improves capability of blocking of common-mode interference of input stage in AW87337 and also helps to reduce pop-click noise.

Take typical application in Figure 1 for instance:

$$f_H(-3dB) = \frac{1}{2\pi(R_{ine}+R_{ini})C_{in}} = \frac{1}{2\pi \cdot 19.6k \cdot 47nF} = 173Hz$$

Besides, take Class AB Receiver Mode with 1V/V gain (Mode8) for instance:

$$f_H(-3dB) = \frac{1}{2\pi(R_{ine}+R_{ini})C_{in}} = \frac{1}{2\pi \cdot 48k \cdot 47nF} = 71Hz$$

Input Low-Pass Cutoff Frequency Setting – Selection of Differential Input Capacitor (C_d)

A differential input capacitor behind external input resistors can block high-frequency component of input audio signals, such as screechy part in a song. A differential input capacitor (C_d) along with input resistors (R_{ine}+R_{ini}) forms an input low-pass filter with a corner frequency (f_L) calculated as below:

$$f_L(-3dB)=\frac{1}{4\pi(R_{ine}//R_{ini})C_d}$$

Take typical application in Figure 1 with C_d=220pF and R_{ine}=3kΩ for instance:

$$f_L(-3dB)=\frac{1}{4\pi\cdot(3k\Omega//16.6k\Omega)\cdot 220pF}=142.5kHz$$

Selection of Power Supply Decoupling Capacitor (C_S)

AW87337 is a high-performance audio power amplifier. It is essential to place a ceramic capacitor (C_S) with low equivalent-series-resistance (ESR) (typical 0.1uF) for power supply decoupling. Optimized selection and placement of decoupling capacitors protect AW87337 from interference injection from power supply, such as high-frequency transients, spikes, or digital noise. Specifically, a layout of decoupling capacitor closer to AW87337 is preferred, since fewer parasitic resistance or inductance between power pin and the capacitor, less decoupling efficiency loss. In addition to a 0.1μF ceramic capacitor, another 10μF capacitor as a charge reservoir is required, providing transient power energy for AW87337 and preventing remarkable drop of the power supply voltage.

Selection of Charge Pump Flying Capacitor (C_F)

Value of charge pump flying capacitors (C_F) affects load regulation and output impedance of the charge pump. Small capacitance may degrade driving capability of AW87337. A 2.2μF/6.3V ceramic capacitor is usually recommended.

Selection of Charge Pump Output Capacitor (C_{OUT})

Capacitance and ESR of charge pump output capacitors (C_{OUT}) directly affect ripple magnitude of charge pump output voltage (PVDD). Increasing C_{OUT} Capacitance reduces variations of PVDD and decreasing C_{OUT} ESR also reduces both ripple and output resistance. A 4.7μF/10V ceramic capacitor is usually recommended.

Usage of Ferrite Bead and Filter Capacitor

Without ferrite beads and filter capacitors, AW87337 can still pass the specifications of FCC and CE. If there is any EMI sensitive device near AW87337 and/or there are long traces routing from the amplifier to a speaker, use ferrite beads and filter capacitors and place beads and capacitors as close as possible to output pins (VOP&VON), as Figure 18 below.

In Class K Speaker Mode, outputs of AW87337 are square-wave PWM signals, which charge and discharge filter capacitors in each period, and result in additional static power consumption. Bigger filter capacitance, larger current consumption. Therefore, 0.1nF ceramic capacitor is usually recommended for low power application.

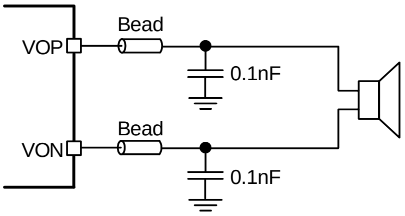


Figure 18 Ferrite Beads and Filter Capacitors

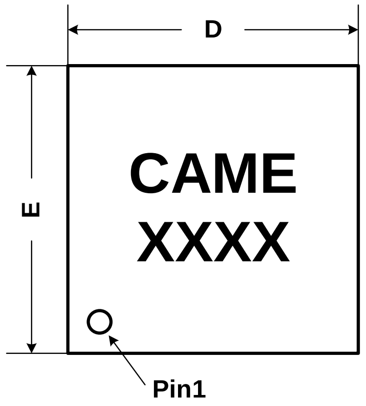
PCB AND DEVICE LAYOUT CONSIDERATION

In order to exploit best performance of AW87337, PCB layout must be carefully considered. Design consideration should be followed as below:

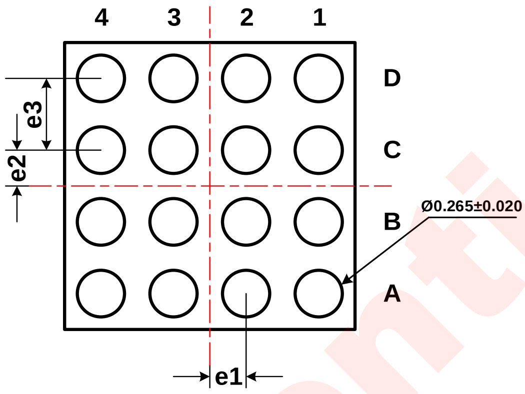
1. Isolated, short and wide power lines for both VDD pin and GND pin are required for better driving-capability of AW87337. The copper width is recommended to be larger than 0.75mm (30mil). Power supply decoupling capacitors should be placed as close as possible to power supply pins.
2. Flying capacitors C_{F1}, C_{F2} should be placed as close as possible to C1N, C1P pins and C2N, C2P pins. Likewise, capacitor C_{OUT} should be close to PVDD pin. The trace from C_{OUT} to both PVDD pin and GND pin should be short and wide.
3. Input capacitors and resistors should be close to INN and INP pins. Differential and ground-shielding input routing is required to suppress noise coupling.
4. Ferrite beads and filter capacitors should be close to VON and VOP pins. The trace from output pins to speaker should be short and wide. The copper width is recommended to be larger than 0.5mm (20mil).

PACKAGE INFORMATION

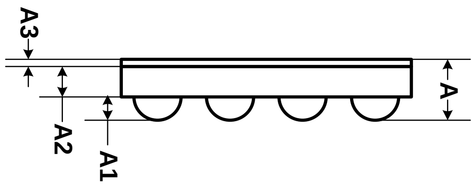
TOP VIEW



BOTTOM VIEW



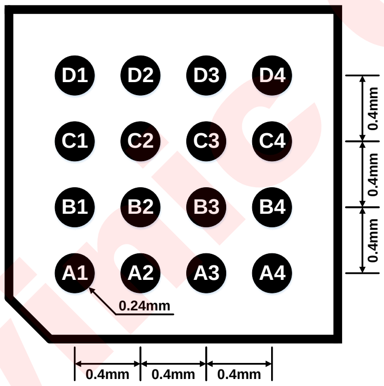
SIDE VIEW



Symbol	NOM	Tolerance
A	0.575	±0.055
A1	0.195	±0.020
A2	0.340	±0.025
A3	0.040	±0.010
D	1.575	±0.025
E	1.575	±0.025
e1	0.200	NA
e2	0.200	NA
e3	0.400	NA

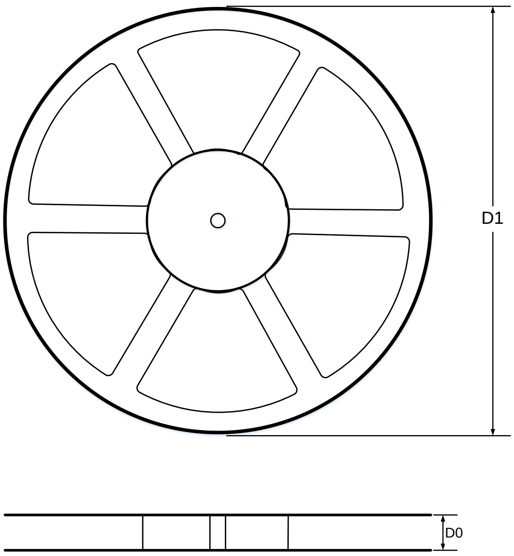
Unit: mm

LAND PATTERN

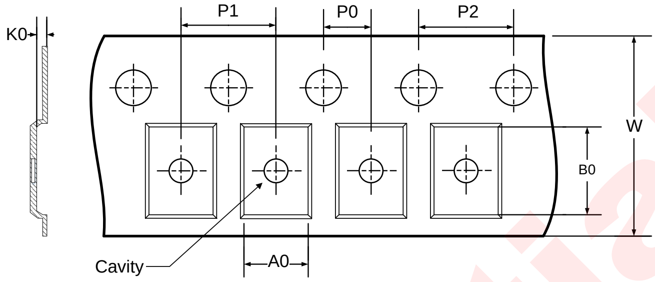


TAPE INFORMATION

REEL DIMENSIONS

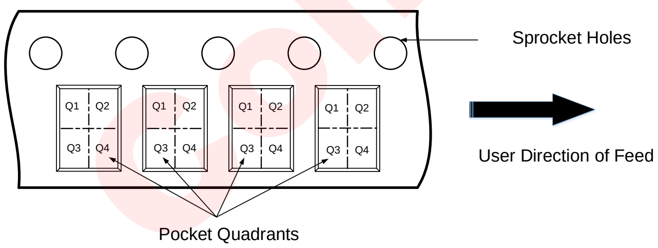


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D0：Reel width
D1：Reel diameter

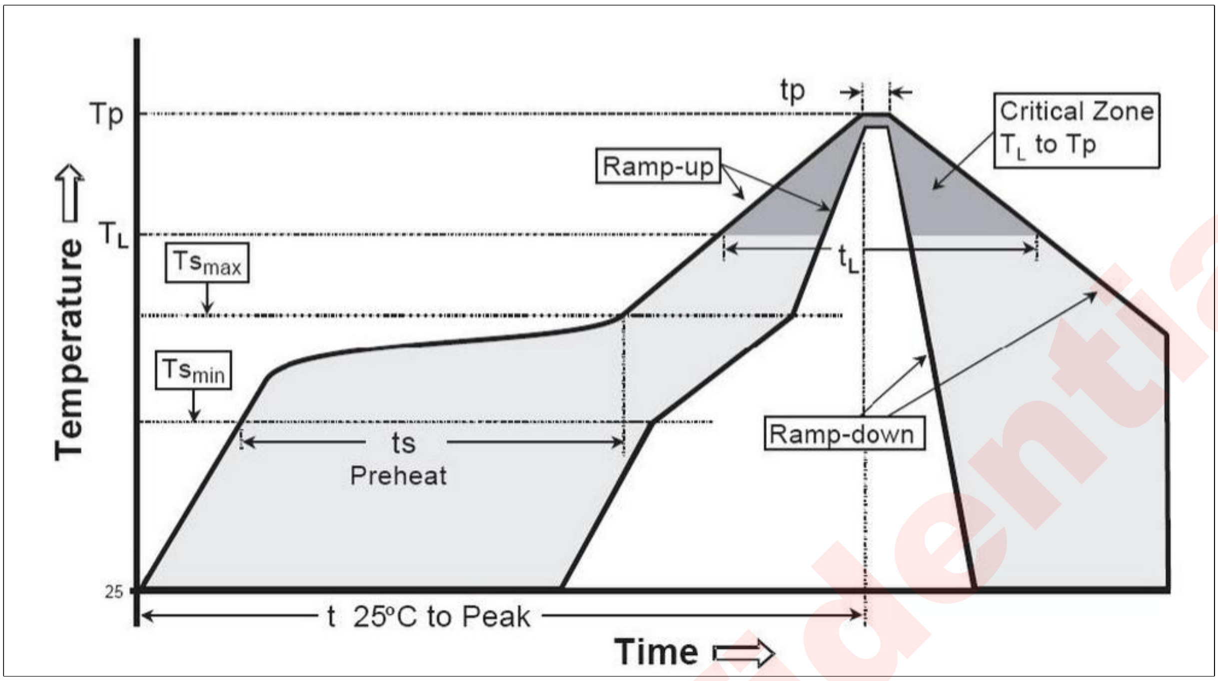
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



All dimensions are nominal

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
179.00	9.00	1.73	1.73	0.72	2.00	4.00	4.00	8.00	Q1

REFLOW SOLDERING CURVE



Reflow Note	Spec
Average Ramp-up Rate (217°C to Peak)	Max. 3°C/sec
Time of Preheat temp. (from 150°C to 200°C)	60sec-120sec
Time to be Maintained above 217°C	60sec-150sec
Peak Temperature	250°C~260°C
Time within 5°C of Actual Peak Temp	20sec-40sec
Ramp-down Rate	Max. 6°C/sec
Time from 25°C to Peak Temp	Max. 8min

VERSION INFORMATION

Version	Date	Description
V1.0	2017-05-07	AW87337CSR datasheet V1.0
V1.1	2018-09-20	Change tape information

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