

## A Low Power One-key Capacitor Touch Sensor

### **Features**

- Sensitivity adjusted by the capacitance (0~50 pF) outside
- Maximum key-on duration time: 16s
- Maximum response time
  - Slow scan mode: 160ms (AW93001CDN R/DDNR)
  - Slow scan mode: 64ms (AW93001EDNR/ FDNR)
  - > Fast scan mode: 48ms
- Push-pull output, active high (AW93001CDNR /EDNR)
- Open-drain output, active low (AW93001DDN R/FDNR)
- Low power consumption
  - Slow scan mode: 1.0μA (AW93001CDNR /DDNR)
  - Slow scan mode: 2.2μA (AW93001EDNR /FDNR)
  - Fast scan mode: 3.2μA
- 2.4V~5.5V power supply
- Operation temperature range: -40°C~85°C
- DFN 1.0mmx1.0mmx0.37mm-4L package

### **General Description**

AW93001X is a single channel capacitive touch controller with low power consumption and wide operation voltage range.

With the help of signal processing algorithms, the device is able to track slow environmental variations, and maintain high performance operation.

AW93001X is designed for replacing traditional mechanical button. It can be applied in many fields, such as consumer electronics, white goods and appliances, etc.

## **Applications**

Wearable device, White goods and appliances Replacing traditional mechanical button

# **Typical Application Circuit**

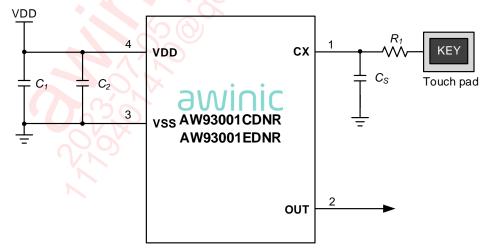


Figure 1 AW93001CDNR/EDNR Typical Application Circuit (push-pull output)



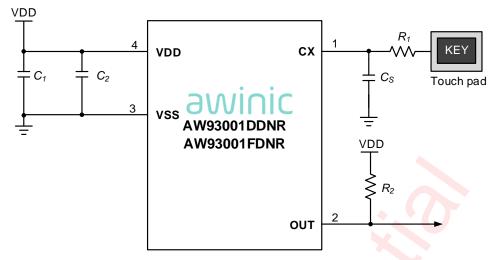
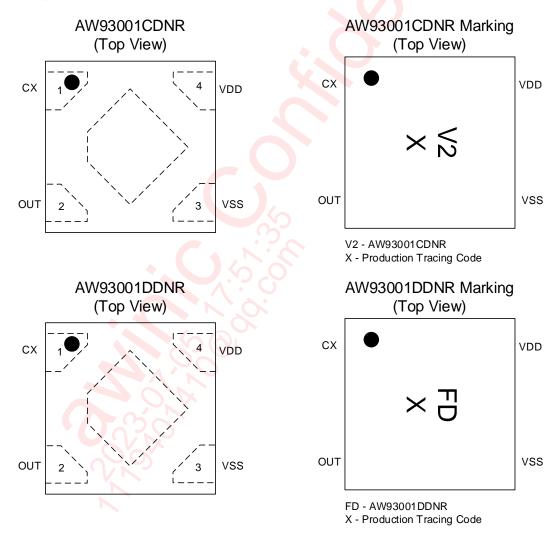
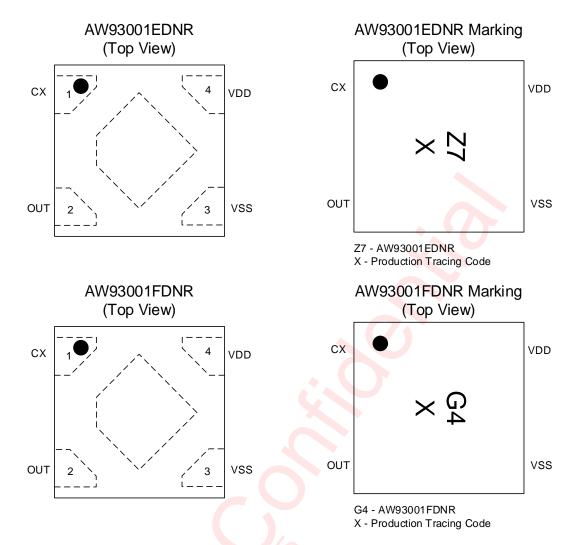


Figure 2 AW93001DDNR/FDNR Typical Application Circuit (open-drain output)

## **Pin Configuration And Top Mark**







Note: The exposed pad in the middle is floating, it can be connected to VSS.

### **Pin Definition**

No.	NAME	DESCRIPTION
1	CX	Capacitive detector input
2	ОИТ	Push-pull output (AW93001CDNR/EDNR) Open-drain output (AW93001DDNR/FDNR), require pull-up resistor
3	VSS	Ground
4	VDD	Power supply (2.4V~5.5V), requires decoupling capacitor

# **Device Comparison**

Table 1 Device Comparison

Device	Dookogo	Scan	Period	мот	Output Mode
Device	Package	Fast scan	Slow scan	WOI	Output Mode
AW93001CDNR	DFN1x1-4L	16ms	128ms		Push-pull
AW93001DDNR	DFN1x1-4L	16ms	128ms	160	Open-drain
AW93001EDNR	DFN1x1-4L	16ms	32ms	16s	Push-pull
AW93001FDNR	DFN1x1-4L	16ms	32ms		Open-drain



# **Functional Block Diagram**

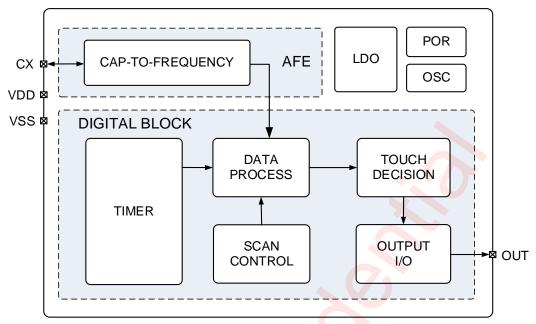


Figure 3 Functional Block Diagram

# **Ordering Information**

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW93001CDNR	-40°C~85°C	DFN 1.0mmx1.0 <mark>m</mark> m-4L	V2	MSL1	ROHS+HF	4500 units/ Tape and Reel
AW93001DDNR	-40°C~85°C	DFN 1.0mmx1.0mm-4L	FD	MSL1	ROHS+HF	4500 units/ Tape and Reel
AW93001EDNR	-40°C~85°C	DFN 1.0mmx1.0mm-4L	<b>Z</b> 7	MSL1	ROHS+HF	4500 units/ Tape and Reel
AW93001FDNR	-40°C~85°C	DFN 1.0mmx1.0mm-4L	G4	MSL1	ROHS+HF	4500 units/ Tape and Reel

# **Absolute Maximum Ratings**(NOTE1)

PARAMETER	PARAMETERS					
Supply voltage rang	je VDD	-0.3V to 6.0V				
Input voltage range	Input vo <mark>ltage range CX</mark>					
Output voltage range	Output voltage range OUT					
Operating free-air tempe	rature range	-40°C to 85°C				
Maximum operating junction to	Maximum operating junction temperature T <sub>JMAX</sub>					
Storage temperature	Storage temperature T <sub>STG</sub>					
Lead temperature (solderin	Lead temperature (soldering 10 seconds)					
ES	OTE 2)					
НВМ	НВМ					
CDM	CDM					



PARAMETERS	RANGE
Latch-Up	
Test condition: JESD78E	+IT: 200mAIT: -200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The human body model is a 100pF capacitor discharged through a 1.5k $\Omega$  resistor into each pin. Test method: ANSI/ESDA/JEDEC JS-001-2017(HBM), ANSI/ESDA/JEDEC JS-002-2018(CDM).

### **Electrical Characteristics**

Note: Typical values are given for T<sub>A</sub> = +25°C, VDD=3.0V unless otherwise specified.

	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
VDD	Operation voltage	-	2.4	3.0	5.5	V
, Current in slow scan		C <sub>S</sub> =20pF, scan period=128ms	-	1.0	-	μΑ
IsL	mode	Cs=20pF, scan period=32ms	1	2.2	-	μΑ
I <sub>FS</sub>	Current in fast scan mode	C <sub>S</sub> =20pF, scan period=16ms	-	3.2	-	μΑ
Іон	Output high current	V <sub>OH</sub> ≥ VDD-0.4V (for AW93001CDNR/EDNR)	1	-	-4	mA
I <sub>OL</sub>	Output low current	V <sub>OL</sub> ≤ 0.4V	8	-	-	mA
		Fast scan mode, scan period=16ms	ı	-	48	ms
T <sub>RESP</sub>	Response time	Slow scan mode, scan period=32ms	-	-	64	ms
		Slow scan mode, scan period=128ms	-	-	160	ms

## **Detailed Functional Description**

#### Initialization

After power-on, the chip executes initialization process automatically, it lasts for about 500ms. During initialization, touch decision does not work, and no touch status can be reported.

#### Scan Mode

For power saving, the devices automatically switches scan mode between fast and slow mode according to touch detection status. After power-on, the devices enters fast scan mode directly. In fast scan mode, if there is no touch detected for 8s continuously, the devices switches to slow scan mode. In slow scan mode, if touch is detected, the devices returns to fast scan mode at once.

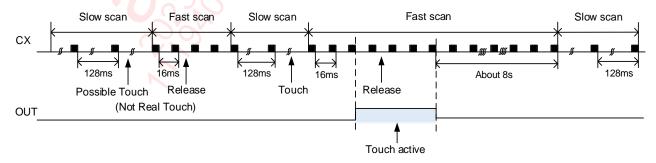


Figure 4 AW93001CDNR Scan Mode



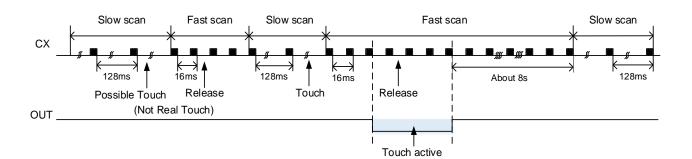


Figure 5 AW93001DDNR Scan Mode

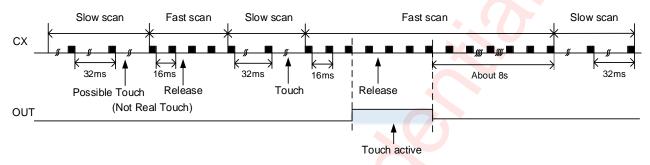
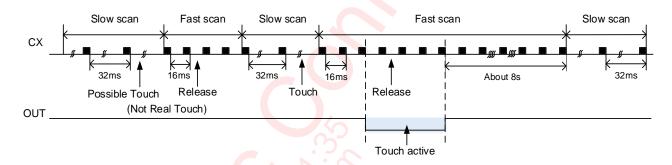


Figure 6 AW93001EDNR Scan Mode



AW93001FDNR Scan Mode Figure 7

### **Maximum Key-on Duration Time**

In order to prevent the false touch detection caused by objects covering the touch pad, the chip sets maximum key-on duration time. If the AW93001CDNR/DDNR/EDNR/FDNR's touch status last over 16s, it will be released until a new touch action.



### **Application Information**

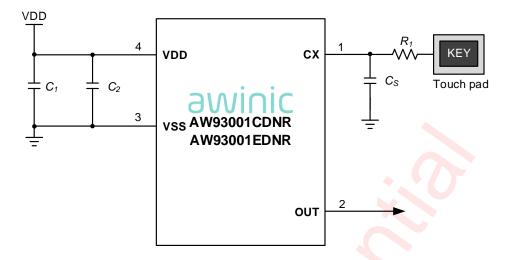


Figure 8 AW93001CDNR/EDNR Typical Application Circuit(push-pull output)

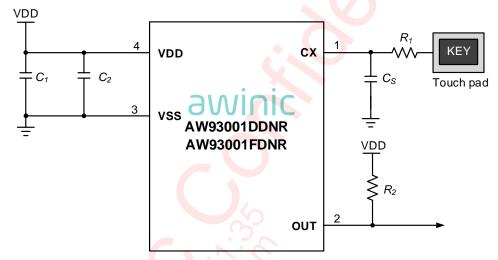


Figure 9 AW93001DDNR/FDNR Typical Application Circuit(open-drain output)

To obtain the optimal performance, the capacitive touch controller's application circuit should be considered carefully. Here are some guidelines:

- 1. The chip should be supplied by stable power, otherwise it may cause abnormal sensitivity or false detection.
- 2. Add a resistor R<sub>1</sub> between C<sub>S</sub> and Touch pad to improve ESD protection and reduce EMI.
- 3. Sensitivity can be adjusted by C<sub>s</sub>. The smaller the C<sub>s</sub>, the higher the sensitivity, the higher the power consumption. The range of C<sub>s</sub> is 0~50pF. It is suggested to use temperature insensitive capacitors to adjust the sensitivity, such as NP0 capacitors.
- 4. Sensitivity can be adjusted by the electrode size. Using a larger electrode size can increase sensitivity, but the electrode size must be used in the effective scope.
- 5. Sensitivity can be adjusted by the panel thickness. Using a thinner panel can increase sensitivity, but the panel thickness must be used in the effective scope.

### **Recommended Components List**

Component	Name	DESCRIPTION	TYP.	UNIT
	C <sub>1</sub>	-	1	μF
С	C <sub>2</sub>	-	0.1	μF
o l	Cs	5% resolution  Low temperature coefficient	-	pF
R	R <sub>1</sub> 5% resolution		4.7	kΩ
K	R <sub>2</sub>	5% resolution	100	kΩ

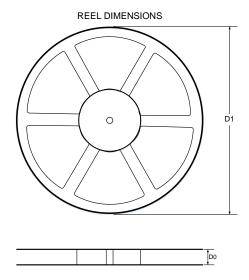
## **PCB Layout Consideration**

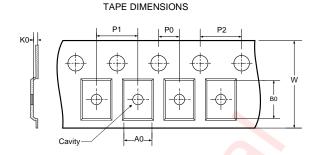
To obtain the optimal performance, PCB layout should be considered carefully. Here are some guidelines:

- 1. The connections between the capacitors  $(C_1, C_2)$  and the IC as short as possible, to reduce noise and EMI.
- 2. The distance from the touch pad to the pin CX as short as possible, and the signal trace as thin as possible.
- 3. The IC and sensor traces surrounded by ground, both top and bottom layers filled with ground plane.
- 4. The sensor and traces away from mic, earphone line, because capacitive sensor will disturb audio line.
- 5. The sensor and traces away from interferences, such as communication lines.
- 6. The material of panel covering the PCB cannot contain metal or electric element, and the surface coating is the same.



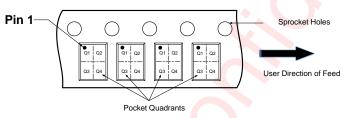
# **Tape And Reel Information**





- A0: Dimension designed to accommodate the component width B0: Dimension designed to accommodate the component length
- K0: Dimension designed to accommodate the component thickness
- W: Overall width of the carrier tape
  P0: Pitch between successive cavity centers and sprocket hole
- P1: Pitch between successive cavity centers
- P2: Pitch between sprocket hole
  D1: Reel Diameter
- D0: Reel Width

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note: The above picture is for reference only. Please refer to the value in the table below for the actual size

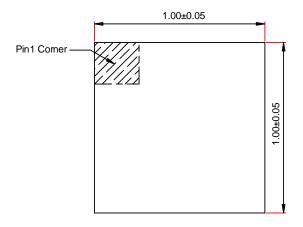
### DIMENSIONS AND PIN1 ORIENTATION

 DIIVILINOI	ONO AND	T IIVI OI	CILIVIAIN	J14						
D1	D0	A0	B0	K0	P0	P1	P2	W	Pin1 Quadrant	
(mm)	(mm)	(mm)	(mm)	(mm)	(mm)	(mm)	(mm)	(mm)	Pili Quadrani	
178	8.4	1.15	1.15	0.5	2	4	4	8	Q1	

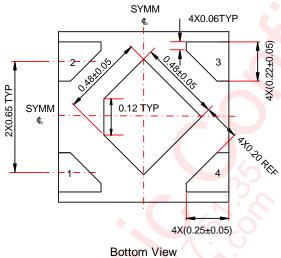
All dimensions are nominal



# **Package Description**



CVMM



Top View

0.100 REF

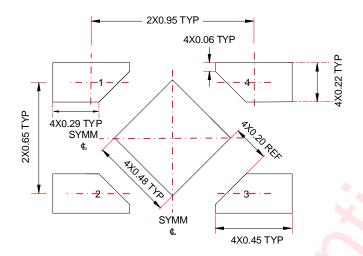
MAX 0.40

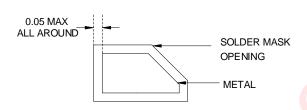
0~0.05

Side View

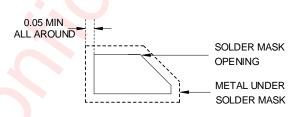
Unit:mm

### **Land Pattern Data**





NON SOLDER MASK DEFINED



SOLDER MASK DEFINED

UNIT: mm



# **Revision History**

Version	Date	Change Record
V1.0	Aug.2022	Officially released
V1.1	Sep.2022	Update the Absolute Maximum Ratings, correct the maximum voltage range. (P4)
V1.2	Jan.2023	Add the note of the exposed pad. (P3)
V1.3	Jun.2023	Update the current in fast scan mode (P1 and P5). Add the I <sub>OH</sub> and I <sub>OL</sub> in the table of Electrical Characteristics (P5).

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