# Smart 27 LED Driving SoC with Audio Synchronization

## FEATURES

- 9 current sink and 3 current switch driving up to 27 LEDs or 9 RGBs in matrix display mode
  - Global 16 current steps, max 75mA
  - Individual 12 bit PWM dimming control
  - Individual 256 steps of constant current
- Embedded MCU, Flash ROM, reloadable lighting effect firmware for dedicated application
- Audio input, 8bit ADC, -12dB~51dB AGC for gain adjustment
- Pre-load LED lighting program
  - Flowing-water music sync lighting effect
  - Skyline breathing lighting
  - 27 independent automatic breathing light
- Cascade for multi-chip synchronization
- LED current accuracy: ±10%
- LED matching accuracy: ±10%
- Low dropout voltage: 100mV
- 400kHz $I^2C^{TM}$ interface ($I^2C$ address: 0x6A/6B)
- Single power supply, 2.7V~5.5V
- QFN4X4-24L package

## GENERAL DESCRIPTION

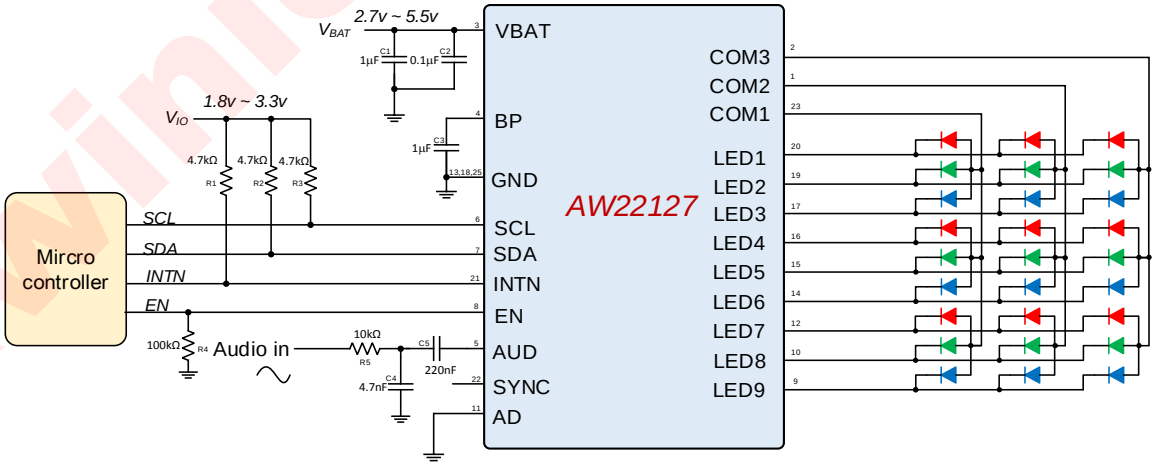
AW22127 is a smart LED driving SoC with audio synchronization, integrated with MCU, Flash ROM, SRAM, ADC, PGA, and LED driver circuit. All lighting effect is implemented by pre-loaded firmware designed for specific application.

There are 9 constant current sinks (LED1~9) and 3 current switch (COM1~3) capable of driving up to 27 LEDs or 9 RGB LEDs in matrix display mode. Each LED has 256 current steps for brightness or color-mixing, 12-bit PWM level for dimming. When the max output current is 75mA with 1/3 cycle rate, 25mA average current is available for each LED.

Additionally, parameter configurable PGA, ADC, digital filters provide flexible sampling and process function for audio input. Unusually brilliant audio sync lighting effects could be achieved by sophisticated firmware design.

AW22127 is available in QFN4X4-24L package, it operates from 2.7V to 5.5V over -40℃ to +85℃.

## TYPICAL APPLICATION CIRCUIT

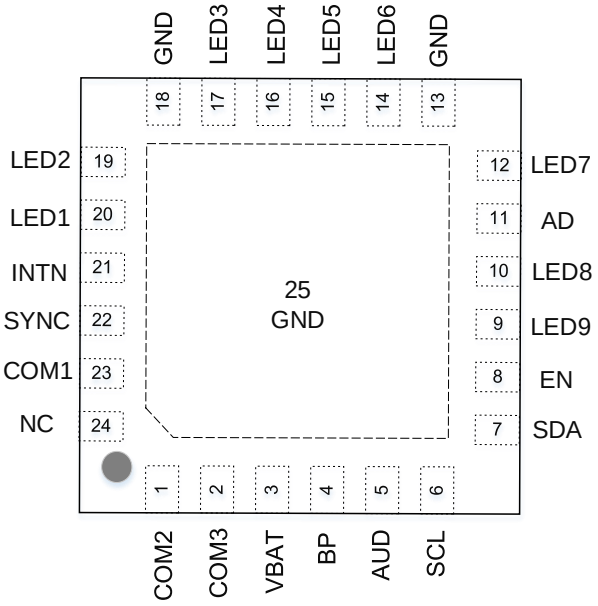




## PIN CONFIGURATION AND TOP MARK

**AW22127QNR Pin Configuration (Top View)**




**AW22127QNR Top Mark (Top View)**


AW22127 - Part Number
XXXX - Manufacture Tracking Code

**Figure 1** AW22127 Pin Configuration and Top Mark

## PIN DEFINITION

| Pin No | NAME | DESCRIPTION |
|---|---|---|
| 1 | COM2 | Current Switch connect to LED's anode in matrix display mode. |
| 2 | COM3 | Current Switch connect to LED's anode in matrix display mode. |
| 3 | VBAT | Power Supply (2.7V-5.5V). |
| 4 | BP | LDO output, externally connect 1uF bypass capacitor. |
| 5 | AUD | Audio in, ac-coupled input |
| 6 | SCL | Serial Clock Input for $I^2C$ Interface. |
| 7 | SDA | Serial Data I/O for $I^2C$ Interface. |
| 8 | EN | Enable pin. When tied to ground, the device is reset. Internally pulled down to GND with a resistor of 300kΩ. |
| 9 | LED9 | Constant Current Sink, connect to LED's cathode. |
| 10 | LED8 | Constant Current Sink, connect to LED's cathode. |
| 11 | AD | $I^2C$ address selection. Internally pull down to ground. |
| 12 | LED7 | Constant Current Sink, connect to LED's cathode. |
| 13,18 | GND | GND |

| | | |
|---|---|---|
| 14 | LED6 | Constant Current Sink, connect to LED's cathode. |
| 15 | LED5 | Constant Current Sink, connect to LED's cathode. |
| 16 | LED4 | Constant Current Sink, connect to LED's cathode. |
| 17 | LED3 | Constant Current Sink, connect to LED's cathode. |
| 19 | LED2 | Constant Current Sink, connect to LED's cathode. |
| 20 | LED1 | Constant Current Sink, connect to LED's cathode. |
| 21 | INTN | Interrupt pin, active low. |
| 22 | SYNC | Synchronize pin, used to synchronize clock in multiple AW22127 application. Should be floated if not used. |
| 23 | COM1 | Current Switch connect to LED's anode in matrix display mode. |
| 24 | NC | No Connect. |
| 25 | GND | Must be connected to GND. |

## FUNCTIONAL BLOCK DIAGRAM

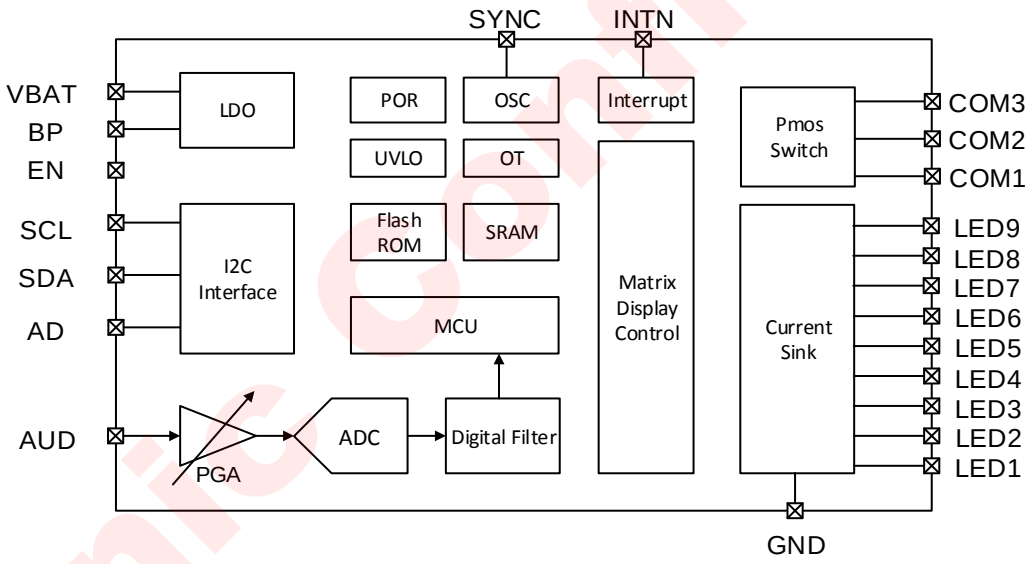



**Figure 2** Function Block



# TYPICAL APPLICATION CIRCUITS

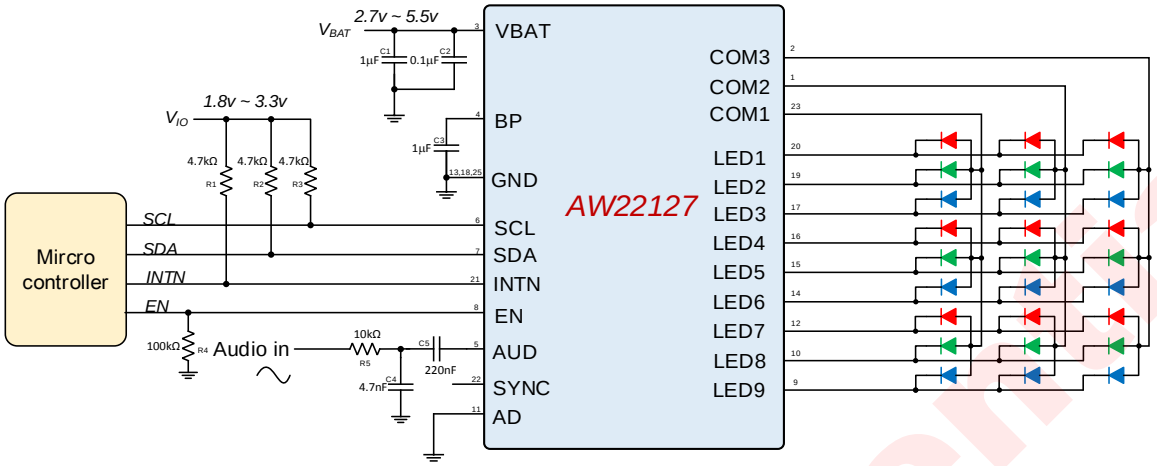



**Figure 3** Application of 9 RGB LED driven by single AW22127

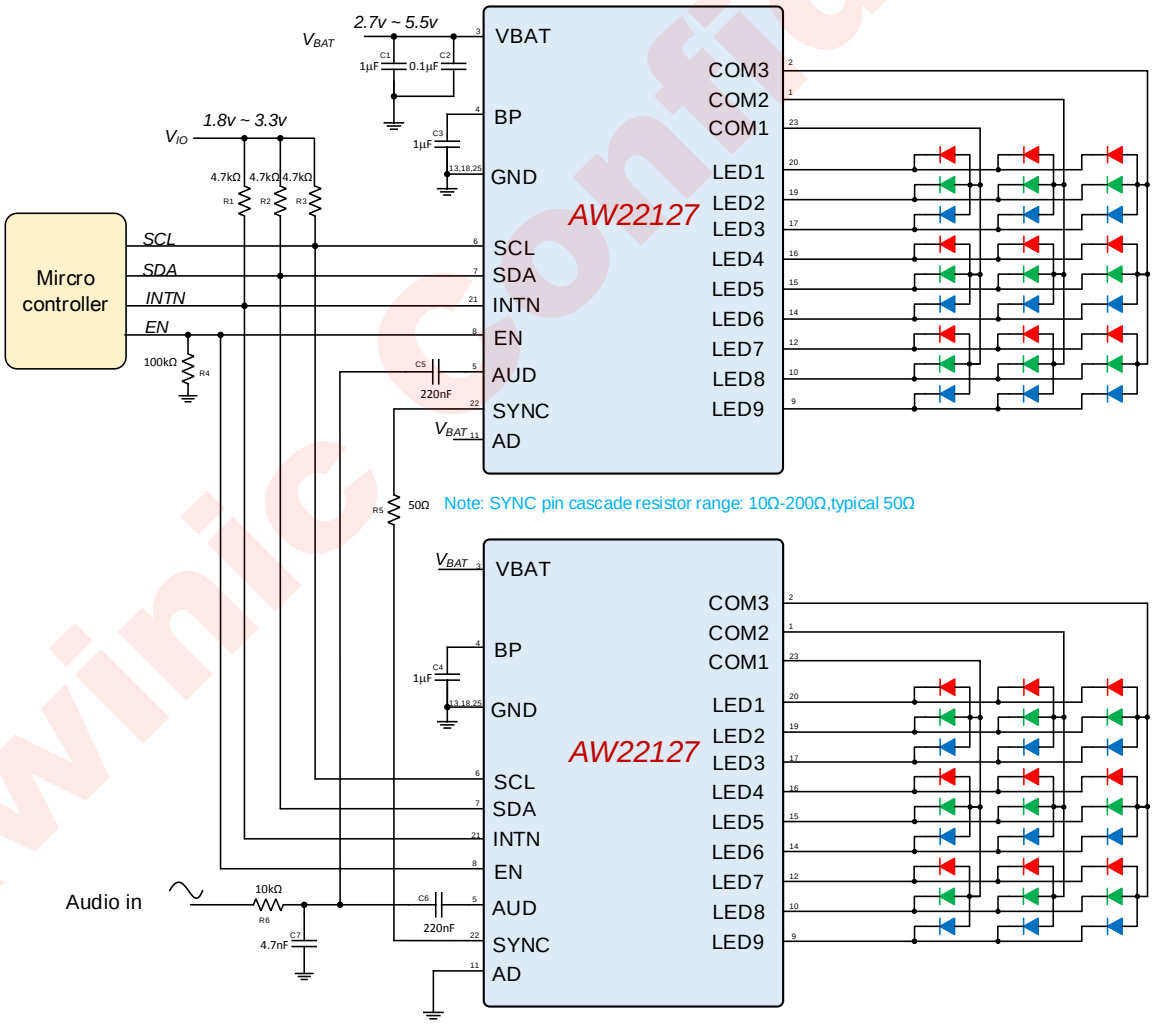
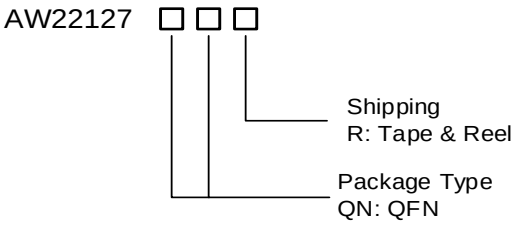



**Figure 4** Application of 18 RGB LEDs driven by dual AW22127

## ORDERING INFORMATION

| Part Number | Temperature | Package | Marking | Moisture Sensitivity Level | Environmental Information | Delivery Form |
|---|---|---|---|---|---|---|
| AW22127 QNR | -40℃ ~ 85℃ | QFN4X4-24L | AW22127 | MSL3 | ROHS+HF | 6000 units/ Tape and Reel |




## ABSOLUTE MAXIMUM RATINGS (NOTE 1)

| PARAMETERS | | RANGE |
|---|---|---|
| Supply voltage range $V_{BAT}$ | | -0.3V to 6.0V |
| Input voltage range | SCL, SDA,EN,AD | -0.3V to 6.0V |
| | LED1~LED9,COM1~COM3 | -0.3V to 6.0V |
| Output voltage range | SDA,INTN | -0.3V to 6.0V |
| Junction-to-ambient thermal resistance $\theta_{JA}$ | | 53℃/W |
| Operating free-air temperature range | | -40℃ to 85℃ |
| Maximum Junction temperature $T_{JMAX}$ | | 150℃ |
| Storage temperature $T_{STG}$ | | -65℃ to 150℃ |
| Lead Temperature (Soldering 10 Seconds) | | 260℃ |
| ESD(NOTE 2) | | |
| HBM | | ±2000V |
| MM | | ±200V |
| CDM | | ±2000V |
| Latch-up | | |
| Test Condition: JEDEC STANDARD NO.78E SEPTEMBER 2016 | | 350mA |

*NOTE1*: *Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.*

*NOTE2*: *The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: MIL-STD-883J Method 3015.9*

# ELECTRICAL CHARACTERISTICS

$V_{BAT}$=3.8V, $T_A$=25℃ for typical values (unless otherwise noted)

| Symbol | Description | Test Conditions | Min | Typ. | Max | Units |
|---|---|---|---|---|---|---|
| **Power Supply** | | | | | | |
| $V_{BAT}$ | Input operation voltage | | 2.7 | | 5.5 | V |
| $I_{SHUTDOWN}$ | Current in Shutdown mode | EN=0V | | | 1 | μA |
| $I_{STANDBY}$ | Current in Standby mode | EN=1.8V, GCR.CHIPEN=0 | | 7 | 15 | μA |
| $I_{ACTIVE}$ | Quiescent Current in Active mode | EN=1.8V ,GCR.CHIPEN= 1 MCU off, display off without LEDs | 0.4 | 0.6 | 1 | mA |
| | | EN=1.8V ,GCR.CHIPEN= 1 MCU off , display on without LEDs | 0.8 | 1.1 | 1.5 | mA |
| | | EN=1.8V ,GCR.CHIPEN= 1 MCU enable, display on without LEDs | 1.4 | 1.8 | 2.5 | mA |
| $V_{POR\_BAT}$ | POR voltage of VBAT | | | 1.75 | | V |
| $V_{POR\_LDO}$ | POR voltage of LDO | | | 1.0 | | V |
| $V_{UVLO}$ | UVLO voltage | Register UVTHR 0x10=0x03 (default) | -7% | 2.2 | +7% | V |
| $V_{UVLO\_HYS}$ | UVLO hysteresis | | | 0.1 | | V |
| $T_{OTP}$ | Over temperature protect | | | 150 | | ℃ |
| $T_{HYS}$ | OT hysteresis | | | 20 | | ℃ |
| $F_{OSC}$ | Oscillator Frequency | | -5% | 24.576 | +5% | MHz |
| **LED Driver** | | | | | | |
| $I_{LED}$ | Sink current of LEDx | IMAX=75mA,PWM=255, CURRENT=255 for LEDx | 0 | - | 75 | mA |
| $I_{ACC}$ | Current accuracy | $I_{LED}$=8~75mA | -10% | | +10% | % |
| | | $I_{LED}$=2~6mA | -15% | | +15% | % |
| $I_{MATCH}$ | Matching accuracy | $I_{LED}$=8~75mA | -10% | | +10% | % |



| | | | | | | |
|---|---|---|---|---|---|---|
| | | $I_{LED}$=2~6mA | -15% | | +15% | % |
| $V_{DROP1}$ | Dropout voltage for LEDx | $I_{LED}$=15mA | | 100 | 130 | mV |
| | | $I_{LED}$=20mA | | 130 | 160 | mV |
| | | $I_{LED}$=30mA | | 150 | 190 | mV |
| | | $I_{LED}$=75mA | | 250 | 320 | mV |
| $V_{DROP2}$ | Dropout voltage for COMx | $I_{LED}$=9*10=90mA | | 45 | 60 | mV |
| | | $I_{LED}$=9*20=180mA | | 90 | 120 | mV |
| | | $I_{LED}$=9*75=675mA | | 350 | 420 | mV |
| $F_{PWM}$ | PWM frequency | Register PWM_FREQ=0, Matrix mode, 3 COM ports | -5% | 375 | +5% | Hz |
| **Digital Logical Interface** | | | | | | |
| $V_{IL}$ | Logic input low level | AD,EN,SDA,SCL,SYNC | | | 0.4 | V |
| $V_{IH}$ | Logic input high level | AD,EN,SDA,SCL,SYNC | 1.3 | | | V |
| $I_{IL}$ | Low level input current | SDA,SCL,SYNC | | 5 | | nA |
| $I_{IH}$ | High level input current | SDA,SCL,SYNC | | 5 | | nA |
| $V_{OL}$ | Logic output low level | SDA,INTN, $I_{OUT}$=3mA | | | 0.4 | V |
| $I_L$ | Output leakage current | SDA ,INTN open drain | | | 1 | nA |



## I²C INTERFACE TIMING

| Parameter Name | | | Min | Typ. | Max | Units |
|---|---|---|---|---|---|---|
| $F_{SCL}$ | Interface Clock frequency | | | | 400 | kHz |
| $T_{DEGLITCH}$ | Deglitch time | SCL | | 200 | | ns |
| | | SDA | | 250 | | ns |
| $T_{HD:STA}$ | (Repeat-start) Start condition hold time | | 0.6 | | | μs |
| $T_{LOW}$ | Low level width of SCL | | 1.3 | | | μs |
| $T_{HIGH}$ | High level width of SCL | | 0.6 | | | μs |
| $T_{SU:STA}$ | (Repeat-start) Start condition setup time | | 0.6 | | | μs |
| $T_{HD:DAT}$ | Data hold time | | 0 | | | μs |
| $T_{SU:DAT}$ | Data setup time | | 0.1 | | | μs |
| $T_R$ | Rising time of SDA and SCL | | | | 0.3 | μs |
| $T_F$ | Falling time of SDA and SCL | | | | 0.3 | μs |
| $T_{SU:STO}$ | Stop condition setup time | | 0.6 | | | μs |
| $T_{BUF}$ | Time between start and stop condition | | 1.3 | | | μs |

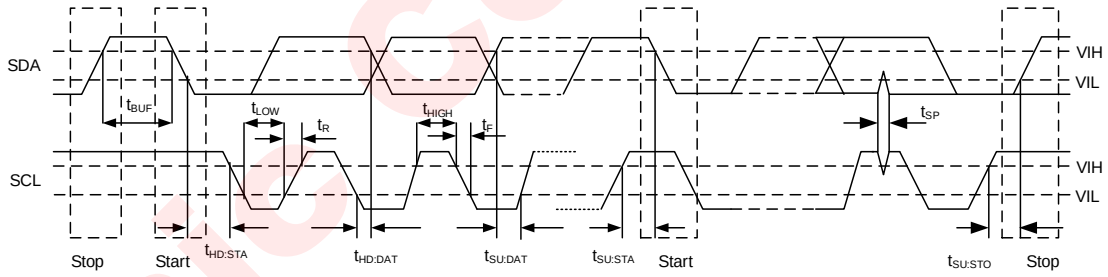



**Figure 5** I²C Timing Parameters



# FUNCTIONAL DESCRIPTION

## POWER-ON-RESET

Upon initial power-up, the AW22127 is reset by internal power-on-reset, and all register are reset to default value, and LED driver is shut down.

Once the supply voltage VBAT drops below the threshold voltage $V_{POR\_VBAT}$ (1.75V), or the LDO output voltage is below $V_{POR\_LDO}$ (1.0V), the power-on-reset will be activated to reset the device again.

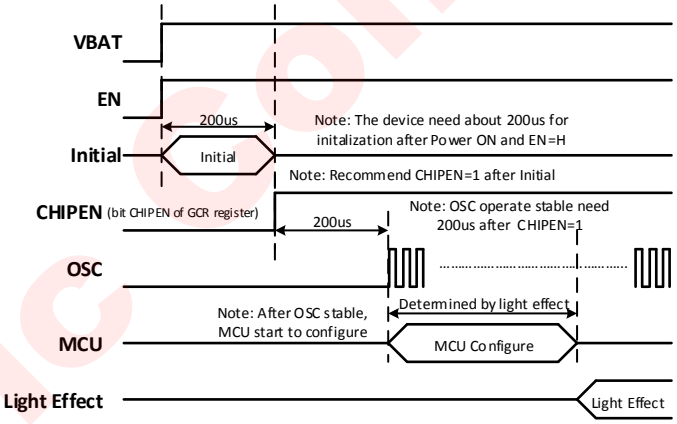
## OPERATING MODE

After power-up, if external pin EN is low, the device keeps in shut-down state. In shut-down state, all internal circuit do not work, $I^2C$ interface is closed and the power current consumption is very low ( <1μA).

If pin EN is pulled high, the device enters stand-by state. In Standby state, only part of the internal circuit can work: the LDO works in low-power mode, the OSC still keeps closed, and $I^2C$ interface is opened. The current consumption in stand-by state is less than 10μA. When bit CHIPEN of GCR register is set to 1 in standby mode, AW22127 enters into active mode.

In active state, the internal LDO switch to full-load mode, and the OSC starts to work to provide stable clock signal. User can configure the device via $I^2C$ interface, invoke MCU to run specified pre-loaded MCU program to produce expected lighting effect.

Below is the recommended operation timing:




In **active** state, If register GCR.CHIPEN is set to 0, the device return to standby state, and all LED drive will be turn off.

## SOFTWARE RESET

Writing 0x55 to register SRSTR (register: 0x01) via $I^2C$ interface will reset the device, including all internal circuits and configuration registers. After the software reset command is input through I2C, it needs to wait at least 2ms before any other I2C command can be accepted.

## UNDER VOLTAGE LOCK OUT (UVLO)

The voltage on pin VBAT is monitored internally by the AW22127. When voltage of VBAT drops below

predefined threshold (2.2v typically, register UVTHR configurable, address 0x10), the bit UIS is set to 1 in ISR register (address 0x0A). After a read, the register ISR can be cleared.
If both bit UVME and UVLOE in register GCR (address 0x02) are set, when UVLO condition is met, the bit CHIPEN in register GCR will be cleared, all current lighting effect is halted, and the device will be forced to standby state.
The bit UVLME enables or disables UVLO monitor, the bit UVLOE control the protection function of UVLO turn on or off. By default, both bits are 0, both UVLO monitor and protection are switched off.

## OVER TEMPERATURE PROTECTION

When the device reaches 150℃, the over-temperature protection be activated, and the bit OIS is set to "1" in register ISR (address 0x0A), and after a read, the register ISR can be cleared. The bit OTMD and bit OTPD in register GCR (address 0x02) control OT monitor and OTP protection function enabled and disabled respectively. By default, both OT monitor and OTP protection are enabled.
When Over Temperature (OT) condition is met and OTP is enabled, the bit CHIPEN in register GCR will be cleared, all current lighting effect is halted, and the device will be forced to standby state.

## INTERRUPT

Interrupt function is provided on pin INTN. When interrupt status is set in register ISR and corresponding interrupt enable bit is set, interrupt occurs.
There are two kind of interrupt mode: Level mode and Pulse mode.
If bit INTMD in register ICR (address 0x08) is 0, Level mode is active, and INTN is pulled low when interrupt takes place, it will keeps until register ISR is read via $I^2C$ interface.
If bit INTMD is set, Pulse mode is active, pin INTN outputs a negative pulse when interrupt occurs. The width of pulse is configured by bits INTWTH in register ICR.
In AW22127, there are 8 interrupt sources, they are all enabled or disabled by register IER (address 0x09).

## $I^2C$ INTERFACE

AW22127 supports the I²C serial bus and data transmission protocol in fast mode at 400kHz. AW22127 operates as a slave on the I²C bus. Connections to the bus are made via the open-drain I/O pins SCL and SDA. The pull-up resistor can be selected in the range of 1k~10kΩ and the typical value is 4.7kΩ. AW22127 can support different high level (1.8V~3.3V) of this $I^2C$ interface.

### *DEVICE ADDRESS*

The $I^2C$ device address (7-bit) of AW22127 is 0x6A (pin AD is low) or 0x6B (pin AD is high), followed by the R/W bit (Read=1/Write=0).

### *DATA VALIDATION*

When SCL is high level, SDA level must be constant. SDA can be changed only when SCL is low level.

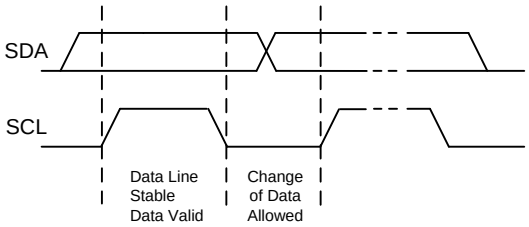



**Figure 6** Data Validation Diagram

### *I²C START/STOP*

I²C start: SDA changes from high level to low level when SCL is high level.

I²C stop: SDA changes from low level to high level when SCL is high level.

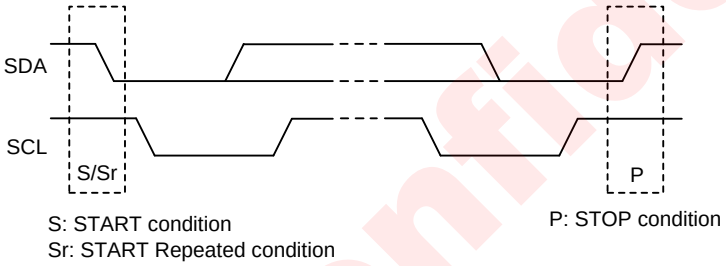



**Figure 7** I²C Start/Stop Condition Timing

### *ACK (ACKNOWLEDGEMENT)*

ACK means the successful transfer of I²C bus data. After master sends 8bits data, SDA must be released; SDA is pulled to GND by slave device when slave acknowledges.
When master reads, slave device sends 8bit data, releases the SDA and waits for ACK from master. If ACK is send and I²C stop is not send by master, slave device sends the next data. If ACK is not send by master, slave device stops to send data and waits for I²C stop.

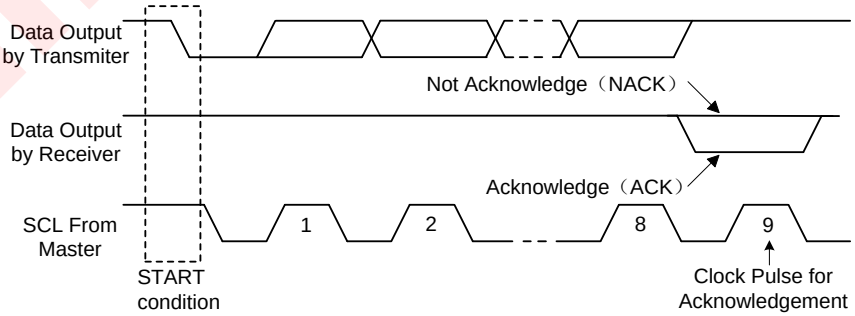



**Figure 8** I²C ACK Timing

***WRITE CYCLE***

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol allows a single data line to transfer both command/control information and data using the synchronous serial clock.
Each data transaction is composed of a Start Condition, a number of byte transfers (set by the software) and a Stop Condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow.
In a write process, the following steps should be followed:

1) Master device generates START condition. The "START" signal is generated by lowering the SDA signal while the SCL signal is high.
2) Master device sends slave address (7-bit) and the data direction bit (R/W = 0).
3) Slave device sends acknowledge signal if the slave address is correct.
4) Master sends control register address (8-bit)
5) Slave sends acknowledge signal
6) Master sends data byte to be written to the addressed register
7) Slave sends acknowledge signal
8) If master will send further data bytes the control register address will be incremented by one after acknowledge signal (repeat step 6,7)
9) Master generates STOP condition to indicate write cycle end

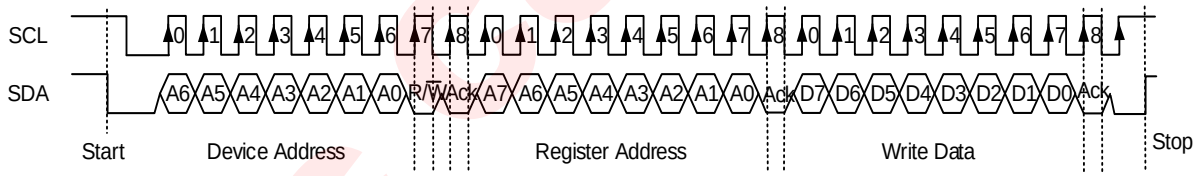



**Figure 9** I²C Write Byte Cycle

***READ CYCLE***

In a read cycle, the following steps should be followed:

1) Master device generates START condition
2) Master device sends slave address (7-bit) and the data direction bit (R/W = 0).
3) Slave device sends acknowledge signal if the slave address is correct.
4) Master sends control register address (8-bit)
5) Slave sends acknowledge signal
6) Master generates STOP condition followed with START condition or REPEAT START condition
7) Master device sends slave address (7-bit) and the data direction bit (R/W = 1).
8) Slave device sends acknowledge signal if the slave address is correct.

9) Slave sends data byte from addressed register.

10) If the master device sends acknowledge signal, the slave device will increase the control register address by one, then send the next data from the new addressed register.

11) If the master device generates STOP condition, the read cycle is ended.

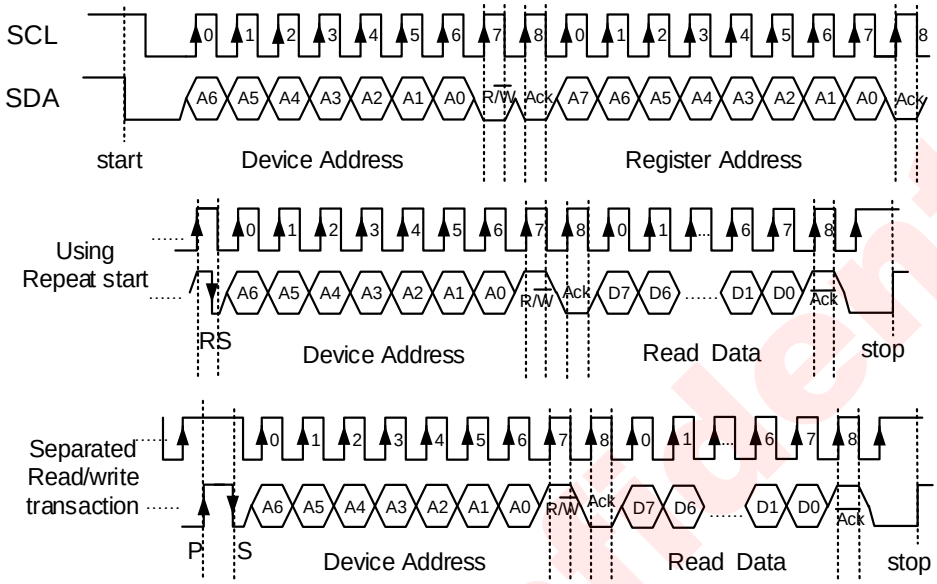



**Figure 10** I²C Read Byte Cycle

## MCU AND PROGRAM CONTROL

AW22127 integrated an 8bit MCU, 18kB Flash ROM and 1kB SRAM. Along with these peripherals such as timer, watchdog, audio sample/process module, LED matrix display control module, a flexible, powerful and LED application-oriented system-on-chip (SoC) platform is built. Upon the SoC platform, all lighting effect are implement by MCU, user can design different firmware program according to different application.

Via I²C interface, external controller can download or update new firmware into internal Flash ROM, and control embedded MCU to execute or stop certain functional program conveniently by send task message to register TASK0 and TASK1 (address 0x05,0x06).

By default, the operating frequency of MCU is 24.576MHz, which can be configured via bits FREQ[3:0] in register CLKCR (address 0x03), the lowest frequency is 1.024MHz. The lower the operating frequency, the less the power consumption by MCU.

## LED MATRIX CONTROL MODULE

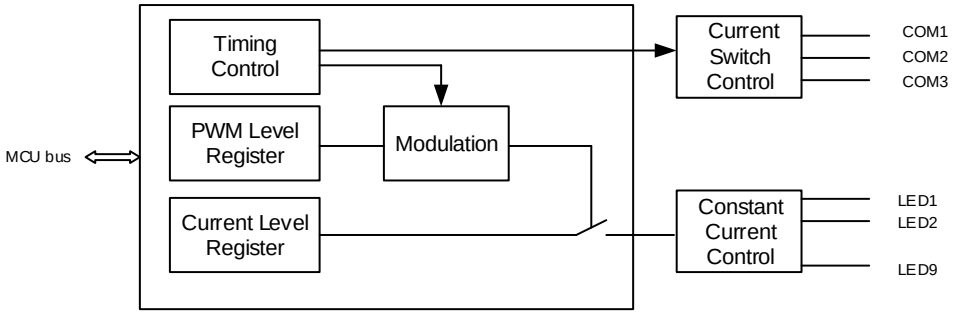



**Figure 11** LED Matrix Display Control Module

There are 9 constant current sink (LED1~ LED9) and 3 current switches (COM1~COM3). In matrix display mode, the device can drive 27 single-color LEDs or 9 RGB LED.

Each LEDx has 256 steps of constant current and 12 bit/4096 levels PWM duty cycle controlled by MCU, 3 COM pins are also controlled by MCU to drive PMOS current switches in time-division mode. In matrix display mode, MCU updates the current, PWM level for each LED periodically, and switches on COM1, COM2, COM3 in turn to generate animation lighting effect.

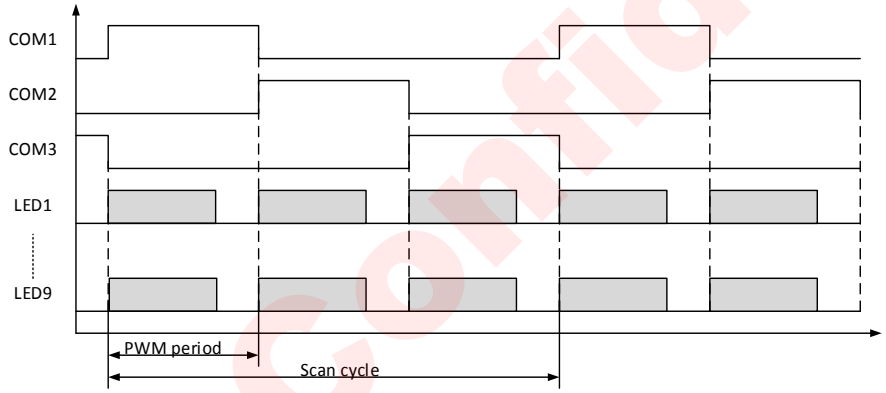



**Figure 12** Scan Timing in Matrix Display Mode

### *LED CURRENT*

Globally, the maximum output current ($I_{MAX}$) for all LEDs is set by register IMAX （address 0x0b）, which only can be set via $I^2C$ interface. The 4 bit max current option provides 16 level current adjustment from 2mA to 75mA (refer to register description of IMAX)

Individual LED is 8bit /256 steps of current selectable, which only can be set by internal MCU according to dedicated lighting effect program in firmware. In RGB application, different current level for R,G and B LED can form to different color mixed, so totally 256x256x256 color-mixing schemes is available.

If the max output current is $I_{MAX}$, and 8bit current level is $M_{SET}$ for LEDx, the practical constant current $I_{OX}$ for LEDx could be denoted as:

$$I_{OX} = I_{MAX} * M_{SET}/255 \ (M_{SET} = 0\sim255)$$

### *PWM DIMMING CONTROL*

Besides of 256 steps of constant current for individual LED, 12bit/4096 levels of PWM is provided for each LED.

The frequency of PWM modulation only can be set by MCU. Every PWM period, and internal interrupt is generated to inform MCU to update the value of current and PWM for each LED as well as change active current switch among 3 COM pin.

Generally, PWM level is used for dimming adjustment, the ramp curve of PWM transition can be arbitrarily set by firmware program in AW22127. Usually exponential curve is applied, different transition curve create different blinking or breathe lighting effect.

## AUDIO SAMPLE AND PROCESS

When bit AUDE in register AUDCTR (address 0x0C) is set, the integrated audio process block is enabled, which contains a programmable-gain amplifier (PGA), an 8-bit ADC and a digital process module.

The block diagram of audio sample and process path is shown in the figure below.

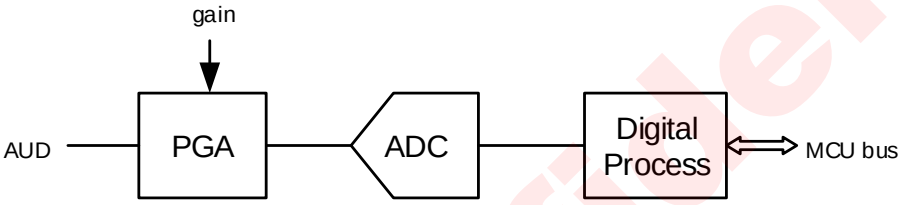



**Figure 13** Audio sample and process path

The analogue audio signal is AC-coupled to pin AUD with an external DC blocking capacitor, and then amplified by PGA. An 8bit ADC converted amplified analog signal to digital code, and then sent to digital process block for filter and analysis. The output of digital process block can be accessed by MCU for further processing for lighting effect generation.

The common mode voltage of PGA is 1.0V, and the input voltage range on pin AUD is 0V to 2.0 V.

The PGA gain is set by an internal 6bit register that is only controlled by MCU, the adjustable range of gain is from -12 dB to +51dB, 1dB/Step. Auto-gain-control (AGC) function is implemented by software algorithm, which adjust gain setting in real-time according to the calculation results of input signal's peak and power.

The sampling rate of ADC is also set by MCU. After a sample obtained, an external interrupt request will be sent to MCU, and MCU responses to this interrupt and read back the sampled data for further process.

The audio synchronized lighting effect is determined by software completely. User can flexibly design program, modify not only current (color) but PWM level (brightness) also to achieve attractive effect.

## FIRMWARE PROGRAM

In the AW22127, the user-programmable Flash ROM space is 17.5kB, which is divided into two area: the main array area (16kB) and the sub-array area (1.5kB). The address of the two area are continuous, and both can be used to store user program. The Flash ROM can be erased, burned, and verified through the $I^2C$ interface.

The main array area supports chip erase and sector (512Byte) erase, while the sub-array area only supports sector erase. Flash erase is the process of changing the storage content from 0 to 1. Programming can only burn flash data from 1 to 0, but not from 0 to 1. Before flash programming, it must be erased first.

The AW22127 supports two programming modes: single-byte programming and sequential multi-byte programming. The single-byte programming mode does not require I²C interface rate, both 100kHz and 400kHz rate are permitted. As the Flash ROM limits the maximum programming accumulation time allowed on the same row, the sequential multi-byte programming mode only can be adopted in 400kHz I²C interface. In application of 100kHz I²C interface only single byte programming mode are recommended.

The following diagrams show the I²C operating flow for different programming modes.

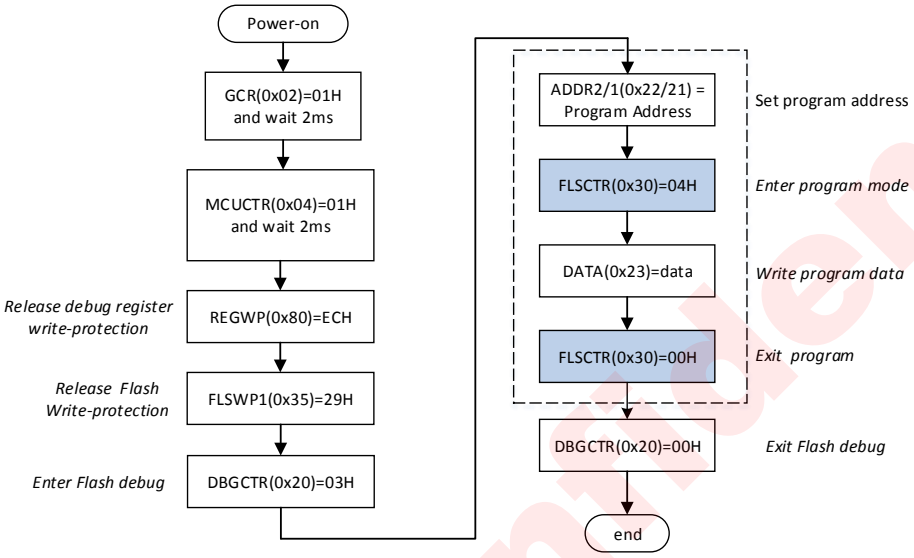



**Figure 14** Single byte programming through 100k/400kHz I²C interface

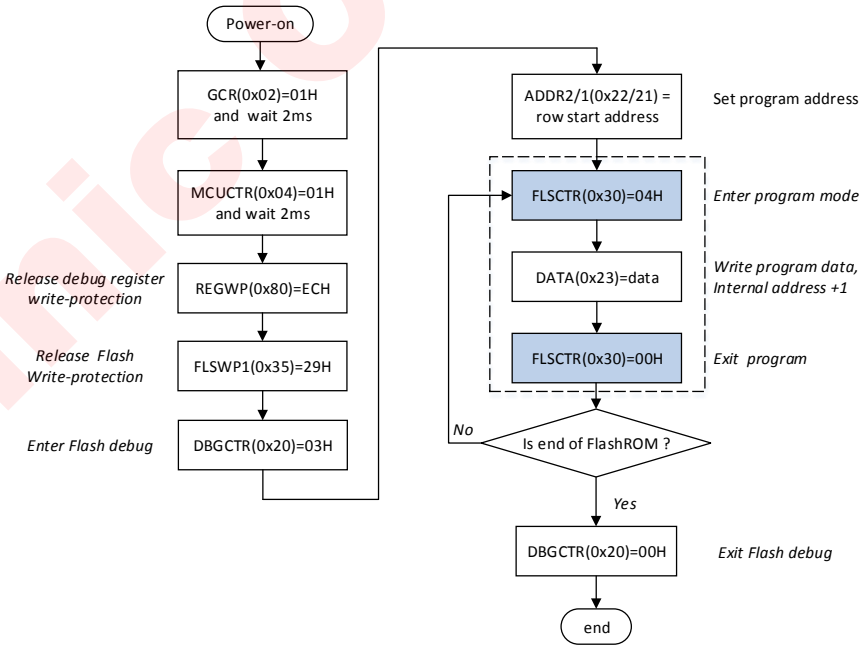



**Figure 15** Continuous single-byte programming through 100kHz/400kHz I²C interface

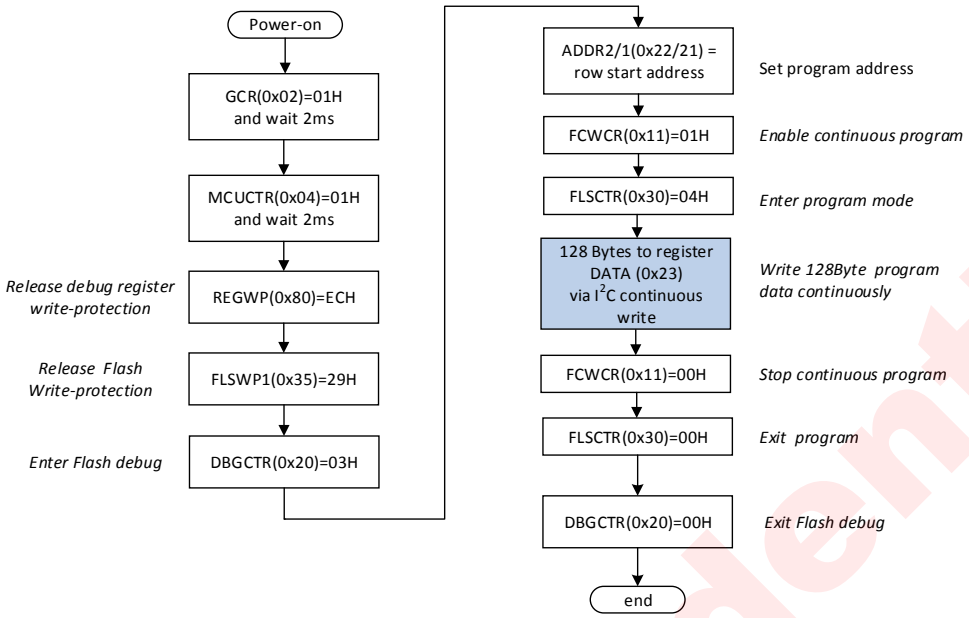



**Figure 16** Sequential 128-bytes programming through 400kHz I$^2$C interface

**Note:**

Due to the strict timing requirements of Flash ROM operation, incorrect operation may results in flash data errors. For detailed firmware programming guide, please contact AWINIC's FAE or refer to document: "**Application note: AW22127/AW22118 FlashROM Program Guide**".



## REGISTER DESCRIPTION

### *REGISTER LIST*

| Addr. | Name | W/R | Function description |
|---|---|---|---|
| 00H | IDR | R | Device ID register |
| 01H | SRSTR | R/W | Software reset control register |
| 02H | GCR | R/W | Global control register |
| 03H | CLKCFG | R/W | clock configuration register |
| 04H | MCTR | R/W | MCU control register |
| 05H | TASK0 | R/W | MCU Task setting register 0 |
| 06H | TASK1 | R/W | MCU Task setting register 1 |
| 07H | PST | R | MCU program status register |
| 08H | ICR | R/W | Interrupt configuration regiser |
| 09H | IER | R/W | Interrupt enable register |
| 0AH | ISR | R | Interrupt status register |
| 0BH | IMAX | R/W | Global max output current for all LED pin |
| 0CH | AUDCTR | R/W | Audio path control register |
| 0DH | PIGR | R/W | PGA initial gain setting register |
| 0EH | PRGR | R | PGA real time gain register |
| 0FH | UVCR | R/W | UVLO detection configuration register |
| 10H | UVTHR | R/W | UVLO detection threshold register |

### *REGISTER BIT MAP*

| Addr | Name | W/R | Bit7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 00H | IDR | RO | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 01H | SRSTR | R/W | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 02H | GCR | R/W | ADPDD | ENPDD | OTMD | OTPD | UVME | UVLOE | OSCDIS | CHIPEN |
| 03H | CLKCR | R/W | LOCS | LOCPD | CLKSEL | | FREQ | | | |
| 04H | MCTR | R/W | - | - | - | - | - | MWE | MRST | ME |
| 05H | TASK0 | R/W | TASK0 | | | | | | | |
| 06H | TASK1 | R/W | TASK1 | | | | | | | |
| 07H | PST | RO | PST | | | | | | | |
| 08H | ICR | R/W | INTWTH | | | | | | | INTMD |
| 09H | IER | R/W | LIE | UIE | OIE | WDIE | SIE3 | SIE2 | SIE1 | SIE0 |
| 0AH | ISR | RO | LIS | UIS | OIS | WDIS | SIS3 | SIS2 | SIS1 | SIS0 |
| 0BH | IMAX | R/W | - | - | - | - | IMAX | | | |
| 0CH | AUDCTR | R/W | - | - | - | - | PRCHG | PGABP | AGCE | AUDE |
| 0DH | PIGR | R/W | | | IGAIN | | | | | |
| 0EH | PRGR | R | | | RGAIN | | | | | |

| Addr | Name | W/R | Bit7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0FH | UVCR | R/W | - | - | DEGTIM | | | | | |
| 10H | UVTHR | R/W | - | - | - | - | - | UVTH | | |

## *DETAILED REGISTER DESCRIPTION*

### *IDR, Chip ID Register*

Address: 0x00, RO, default: 0x27

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

| Bit | Symbol | Description |
|---|---|---|
| 7:0 | IDR | Chip ID, read out is 0x27 for AW22127 |

### *SRSTR, Software Reset Register*

Address: 0x01, R/W, default: 0x76

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

| Bit | Symbol | Description |
|---|---|---|
| 7:0 | IDR | Writing 0x55 to this register will cause reset for this device, including internal logic and configuration register.<br>Read out value is always 0x76 |

### *GCR, Global Control Register*

Address: 0x02, R/W, default: 0x00

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ADPDD | ENPDD | OTMD | OTPD | UVME | UVLOE | OSCDIS | CHIPEN |

| Bit | Symbol | Description |
|---|---|---|
| 7 | ADPDD | Disable internal pulled down resistor of pin AD<br>0: enable pulled-down resistor **(default)**<br>1: disable pulled-down resistor |
| 6 | ENPDD | Disable internal pulled down resistor of pin EN<br>0: enable pulled-down resistor **(default)**<br>1: disable pulled-down resistor |
| 5 | OTMD | Over Temperature monitor disable<br>0: OT monitor enabled **(default)**<br>1: OT monitor disabled. |
| 4 | OTPD | Over Temperature Protection disable control<br>0: enable OTP, clear CHIPEN bit when over-temperature condition is met **(default)**<br>1: disable OTP |
| 3 | UVME | UVLO monitor enable<br>0: enable UVLO monitor **(default)**<br>1: disable UVLO monitor |
| 2 | UVLOE | UVLO protect enable<br>0: enable UVLO protection **(default)**<br>1: disable UVLO protection, clear CHIPEN when UVLO fault is detected. |

| | | |
|---|---|---|
| 1 | OSCDIS | Internal OSC disable control.<br>0: enable **(default)**<br>1: disable |
| 0 | CHIPEN | Device operating Enable<br>0: Disable, the device is in standby state, only $I^2C$ interface is active to keep low power state. **(default)**<br>1: Enable, the device enters active state |

***CLKCR, Clock Configuration Register***

Address: 0x03, W/R, default: 0x00

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| LOCS | LOCPD | CLKSEL | | FREQ | | | |

| Bit | Symbol | Description |
|---|---|---|
| 7 | LOCS | Read only. Loss of Clock status on pin SYNC. LOC detection is only useful in the case of clock being provided from pin SYNC.<br>0: clock input exist<br>1: Loss of Clock Input is detected |
| 6 | LOCPD | Disable protection when external input clock loss is detected<br>0: Enable protection. LED output close when loss of external clock input<br>1: Disable protection. |
| 5:4 | CLKSEL | Internal Clock Source Selection and Output Control<br>00: use internal OSC, and pin SYNC output hi-Z<br>01: use internal OSC and output it to pin SYNC<br>1x: use external input clock from of pin SYNC |
| 3:0 | FREQ | Internal master clock frequency setting<br>0: 24.576MHz (default) 4: 4.096MHz<br>1:12.288 MHz 5: 2.048MHz<br>2: 8.192 MHz 6: 1.024MHz<br>3: 6.144MHz 7: 12.288MHz |

***MCTR, MCU Control Register***

Address: 0x04, W/R, default: 0x00

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| - | - | - | - | - | MWE | MRST | ME |

| Bit | Symbol | Description |
|---|---|---|
| 2 | MWE | MCU Wake Up Enable<br>0: No operation (default)<br>1: Send external to internal MCU to resume program execution |
| 1 | MRST | MCU Reset control<br>0: MCU reset (default)<br>1: MCU no reset |
| 0 | ME | MCU Work Enable<br>0: MCU disabled, no clock send to internal MCU<br>1: MCU enabled |

***TASK0,Task Register0***

Address: 0x05, R/W, default: 0x00

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| TASK0 | | | | | | | |

| Bit | Symbol | Description |
|---|---|---|
| 7:0 | TASK0 | MCU Task Code 0. Internal MCU can read this register to decide which function to execute. Before MCU operates, user should configure this register first, and then start up MCU. |

***TASK1,Task Register1***

Address: 0x06, R/W, default: 0x00

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| TASK1 | | | | | | | |

| Bit | Symbol | Description |
|---|---|---|
| 7:0 | TASK1 | MCU Task Code 1, Its function is similar to register TASK0. |

***PST, MCU Program Execution Status Register***

Address: 0x07, RO, default: 0x00

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PST | | | | | | | |

| Bit | Symbol | Description |
|---|---|---|
| 7:0 | PST | Program Execution Status Code, which is written by internal MCU.<br>0x00: No program is executing<br>0x01: Sleep<br>0x02: IDLE<br>0x10: Breathe Lighting mode is running<br>0x11: Breathe Lighting has finished<br>0x20: Audio sync. Mode is running<br>0x21: Audio sync. Mode has finished.<br>…… |

***ICR, Interrupt Configuration Register***

Address: 0x08, R/W, default: 0x00

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| INTWTH | | | | | | | INTMD |

| Bit | Symbol | Description |
|---|---|---|
| 7:1 | INTWTH | Pulse Width Setting, only used in pulse interrupt mode (INTMD=1)<br>Width = INTWTH +1 (μs) |
| 0 | INTMD | Interrupt Output Mode Selection<br>0: Level mode, pin INTN output low when interrupt occurs<br>1: Pulse mode, pin INTN output negative pulse when interrupt occurs |



***IER, Interrupt Enable Register***

Address: 0x09, R/W, default: 0x00

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| LIE | UIE | OIE | WDIE | SIE3 | SIE2 | SIE1 | SIE0 |

| Bit | Symbol | Description |
|---|---|---|
| 7 | LIE | Loss of Clock (LOC) Fault Interrupt Enable<br>0: Disable (default)<br>1: Enable |
| 6 | UIE | UVLO Fault Interrupt Enable<br>0: Disable (default)<br>1: Enable |
| 5 | OIE | Over Temperature Fault Interrupt Enable<br>0: Disable (default)<br>1: Enable |
| 4 | WDIE | Watch Dog Fault Interrupt Enable.<br>0: Disable (default)<br>1: Enable |
| 3 | SIE3 | Firmware Version Detect Error Interrupt Enable<br>0: Disable (default)<br>1: Enable |
| 2 | SIE2 | Flash-ROM Correction Failure Interrupt Enable<br>0: Disable (default)<br>1: Enable |
| 1 | SIE1 | MCU Check Failure Interrupt Enable<br>0: Disable (default)<br>1: Enable |
| 0 | SIE0 | Functional Program Complete Interrupt Enable<br>0: Disable (default)<br>1: Enable |

***ISR, Interrupt Status Register***

Address: 0x0A, RO, default: 0x00

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| LIS | UIS | OIS | WDIS | SIS3 | SIS2 | SIS1 | SIS0 |

| Bit | Symbol | Description |
|---|---|---|
| 7 | LIS | Loss of Clock (LOC) Fault Interrupt Status<br>0: No interrupt<br>1: Interrupt |
| 6 | UIS | UVLO Fault Interrupt Enable<br>0: No interrupt<br>1: Interrupt |
| 5 | OIS | Over Temperature Fault Interrupt Status |



0: No interrupt
1: Interrupt

| | | |
|---|---|---|
| 4 | WDIS | Watch Dog Fault Interrupt Status.<br>0: No interrupt<br>1: Interrupt |
| 3 | SIS3 | Firmware Version Detect Error Interrupt Status<br>0: No interrupt<br>1: Interrupt |
| 2 | SIS2 | Flash-ROM Correction Failure Interrupt Status<br>0: No interrupt<br>1: Interrupt |
| 1 | SIS1 | MCU Check Failure Interrupt Status<br>0: No interrupt<br>1: Interrupt |
| 0 | SIS0 | Functional Program Complete Interrupt Status<br>0: No interrupt<br>1: Interrupt |

***IMAX, LED Max Current Configuration Register***

Address: 0x0B, R/W, default: 0x00

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| - | - | - | - | IMAX | | | |

| Bit | Symbol | Description |
|---|---|---|
| 7:4 | - | Reserved, should be kept as 0000. |
| 3:0 | IMAX | Max Constant Current Configuration for pin LED1~LED9<br>0000: 3mA 1000: 2mA<br>0001: 6mA 1001: 4mA<br>0010: 9mA 1010: 6mA<br>0011: 15mA 1011: 10mA<br>0100: 30mA 1100: 20mA<br>0101: 45mA 1101: 30mA<br>0110: 60mA 1110: 40mA<br>0111: 75mA 1111: 50mA |

***AUDCTR, Audio Path Control Register***

Address: 0x0C, R/W, default:0x00

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| - | - | - | - | PRCHG | PGABP | AGCE | AUDE |

| Bit | Symbol | Description |
|---|---|---|
| 7:4 | - | Reserved |
| 3 | PRCHG | ADC Pre-charge Enable<br>0: Disable (default)<br>1: Enable |

| | | |
|---|---|---|
| 2 | PGABP | PGA Bypass Control, only used in test.<br>0: ADC source from PGA (default)<br>1: ADC source from pin AUD directly |
| 1 | AGCE | AGC enable<br>0: Disable (default)<br>1: Enable |
| 0 | AUDE | Audio Synchronization Function Enable<br>0: Disable, reset all audio process relative module<br>1: Enable |

***PIGR, PGA Initial Gain Configuration Register***

Address: 0x0D, R/W, default: 0x00

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| - | - | IGAIN | | | | | |

| Bit | Symbol | Description |
|---|---|---|
| 7:6 | - | non-defined |
| 5:0 | IGAIN | PGA Initial Gain Setting.<br>PGA Gain = IGAIN -12dB<br>000000: -12 dB<br>000001: -11 dB<br>……<br>001100: 0 dB<br>001101: +1 dB<br>……<br>111111: +51dB |

***PRGR, PGA Real Gain Register***

Address: 0x0E, RO, default: 0x00

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| - | - | RGAIN | | | | | |

| Bit | Symbol | Description |
|---|---|---|
| 7:6 | - | non-defined |
| 5:0 | RGAIN | PGA Real Gain. Real gain of PGA is adjusted by internal MCU according to audio signal from pin AUD. |

***UVCR, UVLO Detection Configuration Register***

Address: 0x0F, R/W, default: 0x0F

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| - | - | DEGTIM | | | | | |

| Bit | Symbol | Description |
|---|---|---|
| 5:0 | DEGTIM | Ultra-Low Voltage Lock (UVLO) Detection De-bounce Time Setting.<br>De-bounce time = DEGTIM *16μs |



***UVTHR, UVLO Detection Threshold Register***

Address: 0x10, R/W, default: 0x03

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| - | - | - | - | - | UVTH | | |

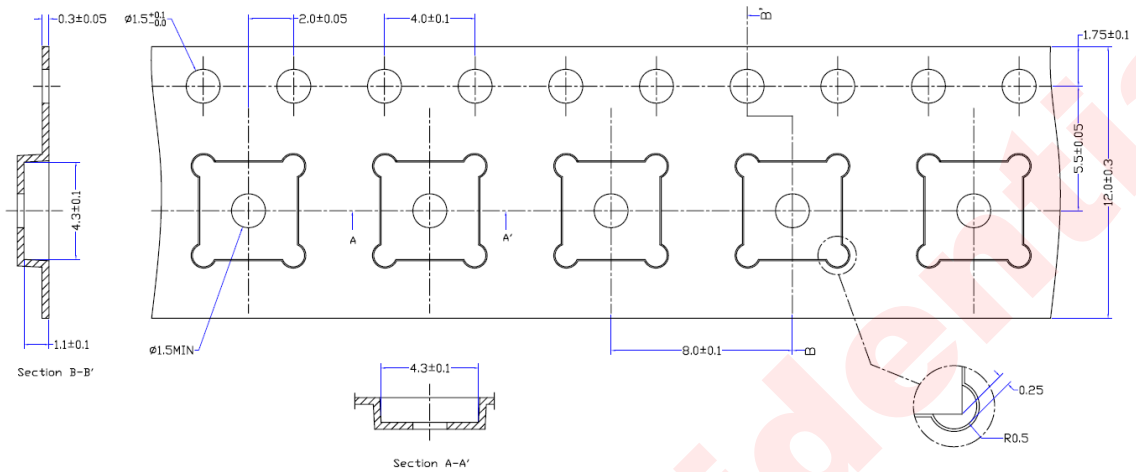
| Bit | Symbol | Description |
|---|---|---|
| 2:0 | UVTH | UVLO Detection Voltage Threshold.<br>000: 1.9v<br>001: 2.0v<br>010: 2.1v<br>011: 2.2v (default)<br>100: 2.3v<br>101: 2.4v<br>110: 2.5v<br>111: 2.6v |



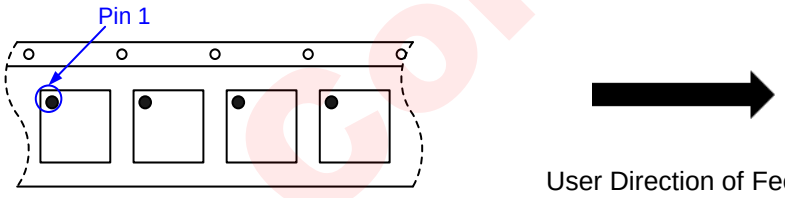
# TAPE AND REEL INFORMATION

## CARRIER TAPE (QFN4X4-24L)




NOTE: ALL DIMS IN mm.

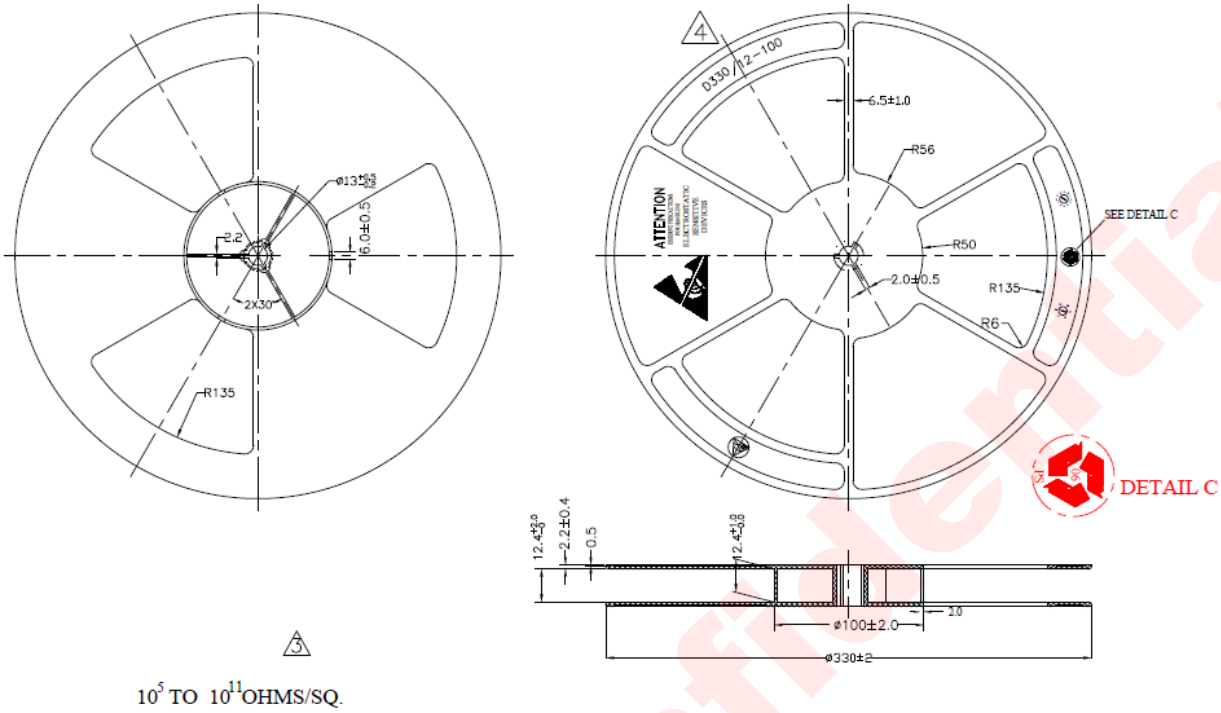
## Pin 1 direction





## REEL (QFN4X4-24L)




NOTE:

1、 ALL DIMS IN mm;

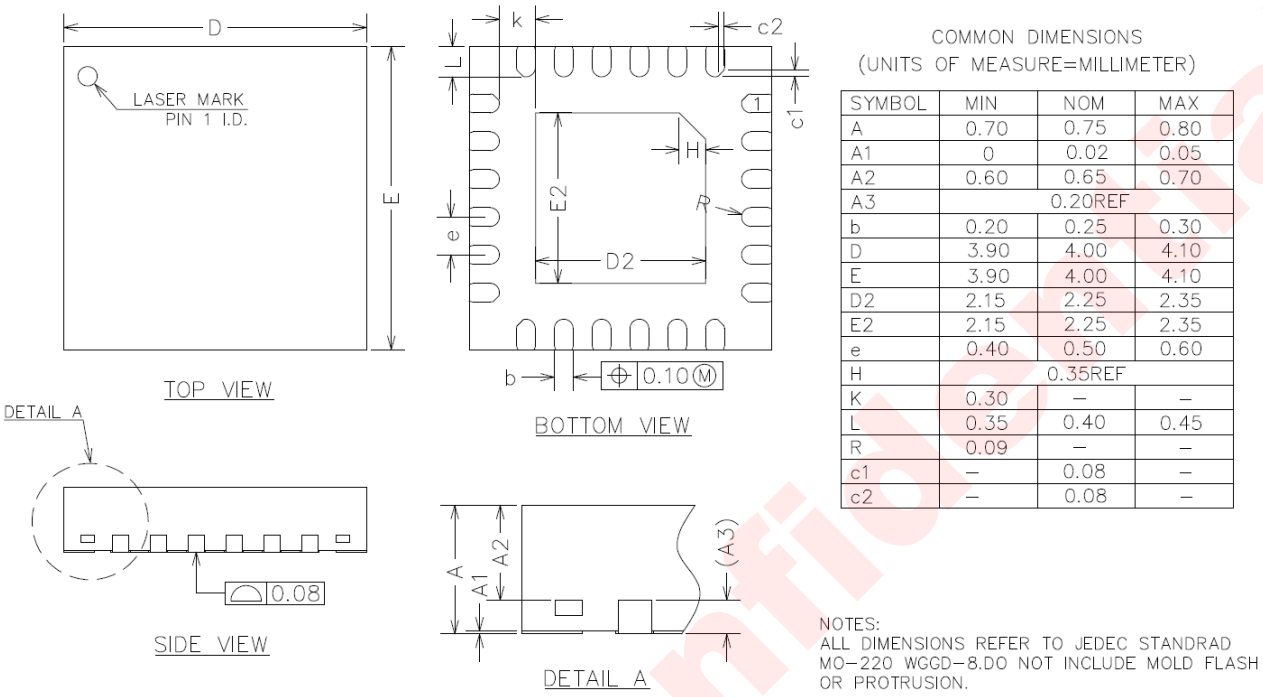
2、 General Tolerance ±0.25mm.



# PACKAGE DESCRIPTION

QFN4x4-24L (P0.50 T0.75) Package Outline Dimensions




COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

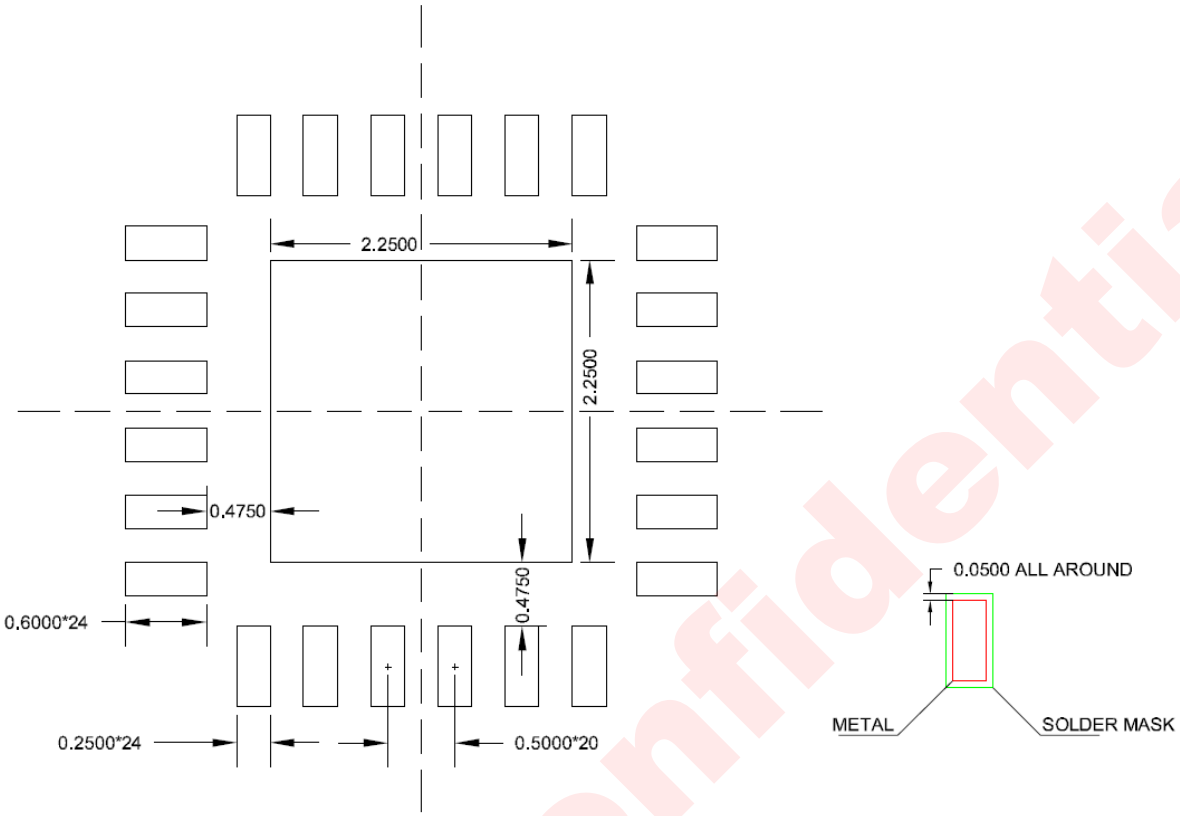
| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0 | 0.02 | 0.05 |
| A2 | 0.60 | 0.65 | 0.70 |
| A3 | | 0.20REF | |
| b | 0.20 | 0.25 | 0.30 |
| D | 3.90 | 4.00 | 4.10 |
| E | 3.90 | 4.00 | 4.10 |
| D2 | 2.15 | 2.25 | 2.35 |
| E2 | 2.15 | 2.25 | 2.35 |
| e | 0.40 | 0.50 | 0.60 |
| H | | 0.35REF | |
| K | 0.30 | – | – |
| L | 0.35 | 0.40 | 0.45 |
| R | 0.09 | – | – |
| c1 | – | 0.08 | – |
| c2 | – | 0.08 | – |

NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDRAD MO-220 WGGD-8.DO NOT INCLUDE MOLD FLASH OR PROTRUSION.



## LAND PATTERN DATA

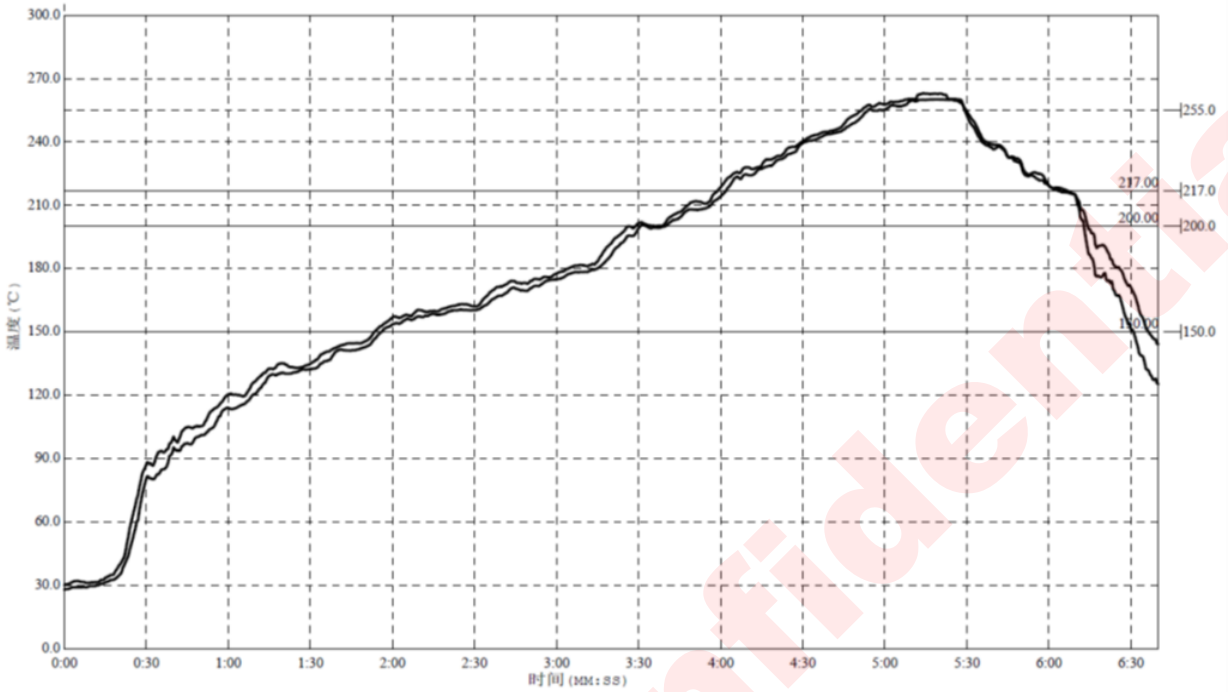



**UNIT:MM**



## REFLOW




| Reflow Note | Spec |
|---|---|
| Average ramp-up rate (217°C to peak) | Max. 3°C /sec |
| Time of Preheat temp. (from 150°C to 200°C) | 60-120sec |
| Time to be maintained above 217°C | 60-150sec |
| Peak Temperature | >260°C |
| Time within 5°C of actual peak temp | 20-40sec |
| Ramp-down rate | Max. 6°C /sec |
| Time from 25°C to peak temp | Max. 8min |

NOTE 1: All data are compared with the package-top temperature, measured on the package surface;

NOTE 2: AW22127 adopted the Pb-Free assembly.



# REVISION HISTORY

| Version | Date | Change Record |
|---|---|---|
| V0.9 | Jul. 2017 | Preliminary Version |
| V1.0 | Dec. 2017 | Datasheet V1.0 Released |
| V1.1 | Jan. 2018 | Added the Land Pattern Data -- page29 |
| V1.2 | Feb. 2018 | Modify the value of resistor on pin INTN and SYNC --page1, 4 |
| V1.3 | July. 2018 | Added the UVLO hysteresis & accuracy<br>Added the Max Voltage of Vdrop1 & Vdrop2<br>Added the Accuracy of Led Current levels --page6, 7 |
| V1.4 | July. 2018 | Added the SYNC cascade resistor range --page4 |
| V1.5 | Sept.2018 | Correction Storage temperature $T_{STG}$ range --page5<br>Modify the Latch-up test condition --page5<br>Correction Reg0x02 bit3 & bit2 definition --page19<br>Added the operation current type --page6 |
| V1.6 | Mar.2019 | Added the Firmware Program description --page15 |
| V1.7 | June.2019 | Update the software reset description --page9 |



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