A Synchronous Boost Converter with Adjustable Output Voltage

FEATURES

- Input Voltage Range: 2.8V to 4.5V
- Adjustable Output Voltage: (V_{IN}+0.5V) to 5.5V
- I_{OUT}≥1.5A at V_{OUT}=5V, V_{IN}≥3.3V (mode 1)
- Up to 92% Efficiency
- Light Load Burst Mode
- Three External Components: 1μH Inductor, Input/ Output Capacitors (Figure 1)
- Over Voltage, Short-circuit Protection
- True Load Disconnect During Shutdown
- 1.19mm x 1.28mm, WLCSP 9-Ball

APPLICATION

- Cell Phones, Smart Phones, PADs, Wearable
- Power Bank
- USB On-The-Go Device
- Digital Camera

DESCRIPTION

The AW3615 is a Large current, High-efficiency synchronous Boost regulator with adjustable output voltage. The AW3615 use PWM peak current mode control method, in Continuous Conduction Mode (CCM), operate at 2MHz to reduce external device size, save more PCB area. At light load condition, the chip will enter Burst mode automatically to realize high efficiency in all load range.

The AW3615 added input peak current limit value adjustable by 1-wire pulse function for Charge banks application, to adjust the maximum load ability. The bulk switch circuit is integrated to isolate the input port and output port, prevent current from V_{OUT} to V_{IN}.

AW3615 can adjust the output voltage by applying external resistors to FB pin. Otherwise, FB should be grounded and the V_{OUT} would be set to 5V for default.

The AW3615 available in a tiny CSP 9-ball package.

TYPICAL APPLICATION CIRCUIT

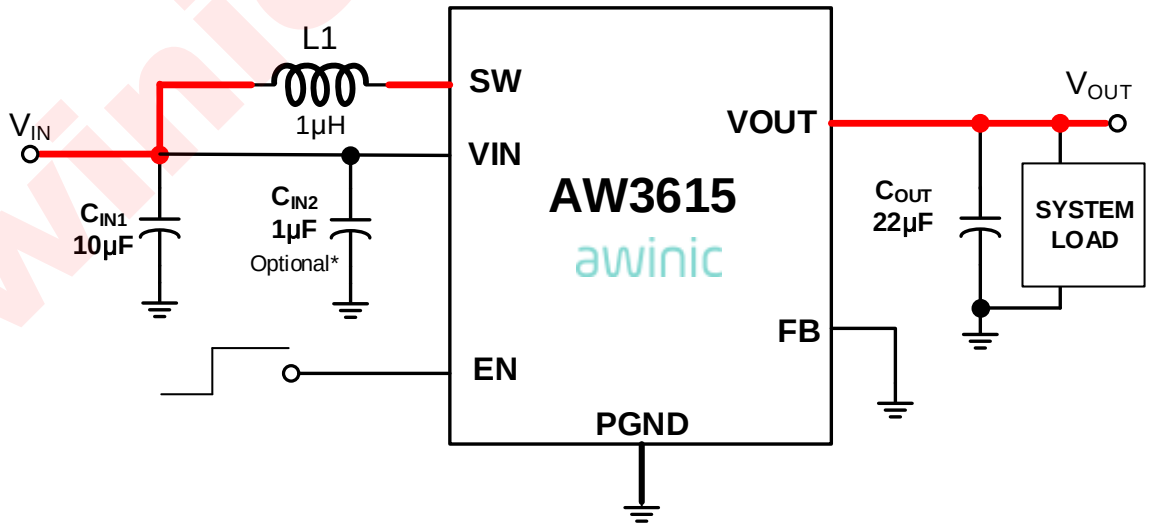
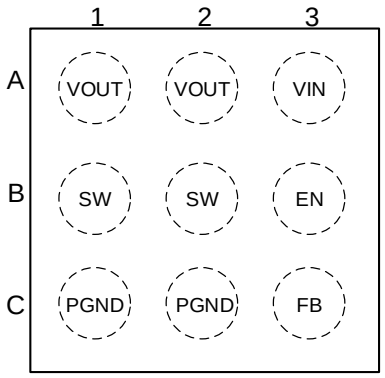


Figure 1 AW3615 adopts internal divider resistors(5V output) by set FB grounded

PIN CONFIGURATION AND TOP MARKING

AW3615 TOP VIEW



AW3615 MARKING

TOP VIEW

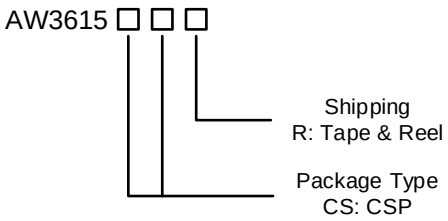
3615----AW3615CSR
XXXX----Production Tracing Code

PIN DEFINITION

No	Name	DESCRIPTION
A1, A2	VOUT	Output terminal, Should be bypassed with a C_{OUT} capacitor
A3	VIN	Power Supply, Connect directly to C_{IN}
B1, B2	SW	Switching Node, Connected to inductor.
B3	EN	Enable. When this pin is HIGH, the circuit is enabled. A 1.35MΩ pull-down resistor is integrated.
C1, C2	PGND	Power Ground. This is the power return for the IC, COUT capacitor should be returned with the shortest path possible to these pins.
C3	FB	Feedback terminal. VFB would be regulated to 1V by the chip if external resistors be adopts. Otherwise, this pin should be connected to ground.

ORDERING INFORMATION

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW3615CSR	-40℃ ~ 85℃	CSP-9B, 1.19mm x 1.28mm	3615	MSL1	RoHS+HF	3000 units/ Tape and Reel



TYPICAL APPLICATION CIRCUITS

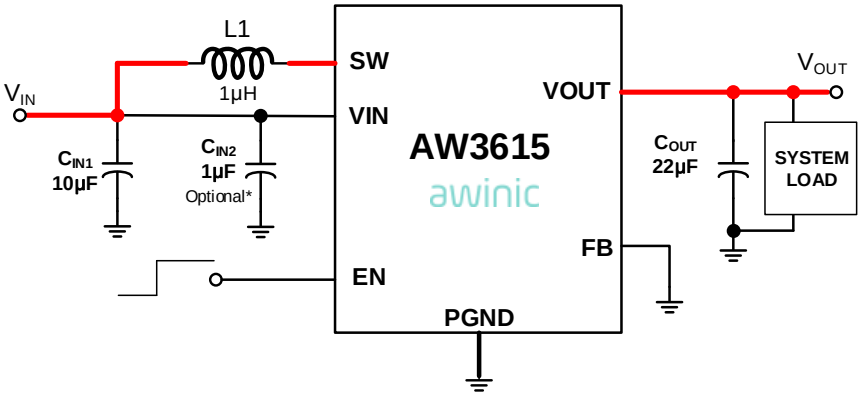


Figure 2 AW3615 adopts internal divider resistors(5V output) by set FB grounded

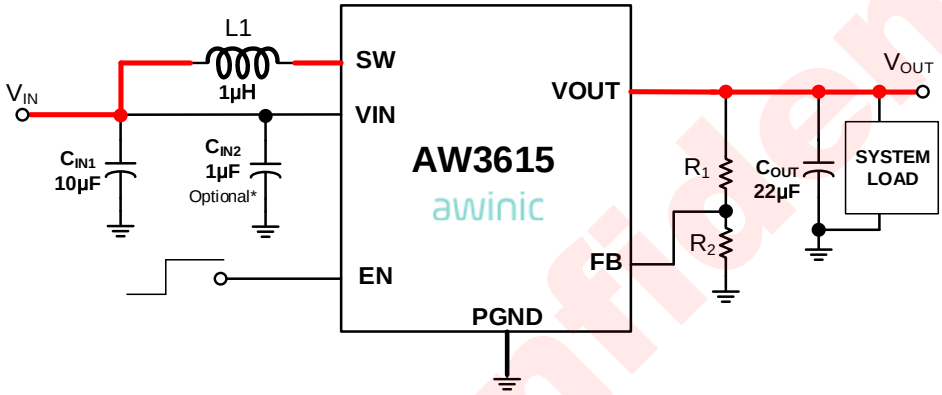


Figure 3 AW3615 adopts external divider resistors at FB pin

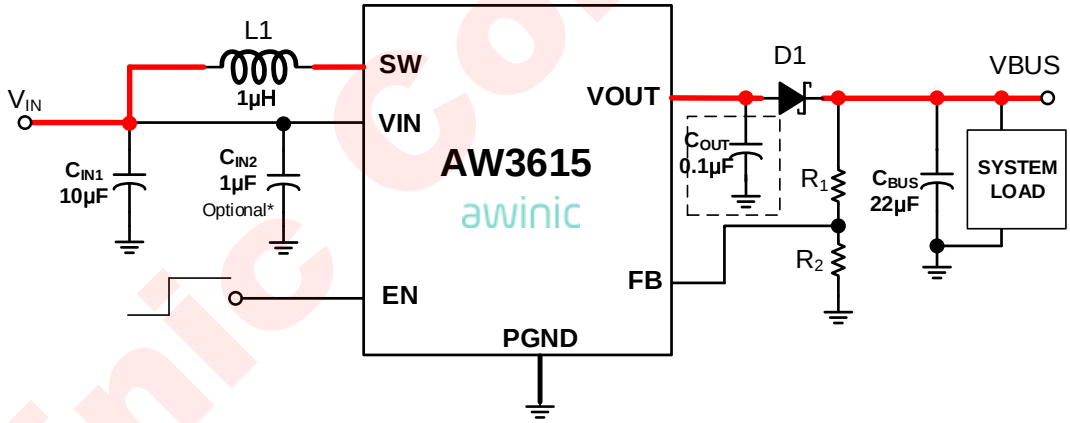


Figure 4 AW3615 adopts external divider resistors and diode

Note1: Inductor L1 recommended is 1μH, the saturated current need no less than 4A.

Note2: The large current path is used **red line**. For the sake of driving capability, the routes V_{IN}-SW, V_{OUT}-V_{BUS} should be short and wide. The proposed width of V_{IN}-SW route is 100mil, and the V_{OUT} trace 60mil.

Note3: Place C_{IN1} and inductor close to V_{IN} pin, an optional C_{IN2} should added if C_{IN1} is far from VIN pin. Place C_{OUT} close to V_{OUT} and the distance between C_{OUT} and V_{OUT} pin must not beyond 5mm. A C_{OUT} of 22μF is recommended.

Note4: In the application of figure3 and figure4, VFB would be regulated to 1V by the chip, then V_{OUT} (VBUS) can be set to **1V · (R1 + R2)/ R2**. For the application adopts D1 in **figure4**, we suggest the VBUS voltage set by divider resistors should among the range of **VIN to 5V**, to keep the chip VOUT voltage among (VIN+0.5V) to 5.5V.

Note5: For the application adopts D1 in **figure4**, the thermal management of D1 would become a noticeable issue if load current exceeds 400mA. Optimized PCB layout design helps reduce peak temperature of D1, contact us for more details.

ABSOLUTE MAXIMUM RATINGS(NOTE1)

PARAMETERS		Range
VIN		-0.3V to 7V
SW	DC	-0.3V to 7V
	Transient: 2ns pulse width, 2MHz	-0.7V to 9V
VOUT (DC, EN=0V)		-0.3V to 9V
Ambient temperature		-40℃ to 85℃
Max Junction Temperature T_{JMAX}		125℃
Storage Temperature T_{STG}		-65℃ to 150℃
Maximum lead temperature (soldering)		260℃
ESD(NOTE2)		
HBM		±2kV
CDM		±2kV
MM		±200V
Latch-up		
JEDEC STANDARD NO.78B DECEMBER 2008		+IT：+450mA -IT：-450mA

NOTE1: *Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.*

NOTE2: *The human body model test method per MIL-STD-883J Method 3015.9. Charged Device Model test method per JEDEC EIA/JESD22-C101F. Machine Mode test method per JEDEC EIA/JESD22-A115.*

RECOMMENDED OPERATING CONDITIONS

		Min	Typ.	Max	Unit
V_{IN}	Power supply	2.8		4.5	V
L	Inductor	0.47	1		μH
C_{IN}	Capacitor at V_{IN} pin		10		μF
C_{OUT}	Capacitor at V_{OUT} pin	10	22		μF
T_A	Ambient Temperature		25		℃

ELECTRICAL CHARACTERISTICS

Recommended operating conditions, unless otherwise noted, circuit per Figure 1, V_{OUT} = (V_{IN}+0.5) ~5.5V, V_{IN}=2.8~4.5V, T_A=-40℃~85℃. Typical values are given V_{IN}=3.8V and T_A=25℃.

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Power Supply						
I_Q	V_{IN} quiescent current	EN=V_{IN}, I_{OUT}=0, V_{OUT}=5.0V, Device not switching		80		μA
		Shutdown: EN=0		0.1	1	μA
V_{UVLO}	Under-Voltage Lockout	VIN Rising		2.7	2.8	V
V_{UVLO_HYS}	Under-Voltage Lockout Hysteresis			200		mV
Inputs						
V_{IH}	Enable High voltage		1.2			V
V_{IL}	Enable Low voltage				0.45	V
R_{PD}	EN pin Pull-down resistor			1.35		MΩ
Outputs						
V_{REG}	Output Voltage Accuracy	FB=0V, V_{OUT}=5V, DC I_{LOAD} from 0.3A to 1A	-4		4	%
V_{FB}	FB Voltage Accuracy	22kΩ≤R_{FB-GND} ≤1MΩ, I_{LOAD} from 0.3A to 1A	0.978	1	1.018	V
V_{PSM}	Power save mode exit V_{OUT} voltage	I_{OUT}=0		101.7		%V_{OUT}
V_{OUT_OVP}	V_{OUT} overvoltage protection			110		%V_{OUT}
Timing						
fsw	Switching Frequency	V_{IN}=3.8V, I_{LOAD}=500mA	1.6	2	2.4	MHz
t_{PSM}	Power save mode enter time	I_{OUT}=0		32		μs
T_{LO}	1-wire pulse low time		0.75	2	10	μs
T_{HI}	1-wire pulse high time		0.75	2	10	μs
T_{OFF}	EN pin shutdown delay		500			μs

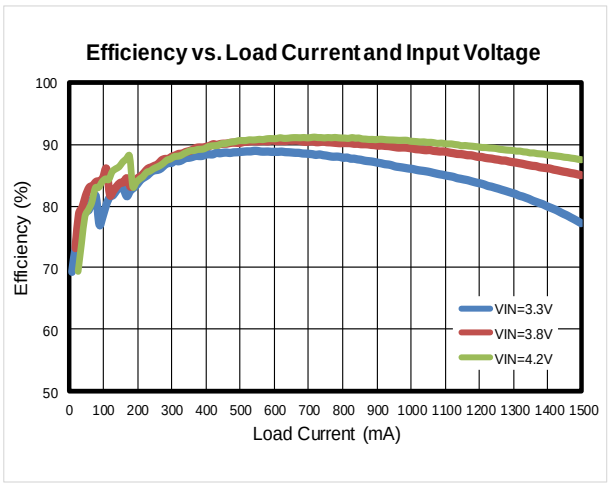
ELECTRICAL CHARACTERISTICS

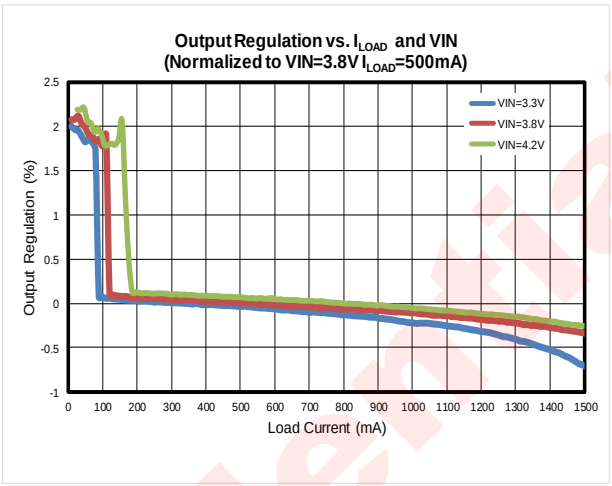
Recommended operating conditions, unless otherwise noted, circuit per Figure 1, V_{OUT} = (V_{IN}+0.5) ~5.5V, V_{IN}=2.8~4.5V, T_A=-40℃~85℃. Typical values are given V_{IN}=3.8V and T_A=25℃.

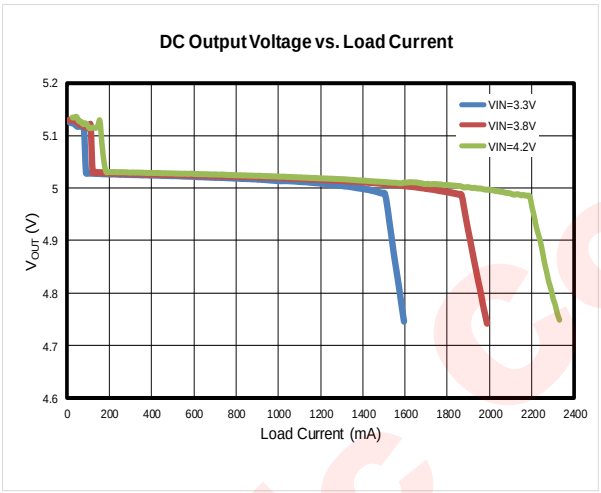
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Power Stage						
$R_{DS(ON)N}$	N-channel Boost Switch $R_{DS(ON)N}$	V_{IN}=3.8V, V_{OUT}=5V, DC I_{TEST}=0.5A		50		mΩ
$R_{DS(ON)P}$	P-channel Boost Switch $R_{DS(ON)P}$			65		mΩ
I_{P_LIM}	Boost peak current limit	Mode1		3.5		A
		Mode2		2.7		A
		Mode3		1.9		A
		Mode4		0.75		A
$I_{P\_LIM\_SS}$	Boost soft-start peak current limit			0.75		A
T_{OTP}	Over temperature protection			160		℃
T_{OTP_HYS}	OTP hysteresis			30		℃

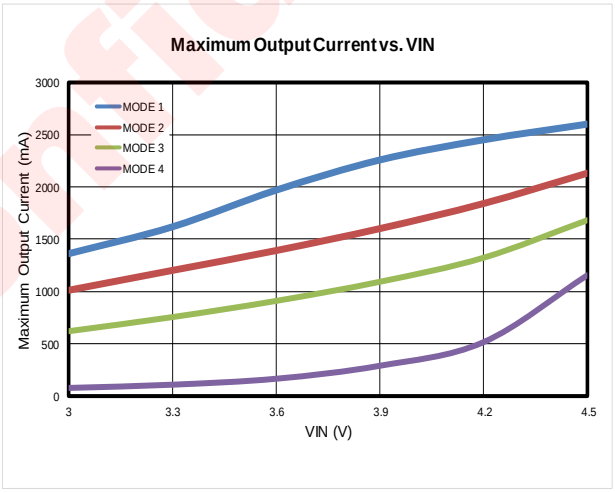
TYPICAL CHARACTERISTICS

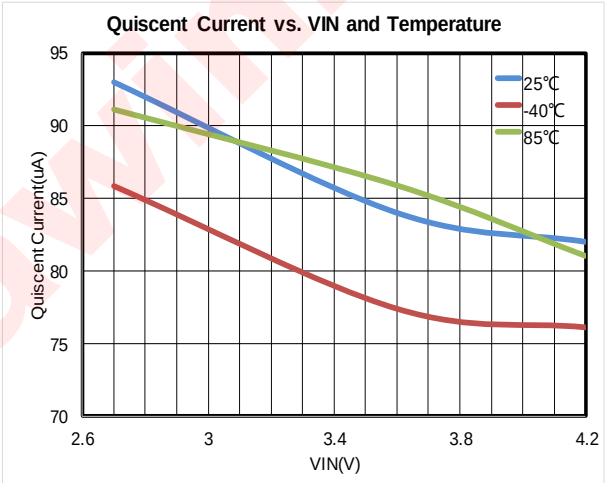
Unless otherwise specified; V_{IN}=3.8V, V_{OUT}=5V, T_A=25℃, and circuit and components according to Figure1.

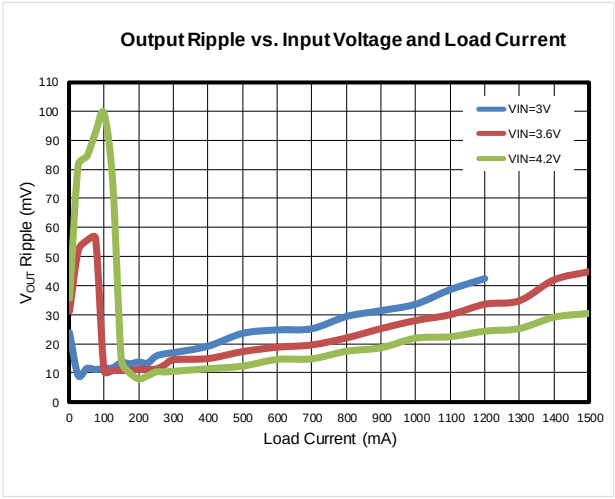








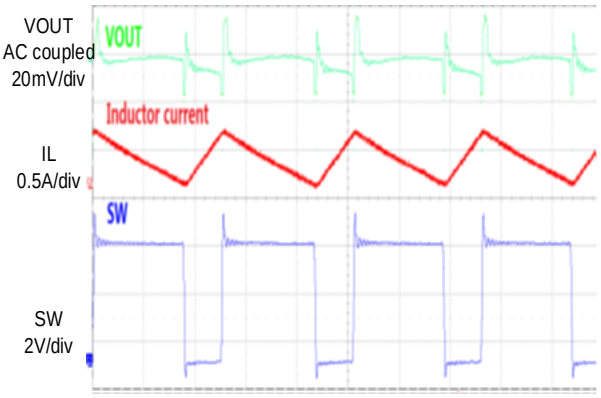




TYPICAL CHARACTERISTICS

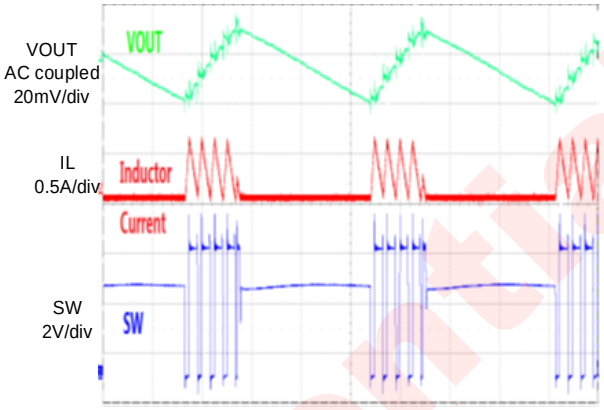
Unless otherwise specified; V_{IN}=3.8V, V_{OUT}=5V, T_A=25℃, and circuit and components according to Figure1.

PWM Operation



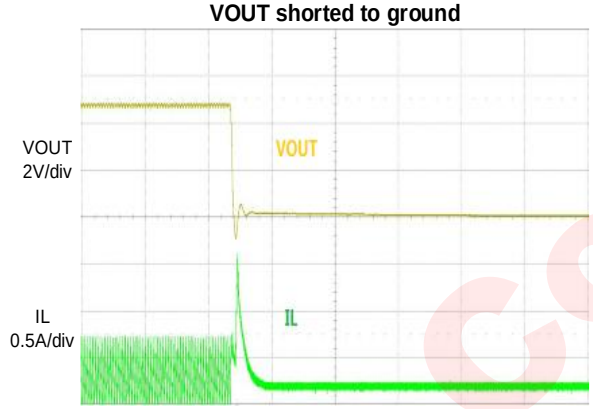
Time(200ns/div)

PFM Operation



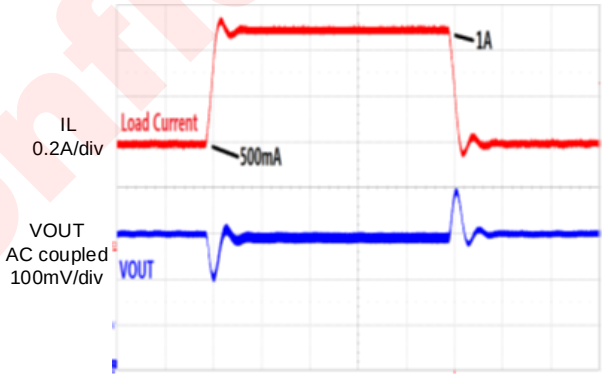
Time(2μs/div)

VOUT shorted to ground



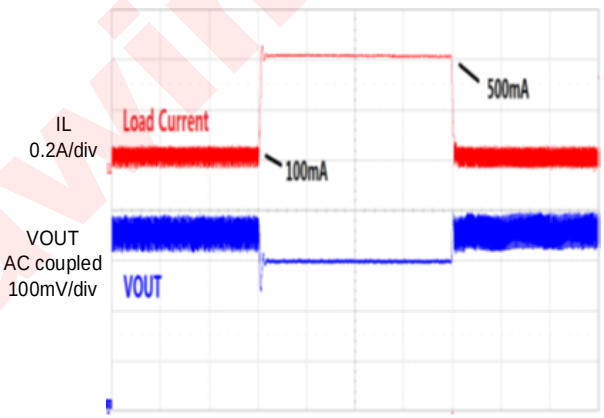
Time(50μs/div)

Load Transient, 500mA to 1A



Time(100μs/div)

Load Transient, 100mA to 500mA



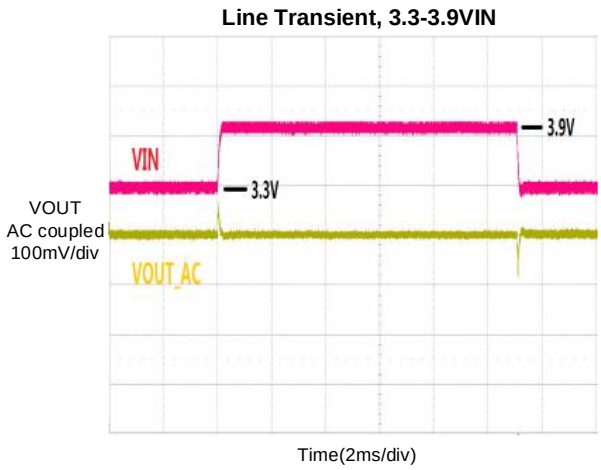
Time(500μs/div)

Soft start

Time(50μs/div)

TYPICAL CHARACTERISTICS

Unless otherwise specified; V_{IN}=3.8V, V_{OUT}=5V, T_A=25℃, and circuit and components according to Figure1.



DETAILED DESCRIPTION

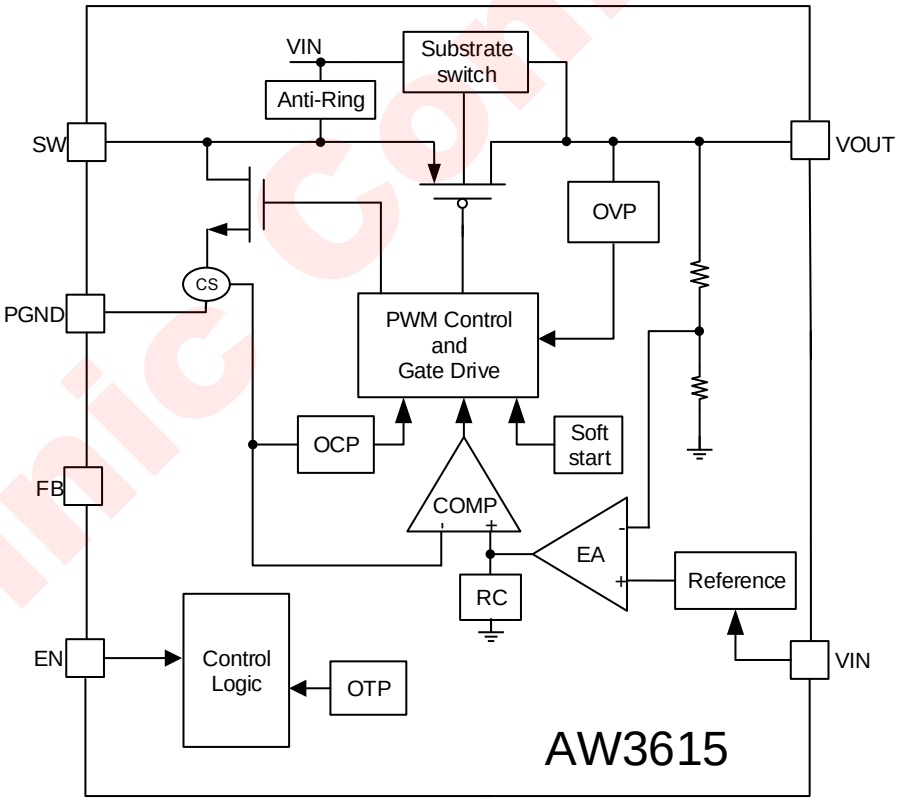
AW3615 is a high current and high efficiency synchronous boost converter, which can supply up to 1.5A@V_{IN}=3.3V and 5V output voltage.

AW3615 designed the intelligent current limit and 1-wire pulse modulate current limit for the application of mobile phone, Power Bank, etc. As the battery voltage decreases, the maximum output current decreases accordingly. To extend the life time of Battery.

AW3615 adopt dynamic loop compensation and peak current mode which can use a very small size LC filter circuit and has a good load transient response characteristics. The internal soft-start circuit and loop compensation circuitry also reduces the number of external components and system costs, and simplifiers the design.

AW3615 integrated low R_{DSON} Power MOSFETs (low-side NMOS and high-side PMOS) as shown in the figure below. In medium and heavy load conditions, the chip operate at a constant 2MHz frequency in the continuous conduction of the PWM mode; In light load conditions, the chip will automatically switch to the burst mode which can optimize the efficiency of light load; In the no-load conditions, the chip will enter the Power Save mode, which will close or de-biased most of the circuit except the output voltage detection module, only when V_{OUT} dropped to a target voltage threshold, the circuit began to resume work, In Power Save mode, the quiescent current will reduced to only 80μA. AW3615 achieve the high efficiency in all load range by reducing the conduction loss and switching losses.

FUNCTIONAL BLOCK DIAGRAM



PWM MODE

In medium and heavy load conditions, AW3615 operate at a constant 2MHz frequency (typ.) peak current PWM mode. The internal constant frequency clock generator controls the conduction of the low-side NMOS and the feedback loop controls its turn-off. The feedback control loop is a double loop: Current inner loop and

Voltage outer loop, once the inductor current reach to a certain threshold current, the current loop turns off the low-side NMOS, and the current threshold is determined by the voltage outer loop.

The advantage of peak current PWM mode is fast and accurate. The current signal which participate in control will cause overload and short circuit protection more effective. Meanwhile the entire system has a fast transient response characteristic.

BURST MODE

AW3615 automatically enters the burst mode in light load conditions and returns to the constant frequency PWM mode when the load increases. During burst mode, the switch frequency would reduce to 1MHz, while the chip uses the same error amplifier and peak current loop compensation circuit as the PWM mode. This control method avoids the excessive fluctuation of the output voltage when the mode is changed. In burst mode, when the output voltage V_{OUT} reaches the target value, the switch FET of AW3615 stop working, but the other internal analog modules are still working to improve the chip load transient response. When V_{OUT} drops slightly, the Power MOSFETs resume working and V_{OUT} rises. The burst mode minimizes switching losses by reducing the number of switching of power MOSFETs, and the efficiency of light loads is greatly improved.

POWER SAVE MODE

On the basis of the Burst Mode, AW3615 integrated Power Save Mode to reduce the no-load quiescent current. The V_{OUT} descent rate is counted when operate in burst mode, once it is found that V_{OUT} has not fallen to 5.085V (5V output) in 32μs period (TYP), it is judged that V_{OUT} is in no-load state and enters Power Save mode. In Power Save mode, most of the circuit modules will be de-biased or disabled. Until V_{OUT} drops below 5.085V, the chip resume operation, raising V_{OUT} to the target value. The Power Save mode reduces the quiescent current of the AW3615 to only 80μA.

The following figure shows the V_{OUT} ripple in PWM mode, Burst mode and Power Save mode.

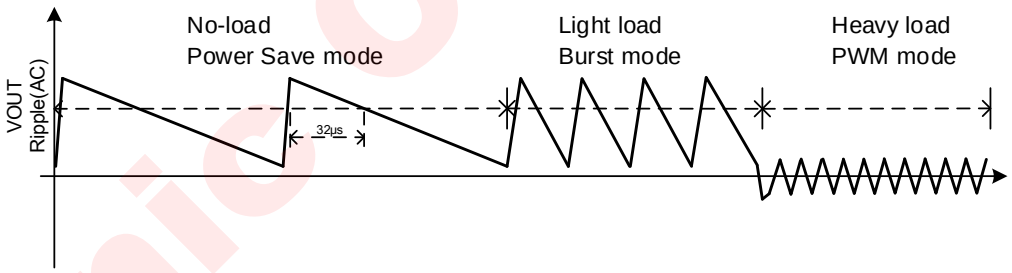


Figure 5 V_{OUT} Ripple

SOFT START

AW3615 integrated soft start function in order to limit the surge current during the start of the power supply. During the start-up period, the chip linearly activates output terminal using the internal constant current source to charge the V_{OUT} to allow V_{OUT} rise gradually. When V_{OUT} is close to V_{IN}, the converter starts to switch. When the V_{OUT} voltage reaches to the target value, the loop stabilizes V_{OUT} at the target value. In order to avoid rush current and overshoot on V_{OUT}, during soft start phase, the switch frequency reduce to 1MHz and the current limit is limited to 750mA. Thus, AW3615 can only support 200mA load (typ.) during soft start. It is recommended to add load after the AW3615 have been start up completely.

What's more, AW3615 sets a time window for switching soft start phase after linear charging, which is 100μs for typical case. If V_{OUT} failed to rise to the target value within the set window, the switch frequency and current limit would return to the normal value.

TRUE ISOLATION AND REVERSE CURRENT PROTECTION

The V_{IN} is connected to the V_{OUT} through the rectifier diode when an asynchronous boost is turn off, V_{OUT} is maintain at a potential lower than V_{IN} by a diode turn-on voltage drop, at this moment V_{IN} and V_{OUT} are not truly electrically isolated. Some synchronous boost will still be connected to V_{OUT} through the internal body diode of High-side PMOS which is the same with asynchronous boost. AW3615 through the substrate selection circuit to truly achieve the electrical isolation of V_{IN} and V_{OUT}. When the chip is turn-off, V_{OUT} will drop to 0V, and will not draw current from V_{IN}, meanwhile, when supply voltage to V_{OUT}, it also will not lead current flow from V_{OUT} to V_{IN}.

CURRENT LIMITING AND PROTECTION

AW3615 provides a cycle by cycle peak current limiting function to protect the switch FET. When the inductor peak current reaches the current limit threshold, the current limiting circuit turns off the power MOSFET until the next cycle turns on, thus limiting the delivered power by adjusting the on-time duty cycle of the power MOSFET.

AW3615 have multi-level current limiting by adjusting the current threshold of the current limit comparator which directly limit the inductance of the peak current, and then according to the correspondence of the DCDC converter's input and output current ($\mathrm{Iout} = \frac{Iin \cdot Vin \cdot \eta}{Vout}$) which can achieve the relative value of current limitation and then achieve the purpose of limiting the output current. Typically, the delay time between response of current limiting to N-channel MOSFET is turned off that is 40ns.

AW3615 can optimize the reliability of the application by adjusting the input peak current limit. It discharges a large current to the device in the typical case and discharges low current to the device when the low battery and high current applications(such as calls, large games, etc.) occurs, which avoid the host battery overload. The following table shows the pattern of AW3615.

Table 1 Mode and EN pulse description

Mode	EN Control Waveform	Boost Peak Current Limit
Mode 1		3.5A
Mode 2		2.7A
Mode 3		1.9A
Mode 4		0.75A

Note: The 1-wire pulse function will be **disabled after the EN consecutive high 220μs**.

EN ONE-WIRE PULSE CONTROL TIMING

AW3615 can select the value of peak current limit by sending one-wire pulse to the EN pin. The default is set to the maximum current level when EN is directly connect to VIN; The number of rising edge at EN determines the peak current limit when EN is connected to 1.8V compatible GPIO port, Table 1 is the relationship between the number of EN rising edge and peak current limit.

Figure 6 shows the timing of the one wire pulse, where T_{HI} refers to the high level width of the pulse, the recommended value: 2μs~10μs; T_{LO} refers to the low width of the pulse, the recommended value: 2μs~10μs; T_{OFF} refers to the required low time when the chip enter shutdown mode. The operation state is the cycle mode, after power on, EN pin input a pulse, the device will enter Mode1. In Mode1, EN pin input a pulse, it will enter Mode2. In Mode2, EN pin input a pulse, it will enter Mode3. In Mode3, EN pin input one pulse, it will enter Mode4. In Mode4, EN pin input one pulse, it will return to the Mode1. When the EN pin control signal is pulled

low and at least 500μs, it enters the shutdown mode, the power consumption in the shutdown mode is very low which is below 0.1μA.

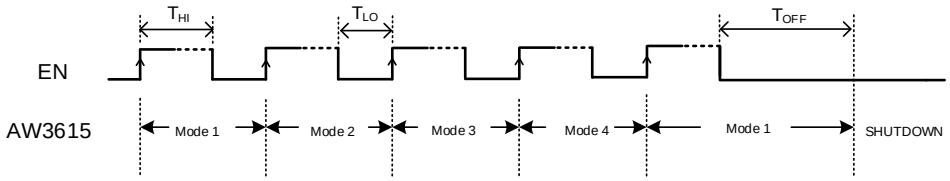


Figure 6 AW3615 Timing Chart of One-wire Pulse Signal

ANTI-RING

When the DC-DC converter operate in the discontinuous conduction mode, a resonant circuit consisting of inductance L1 and SW node capacitance C_{SW} will produce high frequency ringing which energy is small but also cause EMI radiation.

AW3615 integrated an Anti-Ring circuit that connects one terminal of inductor and power supply of the chip through a resistor to suppress the ringing of the SW at the time of DCM.

UVLO

UVLO circuit prevent the malfunction when the chip operate in low voltage. When V_{IN} drops to under-voltage protection threshold V_{UVLO} (TYP: 2.5V), it turns off. When V_{IN} rises to 200mV higher than V_{UVLO} (TYP: 2.7V), it resumes operate.

V_{OUT} PIN MAXIMUM VOLTAGE (EN=0)

V_{OUT} pin is usually connected to the USB port when AW3615 used in OTG and Power Bank which has a high demand for off-state (EN=0) withstand voltage. The off-state DC withstand voltage of AW3615 is above 9V which satisfy most of the 5V charging applications. If the application need to further enhance the capability of anti-surge, we suggest to add a TVS tube to the V_{OUT}.

Moreover, a Schottky diode can be set to in series between chip V_{OUT} and USB port, which can significantly improve the rated voltage of the entire port, as shown in figure 4.

FB MODE DETECTION

Each time VIN power-on-reset occurs, the FB pin would detect external resistance between FB and ground. The detecting process runs as follow: a 300mA (typ.) current source charges the FB pin from VIN, meanwhile the chip starts a 20μs timer. If V_{FB} rises to higher than 2V (typ.) during the timer operating, which means the RFB is greater than 6.7kΩ, the chip would enter external-resistor mode and the V_{OUT} is set to **1V · (R1 + R2)/ R2** (figure 3). On the other hand, if V_{FB} stays below 2V, the V_{OUT} would be set to fixed 5V (typ.) with internal resistors.

The recommended range of R2 is from **22kΩ to 1MΩ**. Then R1 can be set based on the target V_{OUT} and R2 value.

APPLICATION INFORMATION

OUTPUT CAPACITANCE (C_{OUT})

For the output capacitor, in order to keep the system stable, should guaranteed the effective capacitance large than 2.5μF. The capacitance value, capacitance DC BIAS and capacitance materials will affect the effective capacitance. So, when selected Output capacitance should consider these factors. It is recommended to place the Output capacitance as close as possible to the VOUT and GND pins of the IC. If, for any reason, the application requires the use of large capacitors which cannot be placed close to the IC, using a smaller ceramic in parallel to the large one is highly recommended. This small capacitor should be placed as close as possible to the VOUT and GND pins of the IC.

Under continuous current mode, the output ripple can be estimated by the following formula,

$$V_{RIPPLE} = \frac{(V_{OUT} - V_{IN}) * I_{OUT}}{V_{OUT} * f * C_{OUT}}$$

Where f is the switching frequency which is 2 MHz (typ.) and C_{OUT} is the effective capacitance.

From the above equation, if need a small output ripple, the effective capacitance should be large.

AW3615 recommended output capacitor is TDK C1608X5R0J226M (22μF, 0603, X5R, 6.3 V-Rated).

In the application per figure 4, C_{OUT} is separated from system load by a Schottky, so the recommended capacitance (22μF typ.) should be set to the system terminal, and the C_{OUT} is allowed to adopt a smaller capacitance, 0.1μF for example.

INPUT CAPACITOR

Multilayer ceramic capacitors are an excellent choice for input decoupling of the step-up converter as they have extremely low ESR and are available in small footprints. Input capacitors should be located as close as possible to the device. While a 10μF input capacitor is sufficient for most applications, larger values may be used to reduce input current ripple without limitations.

Take care when using only ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output can induce ringing at the VIN pin. This ringing can couple to the output and be mistaken as loop instability or could even damage the part. Additional “bulk” capacitance (electrolytic or tantalum) should in this circumstance be placed between C_{IN} and the power source lead to reduce ringing that can occur between the inductance of the power source leads and C_{IN}.

AW3615 recommended input capacitor is TDK C1608X5R0J106K or Murata GRM188R60J106K (10μF, 0603, X5R, 6.3 V-Rated).

INDUCTOR SELECTION

Recommended nominal inductance value is 1μH.

The AW3615 employs peak-current limiting, so peak inductor current can reach 3.5A for long time when a large load is applied until the output voltage is below input voltage. In order to avoid the inductor saturation, the inductor which has above 4 A saturation current is highly recommended and a part number of Sunlord WPN252012H1R0M is for reference.

CHECKING LOOP STABILITY

The first step of circuit and stability evaluation is to look from a steady-state perspective at the following signals:

- Switching node, SW
- Inductor current I_L
- Output ripple voltage, $V_{OUT(AC)}$

These are the basic signals that need to be measured when evaluating a switching converter. When the switching waveform show large duty cycle jitter or the output voltage or inductor current shows oscillations, the regulation loop may be unstable. This is often a result of board layout and/or L-C combination.

As a next step in the evaluation of the regulation loop, the load transient response is tested. The time between the application of the load transient and the turn on of the P-channel MOSFET, the output capacitor must supply all of the current required by the load. V_{OUT} immediately shifts by an amount equal to $\Delta I_{(LOAD)}$ x ESR, when ESR is the effective series resistance of C_{OUT}. $\Delta I_{(LOAD)}$ begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. The results are most easily interpreted when then device operates in PWM mode.

During this recovery time, V_{OUT} can be monitored for settling time, overshoot or ringing that helps judge the converter's stability. Without any ringing, the loop has usually more than 45° of phase margin. Because the damping factor of the circuitry is directly related to several resistive parameters (e.g., MOSFET $R_{DS(on)}$)that are temperature dependent, the loop stability analysis has to be done over the input voltage range, load current range, and temperature range.

LAYOUT RECOMMENDATION

The layout recommendations below highlight various top-copper pours by using different colors.

To minimize spikes at V_{OUT}, C_{OUT} must be placed as close as possible to chip's PGND and V_{OUT}, as shown below. The PGND is strongly recommended to be connected to the inner layers. The C_{IN} also need to place close to the V_{IN} pin to provide a steady input voltage for chip.

For thermal reasons, it is suggested to maximize the pour area for V_{IN}, V_{OUT}, PGND. Especially the ground pour should be set to fill all available PCB surface area and tied to internal layers with a cluster of thermal vias.

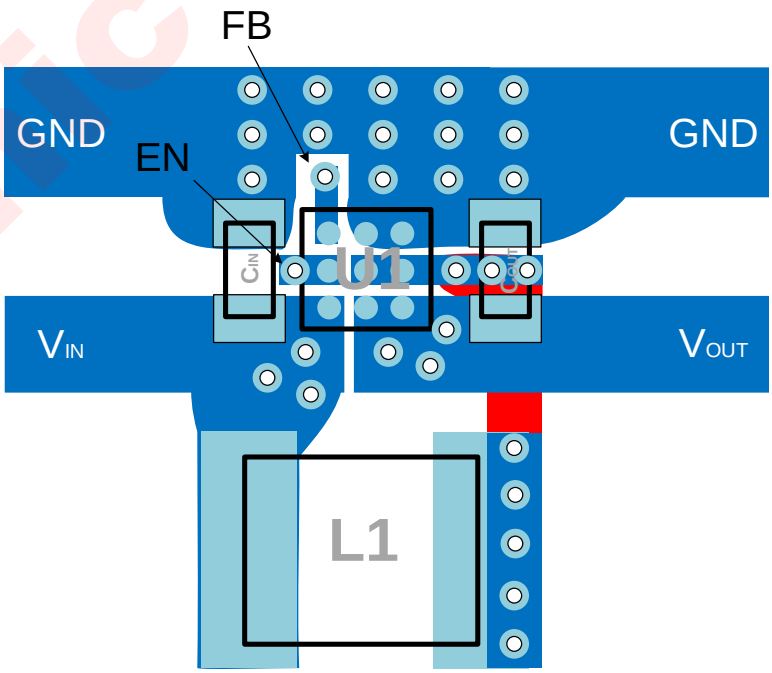
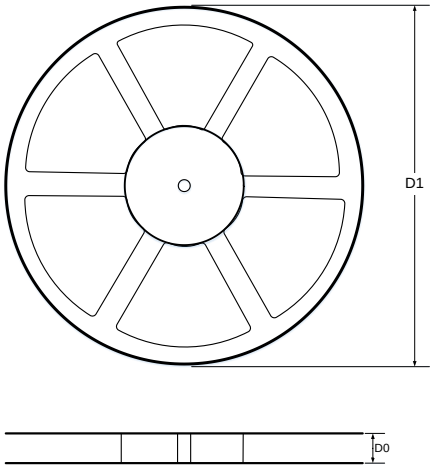


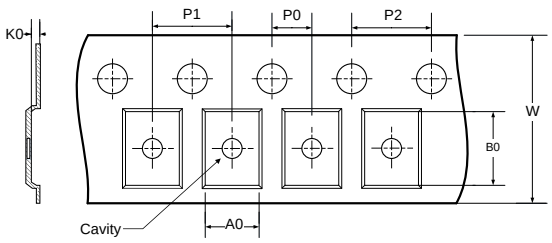
Figure 7 AW3615 Layout Recommendation

TAPE AND REEL INFORMATION

REEL DIMENSIONS

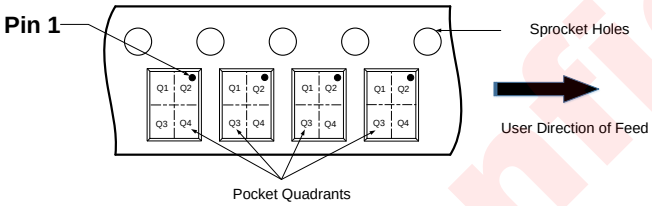


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

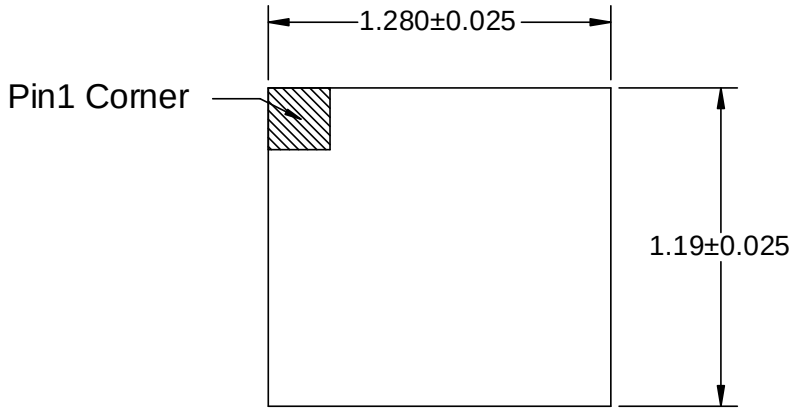


DIMENSIONS AND PIN1 ORIENTATION

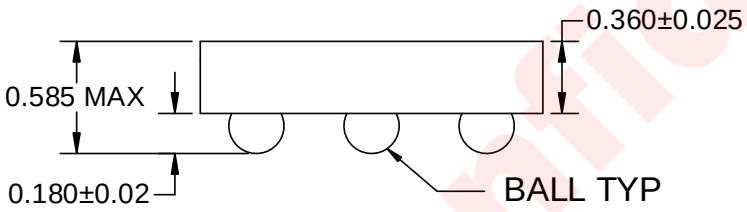
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
179.00	9.20	1.31	1.40	0.67	2.00	4.00	4.00	8.00	Q2

All dimensions are nominal

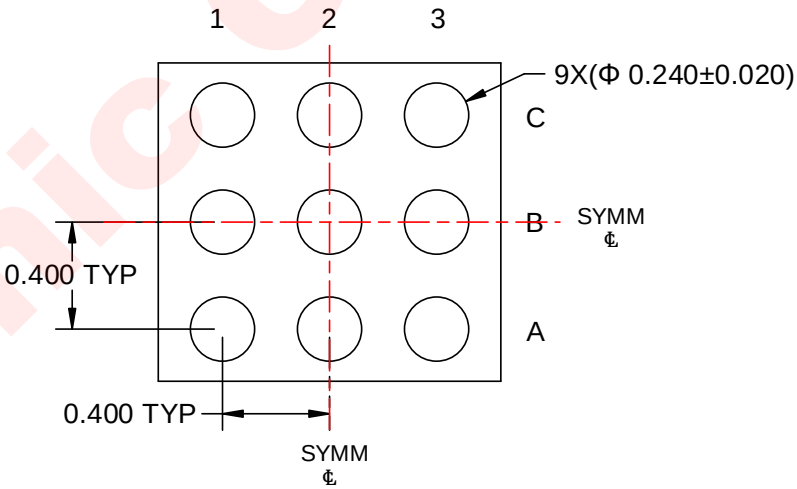
PACKAGE DESCRIPTION



Top View

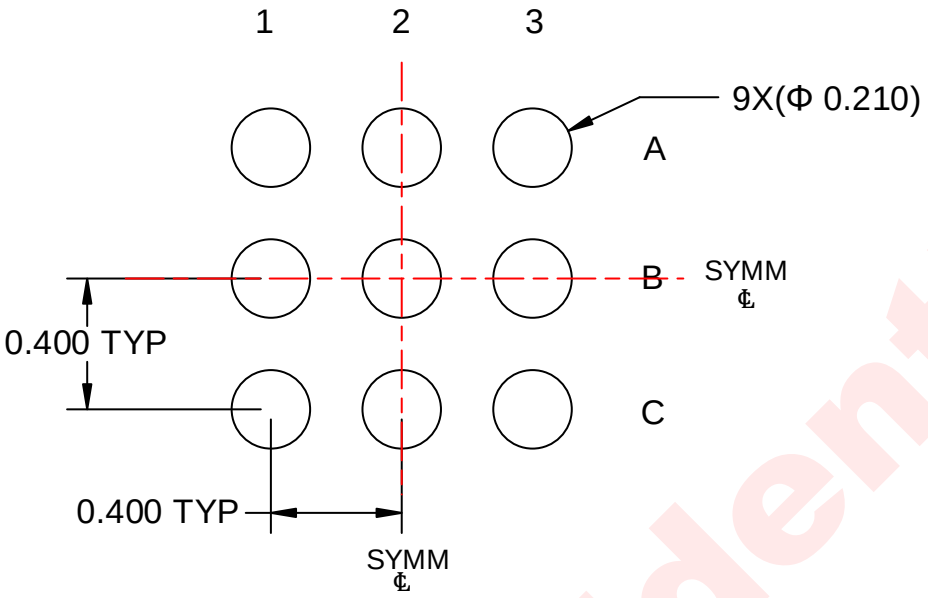


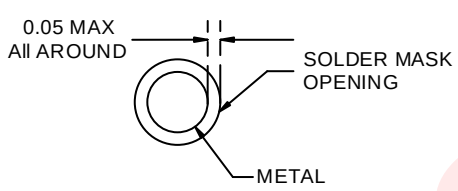
Side View



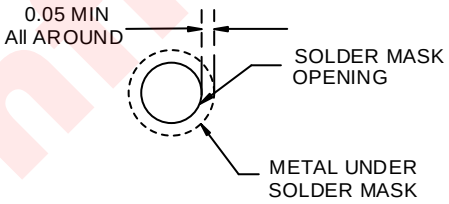
Bottom View Unit: mm

LAND PATTERN





NON-SOLDER MASK DEFINED



SOLDER MASK DEFINED

Unit: mm

REVISION HISTORY

Vision	Date	Change Record
V1.0	2017.3	Draft created
V1.1	2017.6	1. Added some Typical Characteristics figure; 2. Added V_{FB} Electrical Characteristics; 3. Added FB MODE DETECTION detailed description.
V1.2	2018.3	1. Updated Package Description; 2. Updated CURRENT LIMITING AND PROTECTION part table 1; 3. Updated FB MODE DETECTION part; 4. Updated Layout Recommendation.
V1.3	2019.9	1. Updated Detailed Description; 2. Updated Typical Application Circuits; 3. Updated Typical Characteristics curve.

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