AW32001E Single Cell Li-ion Battery Charger with Power Path Management and Full USB Compliance

Features

- Charge Voltage Regulation Accuracy: ±0.5% (0°C to 50°C)
- Charge Current Accuracy: ±5%
- Maximum 28V Input Voltage Rating with Over-Voltage Protection
- Minimum -5V Input Voltage Protection
- Complete Charge Process with Pre-Charge, Fast Charge and Constant Voltage Regulation
- Programmable Charge Parameters Through I²C Compatible Interface
- Programmable Charge Termination and Autonomous Recharge
- Wide Range of Fast Charge Current: 2mA~500mA
- Strong and Robust Protection: V_{IN} OVP, Battery OVP, OCP, Reverse Leakage Protection, Short Protection, Thermal Protection, PCB Over Temperature Protection
- BATFET Control to Support Shipping Mode
- System Reset Function
- Fully Integrated Power Path Management
- Ultra-low Battery Leakage Current to Support Shipping Mode
- WLCSP 1.68mm×1.68mm×0.63mm-9B, 0.5mm Pitch Package
- 7-bit slave address (A7~A1) is 1001001 binary(0x49H)
- IEC62368-1 Approved-File No.BE-37454

Applications

- Smart Handheld Devices
- Wearable Devices
- Smart Watches
- Fitness Accessories

General Description

The AW32001E is a highly-integrated Li-Ion/Li-Polymer battery linear charger with system power path management. The charge process of AW32001E includes: Pre-Charge, Fast Charge and Constant Voltage Regulation. The charge parameters and operating modes are programmable through I²C interface. The charge process runs automatically and recharging occurs when the battery voltage drops below V_{BAT_REG}-V_{RCH} after the charge done status.

The AW32001E is targeted at space limited portable applications. The chip can take input power from either an AC adaptor or a USB port to supply the system load and charge the battery. Meanwhile, the chip provides system short circuit protection function by limiting the current from the input to the system and the battery to the system. These features are effective to protect the battery or chip from damage. The parameters of input current limit, the discharge current limit and safety timer can be programmed by the I²C interface. Additionally, input over voltage protection, input under voltage lockout and input headroom voltage are integrated for good input source detection.

AW32001E separates the charging route from the system power supply to fulfill the power management function. The system power supply is at first priority with no dependency on battery existence. Once a bad power-limited adapter appears at the input, AW32001E would reduce the charging current firstly. If the system load is still too heavy for input source, AW32001E will reduce the input-system current to prevent the input source from being pulled down. Under this circumstance, if the system voltage drops 30mV below the battery voltage, the battery to system supply route will be fully turned on to power the system load, which is supplement mode.

Typical Application Circuit

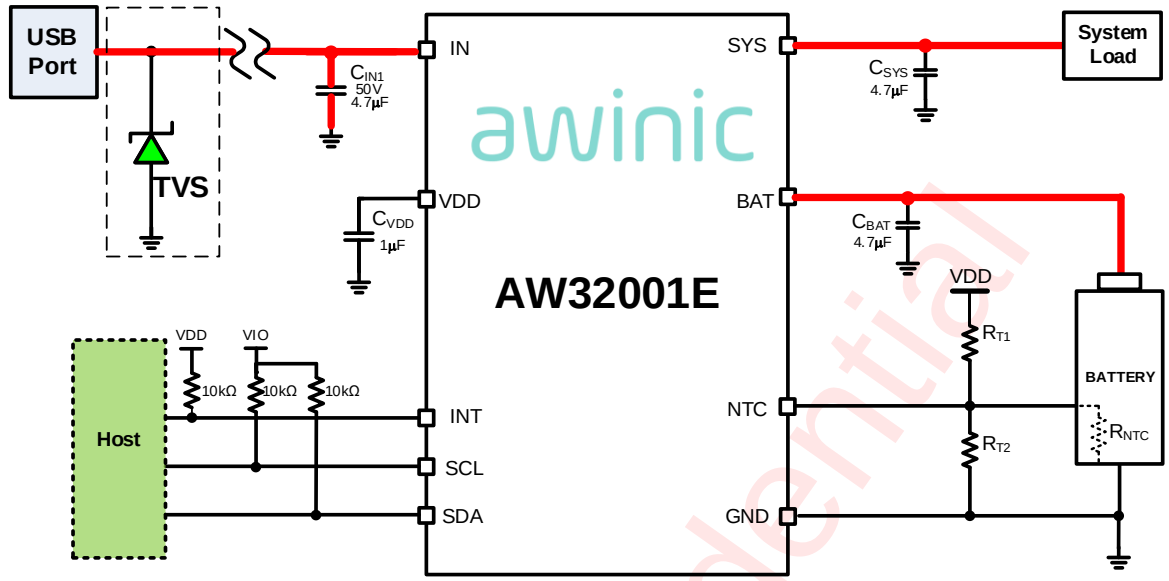


Figure 1 Typical Application Circuit of AW32001E

Pin Configuration and Top Mark

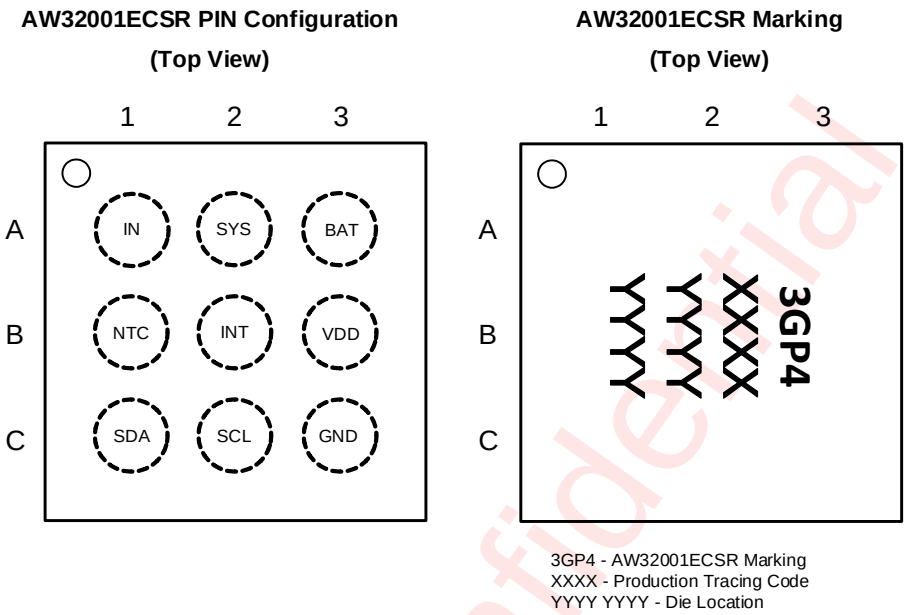


Figure 2 Pin Configuration and Top Mark

Pin Definition

Pin No.	Pin Name	Description
A1	IN	Input power pin. Bypass with a 4.7μF capacitor to GND.
A2	SYS	System power supply pin. Bypass with a 4.7μF capacitor to GND.
A3	BAT	Battery pin. Bypass with a 4.7μF capacitor to GND.
B1	NTC	Temperature sense input. Connect a negative temperature coefficient thermistor. Program the hot and cold temperature window with resistor dividers from VDD to GND, and NTC is the middle node. Pull NTC to VDD if NTC function is not used. If NTC function is unused, it is suggested to disable the NTC function and tie the NTC port to VDD for decreasing leakage current of battery, because PCB_OTP is default.
B2	INT	Interrupt output. The INT pin can send charge status and fault interrupt to the host. This pin is also used to disconnect the system from battery, and awake the chip from shipping mode. If INT is unused, it is suggested to tie INT to VDD by resistor.
B3	VDD	Internal power supply pin. Bypass with a 1μF capacitor to GND. No external load is allowed.
C1	SDA	I^2C Interface serial date.
C2	SCL	I^2C Interface clock.
C3	GND	Ground.

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW32001ECSR	-40°C～85°C	WLCSP 1.68mm×1.68mm-9B	3GP4	MSL1	ROHS+HF	3000 units/ Tape and Reel

Absolute Maximum Ratings(NOTE1)

PARAMETERS		MIN	MAX	UNIT
Input voltage range V_{IN} (with respect to GND)	IN	-5	28	V
NTC voltage range V_{NTC} (with respect to GND)	NTC	-0.3	V_{VDD}+0.3	V
Other pins voltage range (with respect to GND)	SYS, BAT (NOTE 2), INT, VDD, SCL, SDA	-0.3	6	V
Operating free-air temperature range		-40	85	°C
Operating junction temperature T_J		-40	150	°C
Storage temperature T_{STG}		-65	150	°C
Lead temperature (Soldering 10 seconds)			260	°C

NOTE1: *Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.*

NOTE2: BAT pin can handle 8.9V transients for less than 10us

ESD Rating and Latch Up

PARAMETERS	VALUE	UNIT
HBM (Human Body Model) (NOTE 3)	±2	kV
CDM(NOTE 4)	±1.5	kV
Latch-Up(NOTE 5)	+IT：200 -IT：-200	mA

NOTE3: *The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2017*

NOTE4: Test method: ESDA/JEDEC JS-002-2018

NOTE5: Test method: JESD78E

Recommended Operating Conditions

PARAMETERS	MIN	NORM	MAX	UNIT
Supply voltage range V_{IN}	4		5.5	V
Supply current I_{IN}			550	mA
Discharge current I_{BAT}			3.2	A
Charge current I_{CHG}	2		512	mA
Battery regulated voltage V_{BAT_REG}	3.6		4.545	V
Operating junction temperature T_J	-40		125	°C

Thermal Information

PARAMETERS	VALUE	UNIT
Junction-to-ambient thermal resistance θ_{JA}	122	°C/W

Electrical Characteristics

V_{IN}=5V, V_{BAT}=3.5V, T_J=25°C for typical values (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SOURCE AND BATTERY PROTECTION						
V_{IN_UVLO}	UVLO threshold voltage, entry UVLO	V_{IN} falling	3.5	3.6	3.7	V
	Hysteresis for UVLO	V_{IN} rising		300		mV
T_{DGL_UVLO}	Exit Deglitch time for V_{IN_UVLO}	Exits UVLO		30		ms
V_{IN_OVP}	VIN OVP threshold voltage	V_{IN} rising	5.85	6	6.15	V
	VIN OVP hysteresis	V_{IN} falling from above V_{IN_OVP}		350		mV
T_{DGL_OVP}	Exit deglitch time for V_{IN_OVP}	Exits V_{IN} OVP		30		ms
V_{BAT}	BAT input voltage				4.6	V
V_{BAT_UVLO}	UVLO threshold voltage for BAT voltage, V_{BAT} falling, entry UVLO	REG01H[2:0]=000	2.33	2.43	2.53	V
		REG01H[2:0]=100	2.64	2.76	2.88	V
		REG01H[2:0]=111	2.93	3.03	3.13	V
	Hysteresis voltage	V_{BAT_UVLO} =2.76V		190		mV
V_{HDRM}	Input vs. battery voltage headroom threshold	V_{IN} rising	80	130	170	mV
	Input vs. battery voltage headroom threshold hysteresis	V_{IN} falling		60		mV
CHARGE PROCESS						
V_{BAT_PRE}	Pre-charge to fast charge threshold	REG04H[1]=1, V_{BAT} rising	2.9	3.0	3.1	V
		REG04H[1]=0, V_{BAT} rising	2.7	2.8	2.9	V
	Fast charge to pre-charge threshold	V_{BAT} falling		200		mV
V_{BAT_REG}	Battery charge voltage regulation voltage	REG04H[7:2]=000000, V_{BAT_REG}=3.6V	3.585	3.600	3.615	V
		REG04H[7:2]=101000, V_{BAT_REG}=4.2V	4.180	4.200	4.220	V
		REG04H[7:2]=110100, V_{BAT_REG}=4.38V	4.360	4.380	4.400	V
		REG04H[7:2]=111110, V_{BAT_REG}=4.53V	4.507	4.530	4.553	V
V_{RECH}	Recharge threshold voltage	REG04H[0]=0, V_{BAT_REG}=4.2V, below V_{BAT_REG}	60	100	140	mV
		REG04H[0]=1, V_{BAT_REG}=4.2V, below V_{BAT_REG}	160	200	240	mV
	Deglitch time for V_{RCH}	V_{BAT} falling below V_{RECH} after charge termination		130		ms
V_{BAT_OVP}	Battery OVP threshold voltage	V_{BAT} threshold over V_{BAT_REG} to turn off charger during charging		130		mV
	V_{BAT_OVP} hysteresis			50		mV

Electrical Characteristics *(Continued)*

V_{IN}=5V, V_{BAT}=3.5V, T_J=25°C for typical values (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER PATH MANAGEMENT						
V_{SYS_REG}	Regulated system output voltage	V_{IN}=5.0V, REG07H[3:0]=0000, R_{SYS}=100Ω, I_{CHG}=0A, V_{SYS_REG}=4.2V	4.11	4.20	4.29	V
		V_{IN}=5.0V, REG07H[3:0]=1000, R_{SYS}=100Ω, I_{CHG}=0A, V_{SYS_REG}=4.6V	4.51	4.60	4.69	V
		V_{IN}=5.3V, REG07H[3:0]=1111, R_{SYS}=100Ω, I_{CHG}=0A, V_{SYS_REG}=4.6V	4.85	4.95	5.05	V
I_{IN_LIM}	Input current limit	REG00H[3:0]=0000, I_{IN_LIM}=50mA	30	45	60	mA
		REG00H[3:0]=0011, I_{IN_LIM}=140mA	112	125	140	mA
		REG00H[3:0]=1001, I_{IN_LIM}=320mA	275	296	320	mA
		REG00H[3:0]=1111, I_{IN_LIM}=500mA	440	460	500	mA
V_{IN_DPM}	Dynamic input power management clamp voltage	REG00H[7:4]=0000, V_{IN_DPM}=3.88V	3.68	3.88	4.18	V
		REG00H[7:4]=1000, V_{IN_DPM}=4.52V	4.32	4.52	4.82	V
		REG00H[7:4]=1111, V_{IN_DPM}=5.08V	4.88	5.08	5.35	V
R_{ON_Q1}	IN to SYS switches on resistance	V_{IN_DPM}=3.88V, V_{IN}=4.5V, I_{SYS}=100mA		300	350	mΩ
R_{ON_Q2}	BAT to SYS switch on resistance	V_{IN}<2V, V_{BAT}=3.5V, I_{SYS}=100mA		103	115	mΩ
I_{IN_Q}	Input quiescent current (not include the current from external NTC resistor)	V_{IN}=5V, EN_HIZ=0, CEB=0, **(charge enable)**, I_{CHG}=0, I_{SYS}=0		1.7	3.2	mA
		V_{IN}=5V, EN_HIZ=0, CEB=1, **(charge disabled)**, I_{CHG}=0, I_{SYS}=0		1.5	3.0	mA
I_{BAT_Q}	Battery quiescent current (not include the current from external NTC resistor)	V_{IN}=5V, CEB=0, charge done, I_{CHG}=0, I_{SYS}=0		58	80	μA
		V_{IN}=0, CEB=1, V_{BAT}=4.35V, DIS_PCB_OTP=1, I_{SYS}=0		21	32	μA
		V_{IN}=0, CEB=1, V_{BAT}=4.35V, DIS_PCB_OTP=0, I_{SYS}=0		27	38	μA
		V_{IN}=0, CEB=1, V_{BAT}=4.35V, DIS_PCB_OTP=0, I_{SYS}=0, enable watchdog		28	38	μA
		V_{BAT}=4.5V, V_{IN}=V_{SYS}=0, FET_DIS=1, shipping mode			1	μA
$I_{SYS\text{-}BAT\_LKG}$	SYS reverse to BAT switch leakage	V_{SYS}=4.60V, V_{IN}=5V, V_{BAT}=0, CEB=1, EN_HIZ=1, charge disabled			1	μA
I_{DSCHG}	BAT FET discharge current limit	REG03H[7:4]=0001, I_{DSCHG}=400mA	300	440	500	mA
		REG03H[7:4]=1001,I_{DSCHG}=2000mA		2000		mA
V_{FWD}	Ideal diode forward voltage in supplement mode	50mA discharge current		30		mV

Electrical Characteristics *(Continued)*

V_{IN}=5V, V_{BAT}=3.5V, T_J=25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CHARGE CURRENT						
I_{CHG}	Output charge regulation current programmable range	$V_{BAT\_PRE}<V_{BAT}<V_{BAT\_REG}$, REG0BH[7]=1, I_{CHG}=2mA	1.5	2	2.5	mA
		$V_{BAT\_PRE}<V_{BAT}<V_{BAT\_REG}$, REG0BH[7]=0, I_{CHG}=8mA	6.9	8	9	mA
		$V_{BAT\_PRE}<V_{BAT}<V_{BAT\_REG}$, REG0BH[7]=0, I_{CHG}=96mA	89	96	103	mA
		$V_{BAT\_PRE}<V_{BAT}<V_{BAT\_REG}$, REG0BH[7]=0, I_{CHG}=264mA	252	264	276	mA
		$V_{BAT\_PRE}<V_{BAT}<V_{BAT\_REG}$, REG0BH[7]=0, I_{CHG}=456mA	434	456	478	mA
	Charge Current Regulation Accuracy	V_{BAT}=3.8V, I_{CHG}=2mA	-25		25	%
		V_{BAT}=3.8V, 4mA<I_{CHG}≤12mA	-20		20	%
		V_{BAT}=3.8V,12mA<I_{CHG}<264mA	-7		7	%
		V_{BAT}=3.8V, I_{CHG}≥264mA	-5		5	%
I_{PRE}	Pre-charge current programmable range, I_{PRE}=I_{TERM}	V_{BAT}<3.0V	1		31	mA
I_{TERM}	Termination charge current threshold, programmable	REG03H[3:0]=0000, I_{CHG}=1mA	0.8	1	1.2	mA
		REG03H[3:0]=0001, I_{CHG}=3mA	2.6	3	3.3	mA
		REG03[3:0]=0101, I_{CHG}=11mA	9.5	11	13	mA
		REG03H[3:0]=1111, I_{CHG}=31mA	28	31	34	mA
T_{TERM}	Termination deglitch time	I_{CHG}<I_{TERM}, REG0CH[6]=0		3.2		s
I_{DBAT}	Battery detection current before charge done (sink current)	Begins after termination detected and V_{BAT}< V_{BAT_REG}		0.5		mA
T_{DBAT}	Battery detection time			262		ms
INT						
V_{OL_INT}	Low-level output saturation voltage, INT pin	I_O=5mA, sink current			0.4	V
I_{LKG_INT}	High-level leakage current for INT	INT is in High-impedance status, V_{INT}=5V			1	μA
T_{RST_DGL}	INT pulled low time to reset V_{SYS}	V_{INT} low(default setting)		16		s
I²C BUS LOGIC LEVELS AND TIMING CHARACTERISITICS						
V_{OL}	Output low threshold level	I_O=5mA, sink current			0.4	V
V_{IL}	Input low threshold level	V_{pull_up}=1.8V, SDA and SCL			0.4	V
V_{IH}	Input high threshold level	V_{pull_up}=1.8V, SDA and SCL	1.3			V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{BIAS}	Input bias current	V_{pull_up}=1.8V, SDA and SCL			1	μA
THERMAL PROTECTION						
T_{J_REG}	Junction temperature regulation	Junction temperature rising		120		°C
T_{OTP}	Overheating shutdown protection temperature	Junction temperature rising		150		°C
	Thermal hysteresis for T_{OTP}	Junction temperature falling		20		°C
I_{NTC}	NTC pin output current	CEB=0, NTC=3V	-1	0	1	μA
V_{COLD}	NTC cold temp rising threshold	Percentage of VDD	62	64	66	%
	Hysteresis voltage			60		mV
V_{HOT}	NTC hot temp falling threshold	Percentage of VDD	31	33	35	%
	Hysteresis voltage			70		mV
V_{HOT_PCB}	NTC hot temp falling threshold for PCB OTP	Percentage of VDD	31	33	35	%
	Hysteresis voltage			70		mV
SHIPPING MODE EXIT TIME						
$T_{EXIT\_SHIPMODE}$	VBUS Plug in	REG0BH[0]=0	1.8	2	3.3	s
		REG0BH[0]=1	90	100	111	ms
	Put down INT PIN	REG22H[3]=0	1.8	2	3.3	s
		REG22H[3]=1	90	100	111	ms
CLOCK FREQUENCY AND WATCHDOG TIMER						
F_{CLK}	Clock frequency			250		KHz
t_{WDT}	Watchdog timer	REG05H[6:5]=11		160		s

Electrical Characteristics *(Continued)*

V_{IN}=5V, V_{BAT}=3.5V, T_J=25°C for typical values (unless otherwise noted)

I²C INTERFACE TIMING

SYMBOL	DESCRIPTION		MIN	TYP	MAX	UNIT
F_{SCL}	Interface Clock Frequency				400	kHz
$T_{DEGLITCH}$	Deglitch Time	SCL		83		ns
		SDA		115		ns
$t_{HD:STA}$	(Repeat-Start) Start Condition Hold Time		0.6			μs
t_{LOW}	Low Level Width of SCL		1.3			μs
t_{HIGH}	High Level Width of SCL		0.6			μs
$t_{SU:STA}$	(Repeat-Start) Start Condition Setup Time		0.6			μs
$t_{HD:DAT}$	Data Hold Time		0			μs
$t_{SU:DAT}$	Data Setup Time		0.1			μs
t_R	Rising Time of SDA and SCL				0.3	μs
t_F	Falling Time of SDA and SCL				0.3	μs
$t_{SU:STO}$	Stop Condition Setup Time		0.6			μs
t_{BUF}	Time Between Start and Stop Condition		1.3			μs

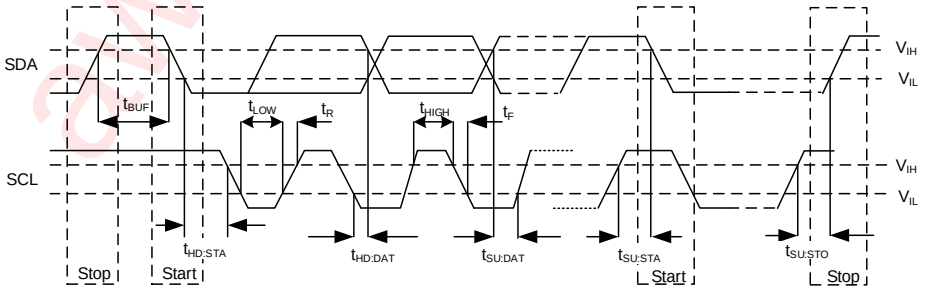


Figure 3 I²C Interface Timing

Typical Characteristics

V_{IN}=5V, T_J=25°C, I_{IN_LIM}=500mA, I_{CHG}=128mA, V_{IN_DPM}=4.6V, unless other noted.

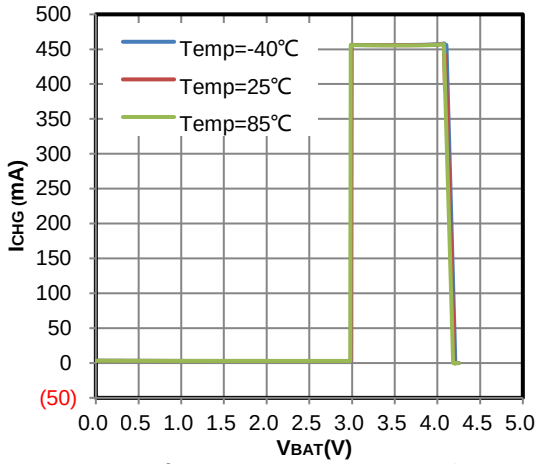


Figure 4 I_{CHG} vs. V_{BAT}, V_{IN}=5.0V

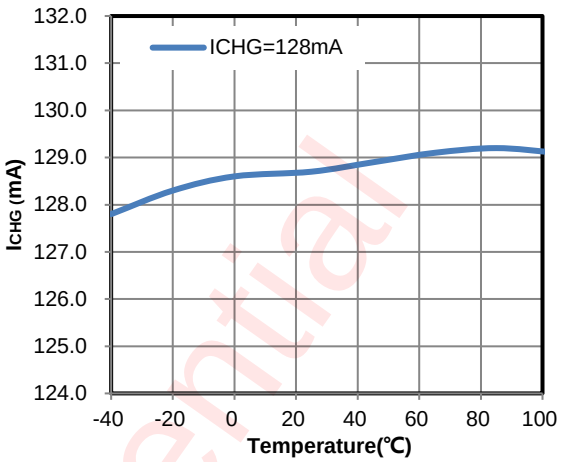


Figure 5 I_{CHG} vs. Temp, I_{LOAD}=0

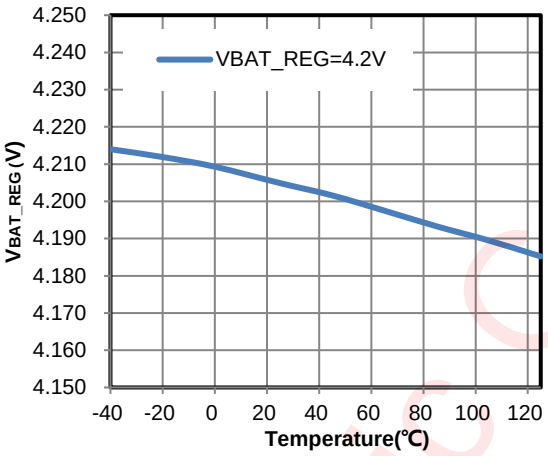


Figure 6 V_{BAT_REG} vs. Temp, I_{BAT}=0

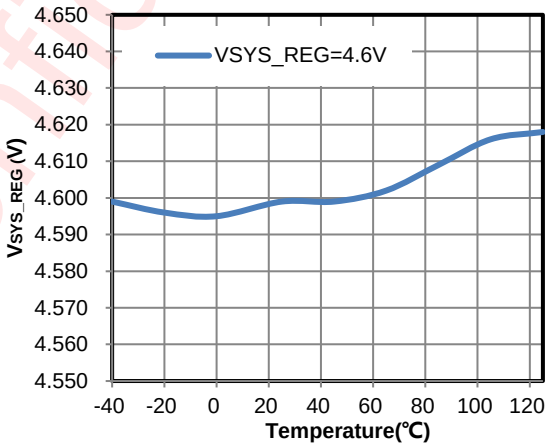


Figure 7 V_{SYS_REG} vs. Temp, I_{SYS}=0

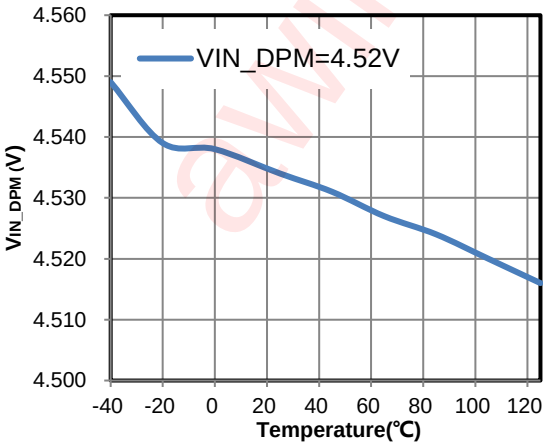


Figure 8 V_{IN_DPM} vs. Temp, I_{SYS}=0

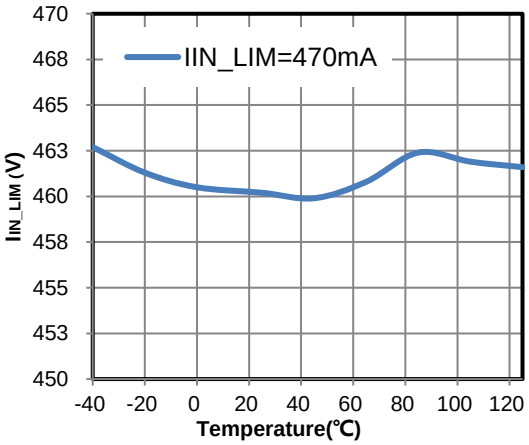
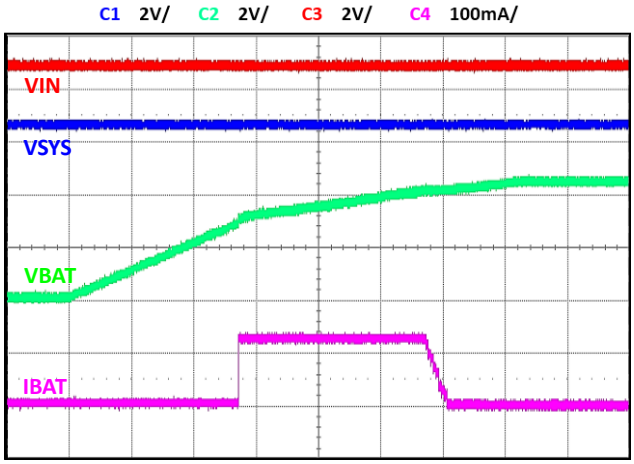


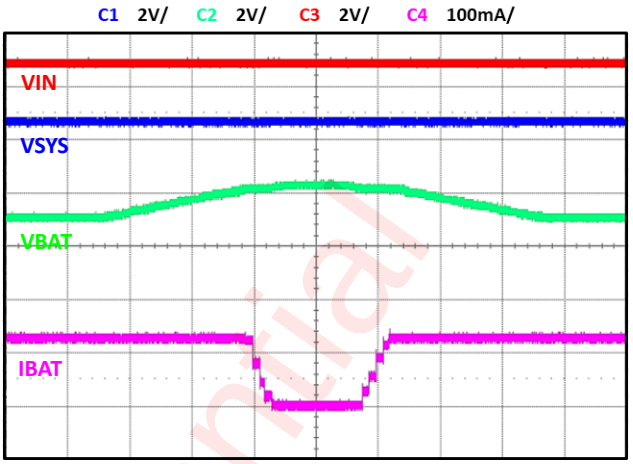
Figure 9 I_{IN_LIM} vs. Temp,

Typical Characteristics

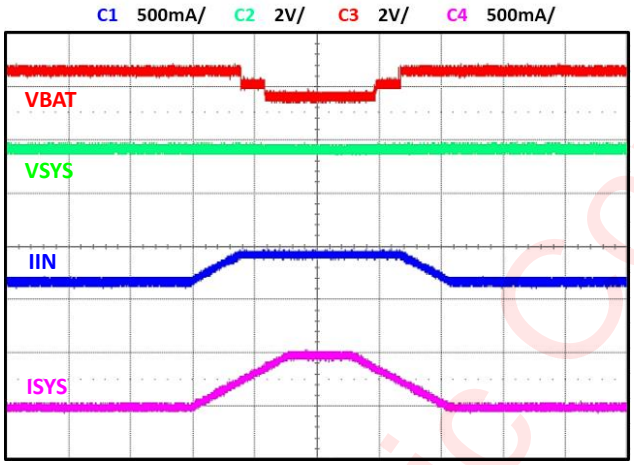
V_{IN}=5V, T_J=25°C, I_{IN_LIM}=500mA, I_{CHG}=128mA, V_{IN_DPM}=4.6V, unless other noted.



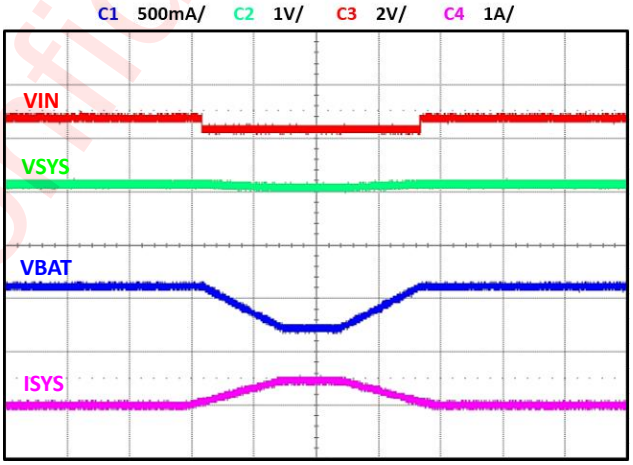
I_{SYS}=0A
Battery Charge Curve



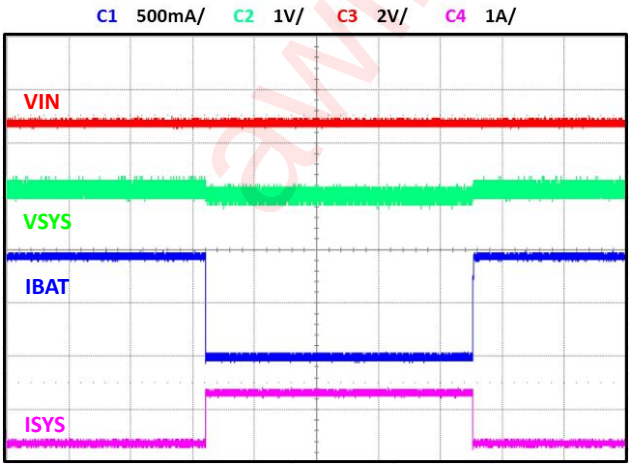
I_{SYS}=0A
Auto-Recharge Curve



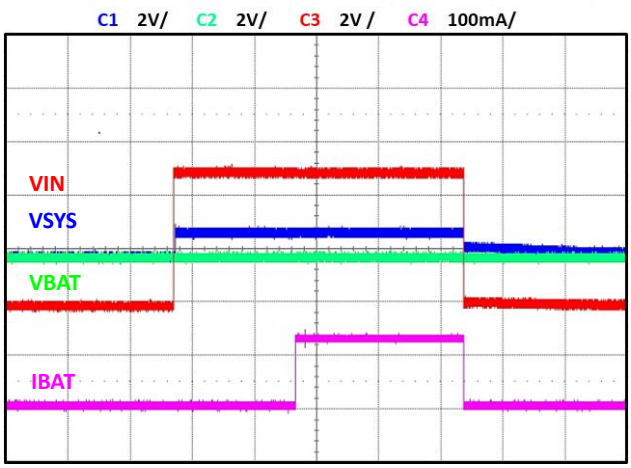
V_{BAT}=3.7V
Input Current Limit-Based PPM



V_{IN}=5V/200mA, V_{BAT}=3.7V
Input Voltage Regulation-Based PPM



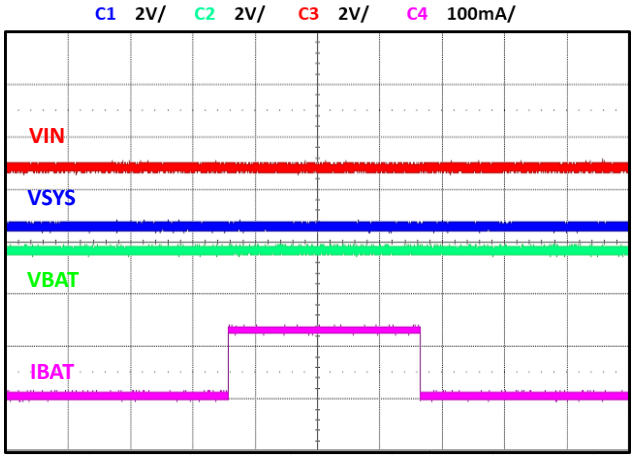
V_{IN}=5V, V_{BAT}=3.7V, I_{CHG}=456mA, I_{SYS}=0A~1A
SYS Load Transient



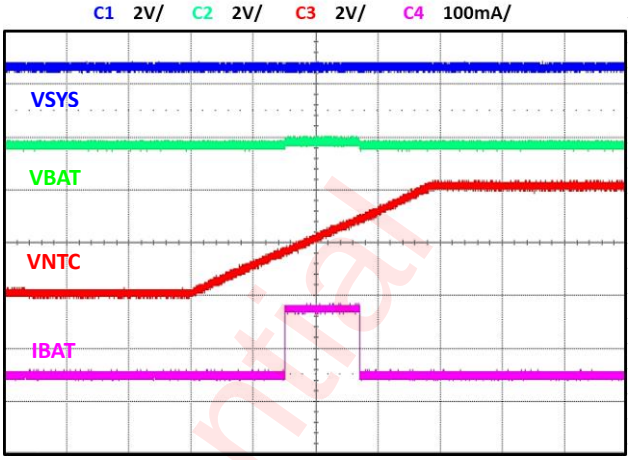
V_{BAT}=3.7V, I_{SYS}=0A
Power On/Off

Typical Characteristics *(Continued)*

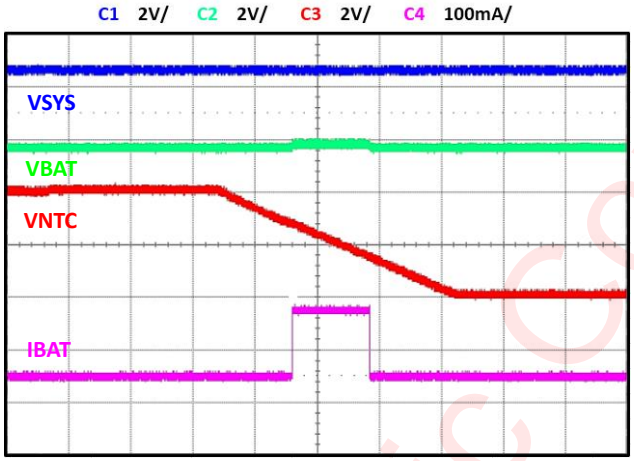
V_{IN}=5V, T_J=25°C, I_{IN_LIM}=500mA, I_{CHG}=128mA, V_{IN_DPM}=4.6V, unless other noted.



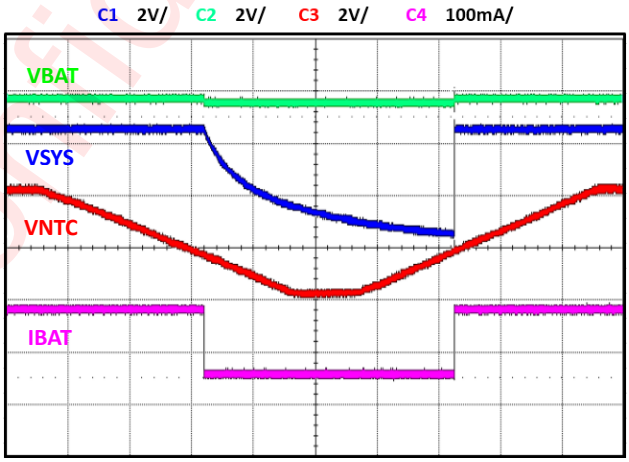
V_{BAT}=3.7V, I_{SYS}=0A
Charge Enable/Disable



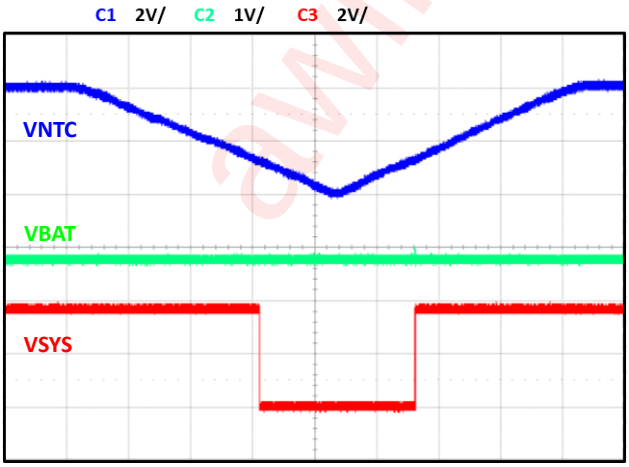
V_{BAT}=3.7V, I_{SYS}=0A, PCB_OTP disabled
NTC Rising



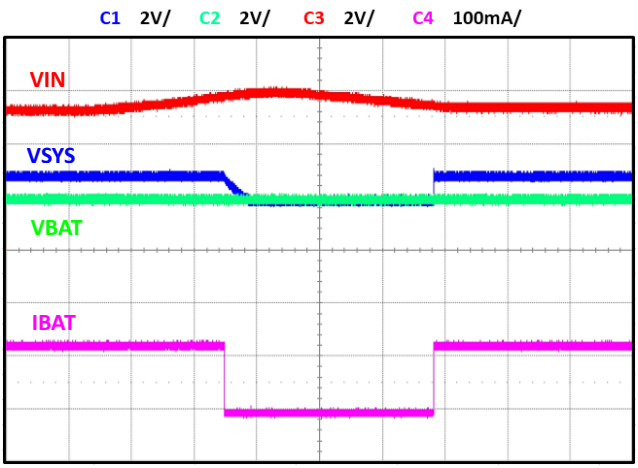
V_{BAT}=3.7V, I_{SYS}=0A, PCB_OTP disabled
NTC Falling



V_{BAT}=3.7V, I_{SYS}=0A
PCB_OTP @Charge mode

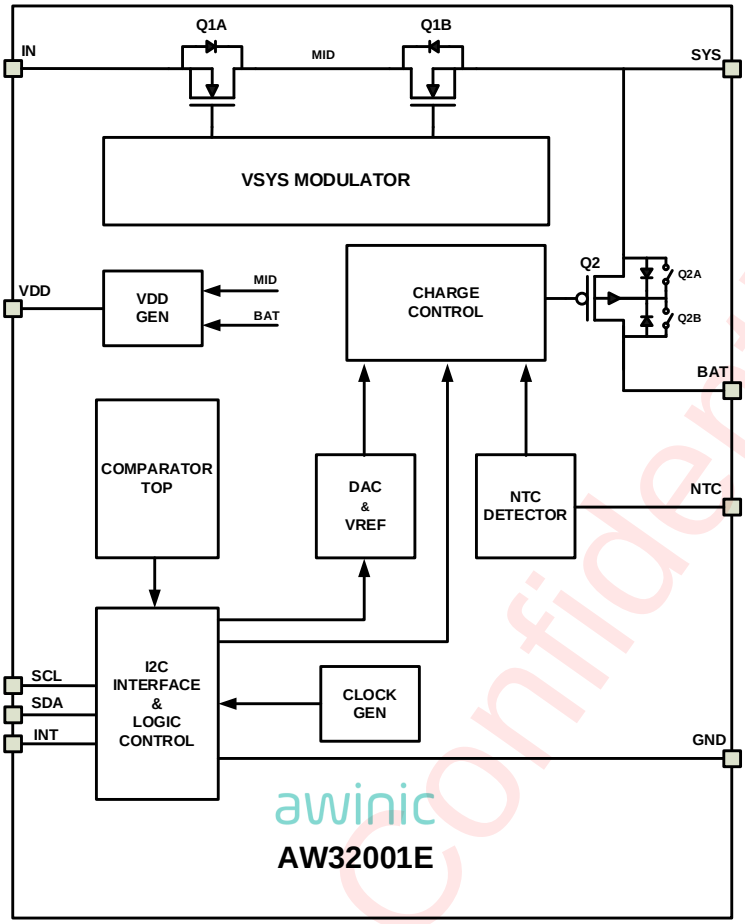


V_{IN}=0V, V_{BAT}=3.7V
PCB_OTP @Discharge mode



V_{BAT}=3.7V, I_{SYS}=0A
V_{IN} OVP Operation

Functional Diagram



SYS	Q2A	Q2B
>V_{BAT}	ON	OFF
<V_{BAT}	OFF	ON

Figure 10 Functional Block Diagram

Detailed Functional Description

The AW32001E is a highly integrated linear battery charger with a complete power path management function (PPMF). The full-charge process of AW32001E not only includes pre-charge, constant-current fast charge (CC) and constant voltage (CV) regulation, but also charge termination, auto-recharge, etc. The PPMF can manage the input source to power the system load and charge the battery simultaneously. The system load has a higher priority than the charge current. When the input power is limited by input current or voltage, the charge current will decrease automatically.

Main Machine

AW32001E includes: START, Battery Discharge Mode(DISCHG), Battery Charge Mode(CHG), Only Power System Mode(OPSM) and Shipping Mode(SHIP), Figure 11 is shown the main state machine conversion.

(1) Battery Discharge Mode: Only Battery to SYS Path is enabled.

(2) Battery Charge Mode: IN to SYS path and SYS to Battery path are enabled.

(3) Only Power System Mode: Only IN to SYS Path is enabled.

(4) Shipping Mode: All paths are disabled, AW32001E enters into low power consumption state.

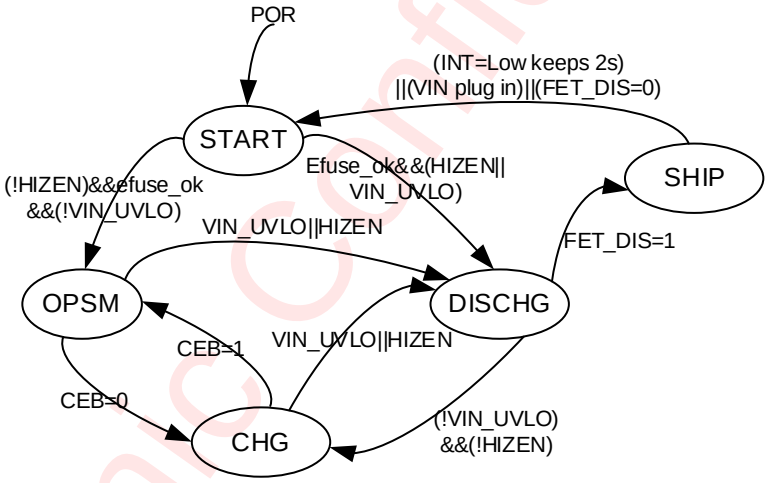


Figure 11 The main state machine conversion

The AW32001E integrates an input reverse-block FET (Q1A), a LDO FET (Q1B) between IN and SYS, and a BATFET (Q2) between SYS and BAT. When VBUS plugs in and CEB=1, the device works in OPSM mode that only IN and SYS path is enabled, the system is powered by VBUS. If CEB=0, the charge function is enabled and Q2 turn on, the status switches to Battery Charge mode(CHG). When the system load demand is over the input power capacity, the PPMF of AW32001E will reduce the charging current or use power from the battery to satisfy the system load. The charge current is limited to maintain the system power supply with higher priority all the time. Figure 12 shows the PPMF structure of the AW32001E, which is called Battery Supplement Mode too. Once the VBUS is unplugged, the BATFET Q2 is turn on fully to supply the system, and the charger enters into Battery Discharge Mode(DISCHG). Further, the device can turn off BATFET so that the system voltage is zero to minimize the battery leakage current. When the host set FET_DIS=1, the charger can turn off BATFET Q2 and entries Shipping Mode(SHIP).

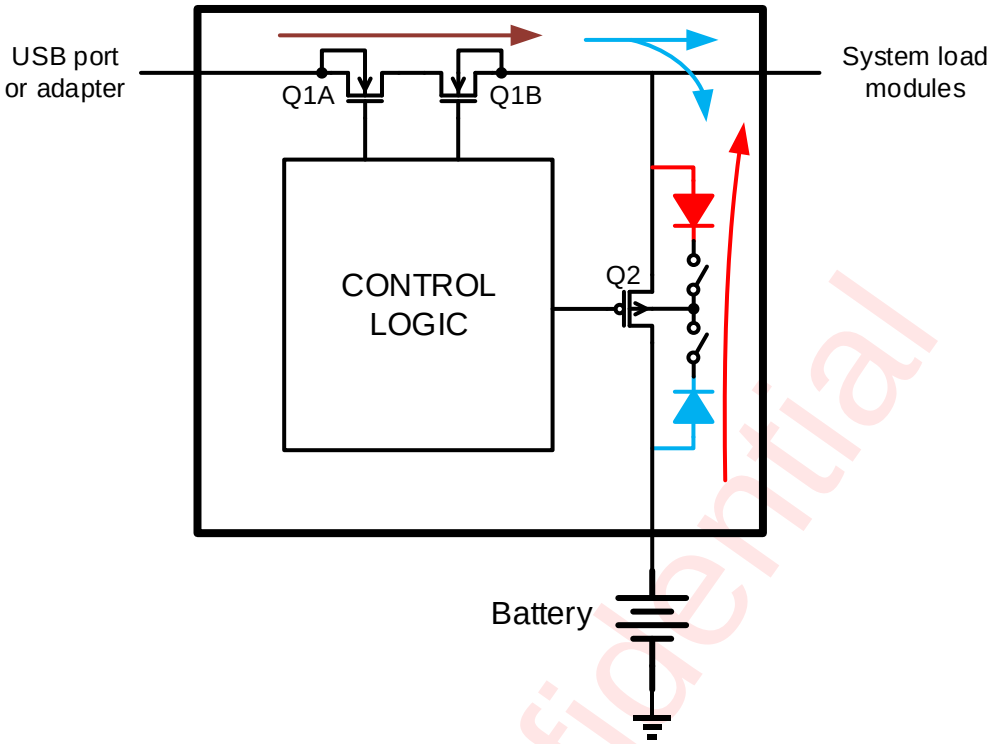


Figure 12 Power Path management Structure

In Battery Charge Mode, the Q2 works as a fully featured linear charger with pre-charge, fast charge, constant voltage charge, charge termination, auto-recharge, thermal protection, built-in timer control and NTC monitoring. The charge current can be programmed via the I²C interface. When the chip's temperature exceeds the thermal regulation threshold (120°C default), the IC controls the charge current to reduce its temperature.

Power Supply

The AW32001E chooses the higher voltage of either BAT or IN to power VDD and the internal bias circuit, showed as Figure 13. When BAT or IN voltage rises above its respective power on reset (POR) threshold, the internal control circuit will wake up and the I²C interface will be ready for communication with all of registers reset to default value. These registers can be controlled by the host.

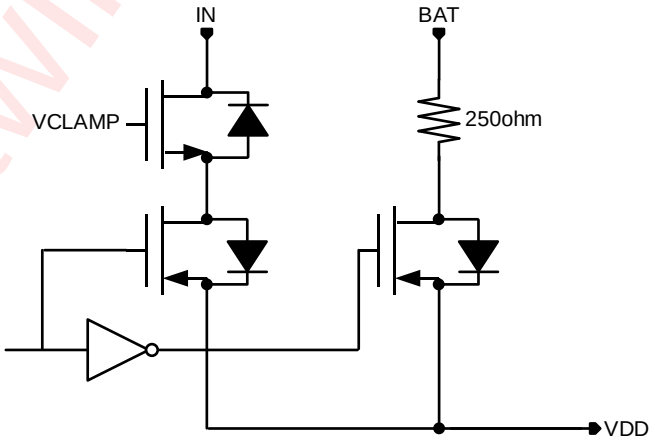


Figure 13 The inner power supply sources selection circuit for VDD

VIN OVP, VIN UVLO and VIN GOOD

The AW32001E has an input UVLO and over-voltage protection (OVP) threshold. The Q1 is turned off immediately when the input voltage is out of its operating range.

The input over-voltage protection is integrated to prevent the device and other components from damage of the high input voltage (Voltage from V_{IN} to GND). If the voltage at V_{IN} pin exceeds V_{IN_OVP} threshold(6V typical), the chip will turn off Q1. When V_{IN} drops lower than the input overvoltage exit threshold (5.65V typical) and continues to exceed T_{DGL_OVP}(30ms typical), Q1 will be turned on again.

When V_{IN} falls below V_{UVLO}, the Q1 is also turned off and the input to system loop controller is shut down. Once V_{IN} rises above V_{UVLO}+300mV and continues to exceed T_{DGL_UVLO}(30ms typical), the Q1 is turned on and relative circuits start working.

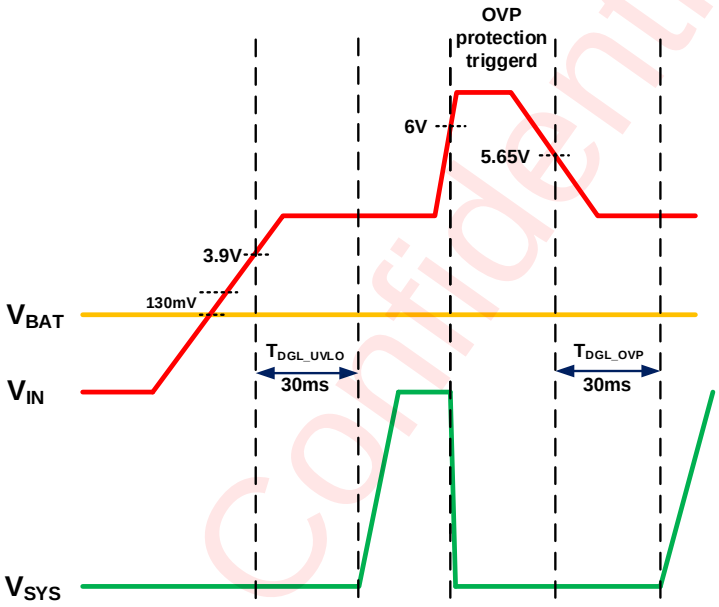


Figure 14 Input Power Detection Operation

Either V_{IN} OVP or V_{IN} UVLO had happened, the device send out a 256μs low-state interrupt pulse from INT port, indicated a power fail status as REG08H[1]=0 and a fault status as REG09H[5]=1, which are read clear.

The VIN GOOD status not only means that VIN is between V_{IN_UVLO} and V_{IN_OVP}, but also .includes that the VIN voltage increase is higher than VBAT+170mV(130mV typical), and higher than VSYS+75mV(50mV typical). The all conditions have satisfied, and enter VIN GOOD. VIN voltage reduction meets VIN<VBAT+60mV or VIN<VSYS, exiting VIN GOOD.

Only Power System Mode

The device meets VIN GOOD, EN_HIZ=0(REG01H[4]=0) and CEB=1(REG01H[3]=1), and firstly enter Only Power System Mode(OPSM) which just turns on Q1A and Q1B, and supplies power the down-stream system by VBUS. If the device is configured CEB=0(REG01H[3]=0), the main state machine switches to Charge Mode from the Only Power System Mode.

Charge Mode

When AW32001E operation in Charge Mode, the DPM, PPMF, Battery Supplement and other functions are available. These functions are useful in some application.

Battery Regulation Voltage

The battery voltage of constant voltage regulation state is V_{BAT_REG}. When V_{BAT_REG} = 4.2V, the accuracy is ±0.5% in the range of 0°C to +50°C ambient temperature.

Input Current-and Input Voltage-Based Power Regulation

The AW32001E has an input current limit regulation to meet the input source's (typically USB) maximum current limit specification. The function is realized by monitoring the input current continuously. If the rating of input source is lower than the preset input current limit, the input current limitation works to protect the input source from being overloaded. The total input current limit value can be set by the register IIN_LIM (REG00H[3:0]), and the function can prevent the input source from being over-loaded.

Otherwise, when the load is over the input power capacity, the input voltage also can be regulated to V_{IN_DPM} for the input voltage-based DPM regulation. V_{IN_DPM} can be set via the register VIN_DPM (REG00H[7:4]), and the V_{IN_DPM} should be at least 250mV higher than V_{BAT_REG} to ensure the stable operation of the regulator. The register DIS_VINLOOP=1 (REG07H[6]=1) can be set to disable the input voltage limit function.

Either the input voltage or input current limit is reached, the total input power is limited by regulating the Q1B FET between IN and SYS. As a result, the system voltage drops. When the system voltage decrease to a **minimum value** of V_{SYS_REG} - 135mV and V_{IN} - 345mV, the charge current is reduced to prevent the system voltage from dropping further.

Power Path Management Function (PPMF)

The AW32001E can decouple the system from the battery by employs a PPMF with the Q2, which allows the device to control Q2 between the system and the battery separately. The system has high priority to start up by regulating the integrated Q1B even the battery is in a deeply discharged or missing state. The function of Q1A, Q1B and Q2 can be controlled by the I^2C as shown in table 1.

Table 1: FET Control via I^2C

FET On/Off Changed by Control	HI-Z Mode and Charge Control	
	Set EN_HIZ = 1	Set CEB = 1
Q1A and Q1B	OFF	x
Q2(Charge Mode)	x	OFF
Q2(Battery Discharge Mode)	x	x

NOTE: x=Don't care.

For the system voltage control, when the input voltage is lower than V_{SYS_REG}, the Q1A and Q1B are fully on with the input current limit. When the input voltage is higher than V_{SYS_REG}, the system voltage is regulated to V_{SYS_REG}. The V_{SYS_REG} can be programmed through REG07H[3:0].

Battery Supplement Mode

When DPM occurs, the charge current is reduced to keep the input current or input voltage in regulation. If the charge current has already reduced to zero and the input source is still overloaded, the system voltage begins decreasing. If the system voltage drops to 30mV below the battery voltage, the AW32001E will enters battery supplement mode, and the ideal diode is enabled. If I_{DSCHG} (supplement current) * R_{ON_BATT} is lower than 30mV, the Q2 is regulated to keep V_{BAT} - V_{SYS} at 30mV. If this regulation cannot maintain 30mV voltage drop due to heavy load from SYS, the Q2 will fully turn on to maintain the ideal forward voltage. When the system load decreases, the system voltage starts to increase. The ideal diode mode is disabled, when V_{SYS} is higher than V_{BAT} + 20mV. Figure 15 shows the DPM and battery supplement mode operation profile.

When V_{IN} is not available, the AW32001E operates in discharge mode. During in discharge mode, the Q2 is fully on to reduce power loss.

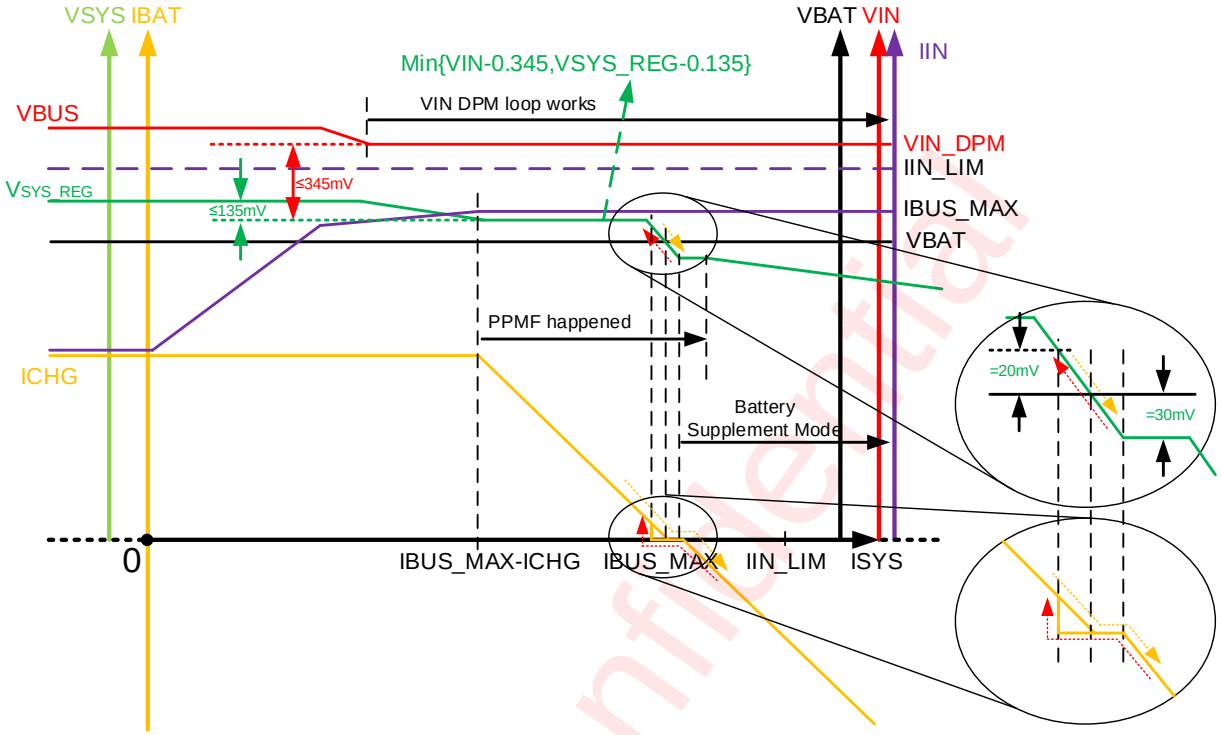


Figure 15 DPM and Battery Supplement Operation Profile (Bad adaptor inserted)

NOTE: IBUS_MAX is the maximum output current of the input source.

Battery Charge Profile

The AW32001E has three main charging processes: pre-charge, fast constant current charge(CC), and fast constant voltage charge(CV):

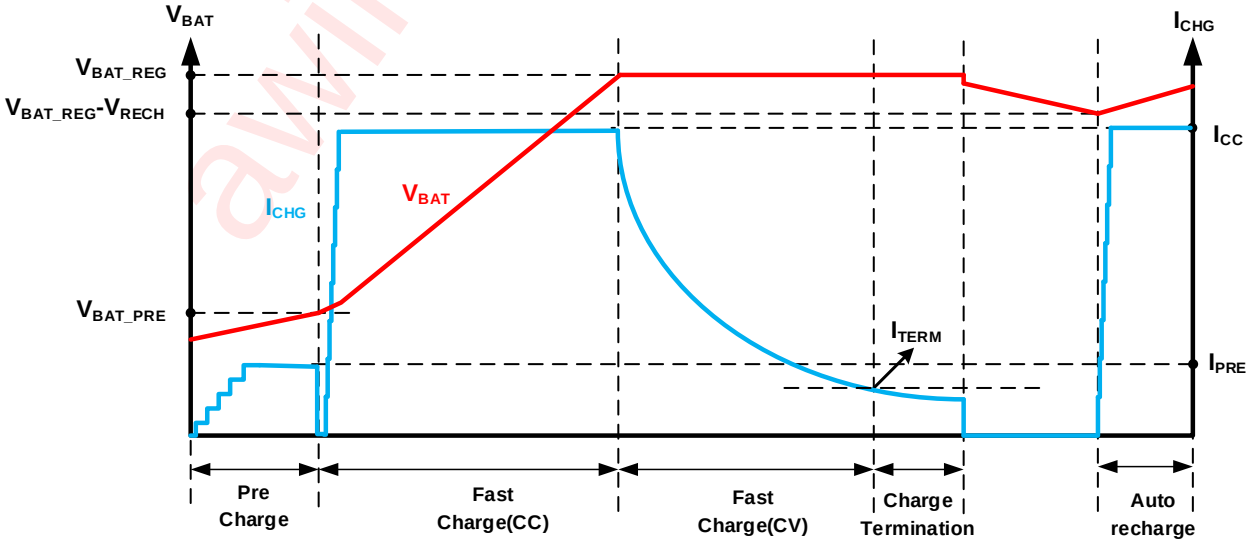


Figure 16 Battery Charge Profile

- Pre-charge: In the pre-charge process, the IC charges the deeply depleted battery safely with small current until the battery voltage rise to the pre-charge threshold (V_{BAT_PRE}), and then the chip enters the fast-charge process. If the V_{BAT} is not increasing to exceed than V_{BAT_PRE} before the pre-charge timer expires (1 hour), the charge cycle stops, and a corresponding timeout fault signal is asserted. The register REG03H[3:0] can be set the current of pre-charge.
- Fast constant current charge: When V_{BAT} exceeds V_{BAT_PRE}, the AW32001E enters the fast constant charge process. The REG02H[5:0] can be set to change the fast-charge current .
- Fast constant voltage charge: The charge mode changes from CC mode to CV mode when the V_{BAT} rises to the battery-full voltage (V_{BAT_REG}) set via REG04H[7:2]. At the same time, the charge current starts decreasing in CV charge process.

Due to multiple loop regulations, such as dynamic power management (DPM) regulation (input voltage, input current) or thermal regulation, the actual charge current may be less than the setting value.

When the charge current is smaller than termination current threshold I_{TERM} for 3.2s in CV process, the charge cycle will be completed, and the charge status is updated to charge done. The register REG03[3:0] can set the termination charge current threshold I_{TERM}. The termination function can be disabled via EN_TERM=0 (REG05H[4]=0). Meanwhile, the register bit TERM_TMR (REG05H[0]) is able to control whether the charge process continue or not when the termination conditions are met. The termination function is shown as table 2.

Table 2: Termination Function Selection Table

EN_TERM	TERM_TMR	After Termination Condition is Met	
		Operation	Charge Status
0	x	Keep CV Charge	Charge
1	0	Charge done	Charge done
1	1	Keep CV Charge	Charge

Note: x=Don't care.

A new charge cycle starts when any of the following conditions are valid:

- Auto-recharge kicks in.
- Battery charging is enabled via the I^2C.
- The input power is recycled .

Under the following conditions:

- No safety timer fault.
- No thermistor fault at NTC.
- BFET is not forced off.
- No battery over-voltage event.

Automatic Recharge

After the charge process is completed and charge cycle is terminated, the system's consumption or battery self-discharge may cause the battery voltage to decrease. When the battery voltage falls below the recharge threshold and V_{IN} is still in the operating range, another new charging cycle will start automatically. The recharge threshold(below V_{BAT_REG}) V_{RECH} can be configured to 100mV or 200mV(default) via REG04H[0]

Battery Discharge Mode

In Battery discharge mode, The device has low quiescent current and low on-resistance of Q2 to help the battery working for a longer time. Once the discharge current exceeds the over discharge current threshold, the over discharge current protection works and ensures the IC work safely in different applications.

Battery Discharge Function

When the input source is absent and battery is connected to chip with the VBAT above V_{BAT_UVLO} threshold, the Q2 is fully on. During discharge mode, the 90mΩ Q2 can minimizes conduction loss.

Battery Disconnection Function

In some applications where the battery is not removable, it is essential to allow the system power to be reset in some applications or disconnect the battery from the system for shipping mode. The AW32001E provides both system reset function and shipping mode for different applications.

The INT pin can be used to cut off the path from the battery to the system under certain condition to reset the system manually. The battery is disconnected from the system, when the logic of INT is set low for longer than t_{RST_DGL} (which can be programmed by REG01H[7:6]). After a delay time of t_{RST_DUR} (REG01H[5]), the Q2 is turned on automatically, and the system is powered by the battery again. The t_{RST_DUR} can be programmed by REG01H[5]. During the off period, the INT pin is not limited to be high or low. Please notes that the t_{RST_DGL} counter is triggered by the falling edge of INT.

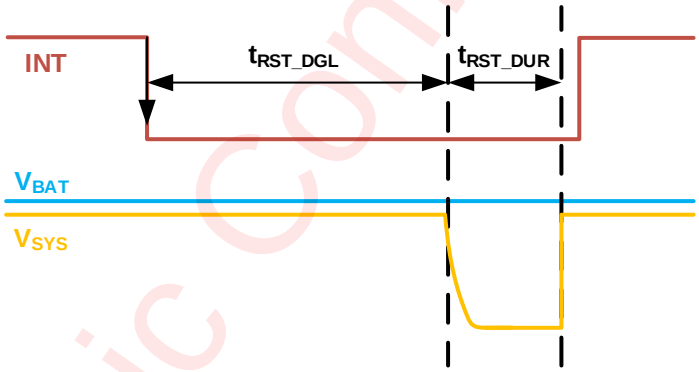


Figure 17 System Reset Function Operation Timing Diagram

Shipping Mode

The register bit FET_DIS (REG06H[5]) can be used to control the battery disconnection too. If the input source is absent, once setting FET_DIS=1, the AW32001E enters shipping mode after a delay time(default 1s). The delay time can be programmed by EN_SHIPPING_DGL(REG09H[7:6]). If the input source is present when FET_DIS is written to 1, chip will turn to shipping mode after 2s deglitch time with input voltage smaller than V_{IN_UVLO} threshold. Plug in the input adapter or pull the INT pin down for 2s or 100ms to wake the AW32001E up from shipping mode. The waking time can be configured in EN_SHIPMD_0P1S (REG0BH[0]) and INT100MS (REG22H[3]).

If INT PIN is shorted to ground or left floating before entering Shipping Mode, DIS_SHIPINT (REG0CH[2]) must be written to 1 to avoid bad Shipping Mode operation. In this case, the only method of exiting shipping mode is plugging in the input adapter.

Table 3: Shipping Mode Control

FET On/Off Changed by Control	Enter Shipping Mode	Exit Shipping Mode	
	Set FET_DIS to 1	INT H to L for 2s	Vin Plug-In
Q1	x	x	On
Q2	Off(1s later)	On	On(2s later)

Note: x=Don't care.

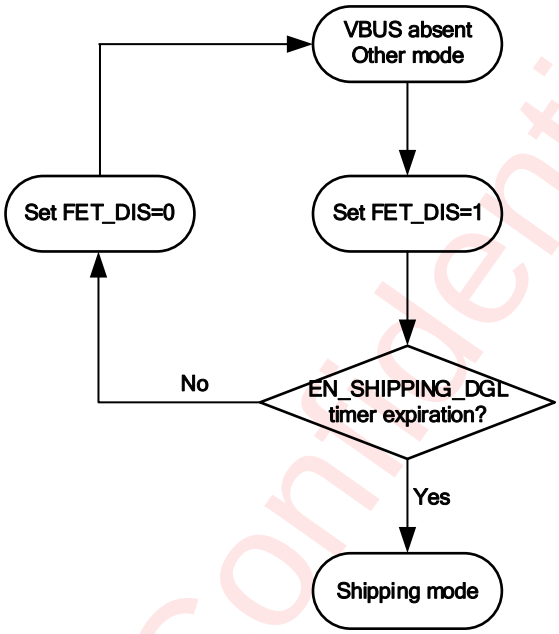


Figure 18 Enter Shipping Mode Timing Diagram(VBUS absent)

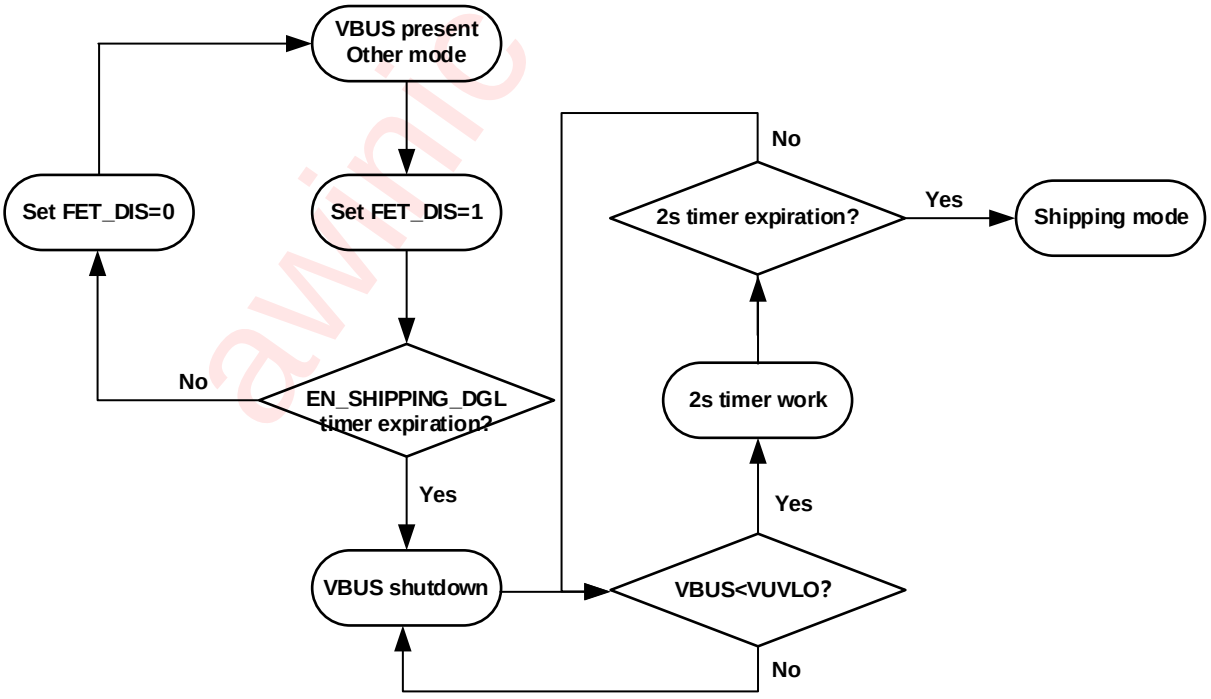


Figure 19 Enter Shipping Mode Timing Diagram(VBUS present)

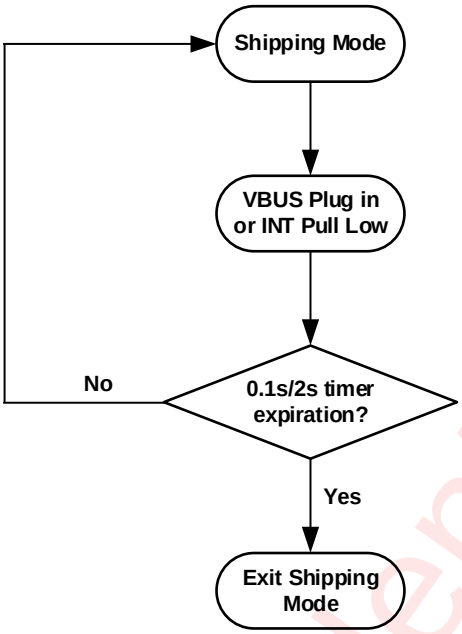


Figure 20 Exit Shipping Mode Timing Diagram

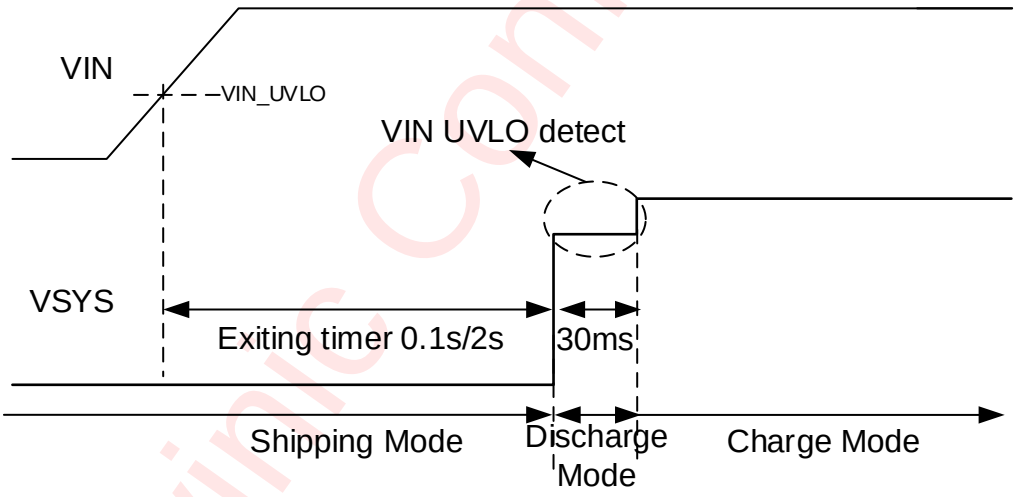


Figure 21 Recovery charging From Shipping Mode Operation Timing Diagram(VBUS Plug-In)

Protection Operation

The AW32001E has input OVP, UVLO, battery OVP and other functions to protect it's normal operation. Additionally, NTC function is integrated to prevent battery from high temperature danger. The following table 4 is all fault functions summary table.

Table 4: All fault functions summary table

Status	Operation Mode	Brief Function Description	Interrupt	Action
VIN GOOD	Charge, OPSM	V_{IN} rises above V_{BAT}+170mV and V_{SYS}+75mV，the device enters into VIN Good, V_{IN} falls down V_{BAT}+60mV or V_{SYS}-50mV, exits VIN GOOD. Entry and exit require 2ms to confirm.	Yes	Turn on Q1A and Q1B.
VIN UVLO	Charge, OPSM	V_{IN} falls down 3.3V, the deivce enters VIN UVLO immediately. V_{IN} rises above 3.6V and keeps 30ms, the device exits.	Yes	Turn off Q1A and Q1B.
VIN OVP	Charge, OPSM	V_{IN} rises above 6V, the device enters into VIN OVP immediately, V_{IN} falls down about 5.65V, exits VIN OVP. Exit requires 2ms to confirm.	Yes	Quickly turn off Q1B in 100ns.
VBAT OVP	Charge	After V_{BAT} rises above V_{BAT_REG}+130mV about 128us, the device enters into VBAT OVP. Once V_{BAT} falls down V_{BAT_REG}+50mV about 2ms, exits VBAT OVP.	Yes	Turn off Q2.
VBAT UVLO	Discharge, OPSM	When V_{BAT} rises above V_{BAT_UVLO}+190mV about 31ms (programmable 128us), the device exits into $V_{BAT\ UVLO}$. Once V_{BAT} falls down V_{BAT_UVLO} (programmable), enters $V_{BAT\ UVLO}$ immediately.	No	Turn off Q2.
OTP	Charge, OPSM, Discharge	When the junction temperature exceeds 150℃, IC shuts down. When the junction temperature falls below the thermal recovery temperature, approximately 120℃, the device restarts by using the soft-start sequence.	Yes	Turn off Q1B and Q2.
PCB OTP	Charge, OPSM, Discharge	PCB_OTP function is default settings. V_{NTC} falls down VDD×33%, PCB OTP is valid; Once V_{NTC} rises up VDD×33%+70mV for 31ms, the device exits PCB OTP.	Yes	Turn off Q1B and Q2.
NTC HOT	Charge	NTC HOT function is configured. V_{NTC} falls down VDD×33%, the device judges battery hot, and reports NTC HOT; Once V_{NTC} rises up VDD×33%+70mV for 31ms, the device exits NTC HOT.	Yes	Turn off Q2.
NTC COOL	Charge	NTC COOL function is configured. V_{NTC} rises up VDD×64%, the device judges battery cold, and reports NTC COOL; Once V_{NTC} falls down VDD×64%-60mV for 31ms, the device exits NTC COOL.	Yes	Turn off Q2.

VSYS SCP	Charge, OPSM, Discharge	When the events including $I_{SYS}>I_{OCP\_INSYS}$(2A), $I_{SYS}>I_{OCP\_BATSYS}$(3.7A), $I_{IN\_LIM}<I_{SYS}<I_{OCP\_INSYS}$ for 60us, and $I_{DSCHG}<I_{SYS}<I_{OCP\_BATSYS}$ for 60us happen during V_{SYS} launch and V_{SYS}<0.7V, or during working normally and V_{SYS}<1.5V, the device triggers V_{SYS} short protection immediately and work in Hiccup Mode. Turn off Q1 and Q2, and start up again after 1ms later.	No	Hiccup Mode. Turn off Q1 and Q2, and start up again after 1ms later
VBAT ODCP	Discharge, Supplement Mode	Over-discharge current protection. Once the I_{BAT} exceeds the programmable discharge current limit I_{DSCHG} (2A default) for 60μs. The AW32001E enters hiccup mode. In addition, if the discharge current goes high and reaches the internal fixed peak current limit (about 3.7A), the Q2 turns off and begins hiccup mode immediately.	No	Q2 turns off
Watch Dog fault	Charge, OPSM, Discharge	When the watchdog timer expires,, both the Q1 and Q2 are turned off, and most registers return to the default value, sent a watch dog fault interrupt to system.	Yes	Turn off Q1B and Q2. Reset CEB to 0.
Safety time fault	Pre Charge, Fast Charge	Pre-charge for more than 1 hour (Configurable), or faster charge for more than 5 hours (Configurable), entry to safety time fault.	Yes	Turn off Q1B and Q2. Reset CEB to 0.

Battery OVP(VBAT OVP)

The AW32001E has battery over-voltage protection (VBAT OVP) function (about 130mV higher than V_{BAT_REG}). When the battery OVP event occurs, AW32001E will stop the current charging cycle immediately and asserts a fault.

Negative Temperature Coefficient (NTC) Temperature Sensor

The AW32001E is able to use NTC to sense the battery temperature. By monitoring the thermistor (usually available in the battery pack), the battery is guaranteed to operate in safe environment.

The NTC function demands appropriately valued resistors connecting from VDD to NTC to ground. At the same time, connect a thermistor from the NTC pin to ground. The NTC voltage is determined by the resistor divider and thermistor, and the divide ratio depends on the temperature of thermistor. The upper and lower bound of NTC voltage is pre-determined in AW32001E.

In the AW32001E, PCB_OTP function is default settings. The I^2C can change the NTC and PCB_OTP functions (see Table 5).

Table 5: NTC Function Selection Table

I^2C Control		**Function**
EN_NTC	**DIS_PCB_OTP**	
0	x	Disable
1	1	NTC(resistor-divided)
1	0	PCB_OTP

NOTE: x=Don't care

When PCB_OTP is selected and the NTC voltage is lower than the NTC hot threshold, both the Q2 and Q1 are turned off. The NTC_FAULT status is set (REG09H[1]) to 1 to show the PCB_OTP fault. The IC Operation resumes, when the NTC voltage returns to safe range.

The NTC function works only in charge mode. Once the temperature is outside of the safe operating range, the IC stops charging state and report it on the status bits. When the temperature comes back to the safe range, the charge process resumes automatically.

Thermal Regulation and Thermal Shutdown

The internal junction temperature is monitored continuously to avoid overheating the chip and maximize power delivery. When the internal junction temperature reaches the preset limit T_{J_REG} (120°C default), the charge current starts reducing to prevent dangerous high power dissipation. The IC can work in diffident thermal requirements applications, because it has multiple thermal regulation thresholds from 60°C to 120°C. register REG07H bit [5:4] can set The junction temperature regulation threshold.

The device has a built-in temperature sensor which monitors the internal junction temperature. When the junction temperature exceeds 150℃, the Q1 and Q2 will turn off. When the junction temperature falls below the thermal recovery temperature, approximately 120℃, the device reworks.

System Short-Circuit Protection(VSYS SCP)

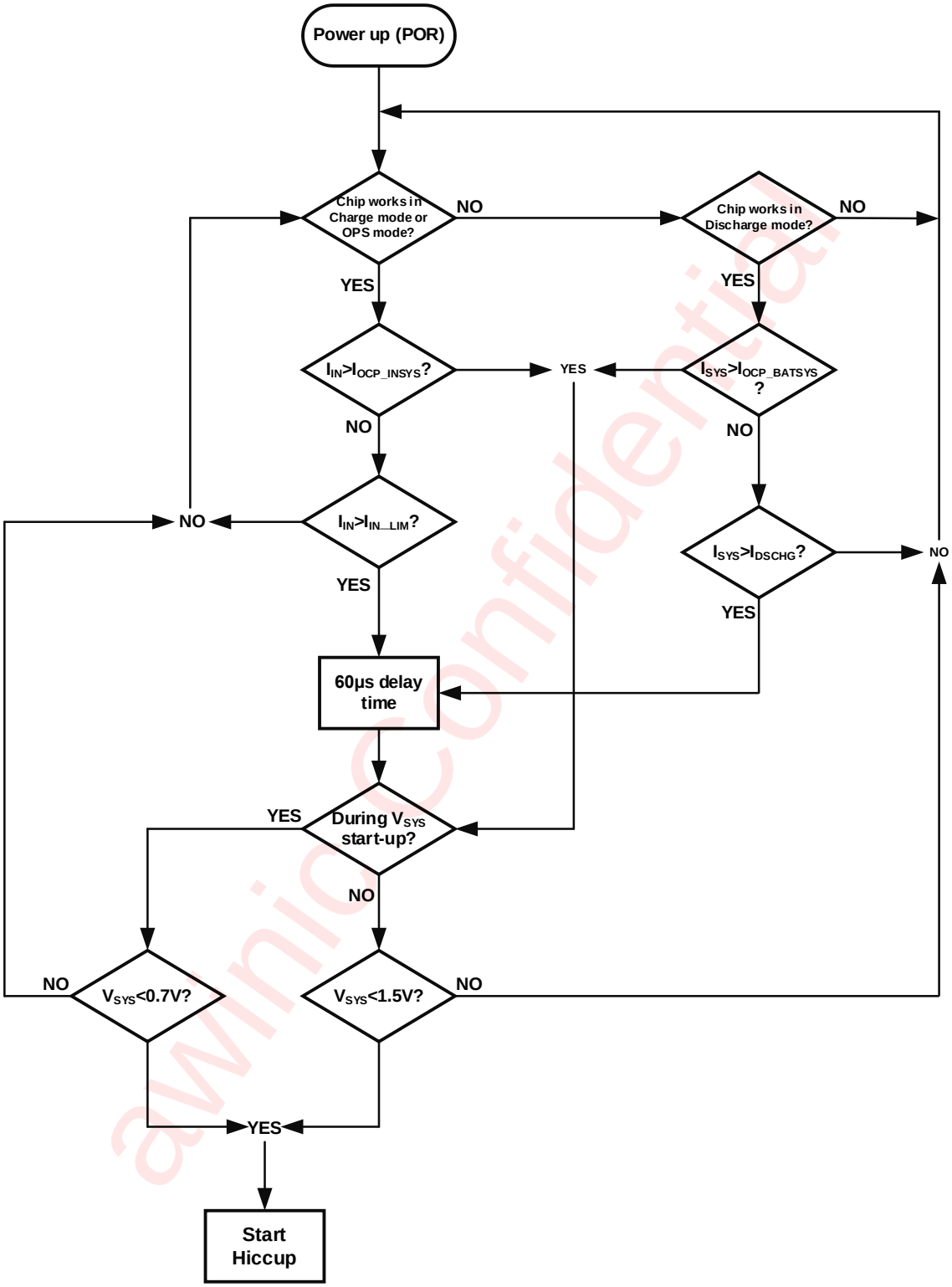


Figure 22 Short Circuit Hiccup Protection Flow Chart

The AW32001E has short-circuit protection (SCP) function in both the IN to SYS path and the BAT to SYS path. The IC monitor the system voltage continuously. If V_{SYS} is lower than 1.5V, The SCP is active, and I_{DSCHG} decreases to half of the original value. For the IN to SYS path, once I_{IN} is over the 2A protection threshold I_{OCP_INSYS}, both the Q1 and Q2 are turned off immediately, and the AW32001E enters hiccup mode. When the

setting input current limit I_{IN_LIM} is reached, I_{IN} is regulated at I_{IN_LIM}. After a 60μs delay, the hiccup mode starts, and the hiccup mode interval is 1ms. For the BAT to SYS path, once I_{BAT} is over the 3.7A protection threshold I_{OCP_BATSYS}, both the Q1 and Q2 are turned off immediately, and the AW32001E enters hiccup mode. When the battery discharge current limit threshold I_{DSCHG} is reached, hiccup mode starts after a 60μs delay, and the hiccup mode interval is 1ms.

Particularly, when system short-circuit occurs in both the input and battery, the both paths protection mechanism works together. The faster path dominates the hiccup operation.

Over-Discharge Current Protection

In discharge mode and supplement mode, the AW32001E is designed to have an over-discharge current protection. Once the I_{BAT} exceeds the programmable discharge current limit (2A default), the Q2 turns off after a 60μs delay. At the same time, the AW32001E enters hiccup mode as part of the over-current protection (OCP). The discharge current can be programmed to maximal 3.2A through the I^2C. in addition, if the discharge current goes high and reaches the internal fixed peak current limit (about 3.7A), the Q2 turns off and begins hiccup mode immediately.

Safety timer

Because the abnormal battery conditions, the AW32001E designed a pre-charge and fast-charge safety timer to prevent an extra-long time charging cycle. The pre-charge safety timer is 1hour, and the fast-charge safety timer can be programmed through the I^2C. Once the battery enters fast-charge mode, The fast charge safety timer starts. The safety timer can be disabled via the I^2C. When charger works in VIN DPM or Temp regulation state, the charge current will decrease. In order to charge as full as possible, the register bit TMR2X_EN(REG06H[6]) could be set 1, which enable the timer slows down, the left safety time is double. If VIN DPM or Temp regulation state exit, or TMR2X_EN=0, the timer recovery normal.

The following actions can restart the safety timer:

- Write REG05H[3] from 0 to 1 (safety timer enable).
- Write REG01H[3] from 1 to 0 (charge enable).
- Write REG02H[7] from 0 to 1 (software reset).
- A new charge cycle is kicked in.

Interrupt to host (INT)

The AW32001E can output a 256μs low-state INT pulse via INT to notify the system of the operation. All of the below events can trigger an INT output:

- Charge completed
- Good input source detected
- Charging status change
- UVLO or input over-voltage protection
- Any fault in REG09H and REG08H (input fault, watchdog timer fault, safety timer fault, thermal fault, battery OVP fault, NTC fault)

When a fault occurs, an INT pulse is send out and latches the fault state in REG09H. After the AW32001E exits the fault state, the fault bit is reset to 0 after the host reads faults registers. The NTC fault bit constantly reports the current thermistor conditions without latches. The INT signal can be masked when the corresponding control bit is set in REG06H[4:0]. When an INT condition is masked, this means that the INT pin signal (and register bit) will not trigger when the corresponding condition occurs. Masking INT pulses is useful when writing software code to avoid unnecessary interruptions due to these events.

Host Mode and Default Mode

The AW32001E is a host-controlled device. After the power-on reset, the AW32001E starts up in a default mode or watchdog timer expiration state. All registers are in their default settings.

In both charge and discharge mode, once the watchdog timer run out, both the Q1 and Q2 are turned off, and most registers return to the default value (refer to the I²C Register Map section). The Q1 and Q2 are turn on again automatically after t_{RST_DUR}, which can be programmed by REG01H[5]. Also the watchdog timer can be turned off in discharge mode by setting REG05H[7]=0. If the watchdog timer (REG05H[6:5]) is not disabled, the host must reset the watchdog timer regularly by writing 1 to REG02H[6] before the watchdog timer expires to keep the device in host mode. When the watchdog timer expires, the AW32001E goes back to default mode. And any writing to the AW32001E will switch it to host mode. The watchdog timer limit can also be programmed or disabled by the host control.

In charge mode and OPSM, the watchdog timer is valid by default. In discharge mode, the watchdog timer is disable by default, and can be turned on by setting REG05H[7]=1. When the REG05H[6:5] is set to 00, the watchdog timer is disabled under both charge mode and discharge mode regardless of the status of REG05H[7]. Operation mode can be switched to default mode when one of the following conditions are valid:

- Register REG02H[7] is reset.
- Refresh input without battery.
- Re-insert battery with no VIN.

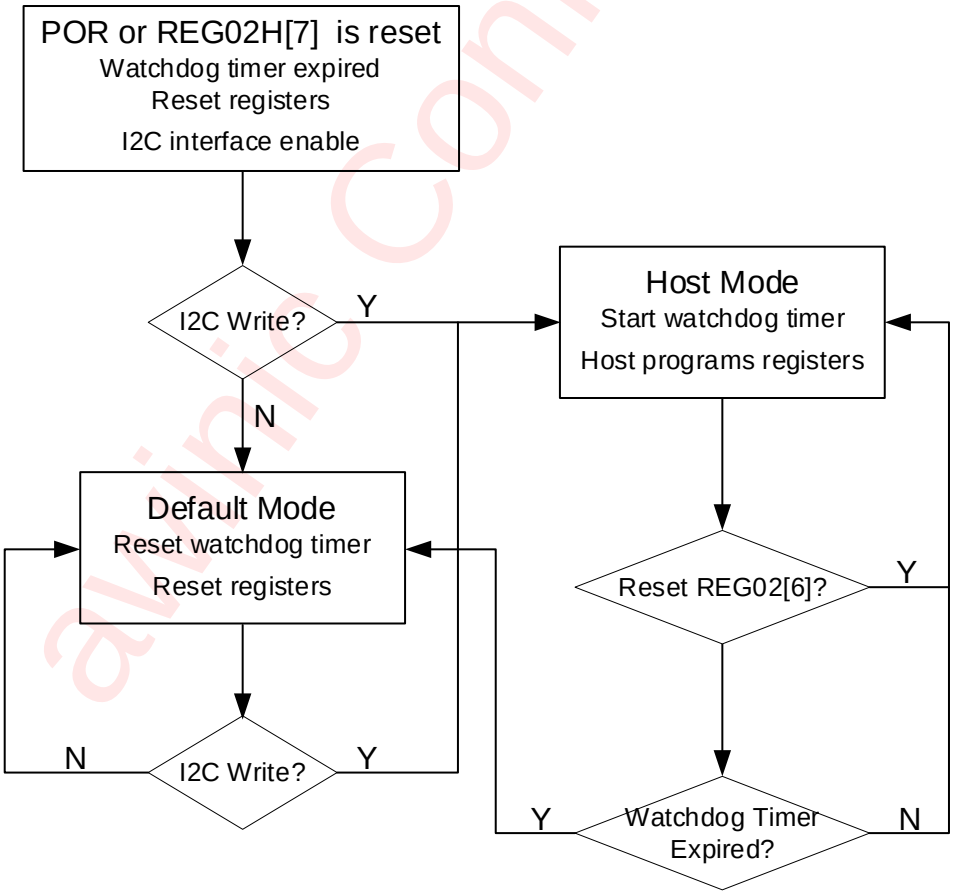


Figure 23 Watchdog Timer Flow Chart

General I²C Operation

The device supports the I²C serial bus and data transmission protocol. It operates as a slave on the I²C bus. The maximum clock frequency specified by the I²C standard is 400kHz. Connect to the bus are made via the open-drain I/O pins SCL and SDA. The pull-up resistor can be selected in the range of 1k~10kΩ and the typical value is 4.7kΩ when I²C frequency is 400kHz. Different high level from 1.2V to 5V of this I²C interface is supported.

Device Address

AW32001E 7-bit slave address (A7~A1) is 1001001 binary(0x49H). After the START condition, the I²C master sends the 7-bit chip address followed by an eighth (A0) read or write bit (R/W). R/W= 0 indicates a WRITE function and R/W = 1 indicates a READ function.

Table 6: Device Address

A7	A6	A5	A4	A3	A2	A1	A0
1	0	0	1	0	0	1	R/W

Data Validation

When SCL is high level, SDA level must be constant. SDA can be changed only when SCL is low level.

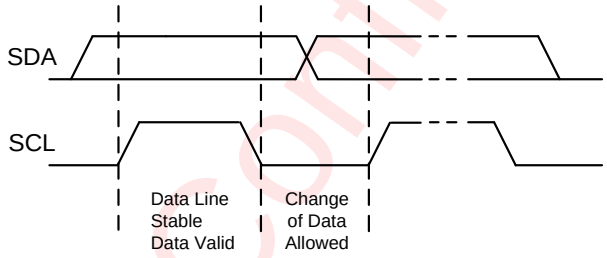


Figure 24 Data Validation Diagram

I²C Start/Stop

I²C start: SDA changes from high level to low level when SCL is high level.

I²C stop: SDA changes from low level to high level when SCL is high level.

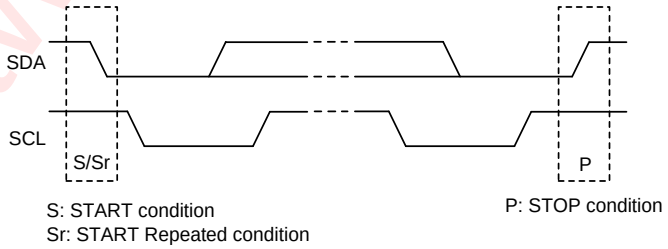


Figure 25 Start and Stop Conditions

ACK (Acknowledgement)

ACK means the successful transfer of I²C bus data. After master sends 8bits data, SDA must be released; SDA is pulled to GND by slave device when slave acknowledges.

When master reads, slave device sends 8bit data, releases the SDA and waits for ACK from master. If ACK is send and I²C stop is not send by master, slave device sends the next data. If ACK is not send by master, slave device stops to send data and waits for I²C stop.

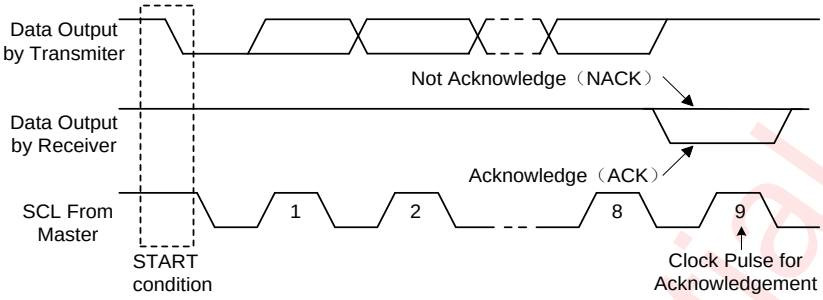


Figure 26 Acknowledgement Diagram

Write Process

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol allows a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a Start Condition, a number of byte transfers (set by the software) and a Stop Condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow.

In a write process, the following steps should be followed:

a) Master device generates START condition. The "START" signal is generated by lowering the SDA signal while the SCL signal is high.

b) Master device sends slave address (7-bit) and the data direction bit (r/w = 0).

c) Slave device sends acknowledge signal if the slave address is correct.

d) Master sends control register address (8-bit)

e) Slave sends acknowledge signal

f) Master sends data byte to be written to the addressed register

g) Slave sends acknowledge signal

h) If master will send further data bytes the control register address will be incremented by one after acknowledge signal (repeat steps f and g)

i) Master generates STOP condition to indicate write cycle end

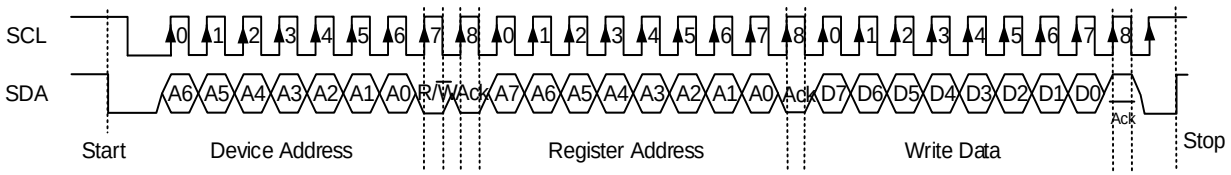


Figure 27 I²C Write Timing

Read Process

In a read cycle, the following steps should be followed:

a) Master device generates START condition

b) Master device sends slave address (7-bit) and the data direction bit (r/w = 0).

c) Slave device sends acknowledge signal if the slave address is correct.

d) Master sends control register address (8-bit)

e) Slave sends acknowledge signal

f) Master generates STOP condition followed with START condition or REPEAT START condition

g) Master device sends slave address (7-bit) and the data direction bit (r/w = 1).

h) Slave device sends acknowledge signal if the slave address is correct.

i) Slave sends data byte from addressed register.

j) If the master device sends acknowledge signal, the slave device will increase the control register address by one, then send the next data from the new addressed register.

k) If the master device generates STOP condition, the read cycle is ended.

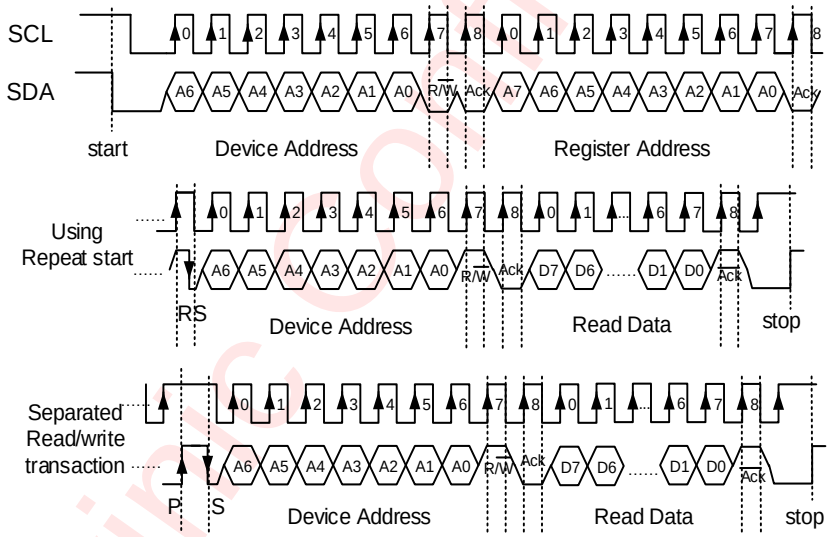


Figure 28 I²C Read Timing

Register List

Register Map

R/W = Read/Write, RC = Read Clear.

ADDR	0x00	0x01	0x02	0x03	0x04
NAME	Input Source Control	Power On Configuration	Charge Current Control	Discharge Current Control	Charge Voltage
Default	0x8F	0xAC	0x0F	0x91	0XA3
Bit7	VIN_DPM[3:0]	t_{RST_DGL}	REG_RST	IDSCHG[3:0]	VBAT_REG[5:0]
Bit6			WD_TMR_RST		
Bit5		t_{RST_DUR}	ICHG[5:0]		
Bit4		EN_HIZ			
Bit3	IIN_LIM[3:0]	CEB		ITERM[3:0]	
Bit2		VBAT_UVLO[2:0]			
Bit1					VBAT_PRE
Bit0					VRECH

ADDR	0x05	0x06	0x07	0x08
NAME	Charger Termination/Timer Control	Main Control	System Voltage Control	System Status
Default	0x7A	0xC0	0x38	0x40
Bit7	EN_WD_DISCHG	EN_NTC	DIS_PCB_OTP	Watchdog_ Fault
Bit6	WATCHDOG[1:0]	TMR2X_EN	DIS_VINLOOP	Rev[1:0]
Bit5		FET_DIS	TJ_REG[1:0]	
Bit4	EN_TERM	PG_INT_CONTROL		CHG_STAT[1:0]
Bit3	EN_TIMER	EOC_INT_CONTROL	VSYS_REG[3:0]	
Bit2	CHG_TMR[1:0]	CHG STATUS_INT_CONTROL		PPM_STAT
Bit1		NTC_INT_CONTROL		PG_STAT
Bit0	TERM_TMR	BATOVP_INT_CONTROL		THERM_STAT

ADDR	0x09	0x0A	0x0B	0x0C	0x22
NAME	Fault	Address	Individual Charge	Additional Function Control	Additional Function Control
Default	0x00	0x49	0x43	0x10	0x03
Bit7	EN_SHIPPING_DGL[1:0]	CHIPID[7:0]	EN_ICHG_DIVD	EN0P55	Reserve[3:0]
Bit6			Reserve	ITERMDEG	
Bit5	VIN_FAULT		EN_IPRE_SET	Reserve[1:0]	
Bit4	THEM_SD		IPRE[3:0]		
Bit3	BAT_FAULT			PRETO	INT100MS
Bit2	STMR_FAULT			EN100KINT	Reserve[2:0]
Bit1	NTC_FAULT[1:0]			Reserve[0]	
Bit0			EN_SHIPMD_0P1S	RSTDLAY	

Input Source Control Register

Address: 00H, Reset State: 1000 1111.

BIT Name	W/R	BIT	SFTRST	WTDRST	Function
VIN_DPM	W/R	B7-B4	Y	N	VIN_DPM voltage regulation setting: BIN VIN_DPM (V) 0000 3.88 **1000 4.52 (default)** 0001 3.96 1001 4.60 0010 4.04 1010 4.68 0011 4.12 1011 4.76 0100 4.20 1100 4.84 0101 4.28 1101 4.92 0110 4.36 1110 5.00 0111 4.44 1111 5.08
IIN_LIM	W/R	B3-B0	Y	N	Input current limit setting: BIN IIN_LIM (mA) 0000 50 1000 290 0001 80 1001 320 0010 110 1010 350 0011 140 1011 380 0100 170 1100 410 0101 200 1101 440 0110 230 1110 470 0111 260 **1111 500(default)**

Power On Configuration Register

Address: 01H, Reset State1010 1100.

BIT Name	W/R	BIT	SFTRST	WTDRST	Function
t_{RST_DGL}	W/R	B7-B6	Y	Y	Pull INT low time period to disconnect the battery: BIN time (s) 00: 8 01: 12 **10: 16(default)** 11: 20
t_{RST_DUR}	W/R	B5	Y	Y	Q2 lasts off time before auto-on: 0: 2s; **1: 4s (default).**
EN_HIZ	W/R	B4	Y	Y	**0: disable (default);** 1:enable.
CEB	W/R	B3	Y	Y	0: charge enable; **1: charge disable (default).**
VBAT_UVLO	W/R	B2-B0	Y	Y	Battery UVLO Threshold: BIN VBAT_UVLO (V) 000 2.43 **100 2.76 (default)** 001 2.49 101 2.85 010 2.58 110 2.94 011 2.67 111 3.03

Charge Current Control Register

Address: 02H, Reset State:0000 1111

BIT Name	W/R	BIT	REGRST	WTDRST	Function
REG_RST	W/R	B7	Y	N	**0: keep current setting (default);** 1: reset.
WD_TMR_RST	W/R	B6	Y	Y	**0: normal (default);** 1: reset.
ICHG	W/R	B5-B0	Y	Y	Fast charge current setting: BIN ICHG(mA) 000000 8 100000 264 000001 16 100001 272 000010 24 100010 280 000011 32 100011 288 000100 40 100100 296 000101 48 100101 304 000110 56 100110 312 000111 64 100111 320 001000 72 101000 328 001001 80 101001 336 001010 88 101010 344 001011 96 101011 352 001100 104 101100 360 001101 112 101101 368 001110 120 101110 376 **001111 128 (default)** 101111 384 010000 136 110000 392 010001 144 110001 400 010010 152 110010 408 010011 160 110011 416 010100 168 110100 424 010101 176 110101 432 010110 184 110110 440 010111 192 110111 448 011000 200 111000 456 011001 208 setting REG0CH[7]=1 and 011010 216 REG00H[3:0]=1111, open 011011 224 111001 464 011100 232 111010 472 011101 240 111011 480 011110 248 111100 488 011111 256 111101 496 111110 504 111111 512

Discharge Current Control Register

Address: 03H, Reset State1001 0001.

BIT Name	W/R	BIT	REGRST	WTDRST	Function
IDSCHG	W/R	B7-B4	Y	Y	BAT to SYS discharge current limit: BIN IDSCHG(mA) 0000 200 1000 1800 0001 400 **1001 2000 (default)** 0010 600 1010 2200 0011 800 1011 2400 0100 1000 1100 2600 0101 1200 1101 2800 0110 1400 1110 3000 0111 1600 1111 3200

ITERM	W/R	B3-B0	Y	Y	Termination current. current range: BIN ITERM(mA) 0000 1 1000 17 **0001 3 (default)** 1001 19 0010 5 1010 21 0011 7 1011 23 0100 9 1100 25 0101 11 1101 27 0110 13 1110 29 0111 15 1111 31

Charge Voltage Register

Address: 04H, Reset State:1010 0011.

BIT Name	W/R	BIT	REGRST	WTDRST	Function
VBAT_REG	W/R	B7-B2	Y	Y	Battery regulation voltage: BIN VBAT_REG(V) 000000 3.600 100000 4.080 000001 3.615 100001 4.095 000010 3.630 100010 4.110 000011 3.645 100011 4.125 000100 3.660 100100 4.140 000101 3.675 100101 4.155 000110 3.690 100110 4.170 000111 3.705 100111 4.185 001000 3.720 **101000 4.200(default)** 001001 3.735 101001 4.215 001010 3.750 101010 4.230 001011 3.765 101011 4.245 001100 3.780 101100 4.260 001101 3.795 101101 4.275 001110 3.810 101110 4.290 001111 3.825 101111 4.305 010000 3.840 110000 4.320 010001 3.855 110001 4.335 010010 3.870 110010 4.350 010011 3.885 110011 4.365 010100 3.900 110100 4.380 010101 3.915 110101 4.395 010110 3.930 110110 4.410 010111 3.945 110111 4.425 011000 3.960 111000 4.440 011001 3.975 111001 4.455 011010 3.990 111010 4.470 011011 4.005 111011 4.485 011100 4.020 111100 4.500 011101 4.035 111101 4.515 011110 4.050 111110 4.530 011111 4.065 111111 4.545
VBAT_PRE	W/R	B1	Y	Y	Pre-charge to Fast charge threshold: 0:2.8V; **1: 3.0V (default).**
VRECH	W/R	B0	Y	Y	Battery recharge threshold (below VBAT_REG): 0: 100mV; **1: 200mV (default).**

Charger Termination/Timer Control Register

Address: 05H, Reset State:0111 1010.

BIT Name	W/R	BIT	REGRST	WTDRST	Function
EN_WD_DISCHG	W/R	B7	Y	N	Watchdog control in discharge mode: **0: disable (default);** 1: enable.
WATCHDOG	W/R	B6-B5	Y	N	Watchdog setting: 00: disable timer 01: 40s 10: 80s **11: 160s (default)** If Bit[6:5]=00, then watchdog timer is disable no matter Bit 7 is set or no.
EN_TERM	W/R	B4	Y	Y	Termination Setting (control the termination is allowed or not): 0: disable ; **1: enable (default).**
EN_TIMER	W/R	B3	Y	Y	Safety timer Setting: 0: disable; **1: enable (default).**
CHG_TMR	W/R	B2-B1	Y	Y	Fast charge timer: 00: 3hrs **01: 5hrs (default);** 10: 8hrs 11: 12hrs.
TERM_TMR	W/R	B0	Y	Y	Termination timer Setting: **0: disable (default);** 1: enable.

Main Control Register

Address: 06H, Reset State:1100 0000.

BIT Name	W/R	BIT	REGRST	WTDRST	Function
EN_NTC	W/R	B7	Y	Y	0: disable ; **1: enable (default).**
TMR2X_EN	W/R	B6	Y	Y	0: disable 2x extended safety timer during PPMF; **1: enable 2x extended safety timer during PPMF (default).**
FET_DIS	W/R	B5	Y	N	**0: enable (default);** 1: turn off.
PG_INT_CONTROL	W/R	B4	Y	Y	**0: on (default);** 1: off.
EOC_INT_CONTROL	W/R	B3	Y	Y	**0: on (default);** 1: off. (EOC: End of Charge)
CHG STATUS_INT_CONTROL	W/R	B2	Y	Y	**0: on (default);** 1: off.
NTC_INT_CONTROL	W/R	B1	Y	Y	**0: on (default);** 1: off.
BATOVP_INT_CONTROL	W/R	B0	Y	Y	**0: on (default);** 1: off.

System Voltage Control Register

Address: 07H, Reset State:0011 1000.

BIT Name	W/R	BIT	REGRST	WTDRST	Function
DIS_PCB_OTP	W/R	B7	Y	Y	PCB OTP Disable. **0: enable PCB OTP (default);** 1: disable PCB OTP.
DIS_VINLOOP	W/R	B6	Y	Y	VIN_DPM loop. **0: enable VIN_DPM loop (default);** 1: disable.
TJ_REG	W/R	B5-B4	Y	Y	Thermal regulation threshold: BIN Temperature(°C) 00 60 01 80 10 100 **11** **120 (default)**

VSYS_REG	W/R	B3-B0	Y	N	System voltage regulation. Range: BIN VSYS_REG(V) 0000 4.20 **1000 4.60 (default)** 0001 4.25 1001 4.65 0010 4.30 1010 4.70 0011 4.35 1011 4.75 0100 4.40 1100 4.80 0101 4.45 1101 4.85 0110 4.50 1110 4.90 0111 4.55 1111 4.95

System Status Register

Address: 08H, Reset State:0100 0000.

BIT Name	W/R	BIT	REG RST	WTDRST	Function
Watchdog_ Fault	R	B7	NA	NA	**0: normal (default);** 1: watchdog timer expiration.
Rev	R	B6-B5	NA	NA	
CHG_STAT	R	B4-B3	NA	NA	**00: not charging (default);** 01: pre charge; 10: charge; 11: charge done.
PPM_STAT	R	B2	NA	NA	**0: no PPM (default);** 1: IN PPM.
PG_STAT	R	B1	NA	NA	0: Power fail; 1: Power good.
THERM_STAT	R	B0	NA	NA	**0: no thermal regulation (default);** 1: in thermal regulation.

Fault Register

Address: 09H, Reset State:0000 0000.

BIT Name	W/R	BIT	REGRST	WTDRST	Function
EN_SHIPPING_ DGL	W/R	B7-B6	Y	N	Enter shipping mode deglitch time: BIN deglitch time(s) **00: 1 (default);** 01: 2 10: 4 11: 8
VIN_FAULT	R	B5	NA	NA	**0: normal (default);** 1: input fault (OVP or bad source).
THEM_SD	R	B4	NA	NA	**0: normal (default);** 1: thermal shutdown.
BAT_FAULT	R	B3	NA	NA	**0: normal (default);** 1: battery OVP.
STMR_FAULT	R	B2	NA	NA	**0: normal (default);** 1: safety timer expiration.
NTC_FAULT[1]	R	B1	NA	NA	**0: normal (default);** 1: NTC hot.
NTC_FAULT[0]	R	B0	NA	NA	**0: normal (default);** 1: NTC cold.

Address Register

Address: 0AH, Reset State:0100 1001.

BIT Name	W/R	BIT	REGRST	WTDRST	Function
CHIP ID	R	B7-B0	N	N	Chip ID used to be identified

Individual Charge Register

Address: 0BH, Reset State:0100 0011.

BIT Name	W/R	BIT	REGRST	WTDRST	Function
EN_ICHG_DIVD	W/R	B7	Y	Y	1: reduce the current value of REG02[3:0] configuration to 1/4; **0: keep the current value of REG02[5:0] configuration. (default).**
Reserve	NA	B6	NA	NA	NA
EN_IPRE_SET	W/R	B5	Y	Y	**0: IPRE is set by REG03[4:1] (default);** 1: IPRE is set by REG0B[4:1].
IPRE[3:0]	W/R	B4-B1	Y	Y	1mA~31mA pre-charge current configuration: 2 mA/step, **3mA (default).** BIN IPRE(mA) 0000 1 1000 17 **0001 3(default)** 1001 19 0010 5 1010 21 0011 7 1011 23 0100 9 1100 25 0101 11 1101 27 0110 13 1110 29 0111 15 1111 31
EN_SHIPMD_0P1S	W/R	B0	Y	Y	VIN Plug: In deglitch time of shipping mode out： 0：2s; **1：100ms(default).**

Additional Function Control Register

Address: 0CH, Reset State:0001 0000.

BIT Name	W/R	BIT	REGRST	WTDRST	Function
EN0P55	W/R	B7	Y	Y	Increase input current limit: **0: The input current limit is set by REG00[3:0] (default);** 1: If REG00[3:0]=1111,this bit increase the input current limit to 550mA, otherwise, it is useless.
ITERMDEG	W/R	B6	Y	Y	Charge termination current deglitch time: **0:3s (default);** 1:1s.
Reserve	NA	B5~B4	NA	NA	NA
PRETO	W/R	B3	Y	Y	**0: Pre-charge timeout is 1h (default);** 1: Pre-charge timeout is 2h.
DIS_SHIPINT	W/R	B2	Y	Y	The function of disabling INT PIN during SHIPPING mode: **0: Nominal INT PIN function(Default);** 1: Disable INT PIN function during SHIPPING mode.
Reserve	NA	B1	NA	NA	NA
RSTDLAY	W/R	B0	Y	Y	The delay time after VSYS is Reset: **0: 0s (Default);** 1: 2s.

Additional Function Control Register1

Address: 22H, Reset State:0000 0011.

BIT Name	W/R	BIT	REGRST	WTDRST	Function
Reserve	NA	B7~B4	NA	NA	NA
INT100MS	W/R	B3	Y	Y	INT 100ms exit shipping mode **0: 2s (default);** 1:100ms.
Reserve	NA	B2~B0	NA	NA	NA

Application Information

NTC FUNCTION

NTC pin is connected to the thermistor paralleled with a resistor R_{F2} to ground. Another resistor R_{F1} is connected to the VDD which is the chip's internal power supply voltage. The high temperature limit and low temperature limit can be varied by using different R_{F1} and R_{F2}. Illustrated in Figure 29, the off chip resistors must be connected as the blue part demonstrated. The resistance of R_{F1} and R_{F2} can be calculated by Equation (1) and Equation (2):

$$R_{F2} = \frac{(V_{COLD} - V_{HOT}) \times R_{NTCH} \times R_{NTCL}}{(V_{HOT} - V_{COLD} \times V_{HOT}) \times R_{NTCL} - (V_{COLD} - V_{COLD} \times V_{HOT}) \times R_{NTCH}} \quad (1)$$

$$R_{F1} = \frac{1 - V_{COLD}}{V_{COLD}} \times (R_{F2} // R_{NTCL}) \quad (2)$$

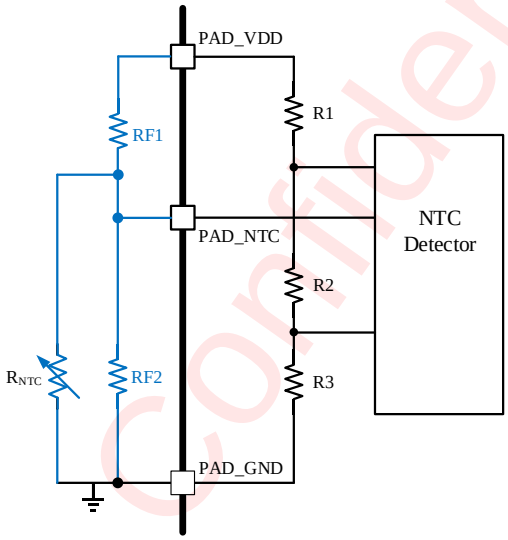


Figure 29 NTC Function(resistor-divided mode)

Where R_{NTCH} is the value of the NTC resistor at the high limit temperature, while the R_{NTCL} is the value of the NTC resistor at a low temperature limit.

External Capacitor

The external capacitor cannot be absent for the operation of AW32001E. Carefully selecting suitable capacitor is important to guarantee the AW32001E working perfectly on the space limited board.

A 4.7μF ceramic capacitor with high level voltage endurance (at least 30V) between IN and GND is recommended. This capacitor rejects input power supply ripple and enhance the stability of DPM loop.

A 1μF ceramic capacitor is required between the VDD and GND to maintain internal power supply voltage higher than the POR threshold. Without this capacitor, the chip logic block may work abnormally when working state changes.

Connect a ceramic capacitor between SYS and GND with least capacitance of 4.7μF to guarantee the stability of the system power supply loop. Larger capacitor will further reduce the system output's overshoot and undershoot.

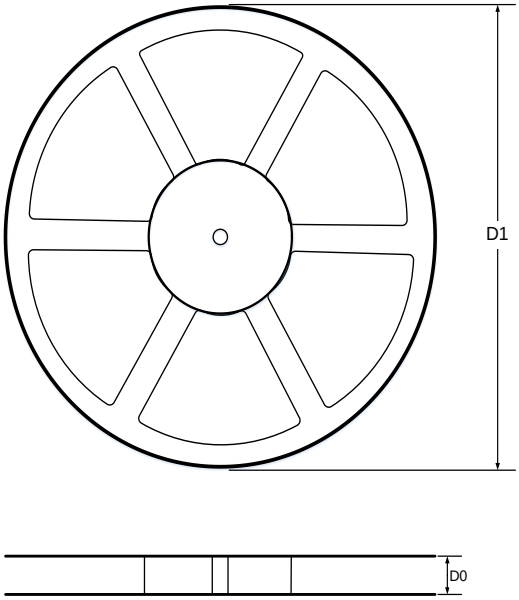
A least 4.7μF ceramic capacitor is also needed between BAT and GND for some application.

Table 6: Recommended external capacitors

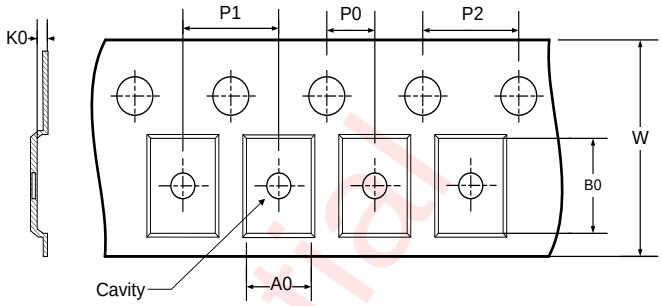
Comments	Capacitor	Supplier	Description	ELA Size	Effective Capacitance
C_{IN}	4.7μF	Any	Ceramic Capacitor;50V; X5R or X7R	0603	>2μF
C_{VDD}	0.1μF	Any	Ceramic Capacitor;16V; X5R or X7R	0603	>50nF
C_{SYS}	4.7μF	Any	Ceramic Capacitor;16V; X5R or X7R	0603	>3μF
C_{BAT}	4.7μF	Any	Ceramic Capacitor;16V; X5R or X7R	0603	>3μF

Tape and Reel Information

REEL DIMENSIONS

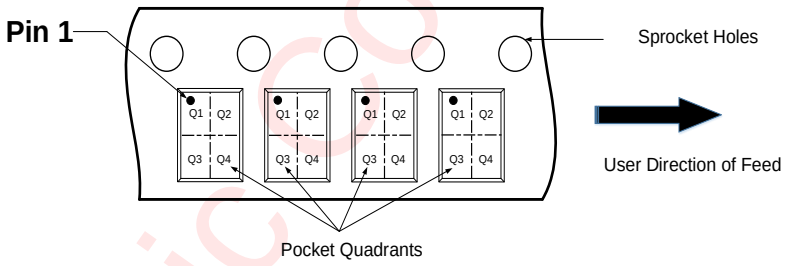


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

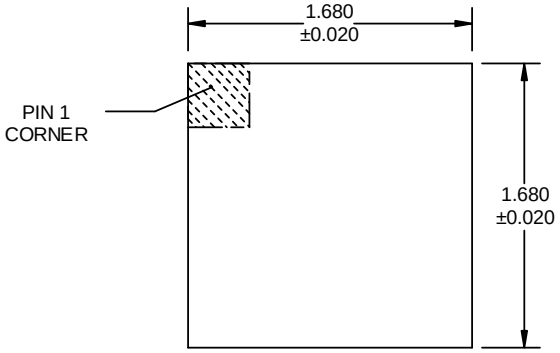


DIMENSIONS AND PIN1 ORIENTATION

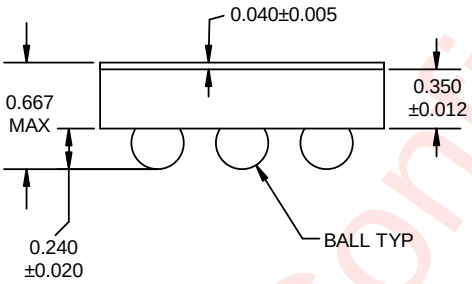
D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
179.00	9.00	1.81	1.81	0.76	2.00	4.00	4.00	8.00	Q1

All dimensions are nominal

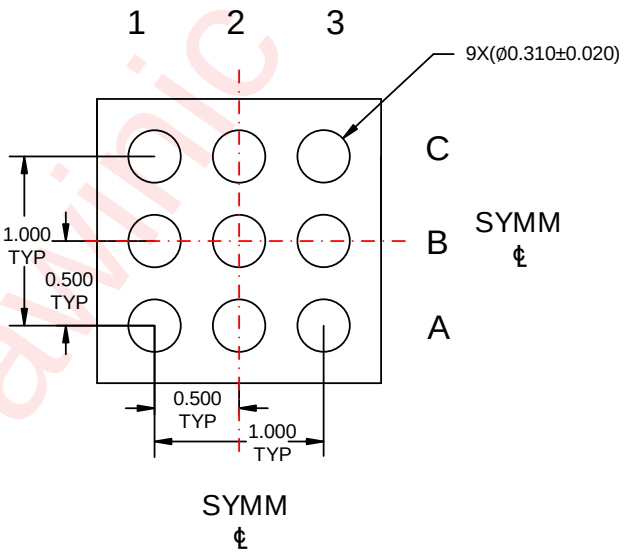
Package Description(POD)



Top View



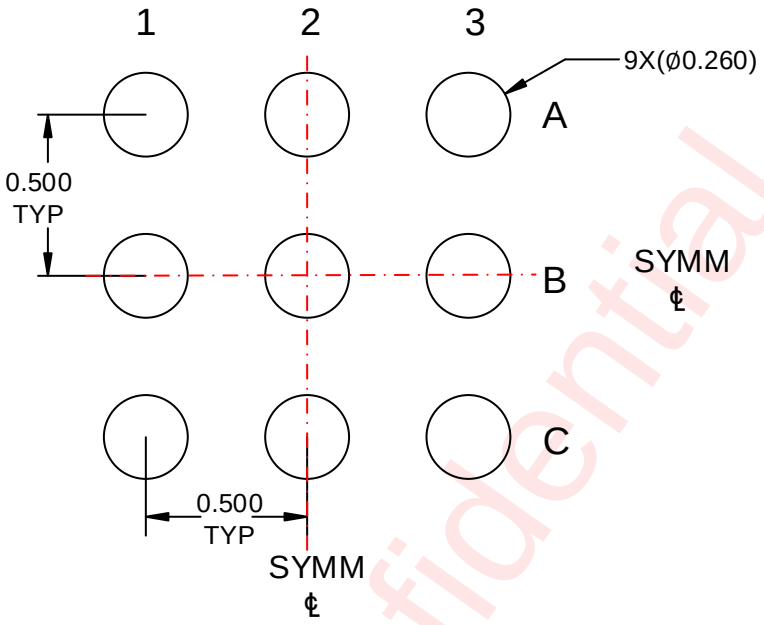
Side View

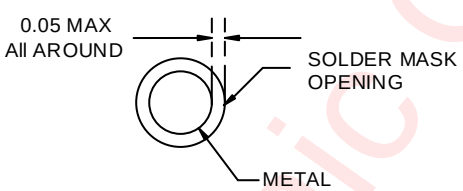


Bottom View

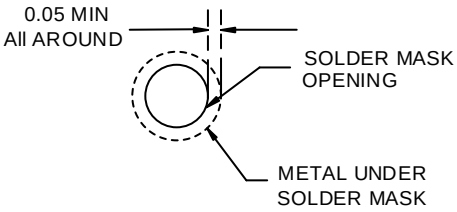
Unit：mm

Land Pattern Data





NON-SOLDER MASK DEFINED



SOLDER MASK DEFINED

Unit: mm

Revision History

Version	Date	Change Record
V1.0	Jun. 2021	Official Released
V1.1	Aug. 2021	1.1 Changed V_{BAT_REG}=4.38V, REG04[7:2]=110100 to 110010 in EC table 1.2 Changed V_{SYS_REG} test condition from "V_{IN}=5.5V, EN_HIZ=0, R_{SYS}=100Ω, I_{CHG}=0A, V_{SYS_REG}=4.6V" to "V_{IN}=5.0V, REG07[3:0]=0000, R_{SYS}=100Ω, I_{CHG}=0A, V_{SYS_REG}=4.6V", added V_{SYS_REG}=4.2V and V_{SYS_REG}=4.95V test condition description. 1.3 Changed deglitch time V_{RECH} for test condition from "V_{BAT} falling after charge termination" to "V_{BAT} falling below V_{RECH} after charge termination" 1.4 Added T_{DGL_UVLO}, T_{DGL_OVP} and I_{LKG_INT} parameter in EC table. 1.5 Changed the parameter VSYS name to V_{SYS_REG} in EC table 1.6 Changed the parameter VIN_MIN name to VIN_DPM and V_{IN_DPM} in EC table. 1.7 Changed the parameter IIN_LMT name to IIN_LIM and I_{IN_LIM} in EC table. 1.8 Changed the parameter $V_{OL(STAT)}$ name to $V_{OL(INT)}$ in EC table. 1.9 Added Register Map. 1.10 Changed the REG22H default value from 00000000 to 00000011. 1.11 Added NTC current mode description. 1.12 Added Table 6: Recommended external capacitors. 1.13 Other detail description. 1.14 Change the Supply current I_{IN} and Charge current ICHG value of Recommended Operating Conditions
V1.2	Mar. 2022	1.1 Deleted NTC current mode description 1.2 Added the BAT pin handle Voltage

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