Ultra-Low Noise Amplifier for Global Navigation Satellite Systems (GNSS)

FEATURES

- Reduce RF environment Interference with patented Smart-Linearity-Technology (SLT);
- Ultra low current=4mA;
- Ultra low noise figure(NF)=0.60dB;
- High power gain=18.5dB;
- High input 1dB-compression point=-5.5dBm;
- GPS L1 requires only one input matching inductor;
- RF output internally matched to 50 ohm for GPS L1;
- Supply voltage: 1.5V to 3.3V;
- Operating frequencies: 1550~1615MHz; 1164~1215MHz;
- DFN 1.1 mmX0.7 mmX0.37 mm-6L package
- ±2kV HBM ESD protection (including RFIN and RFOUT pin)

APPLICATIONS

- Smart Phones, Feature Phones;
- Tablet PCs;
- Personal Navigation Devices;
- Digital Still Cameras, Digital Video Cameras;
- RF Front End modules;
- Complete GPS chipset modules;
- Theft protection(laptop, ATM);

GENERAL DESCRIPTION

The AW15065DNR is a Low Noise Amplifier designed for Global Navigation Satellite Systems (GNSS) as GPS, Beidou, GLONASS, Galileo and Compass. With on-chip DC blocking capacitors at RFIN and RFOUT, The AW15065DNR can be close to the antenna, requires only one external input matching inductor for GPS L1, and reduces assembly complexity and the PCB area, enabling a cost-effective solution.

The AW15065DNR with patented Smart Linearity Technology (SLT) achieves ultra-low noise figure, high linearity, high gain, over a wide range of supply voltages from 1.5V up to 3.3V. All these features make AW15065DNR an excellent choice for GNSS LNA as it improves sensitivity with low noise figure and high gain, provide better immunity against out-of-band jammer signals with high linearity, reduces filtering requirement of preceding stage and hence reduces the overall cost of the GNSS receiver.

The AW15065DNR is available in a small lead-free, RoHS-Compliant, DFN 1.1 mm X 0.7 mm X 0.37 mm-6L package.

TYPICAL APPLICATION CIRCUIT

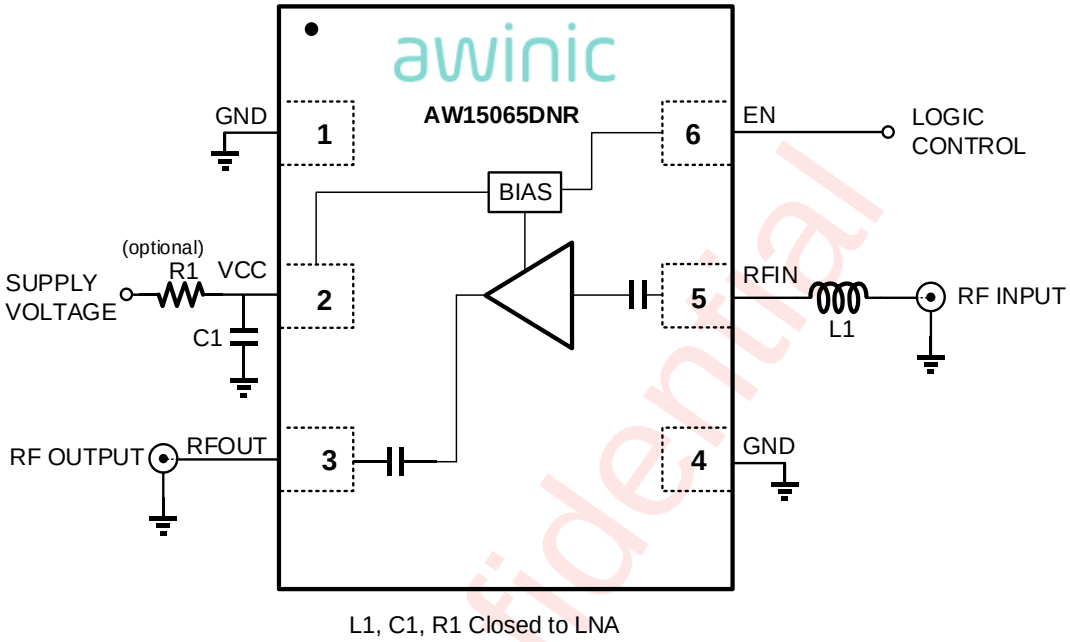


Figure 1(a) Typical Application Circuit of AW15065DNR for GPS L1

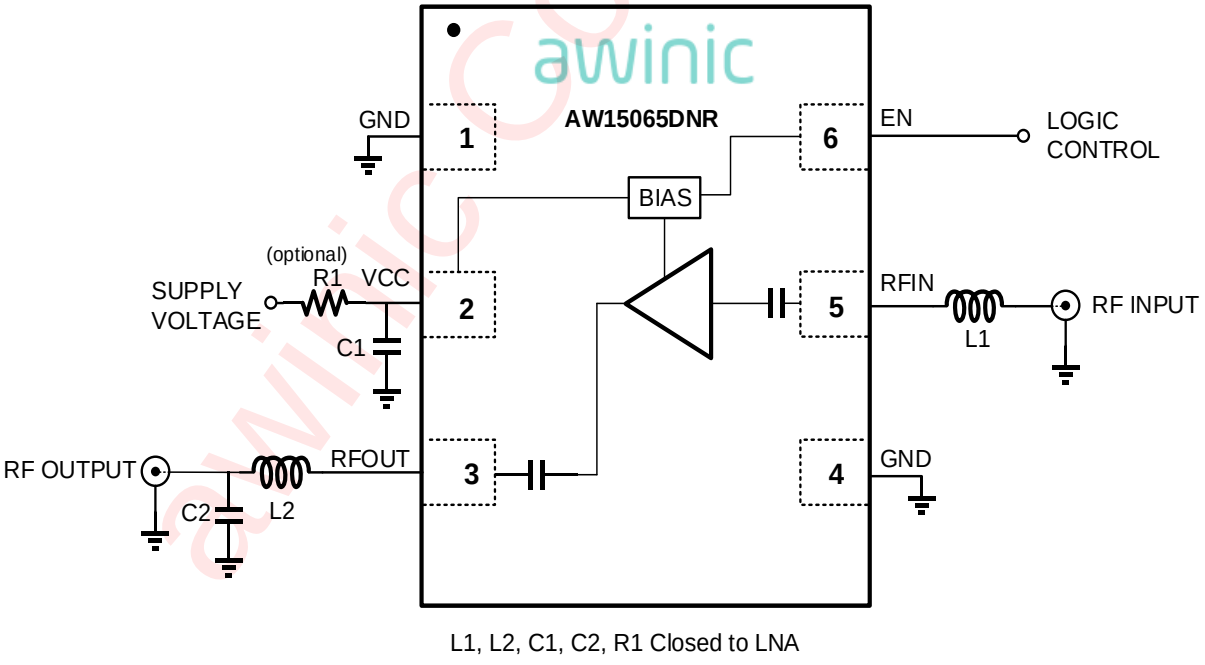
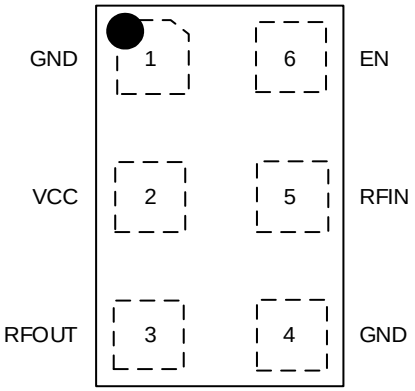


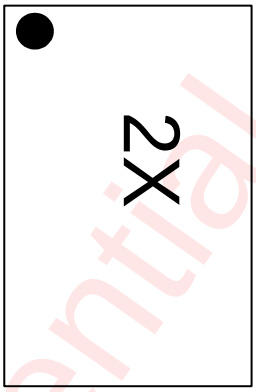
Figure 1(b) Typical Application Circuit of AW15065DNR for GPS L5

PIN CONFIGURATION AND TOP MARK

AW15065DNR
(Top View)



AW15065DNR Marking
(Top View)



2 – AW15065DNR
X – Production Tracing Code

Figure 2 Pin Configuration and Top Mark

PIN DEFINITION

No.	NAME	DESCRIPTION
1	GND	Ground
2	VCC	DC Supply
3	RFOUT	LNA output
4	GND	Ground
5	RFIN	LNA input
6	EN	Logic control

FUNCTIONAL BLOCK DIAGRAM

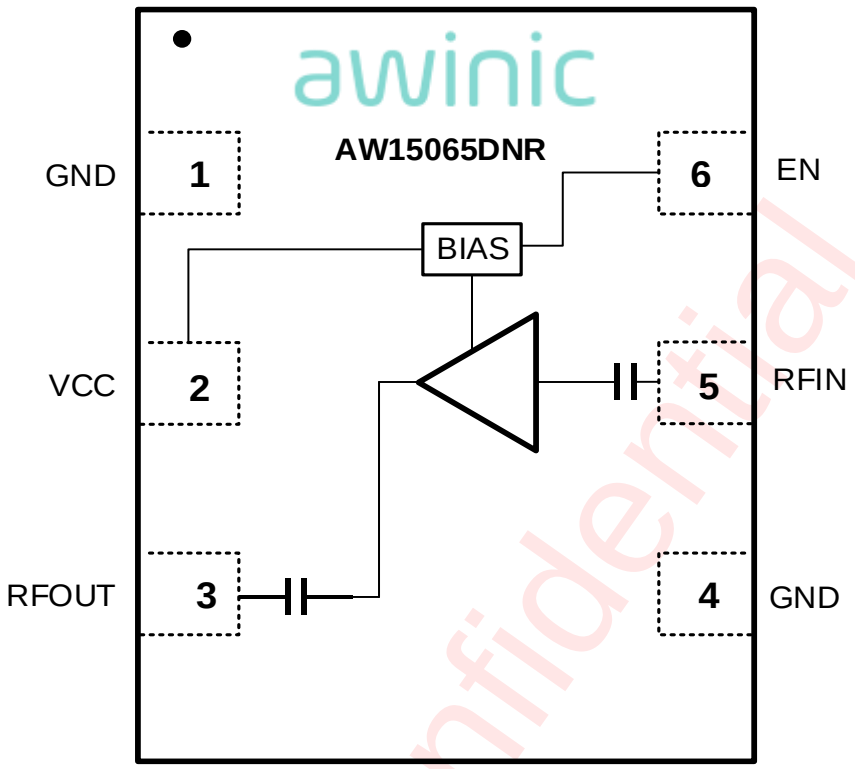


Figure 3 Functional Block Diagram

ORDERING INFORMATION

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW15065DNR	-40°C ~ 105°C	DFN 1.1mmx0.7mm-6L	2	MSL1	ROHS+HF	3000 units/ Tape and Reel

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETERS	Symbol	Values			
		Min.	Typ.	Max.	
Supply Voltage at pin VCC	V_{CC}	-0.3	-	3.6	V
Voltage at pin EN [2]	V_{EN}	-0.3	-	3.6	V
Current into pin VCC	I_{CC}	-	-	30	mA
RF input power [3]	P_{IN}	-	-	10	dBm
Package thermal resistance	θ_{JA}	-	148	-	℃/W
Junction temperature	T_J	-	-	150	℃
Storage temperature range	T_{STG}	-65	-	150	℃
Ambient temperature range	T_{amb}	-40	-	105	℃
Solder temperature(10s)		-	260	-	℃
ESD range					
HBM [4]		±2000			V
CDM [4]		±1000			V
Latch-up					
Test condition: JESD78E		+IT: +200 -IT: -200			mA mA

***Note1**: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.*

***Note2:** Warning: due to internal ESD diode protection, the applied DC voltage should not exceed 3.6V in order to avoid excess current.*

***Note3**: The RF input and RF output are AC coupled through internal DC blocking capacitor.*

***Note4**: HBM standard: ESDA/JEDEC JS-001. CDM standard: ESDA/JEDEC JS-002.*

ELECTRICAL CHARACTERISTICS

(AW15065DNR EVB[1]; Typical values are at V_{CC}=V_{EN}=2.8V and T_A=+25°C, f=1575.42MHz, unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
DC ELECTRICAL CHARACTERISTICS						
V_{CC}	Supply Voltage		1.5	-	3.3	V
I_{SD}	Shut-Down Current	EN=Low			2	μA
I_{CC}	Supply Current	EN=High; T_A=+25°C;		4.0	5.5	mA
		EN=High; T_A=-40°C to +105°C;		4.0	6.0	mA
V_{EN}	Digital Input-Logic High		1.0		3.3	V
V_{EN}	Digital Input-Logic Low				0.3	V
AC ELECTRICAL CHARACTERISTICS						
Gp	Power Gain	T_A=+25°C	16	18.5	20	dB
		T_A=-40°C to +105°C	14.5	18.5	21.5	
RL_{in}	Input Return Loss	T_A=+25°C	8	13		dB
		T_A=-40°C to +105°C	7	13		
RL_{out}	Output Return Loss	T_A=+25°C	9	17		dB
		T_A=-40°C to +105°C	8	17		
ISL	Reverse Isolation	T_A=+25°C	24	29		dB
		T_A=-40°C to +105°C	23	29		
NF	Noise Figure[2]	Zs=50 ohm; No jammer; T_A=+25°C;		0.60	0.90	dB
		Zs=50 ohm; No jammer; T_A=-40°C to +105°C;		0.60	1.30	
Kf	Stability factor	f=20MHz…10GHz; T_A=-40°C to +105°C;	1			
IP1dB	Inband input 1dB-compression point	f=1575.42MHz; T_A=+25°C;	-8.5	-5.5		dBm
		f=1575.42MHz; T_A=-40°C to +105°C;	-9.5	-5.5		
$IIP3_{ib}$	Inband input 3^{rd}-order intercept point	f1=1574.42MHz; f2=1575.42MHz; Pin=-25dBm;	-3	0		dBm

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$IIP3_{oob}$	Out-of-band input 3^{rd}-order intercept point[3]	f1=1713MHz; f2=1851MHz; Pin_f1=-20dBm; Pin_f2=-65dBm;	-2	2		dBm
IMD3	3^{rd}-order intermodulation distoration	f1=1713MHz; f2=1851MHz; Pin_f1=-20dBm; Pin_f2=-65dBm;		-89		dBm
t_{on}	turn-on time	time from V_{EN} ON to 90% of the final gain; T_A=-40°C to +105°C;			2	μs
t_{off}	turn-off time	time from V_{EN} OFF to 10% of the gain; T_A=-40°C to +105°C;			1	μs

Note1: *input matched to 50 ohm using a high quality-factor 6.8nH inductor.*

Note2: *PCB losses are subtracted.*

Note3: *IP3=P1+(P2+Gain$_{1575MHZ}$-IM3)/2*

(AW15065DNR EVB[1]; Typical values are at V_{CC}=V_{EN}=1.8V and T_A=+25°C, f=1575.42MHz, unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
DC ELECTRICAL CHARACTERISTICS						
V_{CC}	Supply Voltage		1.5	-	3.3	V
I_{SD}	Shut-Down Current	EN=Low			2	μA
I_{CC}	Supply Current	EN=High; T_A=+25°C;		3.8	5.5	mA
		EN=High; T_A=-40°C to +105°C;		3.8	6.0	mA
V_{EN}	Digital Input-Logic High		1.0		3.3	V
V_{EN}	Digital Input-Logic Low				0.3	V
AC ELECTRICAL CHARACTERISTICS						
Gp	Power Gain	T_A=+25°C	16	18	20	dB
		T_A=-40°C to +105°C	14.5	18	21.5	
RL_{in}	Input Return Loss	T_A=+25°C	8	12		dB
		T_A=-40°C to +105°C	7	12		
RL_{out}	Output Return Loss	T_A=+25°C	9	17		dB
		T_A=-40°C to +105°C	8	17		

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
ISL	Reverse Isolation	T_A=+25°C	24	29		dB
		T_A=-40°C to +105°C	23	29		
NF	Noise Figure[2]	Zs=50 ohm; No jammer; T_A=+25°C;		0.60	0.90	dB
		Zs=50 ohm; No jammer; T_A=-40°C to +105°C;		0.60	1.30	
Kf	Stability factor	f=20MHz…10GHz; T_A=-40°C to +105°C;	1			
IP1dB	Inband input 1dB-compression point	f=1575.42MHz; T_A=+25°C;	-11.5	-8.5		dBm
		f=1575.42MHz; T_A=-40°C to +105°C;	-12.5	-8.5		

$IIP3_{ib}$	Inband input
	3rd-order intercept point
		f1=1574.42MHz;
		f2=1575.42MHz;
		Pin=-25dBm;
			-5	-1		dBm

$IIP3_{oob}$	Out-of-band input
	3rd-order intercept point[3]
		f1=1713MHz;
		f2=1851MHz;
		Pin_f1=-20dBm;
		Pin_f2=-65dBm;
			-2	2		dBm

IMD3	3rd-order
	intermodulation distoration
		f1=1713MHz;
		f2=1851MHz;
		Pin_f1=-20dBm;
		Pin_f2=-65dBm;
				-89		dBm

t_{on}	turn-on time	time from V_{EN} ON to 90% of the final gain; T_A=-40°C to +105°C;			2	μs
t_{off}	turn-off time	time from V_{EN} OFF to 10% of the gain; T_A=-40°C to +105°C;			1	μs

Note1: *input matched to 50 ohm using a high quality-factor 6.8nH inductor.*

Note2: *PCB losses are subtracted.*

Note3: *IP3=P1+(P2+$Gain_{1575MHZ}$-IM3)/2.*

(AW15065DNR EVB[1]; Typical values are at V_{CC}=V_{EN}=2.8V and TA=+25°C, f=1176.45MHz, unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
DC ELECTRICAL CHARACTERISTICS						
V_{CC}	Supply Voltage		1.5	-	3.3	V
I_{SD}	Shut-Down Current	EN=Low			2	μA
I_{CC}	Supply Current	EN=High; T_A=+25°C;		4.0	5.5	mA
		EN=High; T_A=-40°C to +105°C;		4.0	6.0	mA
V_{EN}	Digital Input-Logic High		1.0		3.3	V
V_{EN}	Digital Input-Logic Low				0.3	V
AC ELECTRICAL CHARACTERISTICS						
Gp	Power Gain	T_A=+25°C	16	18.5	20	dB
		T_A=-40°C to +105°C	14.5	18.5	21.5	
RL_{in}	Input Return Loss	T_A=+25°C	7	12		dB
		T_A=-40°C to +105°C	6	12		
RL_{out}	Output Return Loss	T_A=+25°C	9	13		dB
		T_A=-40°C to +105°C	8	13		
ISL	Reverse Isolation	T_A=+25°C	25	31		dB
		T_A=-40°C to +105°C	24	31		
NF	Noise Figure[2]	Zs=50 ohm; No jammer; T_A=+25°C;		0.60	0.90	dB
		Zs=50 ohm; No jammer; T_A=-40°C to +105°C;		0.60	1.30	
Kf	Stability factor	f=20MHz…10GHz; T_A=-40°C to +105°C;	1			
IP1dB	Inband input 1dB-compression point	f=1176.45MHz; T_A=+25°C;	-14	-11		dBm
		f=1176.45MHz; T_A=-40°C to +105°C;	-15	-11		
$IIP3_{ib}$	Inband input 3^{rd}-order intercept point	f1=1175.45MHz; f2=1176.45MHz; Pin=-20dBm;	-5	-2		dBm
t_{on}	turn-on time	time from V_{EN} ON to 90% of the final gain; T_A=-40°C to +105°C;			2	μs

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
t_{off}	turn-off time	time from V_{EN} OFF to 10% of the gain; T_A=-40°C to +105°C;			1	μs

***Note1**: input matched to 50 ohm using a high quality-factor 13nH inductor. Output matching using 9.1nH inductor and 2pF capacitor.*

***Note2**: PCB losses are subtracted.*

(AW15065DNR EVB[1]; Typical values are at V_{CC}=V_{EN}=1.8V and T_A=+25°C, f=1176.45MHz, unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
DC ELECTRICAL CHARACTERISTICS						
V_{CC}	Supply Voltage		1.5	-	3.3	V
I_{SD}	Shut-Down Current	EN=Low			2	μA
I_{CC}	Supply Current	EN=High; T_A=+25°C;		3.8	5.5	mA
		EN=High; T_A=-40°C to +105°C;		3.8	6.0	
V_{EN}	Digital Input-Logic High		1.0		3.3	V
V_{EN}	Digital Input-Logic Low				0.3	V
AC ELECTRICAL CHARACTERISTICS						
Gp	Power Gain	T_A=+25°C	16	18	20	dB
		T_A=-40°C to +105°C	14.5	18	21.5	
RL_{in}	Input Return Loss	T_A=+25°C	7	11		dB
		T_A=-40°C to +105°C	6	11		
RL_{out}	Output Return Loss	T_A=+25°C	9	14		dB
		T_A=-40°C to +105°C	8	14		
ISL	Reverse Isolation	T_A=+25°C	25	31		dB
		T_A=-40°C to +105°C	24	31		
NF	Noise Figure[2]	Zs=50 ohm; No jammer;		0.60	0.90	dB

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
		T_A=+25°C;				
		Zs=50 ohm; No jammer; T_A=-40°C to +105°C;		0.60	1.30	
Kf	Stability factor	f=20MHz…10GHz; T_A=-40°C to +105°C;	1			
IP1dB	Inband input 1dB-compression point	f=1176.45MHz; T_A=+25°C;	-16	-13		dBm
		f=1176.45MHz; T_A=-40°C to +105°C;	-17	-13		

$IIP3_{ib}$	Inband input
	3^{rd}-order intercept point
		f1=1175.45MHz;
		f2=1176.45MHz;
		Pin=-20dBm;
			-9	-5		dBm

t_{on}	turn-on time	time from V_{EN} ON to 90% of the final gain; T_A=+25°C;			2	μs
t_{off}	turn-off time	time from V_{EN} OFF to 10% of the gain; T_A=-40°C to +105°C;			1	μs

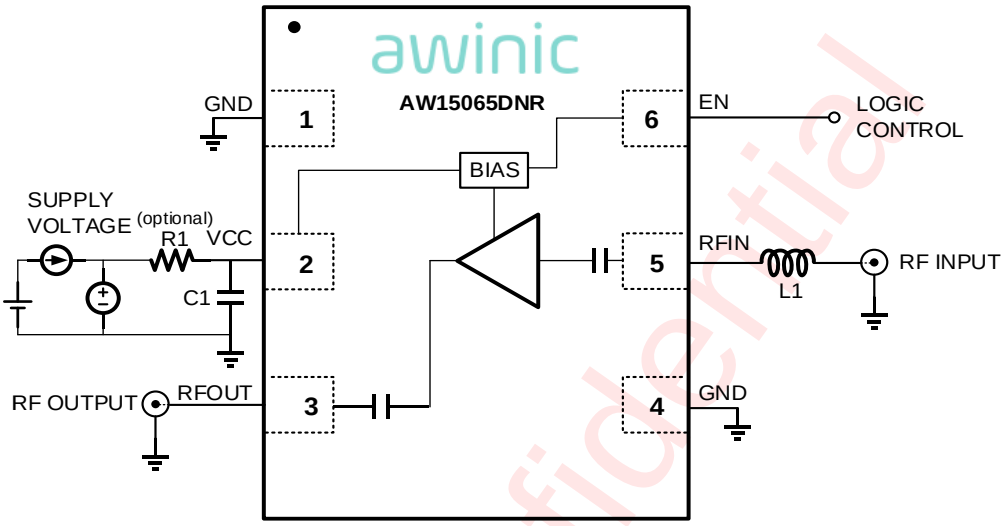
***Note1**: input matched to 50 ohm using a high quality-factor 13nH inductor. Output matching using 9.1nH inductor and 2pF capacitor.*

***Note2**: PCB losses are subtracted.*

TEST CIRCUITS

DC Characteristics

The following is the test bench for power supply, pin voltage, supply current, standby current



L1, C1, R1 Closed to LNA

Figure 4 Test Circuits

S Parameter

The following is the test bench for input return loss, output return loss, reverse isolation, forward gain, and 1dB gain compression.

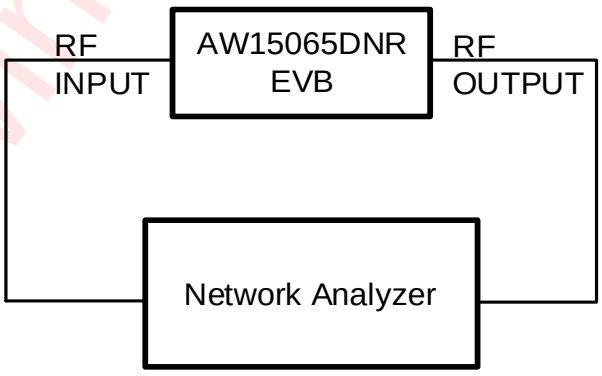


Figure 5 S Parameter Test Bench

Noise Figure

The following is the test bench for noise figure, power gain.

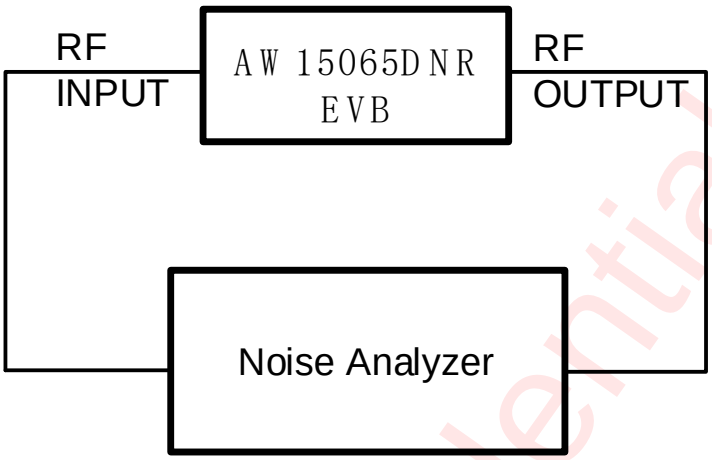


Figure 6 Noise Figure Test Bench

Intermodulation distortion

The following is the test bench for third-order intercept point and second-order intercept point.

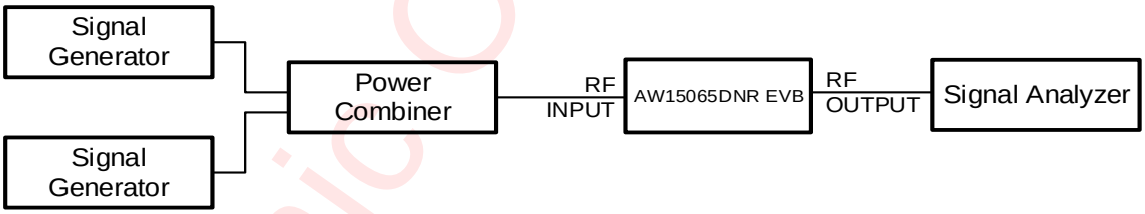


Figure 7 IIP3 Test Bench

RECOMMENDED COMPONENTS LIST

Table1 and talble2 list the recommended inductor types and values; Table 3 lists the recommended capacitor types and values.

Table1: list of inductor for GPS L1

Component	Part Number	Inductance	Q(min)	Q Test Frequency	Supplier	Size
	Units	nH		MHz		
L1	LQW15A	6.8	25	250	Murata	0402
L1	SDWL1005C	6.2	24	250	Sunlord	0402

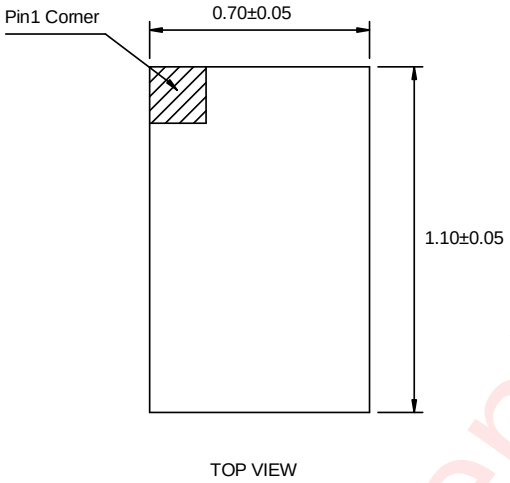
Table2: list of inductor for GPS L5

Component	Part Number	Inductance	Q(min)	Q Test Frequency	Supplier	Size
	Units	nH		MHz		
L1	LQW15A	13	25	250	Murata	0402
L2	LQW15A	9.1	25	250	Murata	0402

Table3: list of capacitor

Component	Part Number	Capacitance	Rated Voltage	Supplier	Size
	Units	pF	V		
C1	GRM155	1000	50	Murata	0402
C2	GRM155	2	50	Murata	0402

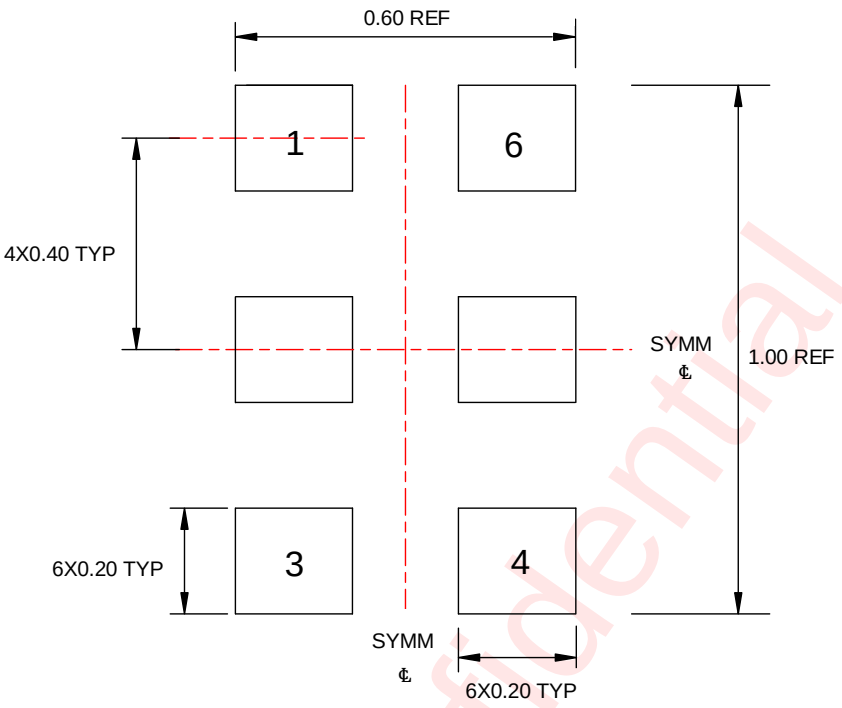
Package Description

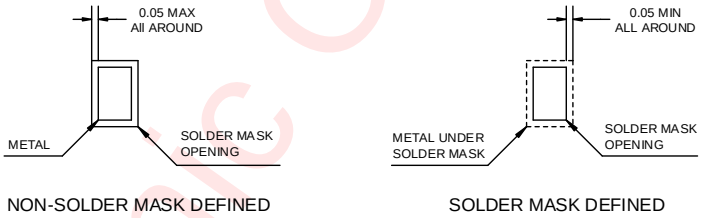


Unit：mm

Package Outline

LAND PATTERN

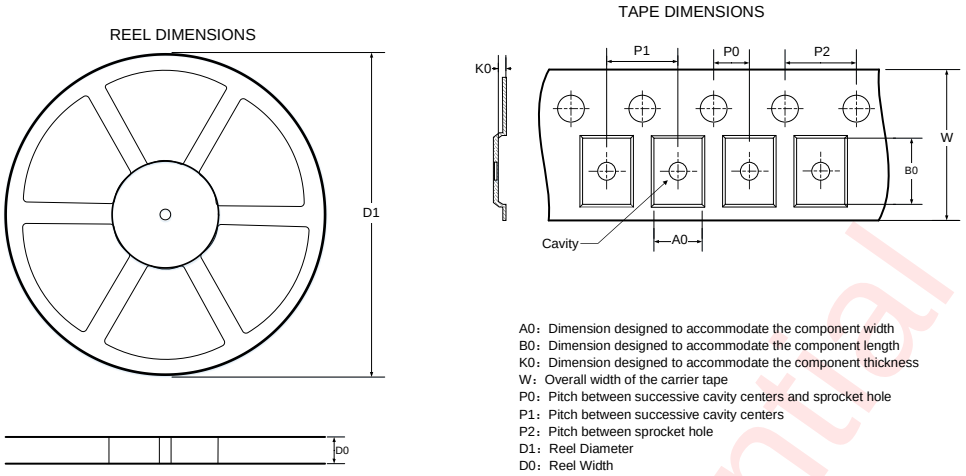




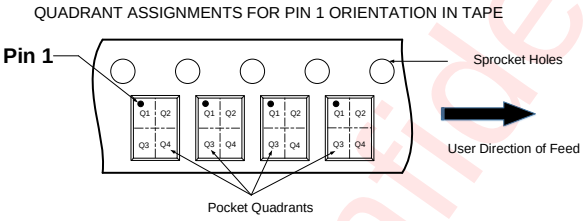
Unit: mm

Figure 9 Land Pattern

TAPE & REEL DESCRIPTION



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width



Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.4	0.82	1.22	0.46	2	2	4	8	Q1

All dimensions are nominal

Figure 10 Tape & Reel Description

REVISION HISTORY

Version	Date	Change Record
V1.0	May. 2020	Officially Released
V1.1	Feb. 2021	Update and modify the electrical characteristics
V1.2	Jul. 2022	Update and modify the electrical characteristics
V1.3	Jul. 2022	Update and modify the electrical characteristics

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