300mA Low Quiescent Current Low-Dropout Linear Regulator

Features

- Input voltage range: 1.2V to 5.5V
- Fixed outputs of 0.8V, 0.9V, 1.2V, 1.5V, 2.5V,1.8V, 2.8V, 3.0V, 3.3V
- Rated output current: 300mA
- Quiescent current: typical 2μA
- Typical 0.1μA shutdown current
- Typical 320mV dropout voltage (I_{OUT}=300mA, 1.8V output)
- Power supply rejection ratio: typical 75dB (I_{OUT}=30mA, freq=1kHz, 1.8V output)
- Noise: typical 60μVrms (I_{OUT}=30mA, BW=10Hz to 100kHz, 1.8V output)
- Built-in output short protection: typical 300mA when output short to ground
- DFN 1mmX1mmX0.37mm-4L package and SOT 23-5L package

General Description

AW37103YXXX is a low quiescent current low dropout voltage regulator featuring low ON resistance, high PSRR, low Noise, good load/line transient response and smooth soft-start.

AW37103YXXX integrates current limit, short circuit protection, thermal shutdown, sufficiently protecting IC from being damaged.

AW37103YXXX is designed to work with a 1μF or more input ceramic capacitor and a 1μF or more output ceramic capacitor. The low quiescent current make AW37103YXXX very suitable for battery application with long service life. Tiny package makes high density mounting of the IC on boards possible.

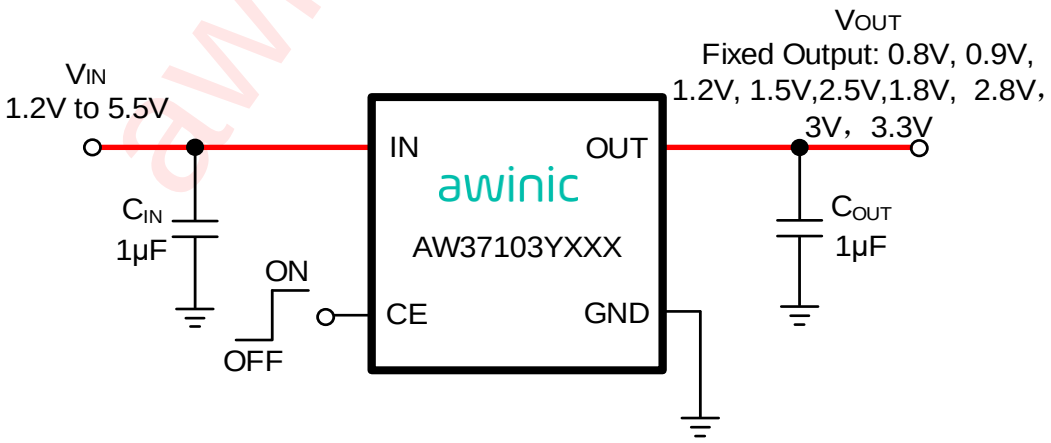
Applications

Battery-powered equipment

Smart phone

Wearables electronics

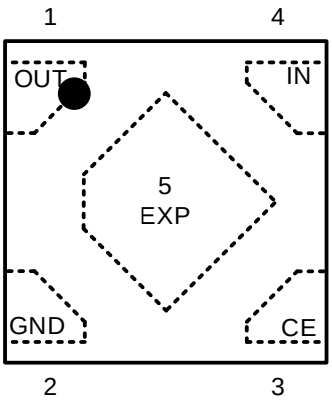
Typical Application Circuit



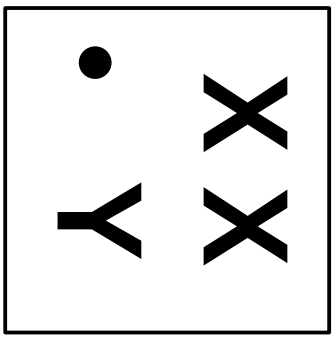
Pin Configuration And Top Mark

DFN 1mmX1mmX0.37mm-4L

AW37103YXXXDNR (Top View)



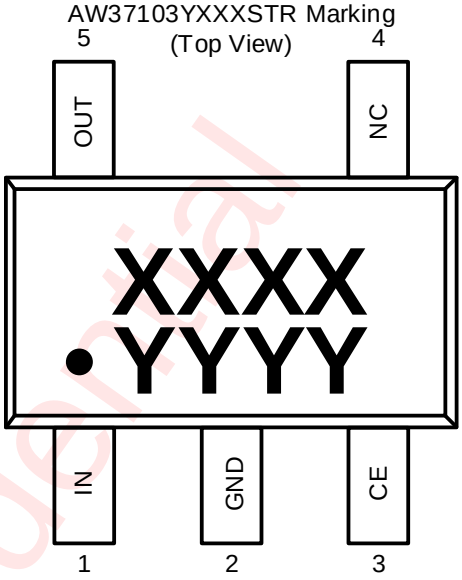
AW37103YXXXDNR Marking (Top View)



XX – AW37103YXXXDNR
Y – Production Tracing Code

SOT23-5L

AW37103YXXXSTR Marking (Top View)

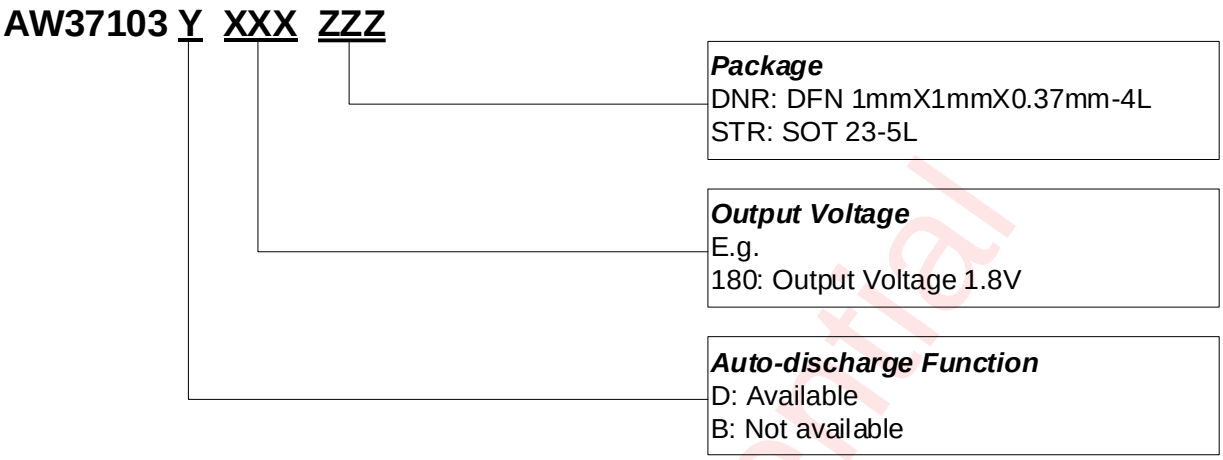


XXXX – AW37103YXXXSTR
YYYY – Production Tracing Code

Pin Definition

Pin No.		Pin NAME	DESCRIPTION
DFN1*1-4L	SOT23-5L		
1	5	OUT	Regulated output voltage pin. Put a 1μF or more ceramic capacitor at the output pin.
2	2	GND	Ground.
3	3	CE	Chip enable pin. Built-in 30nA pull-down current. (High Active)
4	1	IN	Input supply pin. Put a 1μF or more bypass capacitor at the power supply.
5	-	EXP	Expose pad should be tied to ground plane for better power dissipation.

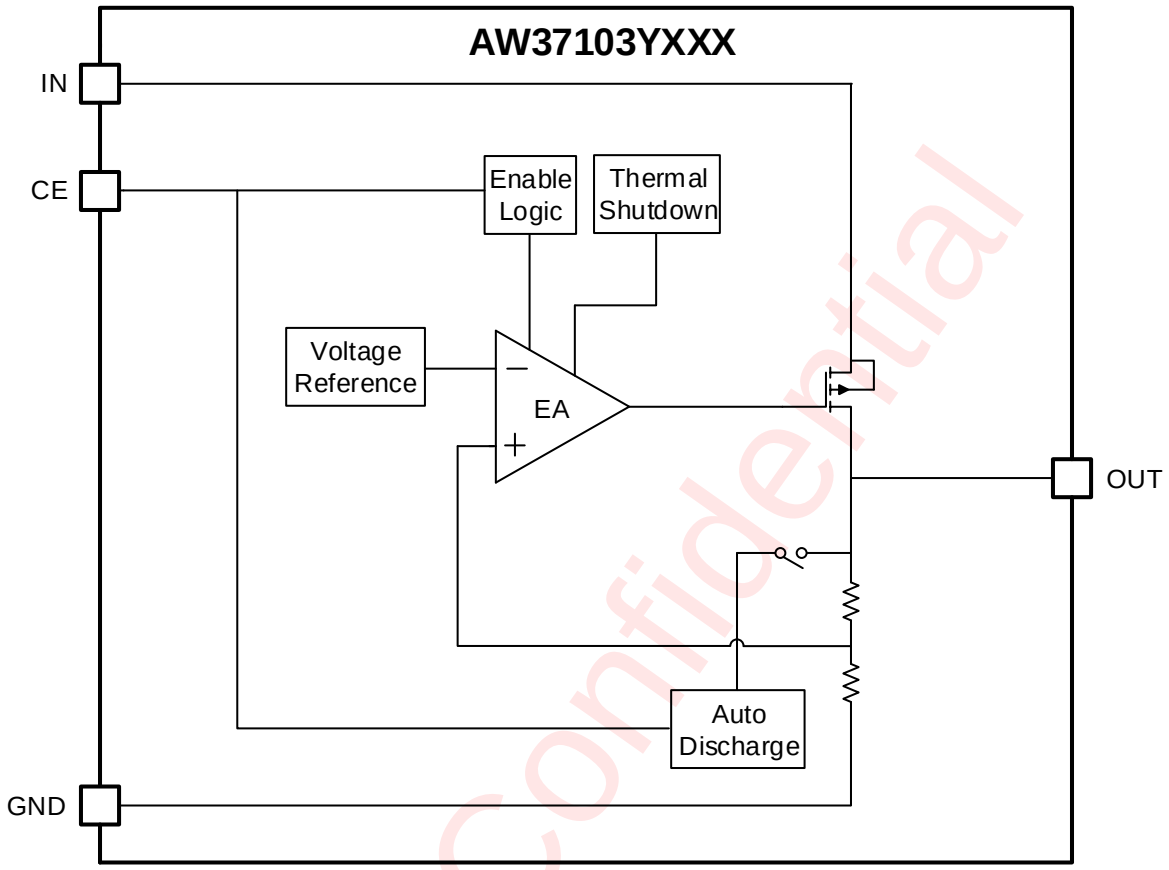
Name Rule



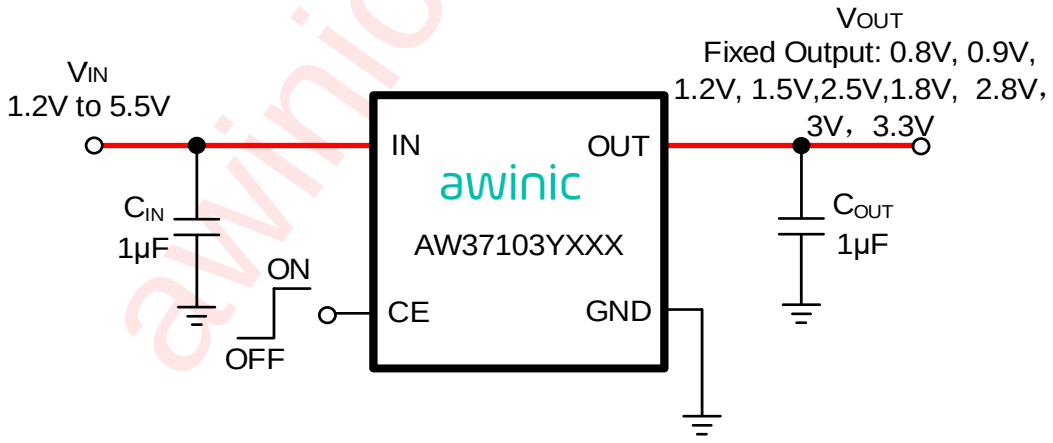
Device Comparison Table

Part Number	$V_{OUT(SET)}$	Rated Current	CE Active	Auto Discharge
AW37103D080DNR	0.8V	300mA	High	YES
AW37103D090DNR	0.9V	300mA	High	YES
AW37103D120DNR	1.2V	300mA	High	YES
AW37103D150DNR	1.5V	300mA	High	YES
AW37103D180DNR	1.8V	300mA	High	YES
AW37103D250DNR	2.5V	300mA	High	YES
AW37103D280DNR	2.8V	300mA	High	YES
AW37103D300DNR	3.0V	300mA	High	YES
AW37103D330DNR	3.3V	300mA	High	YES
AW37103D080STR	0.8V	300mA	High	YES
AW37103D090STR	0.9V	300mA	High	YES
AW37103D120STR	1.2V	300mA	High	YES
AW37103D150STR	1.5V	300mA	High	YES
AW37103D180STR	1.8V	300mA	High	YES
AW37103D250STR	2.5V	300mA	High	YES
AW37103D280STR	2.8V	300mA	High	YES
AW37103D300STR	3.0V	300mA	High	YES
AW37103D330STR	3.3V	300mA	High	YES

Functional Block Diagram



Typical Application Circuits



AW37103YXXX Application circuit

Notice for typical application circuits:

Capacitance of C_{IN} and C_{OUT} should be 1μF or more.`

A ceramic capacitor has different temperature characteristics and bias dependencies depending on the size, manufacturer or part number of a capacitor. Careful evaluation is required. The effective capacitance of C_{OUT} should be greater than 0.7μF over the full range of operating conditions. When OUT<1.2V,choose a 2.2uF or more C_{OUT} .

Ordering Information

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW37103D080DNR	-40°C～85°C	DFN 1mmX1mm-4L	CR	MSL1	ROHS+HF	3000 units/ Tape and Reel
AW37103D090DNR	-40°C～85°C	DFN 1mmX1mm-4L	SW	MSL1	ROHS+HF	3000 units/ Tape and Reel
AW37103D120DNR	-40°C～85°C	DFN 1mmX1mm-4L	VF	MSL1	ROHS+HF	3000 units/ Tape and Reel
AW37103D150DNR	-40°C～85°C	DFN 1mmX1mm-4L	FR	MSL1	ROHS+HF	3000 units/ Tape and Reel
AW37103D180DNR	-40°C～85°C	DFN 1mmX1mm-4L	FV	MSL1	ROHS+HF	3000 units/ Tape and Reel
AW37103D250DNR	-40°C～85°C	DFN 1mmX1mm-4L	NN	MSL1	ROHS+HF	3000 units/ Tape and Reel
AW37103D280DNR	-40°C～85°C	DFN 1mmX1mm-4L	YM	MSL1	ROHS+HF	3000 units/ Tape and Reel
AW37103D300DNR	-40°C～85°C	DFN 1mmX1mm-4L	NS	MSL1	ROHS+HF	3000 units/ Tape and Reel
AW37103D330DNR	-40°C～85°C	DFN 1mmX1mm-4L	XN	MSL1	ROHS+HF	3000 units/ Tape and Reel
AW37103D080STR	-40°C～85°C	SOT23-5L	WDTW	MSL3	ROHS+HF	3000 units/ Tape and Reel
AW37103D090STR	-40°C～85°C	SOT23-5L	H4N5	MSL3	ROHS+HF	3000 units/ Tape and Reel
AW37103D120STR	-40°C～85°C	SOT23-5L	ZSKN	MSL3	ROHS+HF	3000 units/ Tape and Reel
AW37103D150STR	-40°C～85°C	SOT23-5L	ZC77	MSL3	ROHS+HF	3000 units/ Tape and Reel
AW37103D180STR	-40°C～85°C	SOT23-5L	2JTY	MSL3	ROHS+HF	3000 units/ Tape and Reel
AW37103D250STR	-40°C～85°C	SOT23-5L	0KSU	MSL3	ROHS+HF	3000 units/ Tape and Reel

AW37103D280STR	-40°C～85°C	SOT23-5L	QWU5	MSL3	ROHS+HF	3000 units/ Tape and Reel
AW37103D300STR	-40°C～85°C	SOT23-5L	F3EK	MSL3	ROHS+HF	3000 units/ Tape and Reel
AW37103D330STR	-40°C～85°C	SOT23-5L	U2M0	MSL3	ROHS+HF	3000 units/ Tape and Reel

Absolute Maximum Ratings(NOTE1)

PARAMETERS	RANGE	
Input voltage range	-0.3V to 6.5V	
Enable control voltage range	-0.3V to 6.5V	
Output voltage range	-0.3V to VIN+0.3V, max. 6.5V	
Maximum operating junction temperature T_{JMAX}	150°C	
Recommended operating junction temperature T_{JREC}	-40°C to 125°C	
Operating free-air temperature range	-40°C to 85°C	
Storage temperature T_{STG}	-65°C to 150°C	
Lead temperature (soldering 10 seconds)	260°C	
Junction-to-ambient thermal resistance θ_{JA} (NOTE2)	DFN1*1-4L	232°C/W
	SOT23-5L	180°C/W
ESD		
HBM (Human body model)(NOTE3)	±2kV	
CDM(Charged device model) (NOTE4)	±1.5kV	
Latch-Up		
Latch-Up(NOTE5)	+IT：200mA - IT：-200mA	

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: Thermal resistance from junction to ambient follows JEDEC 2S2P standards, and is highly dependent on PCB layout.

NOTE3: All pins. Test Condition: ESDA/JEDEC JS-001-2017.

NOTE4: All pins. Test Condition: ESDA/JEDEC JS-002-2018.

NOTE5: Test Condition: JESD78E.

Electrical Characteristics

V_{IN}=$V_{OUT(SET)}$+1V, V_{CE}>1V, I_{OUT}=1mA, C_{IN}=C_{OUT}=1μF, T_A=25°C (unless otherwise noted)

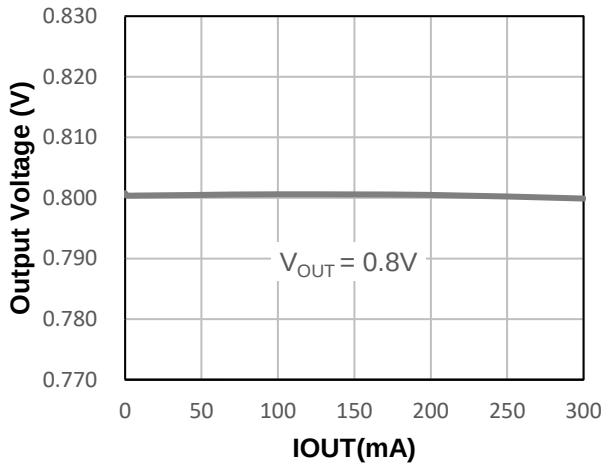
PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IN}	Input Voltage Range		1.2		5.5	V
V_{OUT_ACC}	Output Voltage Accuracy	T_A=25°C, I_{OUT}=1mA	-2		2	%
$LOAD_{Reg}$	Load Regulation	1mA≤I_{OUT}≤300mA		0.5		%
$LINE_{Reg}$	Line Regulation	$V_{OUT(SET)}$+0.5V≤V_{IN} ≤5.5V , I_{OUT}=1mA		1		mV
$V_{dropout}$	Dropout Voltage(1) I_{OUT}=300mA	$V_{OUT(SET)}$=1.8V		330		mV
		$V_{OUT(SET)}$=2.8V		203		
		$V_{OUT(SET)}$=3.0V		187		
		$V_{OUT(SET)}$=3.3V		179		
I_{SD}	Shutdown Current	V_{CE}<0.4V		0.1	1	μA
I_Q	Quiescent Current	I_{OUT}=0mA		2	4	μA
V_{CEH}	CE Input Voltage “H”	-40°C ≤T_A≤85°C	1			V
V_{CEL}	CE Input Voltage “L”	-40°C ≤T_A≤85°C			0.4	V
PSRR	Power Supply Ripple Rejection	I_{OUT}=30mA, f=1kHz $V_{OUT(SET)}$=1.8V		75		dB
V_N	Output Voltage Noise I_{OUT}=30mA BW=10Hz to 100kHz	$V_{OUT(SET)}$=0.8V		50		μVrms
		$V_{OUT(SET)}$=1.8V		60		
		$V_{OUT(SET)}$=2.8V		80		
		$V_{OUT(SET)}$=3.0V		84		
		$V_{OUT(SET)}$=3.3V		90		
I_{CL}	Output Current Limit	V_{OUT}=90%*$V_{OUT(SET)}$	300			mA
I_{SC}	Short Current Limit	V_{OUT}<10%*$V_{OUT(SET)}$		300		mA
VTC	Output Voltage Temperature Coefficient	-40°C ≤T_A≤85°C		±100		ppm/°C
R_{DISC}	Auto Discharge Resistance	V_{IN}=4.3V, V_{CE}<0.4V		80		Ω
I_{CE}	CE Pull Down Current			30		nA
T_{SDH}	Thermal Shutdown Threshold	Temperature Rising		155		°C
T_{SDL}	Thermal Shutdown Reset Threshold	Temperature Falling		130		°C

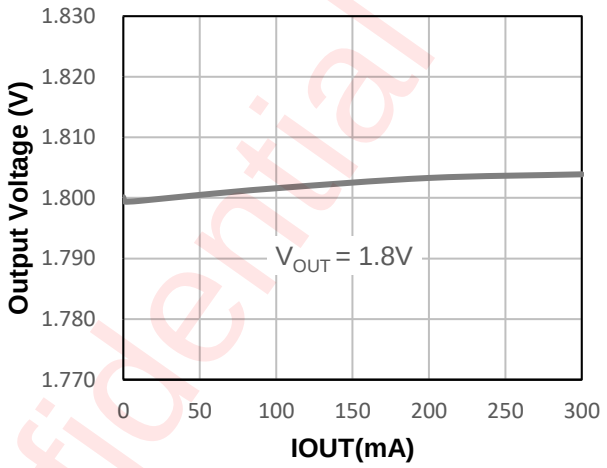
(1) Dropout voltage is the voltage difference between the input and the output at which the output voltage drops to 98% of its nominal value.

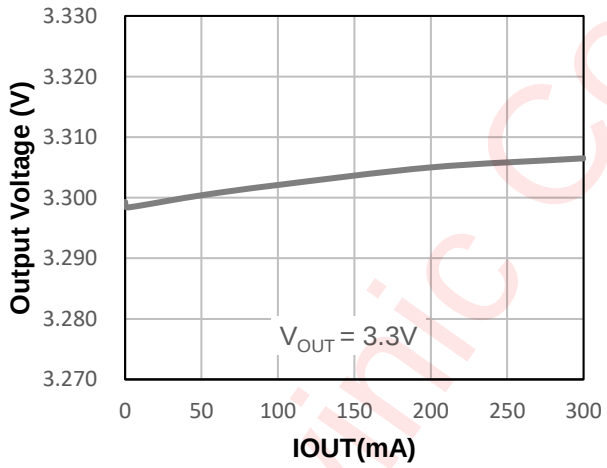
Typical Characteristics

V_{IN}=$V_{OUT(SET)}$+1V, V_{CE}>1V, I_{OUT}=1mA, C_{IN}=C_{OUT}=1μF, T_A=25°C, In Typical Application Circuit, unless otherwise noted.

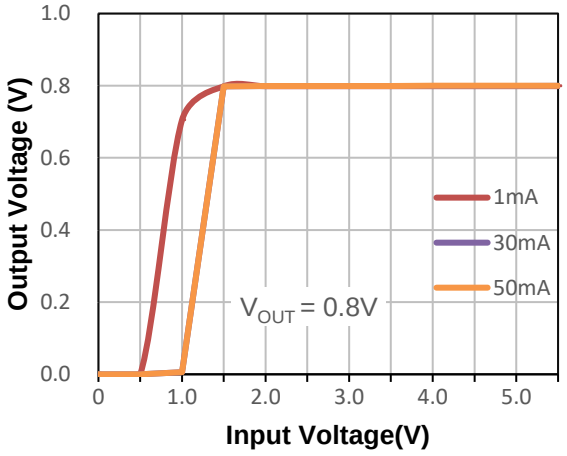
1) Ouput Voltage vs. Output Current (C_{IN}=C_{OUT}=1μF, T_A=25°C)

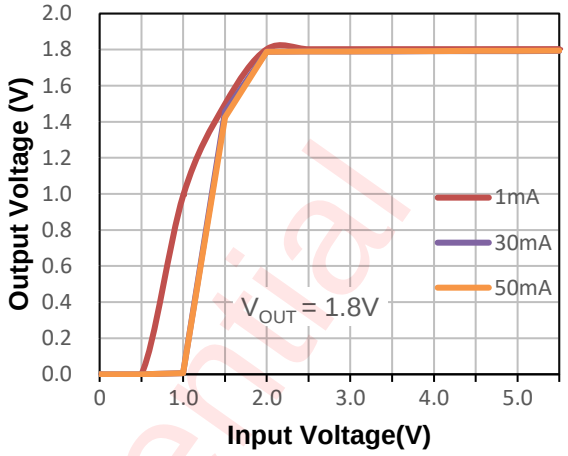


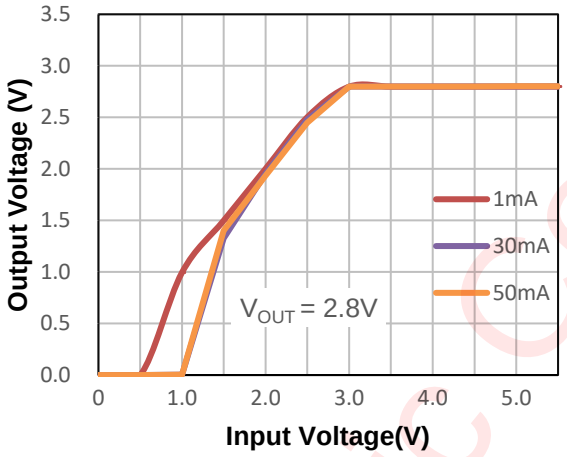


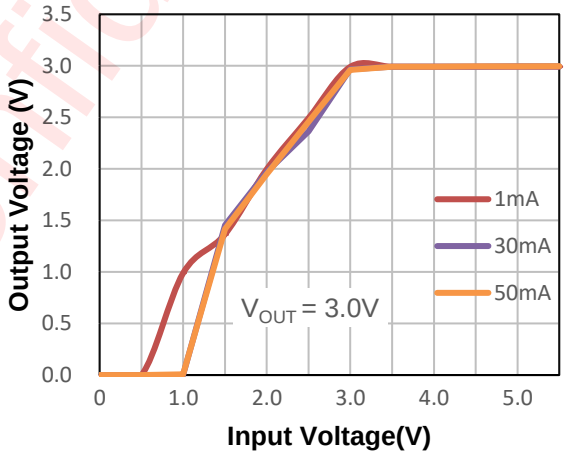


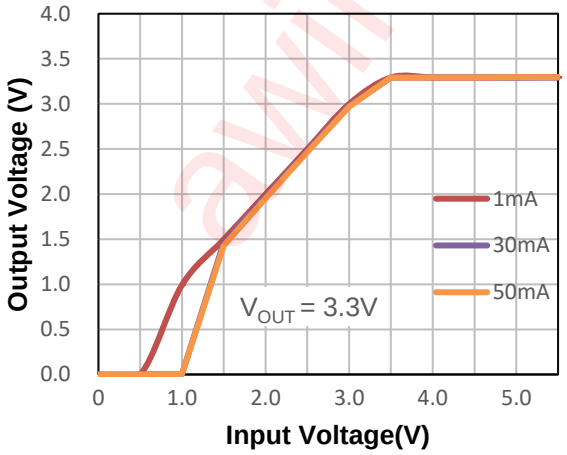
2) Ouput Voltage vs. Input Voltage (C_{IN}=C_{OUT}=1μF, T_A=25°C)



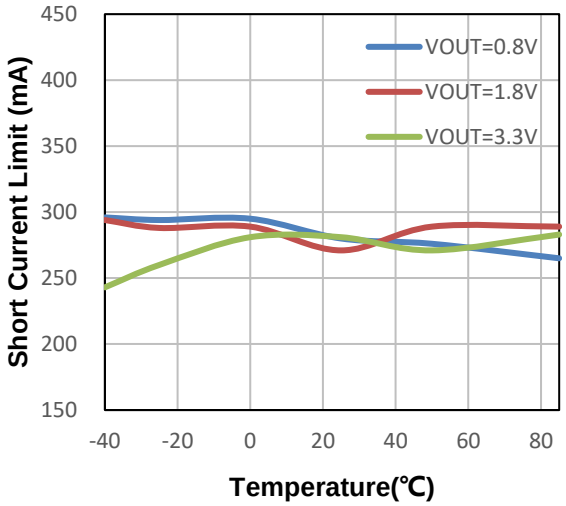




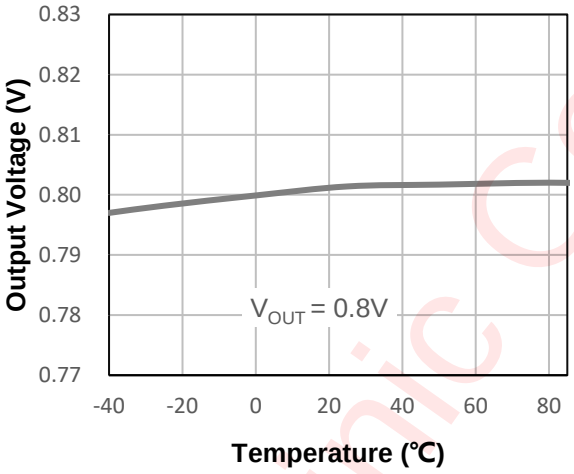


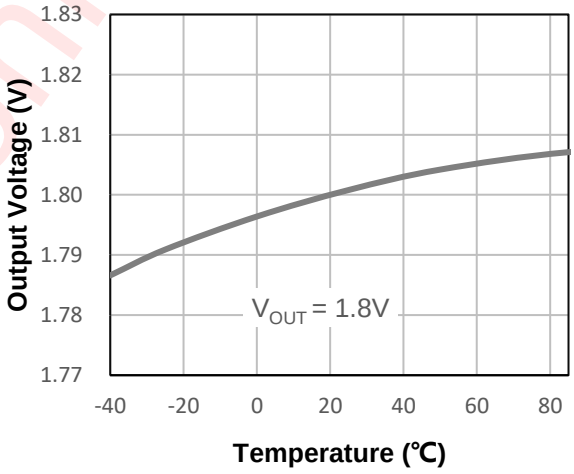


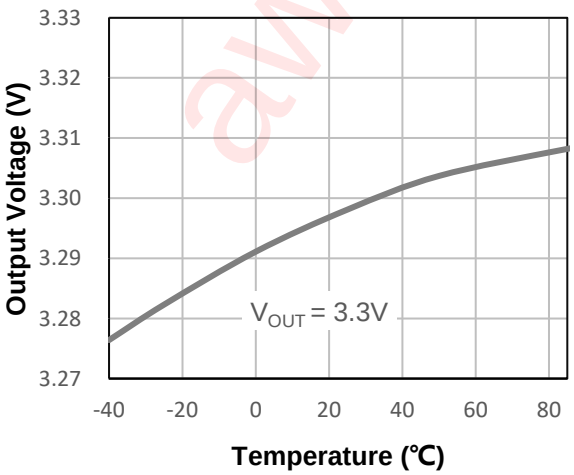
3) Short Current Limit vs. Temperature (C_{IN}=C_{OUT}=1μF)



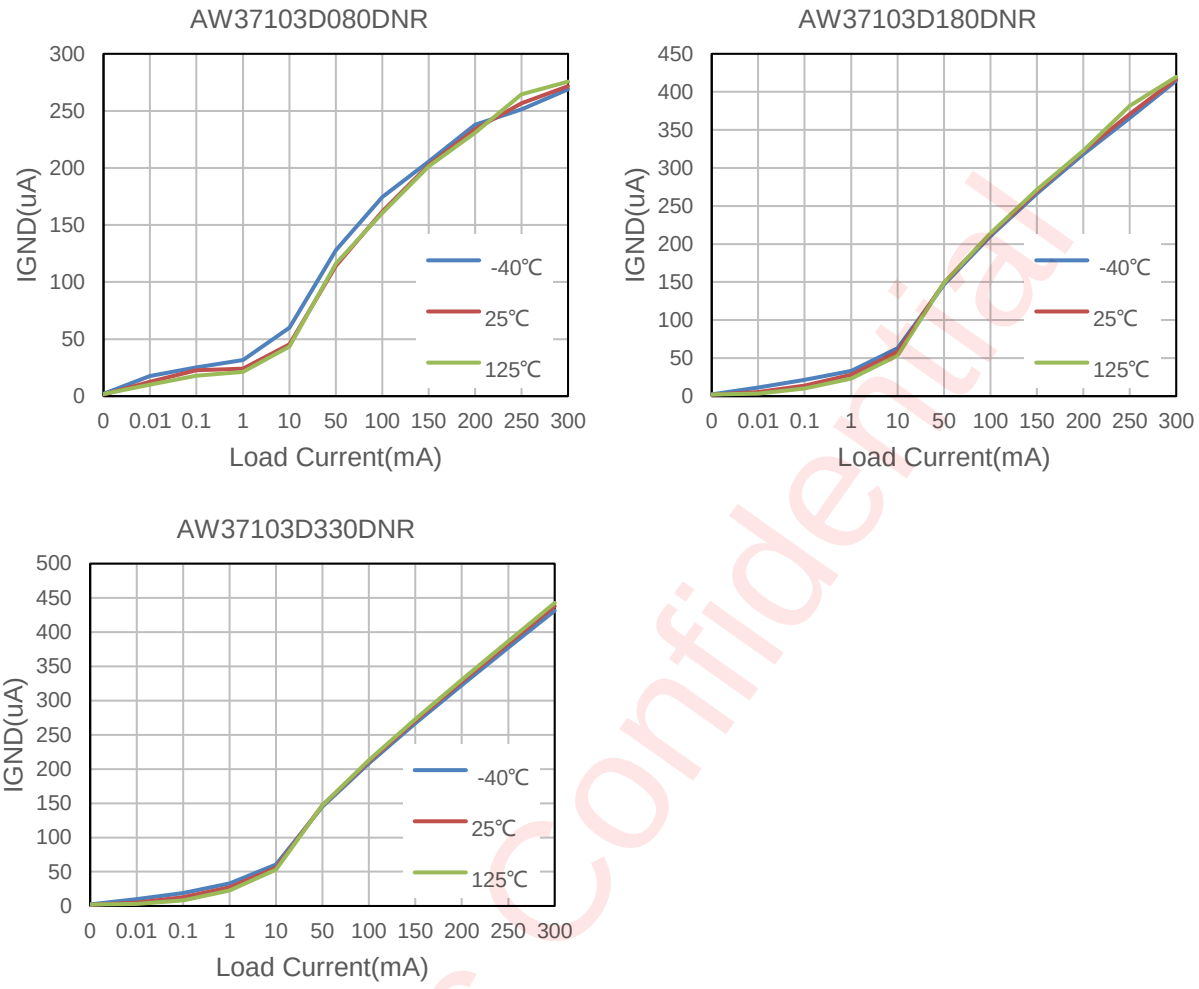
4) Ouput Voltage vs. Temperature (C_{IN}=C_{OUT}=1μF, I_{OUT}=1mA)



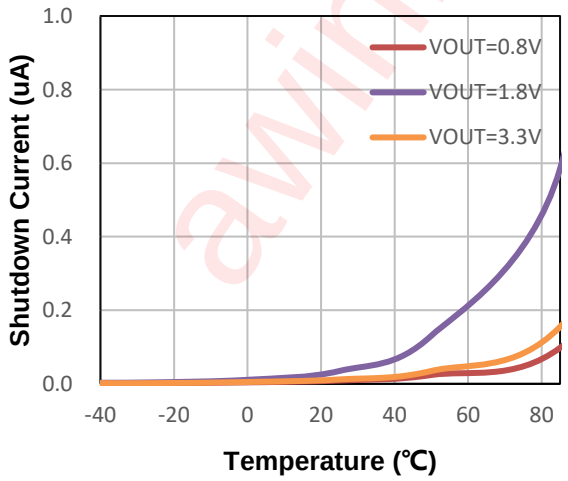




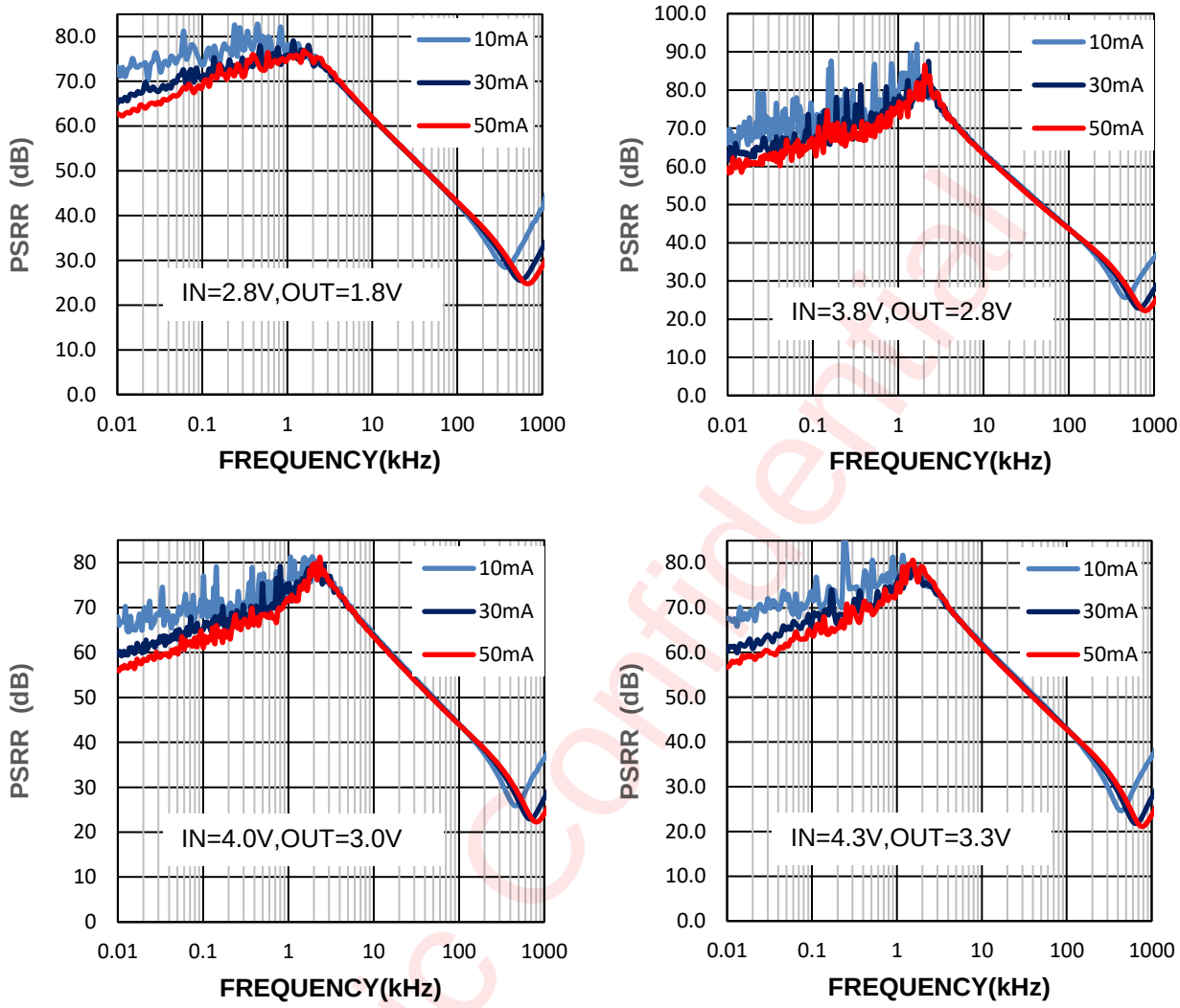
5) Ground Current vs. Load Current (C_{IN}=C_{OUT}=1μF)



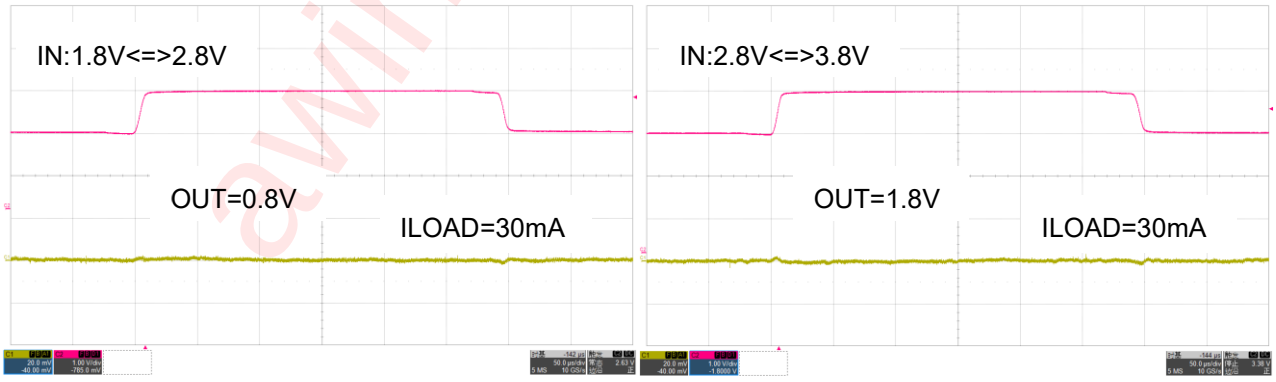
6) Shutdown Current vs. Temperature (C_{IN}=C_{OUT}=1μF)



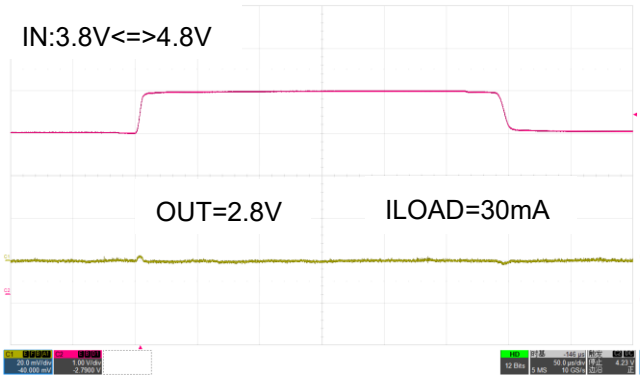
7) Ripple Rejection vs. Frequency (C_{IN}=0.1uF,C_{OUT}=1μF, T_A=25°C)



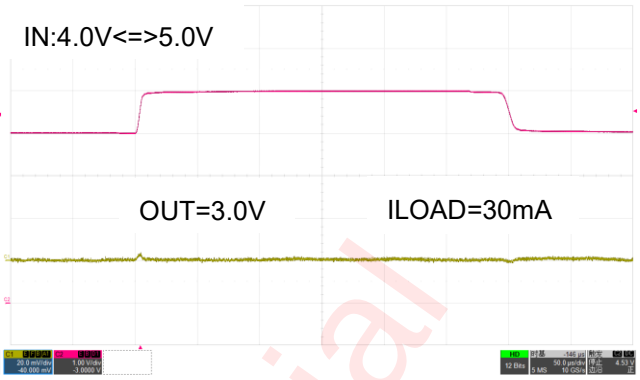
8) Line Transient (C_{IN}=C_{OUT}=1μF, tr = tf =10us, T_A=25°C)



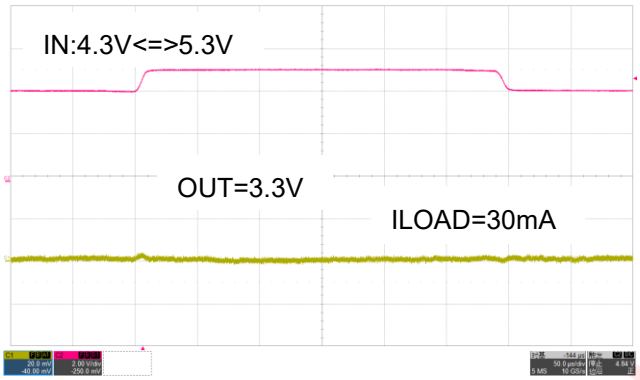
C1: 20.0mV/div C2: 1V/div C1: 20.0mV/div C2: 1V/div



C1: 20.0mV/div C2: 1V/div

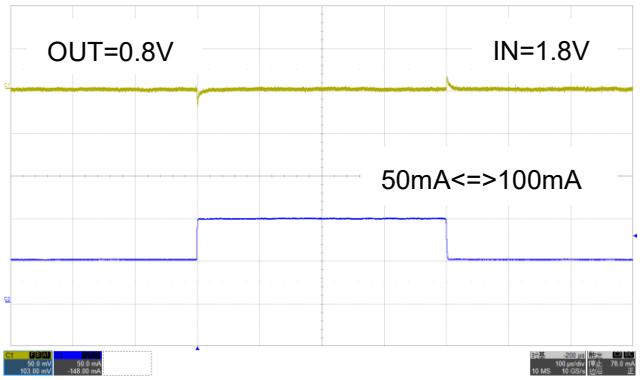


C1: 20.0mV/div C2: 1V/div

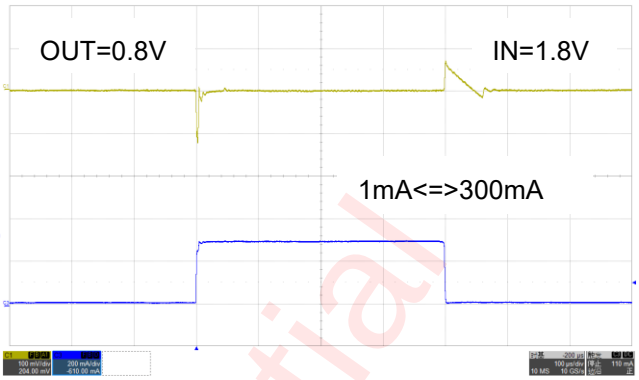


C1: 20.0mV/div C2: 2V/div

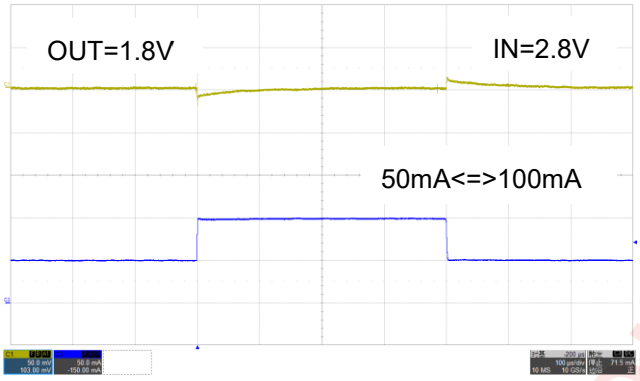
9) Load Transient (C_{IN}=C_{OUT}=1μF, tr=tf=1us, T_A=25°C)



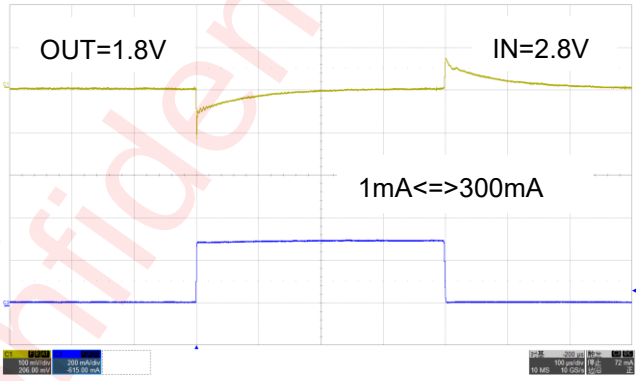
C1: 50.0mV/div C3: 50.0mA/div



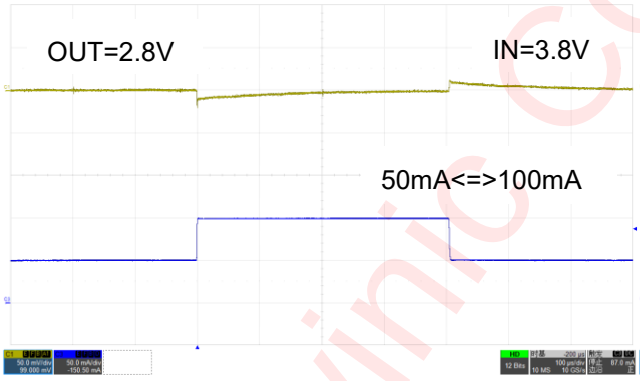
C1: 100.0mV/div C3: 200.0mA/div



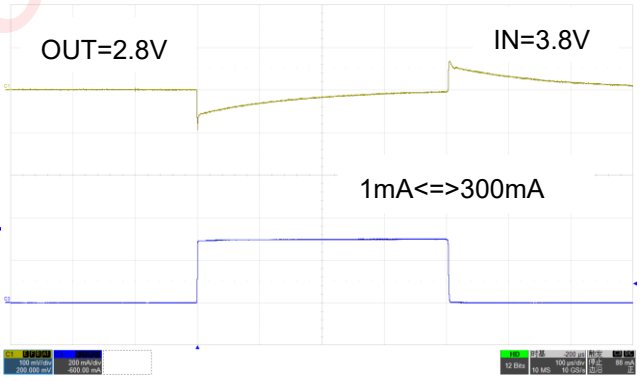
C1: 50.0mV/div C3: 50.0mA/div



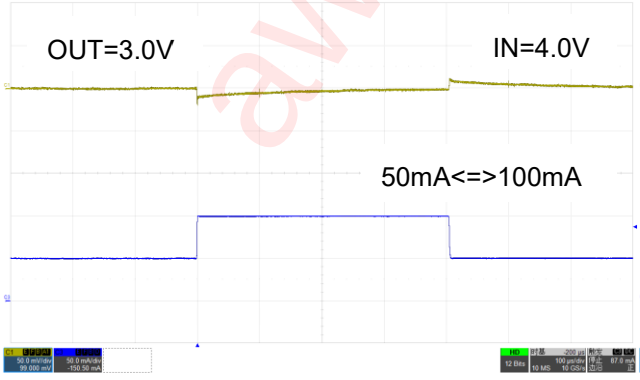
C1: 100.0mV/div C3: 200.0mA/div



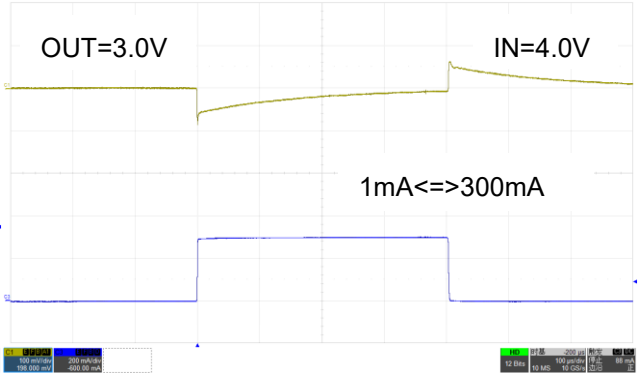
C1: 50.0mV/div C3: 50.0mA/div



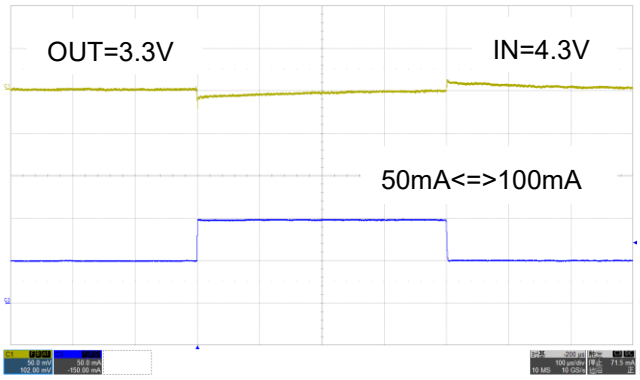
C1: 100.0mV/div C3: 200.0mA/div



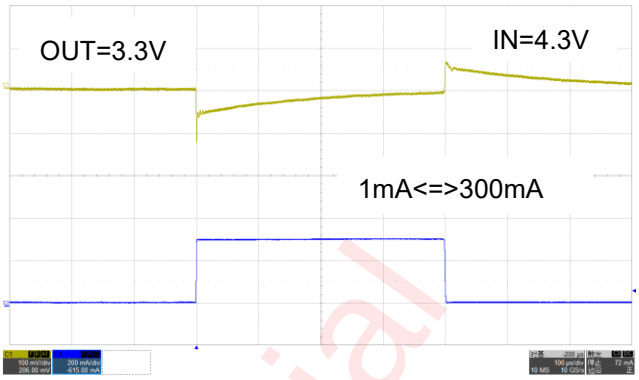
C1: 50.0mV/div C3: 50.0mA/div



C1: 100.0mV/div C3: 200.0mA/div

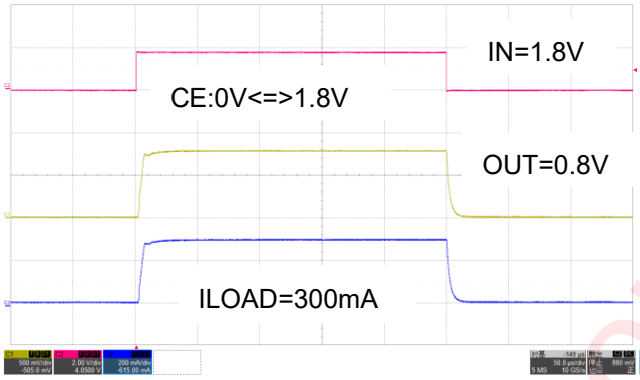


C1: 50.0mV/div C3: 50.0mA/div

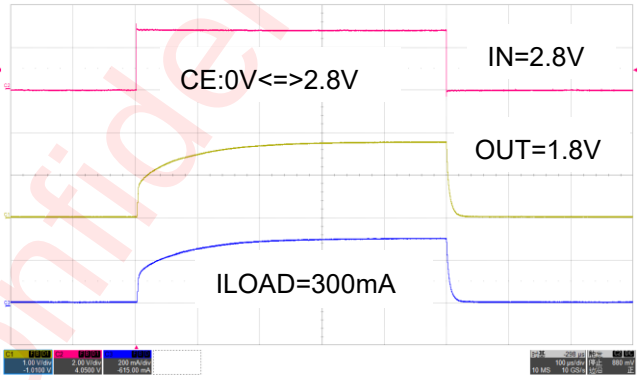


C1: 100.0mV/div C3: 200.0mA/div

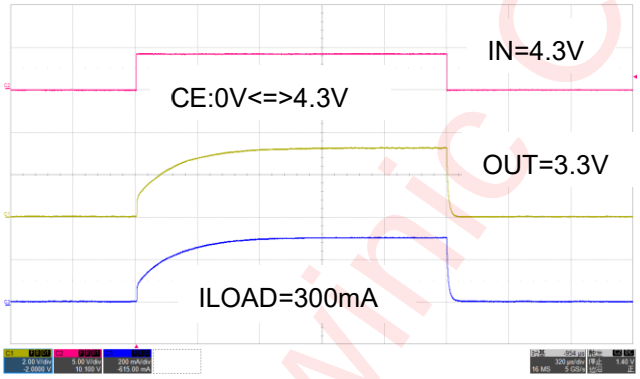
10) Turn-on/off Waveform by CE Pin signal (C_{IN}=C_{OUT}=1μF, T_A=25°C)



C1: 500mV/div C2: 2V/div C3: 200.0mA/div



C1: 1V/div C2: 2V/div C3: 200.0mA/div



C1: 2V/div C2: 5V/div C3: 200.0mA/div

Detailed Functional Description

AW37103YXXX is a low quiescent current low dropout voltage regulator. After powered on, with CE pin assertion, feedback voltage signal from the integrated resistor network and a voltage related to the voltage reference are transmit to positive input terminal and negative input terminal of an error amplifier (EA) respectively. The output signal of EA is used to control the open-state of power MOSFET. After soft-start, feedback voltage signal compares with the established reference voltage, making output voltage stable and accurate. AW37103YXXX integrates function of load transient accelerating, making LDO obtain excellent dynamic load transient response performance.

Enable Operation

AW37103YXXX uses CE pin to realize enable operation. Applying proper value of voltage to CE pin can make IC enable/disable.

If the voltage of CE pin is less than 0.4V, AW37103YXXX is guaranteed to be disabled. In this state, function modules of IC and power MOSFET are turned off. And the auto discharge function is enabled making output discharge through a on-state NMOSFET to Ground. In disable state, the ground current is reduced to a maximum of 0.5uA.

If the voltage of CE pin is more than 1V, AW37103YXXX is guaranteed to be enabled. In this state, the auto discharge function is disabled, and AW37103YXXX regulates output voltage to the designed value of voltage.

A 30nA pull down current to Ground is built-in at CE pin, making sure that the IC is disabled when CE pin floats. If Enable function is not required, CE pin should be connected directly to IN pin.

Output Current Limit

AW37103YXXX integrates output current limit function, protecting IC from excessive current.

When the load is excessively heavy, AW37103YXXX limits the current flowing through the IC to a typical 500mA current. This value is specially designed, so that IC is protected properly and the output capability of 300mA is not influenced either.

Meanwhile, AW37103YXXX integrates a 300mA fold-back current limit function, lowering the system dissipation when output overload or short to Ground.

Thermal Shutdown

AW37103YXXX integrates thermal shutdown function, protect IC from excessively high temperature.

When the chip temperature exceeds 155°C and the output current exceeds 50mA, AW37103YXXX detects it as an over-temperature event, triggering thermal shutdown, which will turn off the main function module, including power MOSFET. This inhibits increase of chip's temperature. IC would keep the protection-state on until the chip's temperature falls below to 130°C. At this moment, the over-temperature protection-state is released, IC resumes to work again.The hysteresis avoids IC's turning off and on frequently around the the Thermal Shutdown threshold.

Auto Discharge

AW37103YXXX makes output voltage discharge quickly when in CE disable state or thermal shutdown state, benefit from integrating auto discharge function. Auto discharge function is implemented by integrated a NMOSFET of typical 80Ω Rdson route from Output to Ground, and the route is get through in CE disable state or thermal shutdown state. This feature prevents residual charge voltage on the output capacitor, which may impact proper power up of the system connected to the converter. It should be noted that auto discharge

function is optional according to different specs.

Application Information

Power Dissipation and Device Operation

The permissible power dissipation is dependent on the ambient temperature T_A and the junction-to-ambient thermal resistance $R_{\theta JA}$.

The absolute maximum allowable power dissipation for the device in a given package can be calculated using Equation below, where T_{J_MAX} = 150°C :

$$PD_{MAX\_ABS} = (T_{J\_MAX} - T_A) / R_{\theta JA}$$

The recommended maximum allowable power dissipation for the device in a given package can be calculated using Equation below, where T_{J_REC} = 125°C :

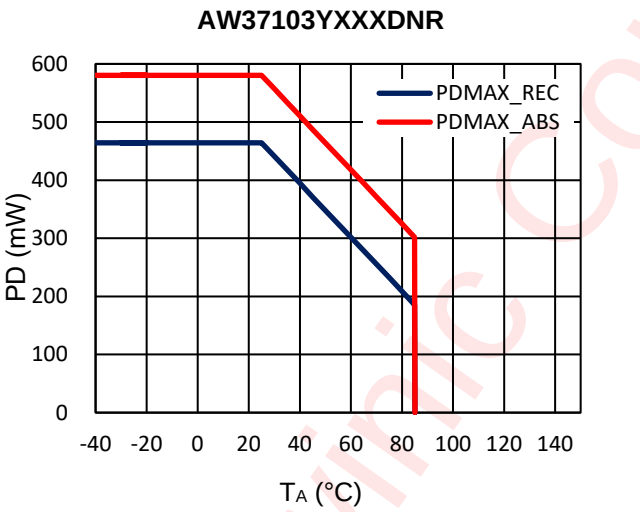
$$PD_{MAX\_REC} = (T_{J\_REC} - T_A) / R_{\theta JA}$$

The actual power being dissipated in the device can be represented by Equation below:

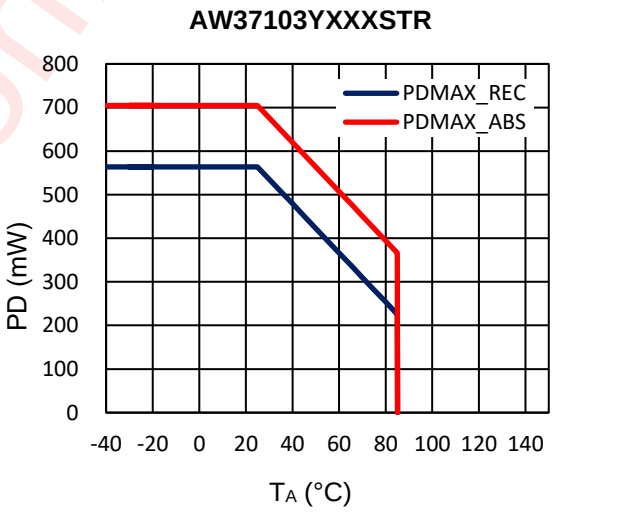
$$PD_{ACT} = (V_{IN} - V_{OUT}) \times I_{OUT}$$

These equations above establish the relationship between the maximum power dissipation allowed due to thermal consideration, the voltage drop across the device, and the continuous current capability of the device.

The graphs of Power Dissipation vs. Ambient Temperature are showed below :



Power Dissipation vs. Ambient Temperature



Power Dissipation vs. Ambient Temperature

The above graphs show the maximum power dissipation of the respective package at T_{J_REC} = 125°C and T_{J_MAX} = 150°C. Operating the device in the region between PD_{MAX_REC} and PD_{MAX_ABS} might have a negative influence on its lifetime.

Capacitors Selection

IN pin: Input Capacitor C_{IN}

AW37103YXXX advises to use a 1μF or more X5R or X7R ceramic capacitor at IN pin as shown in Typical Application Circuit.

OUT pin: Output Capacitor C_{OUT}

AW37103YXXX advises to use a 1μF or more X5R or X7R ceramic capacitor at OUT pin as shown in Typical Application Circuit.

Recommended Components List

Component	PART No.	DESCRIPTION	MFR	TYP.	UNIT
C_{IN}	GRM155R61A105KE15	10V, X5R, 0402	MURATA	1	μF
C_{OUT}	GRM155R61A105KE15	10V, X5R, 0402	MURATA	1	μF
	GRM153R60J225ME95	6.3V, X5R, 0402	MURATA	2.2	μF
	GRM153R60J475ME15	6.3V, X5R, 0402	MURATA	4.7	μF

PCB Layout Consideration

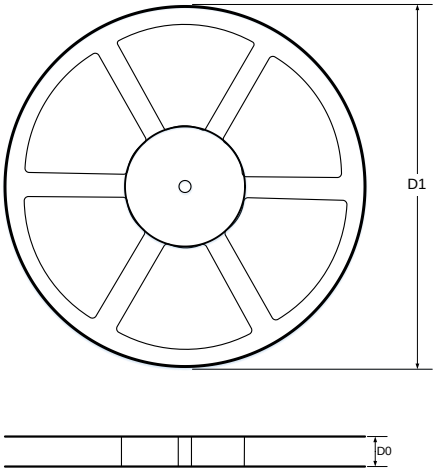
The performance of a power source circuit using this device is highly dependent on a peripheral circuit. To obtain the optimal performance, a peripheral component or the device mounted on PCB should not exceed its rated voltage, rated current or rated power. When designing a peripheral circuit, guidelines below for PCB layout of AW37103YXXX should be obeyed:

1. All peripheral components should be placed as close to the chip as possible. C_{IN} and C_{OUT} should be close to IN and OUT pins respectively. Avoid connecting device and chip pins with two different layers of copper, use the same layer of copper instead.
2. IN and OUT pin are the large current input and output of the chip, make IN, OUT, and meanwhile GND lines sufficient.
3. The connection lines between the planes of C_{IN} or C_{OUT} and respective chip pin should be as short and wide as possible, to reduce noise and EMI interference, or it may cause noise pickup or unstable operation.
4. The exposed plane of chip and GND pins must be connected to the large-area ground layer of PCB directly, meanwhile place sufficient vias below the exposed plane. Thus we can decrease the thermal resistor on the board to optimize heat-diffusion performance.

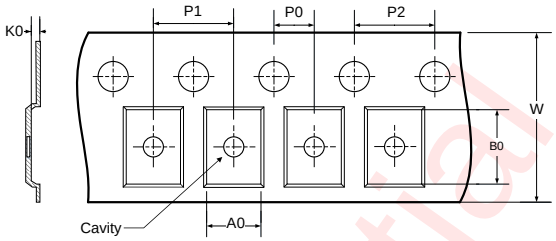
Tape And Reel Information

DFN 1mmX1mm-4L

REEL DIMENSIONS

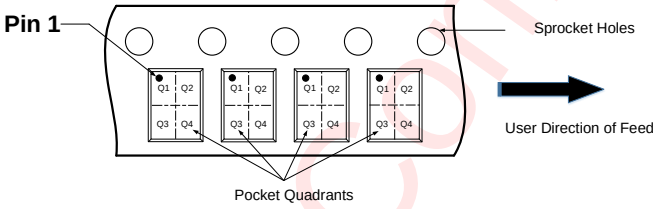


TAPE DIMENSIONS



A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

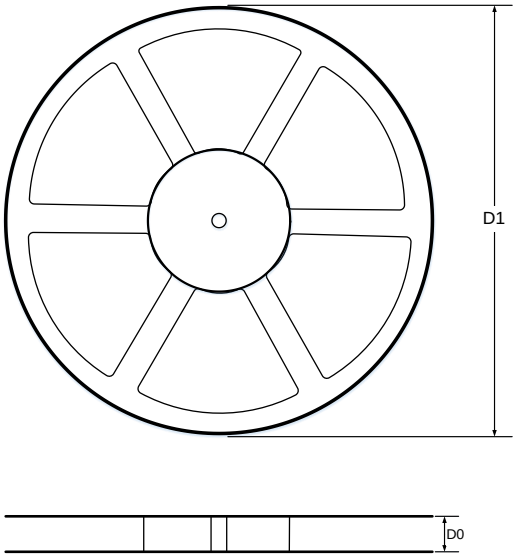
DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.4	1.14	1.17	0.56	2	4	4	8	Q1

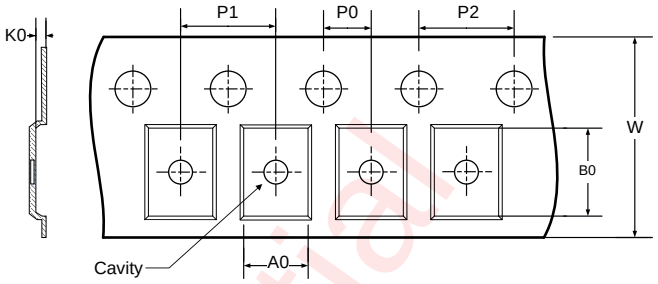
All dimensions are nominal

SOT 23-5L

REEL DIMENSIONS



TAPE DIMENSIONS



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W：Overall width of the carrier tape
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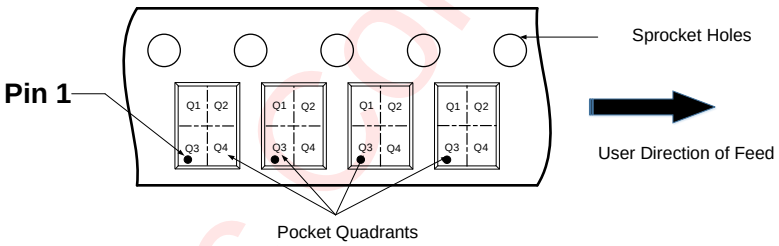
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note：The above picture is for reference only. Please refer to the value in the table below for the actual size

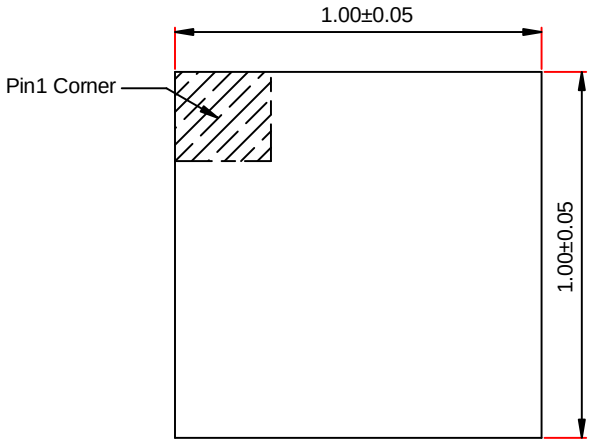
DIMENSIONS AND PIN1 ORIENTATION

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
178	8.4	3.3	3.2	1.4	2	4	4	8	Q3

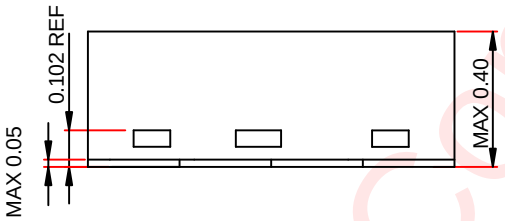
All dimensions are nominal

Package Description

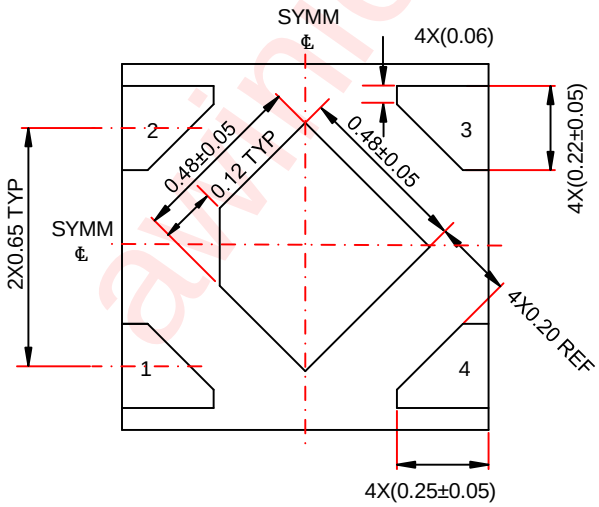
DFN 1mmX1mm-4L



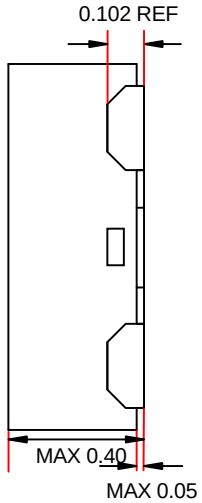
Top View



Side View



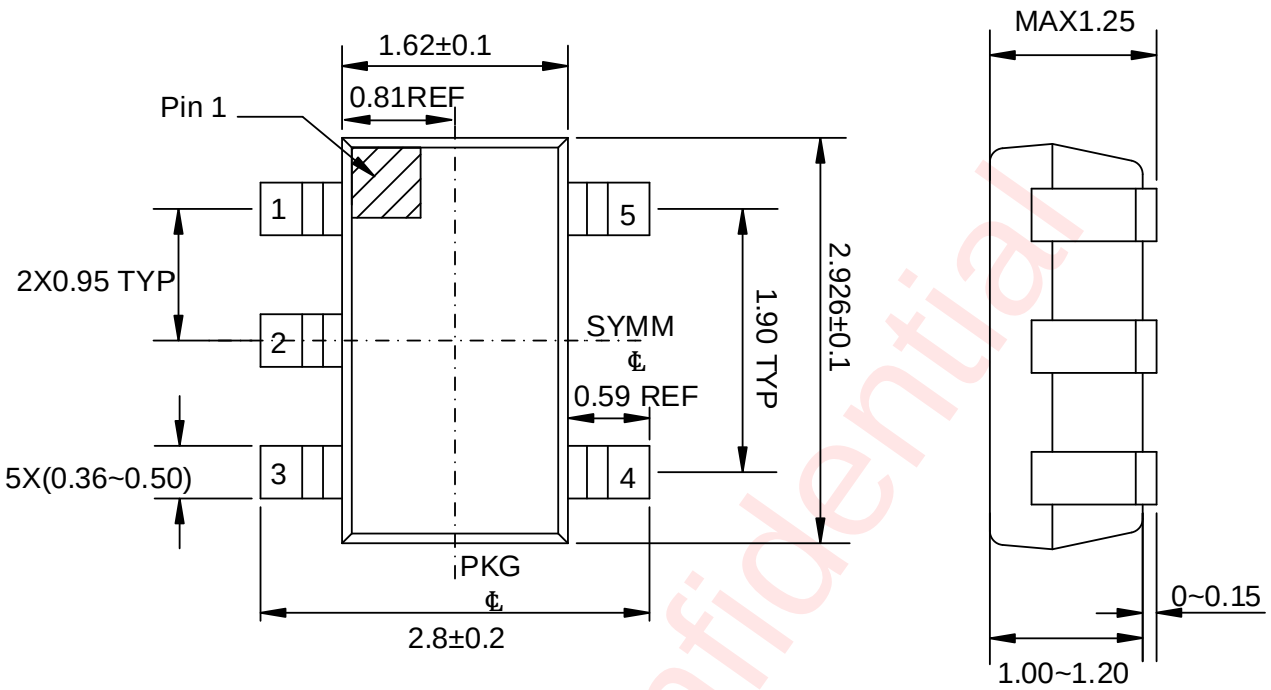
Bottom View



Side View

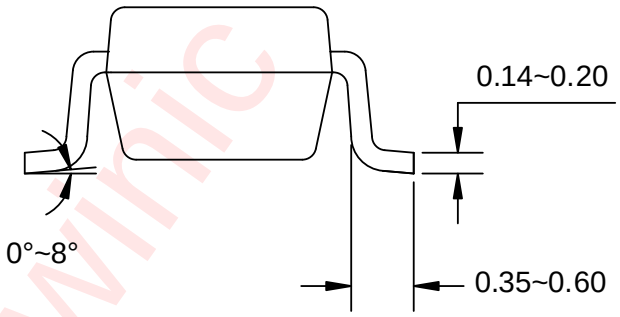
Unit:mm

SOT 23-5L



Top View

Side View

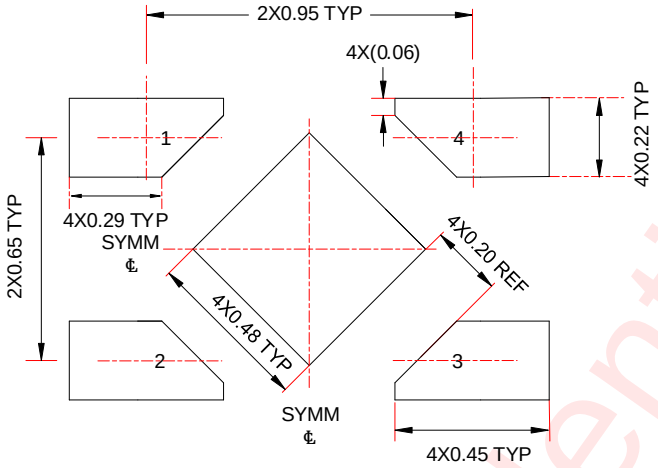


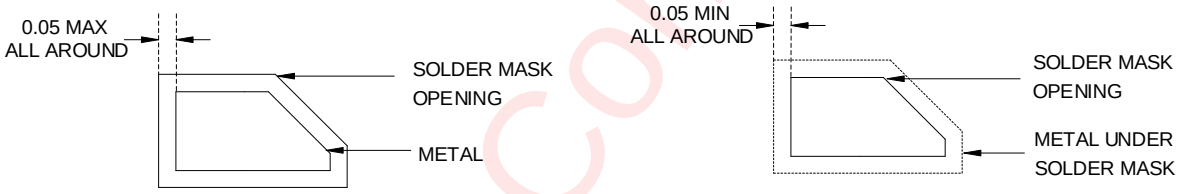
Side View

Unit: mm

Land Pattern Data

DFN 1mmX1mm-4L



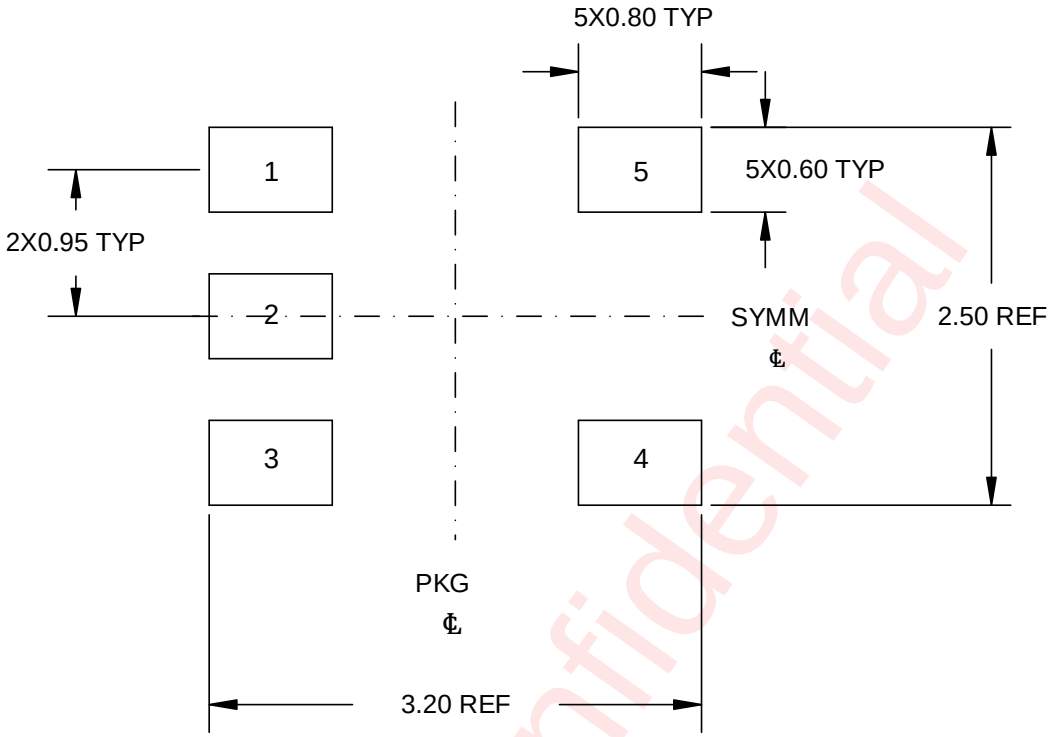


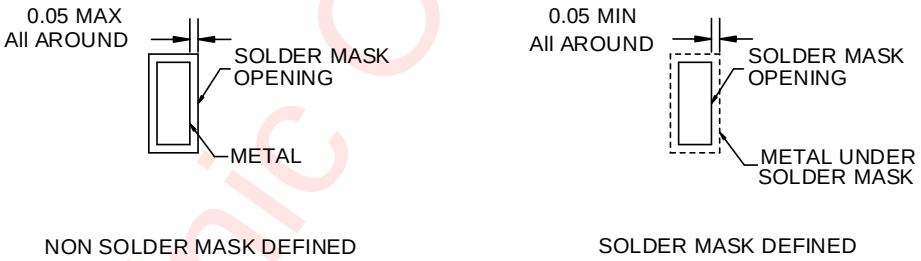
NON SOLDER MASK DEFINED

SOLDER MASK DEFINED

UNIT : mm

SOT 23-5L



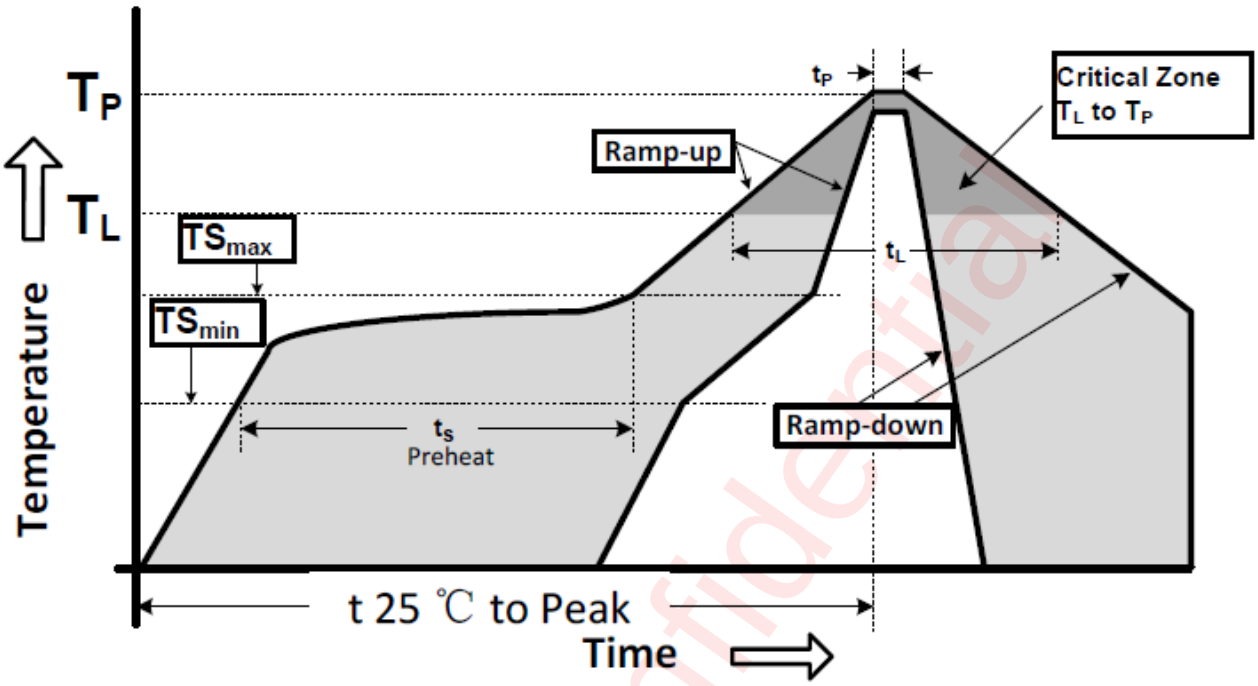


NON SOLDER MASK DEFINED

SOLDER MASK DEFINED

Unit: mm

Reflow



Reflow Note	Spec
Ramp-up rate（TSmax to T_P）	3°C/second max.
Preheat temperature（TSmin to TSmax）	150°C to 200°C
Preheat time（t_s）	60 - 180 seconds
Time above T_L , 217°C（t_L）	60 - 150 seconds
Peak temperature（T_P）	260°C
Time within 5°C of peak temperature(t_P)	20 - 40 seconds
Ramp-down rate	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

Revision History

Version	Date	Change Record
V1.0	Mar. 2021	Officially released
V1.1	Jul. 2021	Add curve: Ground Current vs. Load Current
V1.2	Oct. 2021	Add 2.8V and 3.0V curve
V1.3	Jan. 2022	Add 1.2V edition
V1.4	Jun. 2022	Add max value of Quiescent Current; Add graphs of Power Dissipation vs. Ambient Temperature; Add reflow curve; Update Tape And Reel Information
V1.5	Aug. 2022	Update SOT 23-5L package description
V1.6	Sep. 2022	Add 1.5V and 2.5V edition

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