36-CHANNEL INTELLIGENT 8-BIT RGB LED DRIVER

FEATURES

- AEC-Q100 Qualified
- 36-channel RGB LED Driver
  - Global 256-level DC current configuration
  - Individual 256-level PWM for dimming
  - Individual 256-level current for color-mixing
- High-precision current sinks
  - Device-to-device error: ±7%
  - Channel-to-channel error: ±6%
- EMI and audible noise reduction
  - Phase delay and phase inverting scheme
  - Spread spectrum function
- Flexible LED lighting pattern control
- LED open/short detection per channel
- Auto power saving mode when all LEDs off > 32ms
- Over-temperature protection
- 400 kHz I^2C interface, four selectable addresses
- Power supply: 2.7V~5.5V
- -40°C to +125°C temperature range
- QFP 7mmX7mmX1.2mm-48L package

APPLICATIONS

Automotive atmosphere lamp
Automotive dashboards backlight
Automotive ambient light
E-sports devices
Smart home appliance

GENERAL DESCRIPTION

AW21036QPY-Q1 is a 36-channel high precision constant current LED driver. Each channel has individual 8-bit DC current setting for color-mixing and 8-bit PWM current for brightness control. The maximum global current of each channel is recommended to be 50mA configured via register GCCR and external Resistor R_{EXT}.

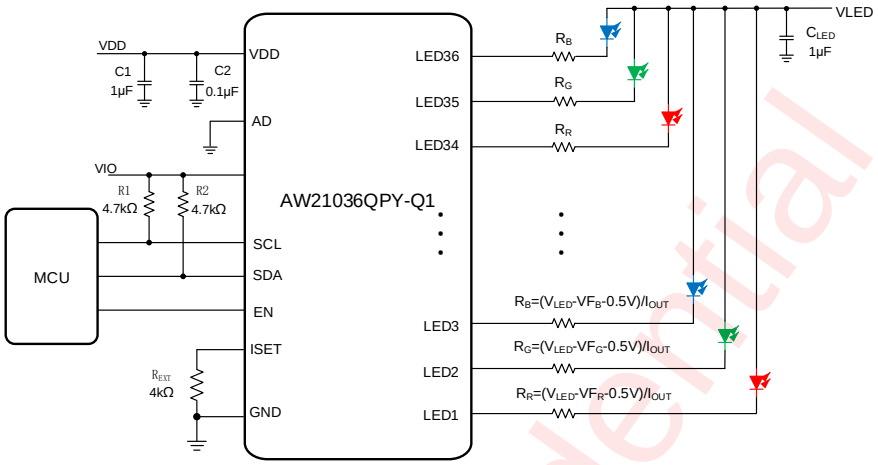
Group control mode, autonomous breathing pattern and rapid RGB control mode are provided for flexible, high efficiency lighting effect programming and fast display updating.

Programmable phase-shifting and spread spectrum technology are utilized to reduce EMI and audible noise caused by MLCC when LEDs turn on or off simultaneously.

AW21036QPY-Q1 can be turned off with minimum current consumption by either pulling the EN pin low or using the software reset feature.

AW21036QPY-Q1 is available in QFP 7mmX7mmX1.2mm-48L package. It operates from 2.7V to 5.5V over the temperature range of -40°C to +125°C.

TYPICAL APPLICATION CIRCUIT

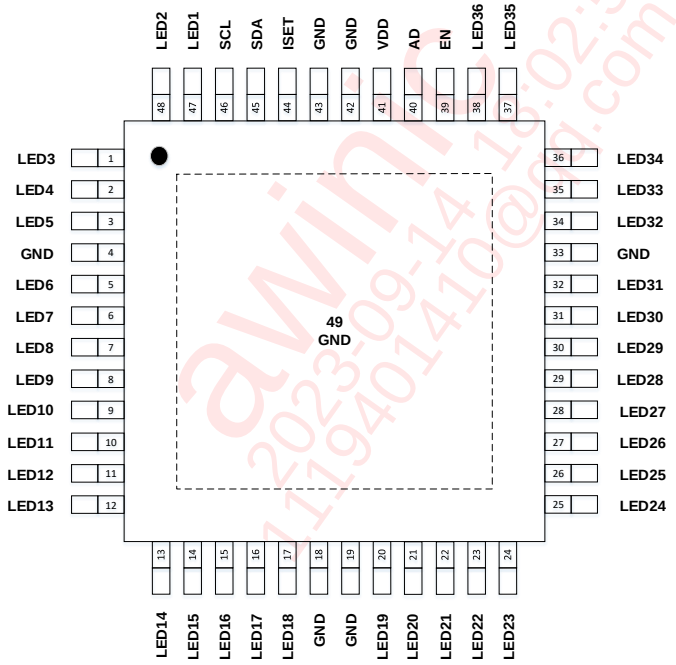


Note:The resistors(R_R,R_G,R_B) between LED and IC are only for thermal reduction

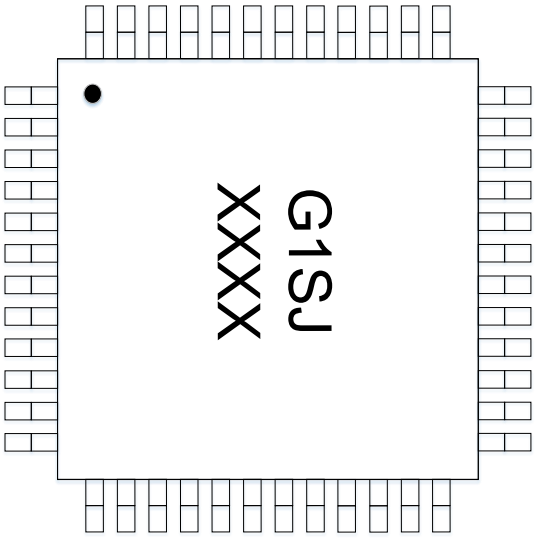
AW21036QPY-Q1 Application circuit

PIN CONFIGURATION AND TOP MARK

AW21036QPY-Q1 (Top View)



AW21036QPY-Q1 (Top View)

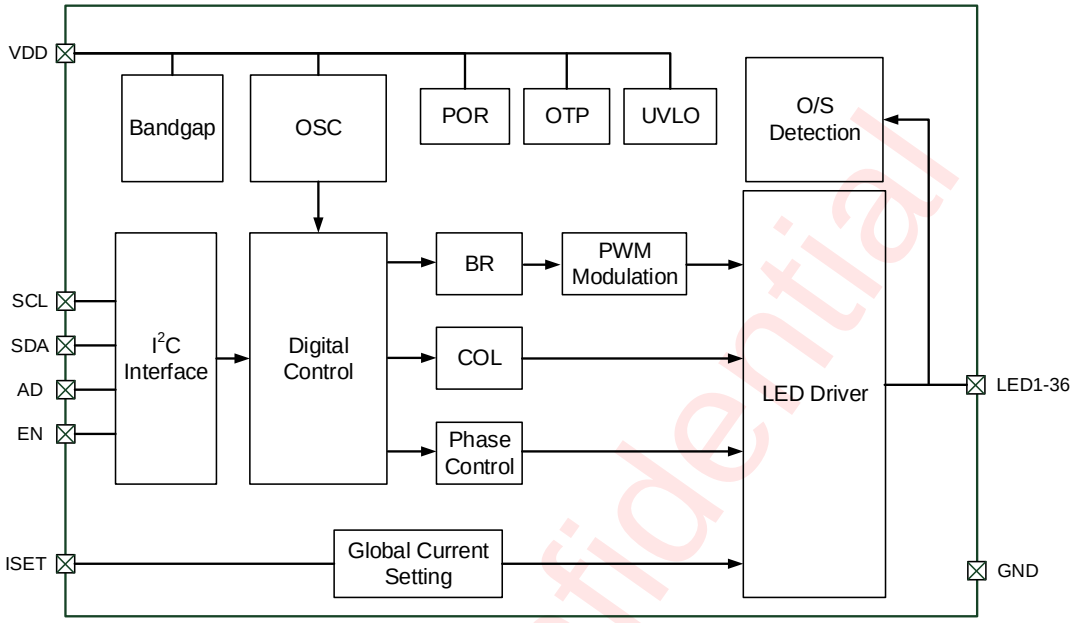


G1SJ – AW21036QPY-Q1
XXXX – Production Tracing Code

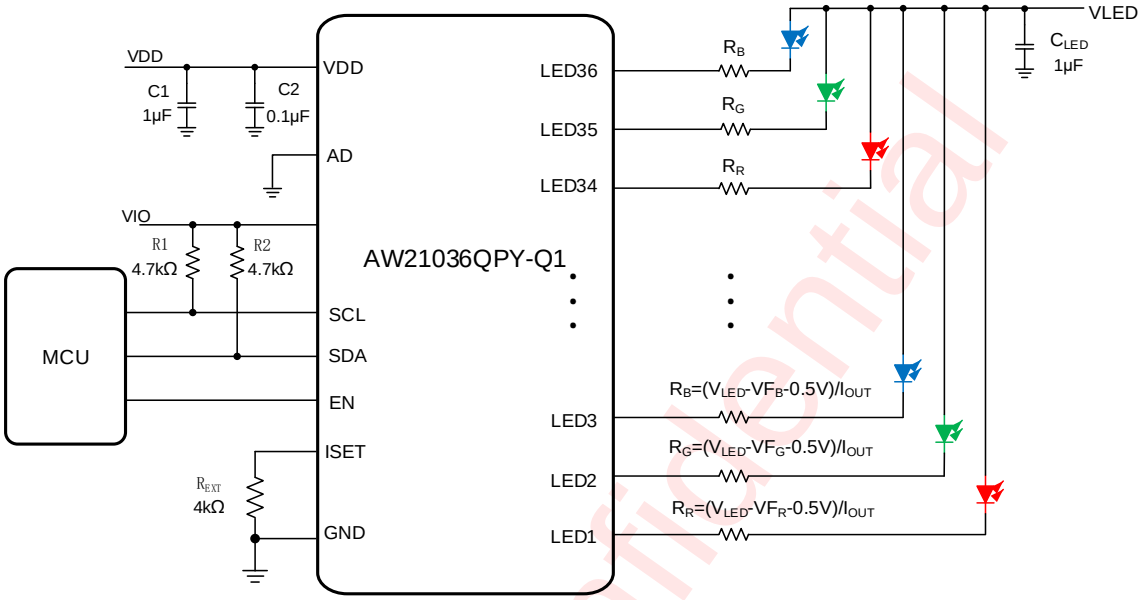
PIN DEFINITION

No.	NAME	DESCRIPTION
1~3	LED3~LED5	Constant current sink, connect to LED's cathode.
4	GND	Ground.
5~17	LED6~LED18	Constant current sink, connect to LED's cathode.
18,19	GND	Ground.
20~32	LED19~LED31	Constant current sink, connect to LED's cathode.
33	GND	Ground.
34~38	LED32~LED36	Constant current sink, connect to LED's cathode.
39	EN	Shutdown the chip when pulled low.
40	AD	I^2C address setting, connects to GND, VDD, SCL or SDA for different device address of I^2C. Internally pulled down to GND with a resistor of 1MΩ.
41	VDD	Power supply：2.7V~5.5V
42,43	GND	Ground.
44	ISET	When R_{EXT}=4.0kΩ, global current of LED is 20mA.
45	SDA	Serial data I/O for I^2C interface.
46	SCL	Serial clock input for I^2C interface.
47,48	LED1, LED2	Constant current sink, connect to LED's cathode.
49	GND	Ground.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL APPLICATION CIRCUITS



Note:The resistors(R_R,R_G,R_B) between LED and IC are only for thermal reduction

AW21036QPY-Q1 Application circuit

ORDERING INFORMATION

Part Number	Temperature	Package	Marking	Moisture Sensitivity Level	Environmental Information	Delivery Form
AW21036QPY-Q1	-40°C~125°C	QFP 7X7-48L	G1SJ	MSL3	ROHS+HF	2500 units/ 10Tray

ABSOLUTE MAXIMUM RATINGS(NOTE1)

PARAMETERS		RANGE
Supply voltage range V_{DD}		-0.3V to 6V
Input voltage range	SCL, SDA, EN, AD	-0.3V to 6V
Output voltage range	LED1~LED36	-0.3V to 6V
Junction-to-ambient thermal resistance θ_{JA}		32.69°C/W
Operating free-air temperature range		-40°C to 125°C
Maximum operating junction temperature T_{JMAX}		150°C
Storage temperature T_{STG}		-65°C to 150°C
Lead temperature (soldering 10 seconds)		260°C
ESD		
HBM (NOTE 2)		±2000V
CDM (NOTE 3)		±750V
Latch-Up		
Test condition: ***AEC-Q100-004-REC-D***		+IT：200mA -IT：-200mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method：AEC-Q100-002.

NOTE3: The charged device model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method：AEC-Q100-011.

ELECTRICAL CHARACTERISTICS

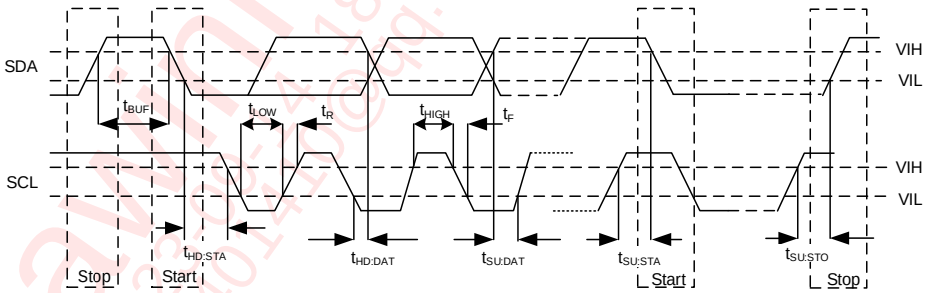
T_A=-40~125°C，V_{DD}=3.6V (unless otherwise noted) , R_{EXT}=4kΩ

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
Power supply voltage and current						
V_{DD}	Power supply voltage		2.7		5.5	V
I_{STB_VDD}	Standby current of V_{DD}	EN=GND		3	15	μA
	Power-save mode current consumption	V_{EN}=3.6V, GCR.APSE=1, All LEDs off >32ms		3	15	μA
I_{ACT_VDD}	Quiescent current in active mode	V_{EN}=V_{DD}, GCR.CHIPEN=1,		2	3	mA
		V_{EN}=V_{DD}, GCR.CHIPEN=1, GCCR.GCC=0xFF, COL_X=0xFF		9	11	mA
$I_{LEAKAGE}$	Output leakage current	V_{EN}=0V, $VLED_X$=5.5V		0.1	1	uA
I_{MAX}	Maximum global current of LED_X	GCCR.GCC=0xFF, BR_X=COL_X=0xFF	18.6	20	21.4	mA
I_{MATCH}	Output current match accuracy	GCCR.GCC=0xFF, BR_X=COL_X=0xFF	-6		6	%
$V_{DROPOUT}$	Dropout voltage when the LED current has dropped 5%	$ILED_X$=20mA		200	300	mV
F_{OSC}	OSC clock frequency		14.88	16	17.12	MHz
T_{SD}	Thermal shutdown threshold			150		°C
	Thermal shutdown hysteresis			20		°C
AD, EN						
V_{IL}	Input low level	AD,EN			0.4	V
V_{IH}	Input high level	AD,EN	1.2			V
R_{ADPD}	Internal pull down resistance	AD, VDD=3.6V		1M		Ω
R_{ENPD}	Internal pull down resistance	EN, VDD=3.6V		400k		Ω
I²C Interface						
V_{OL}	Output low level	SDA,I_{OL} = 10 mA			0.1	V

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IH}	Input high level	SCL, SDA	1.2			V
V_{IL}	Input low level	SCL, SDA			0.4	V

I2C INTERFACE TIMING

PARAMETER		MIN	TYP	MAX	UNIT
F_{SCL}	Interface Clock frequency	-		400	kHz
$T_{HD:STA}$	(Repeat-start) Start condition hold time	0.6		-	μs
T_{LOW}	Low level width of SCL	1.3		-	μs
T_{HIGH}	High level width of SCL	0.6		-	μs
$T_{SU:STA}$	(Repeat-start) Start condition setup time	0.6		-	μs
$T_{HD:DAT}$	Data hold time	0		-	μs
$T_{SU:DAT}$	Data setup time	0.1		-	μs
T_R	Rising time of SDA and SCL	-		0.3	μs
T_F	Falling time of SDA and SCL	-		0.3	μs
$T_{SU:STO}$	Stop condition setup time	0.6		-	μs
T_{BUF}	Time between start and stop condition	1.3		-	μs



I²C Interface Timing

DETAILED FUNCTIONAL DESCRIPTION

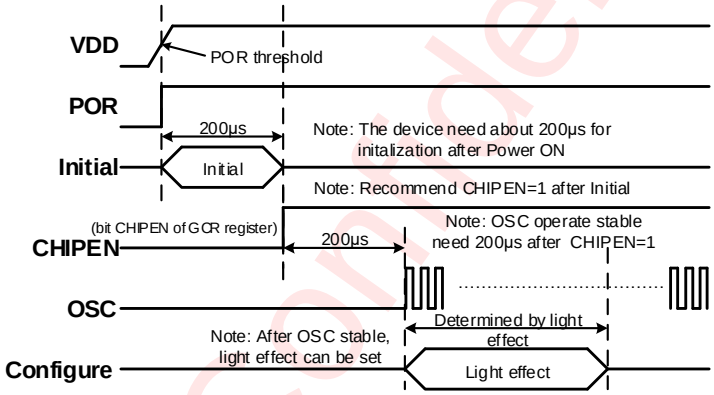
OPERATION MODE AND RESET

POWER ON RESET

Upon initial power-up, the AW21036QPY-Q1 is reset by internal power-on-reset, and all register are reset to default value, and LED driver is shut down.

Once the supply voltage VDD drops below the threshold voltage V_{POR_VDD} (2.0V), the power-on-reset will be activated to reset the device again. By reading the bit PORST of the register UVCR (address 79h), whether the device has been reset can be determined.

Below is the recommended operation timing:

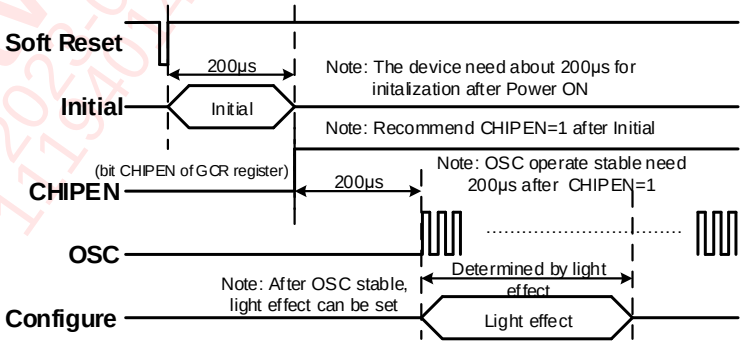


Power Up Timing

SOFTWARE RESET

By writing 00H to register RESET (address 7Fh), the software reset is triggered. After software reset, all registers will be reset to the default value and enter into standby mode.

After the software reset command is input through I^2C or power on reset, it needs to wait at least 2ms before any other I^2C command can be accepted.



Software Reset Timing

STANDBY MODE

The AW21036QPY-Q1 enters into standby mode automatically when EN is pulled low or the bit CHIPEN of the register GCR (address 00h) is set to "0" or UVLO is triggered(UVST=1) in active mode, meanwhile all registers will not be reset. In standby mode, all analog blocks are power down but I²C interface is accessible, and all registers can be configured.

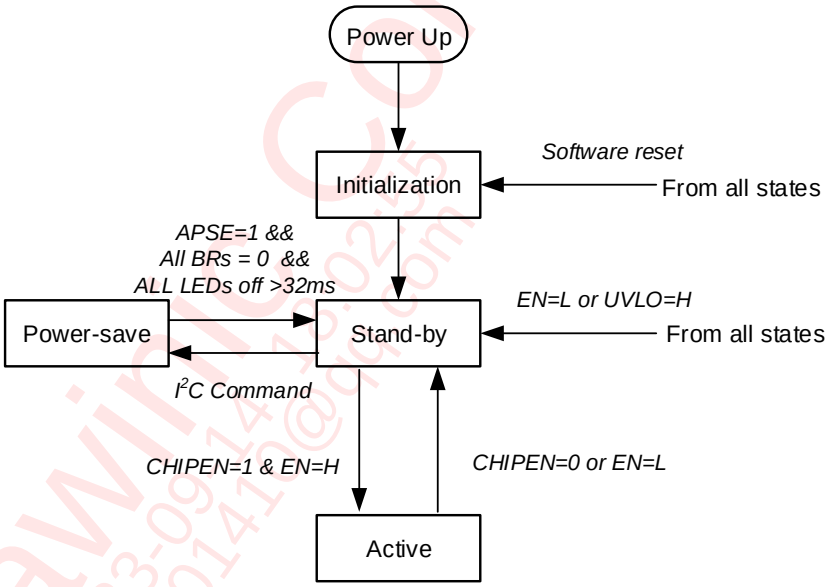
When POR is triggered, the device enters into standby mode and all registers will be reset (more information is showed in POWER ON RESET).

ACTIVE MODE

When EN is in high level, and the bit CHIPEN of the register GCR (address 00h) is set to "1", the AW21036QPY-Q1 enters into the active mode.

AUTO POWER-SAVE MODE

The bit APSE of the register GCR (address 00h) is set to "1", the auto power-save mode is enabled. When all LEDs are off and the value of all register BR0~BR35 are 0x00H for more than 32ms, AW21036QPY-Q1 automatically enters into standby mode for power saving. Once writing a non-zero value into any register among BR0~BR35, the device exits power-save mode immediately.



AW21036QPY-Q1 operating mode transition

I²C INTERFACE

The AW21036QPY-Q1 supports the I²C protocol. The maximum frequency supported by the I²C is 400kHz. The pull-up resistor for the SDA and SCL can be selected from 1k to 10kΩ. Usually, 4.7kΩ is recommended for 400kHz I²C. The voltage from 1.8V to 3.3V is allowed for the I²C interface. Additionally, the I²C device supports continuous read and write operations.

DEVICE ADDRESS

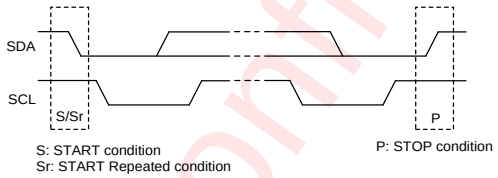
The I²C device address is 7-bit (A7~A1), followed by a R/W bit A0 (Read=1/Write=0). Set A0 to "0" for writing and "1" for reading. The values of bit A1 and bit A2 are depended on the connection of pin AD, there are 4 options: VDD, GND, SCL and SDA. The A7 to A3 is "01110" constantly. The device also supports using a broadcast slave address of 1Ch to access registers. All slave addresses as followed.

AD PIN	A7:A3	A2:A1	A0	Device Address	Broadcast Address
GND	01101	00	0/1	34h	1Ch
VDD		01		35h	
SCL		10		36h	
SDA		11		37h	

I²C START/STOP

I²C start: SDA changes from high level to low level when SCL is high level.

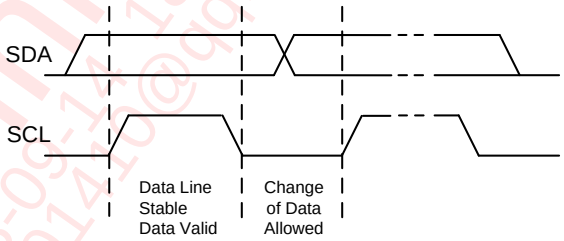
I²C stop: SDA changes from low level to high level when SCL is high level.



I²C Start/Stop Condition Timing

DATA VALIDATION

When SCL is high level, SDA level must be constant. SDA can be changed only when SCL is low level.

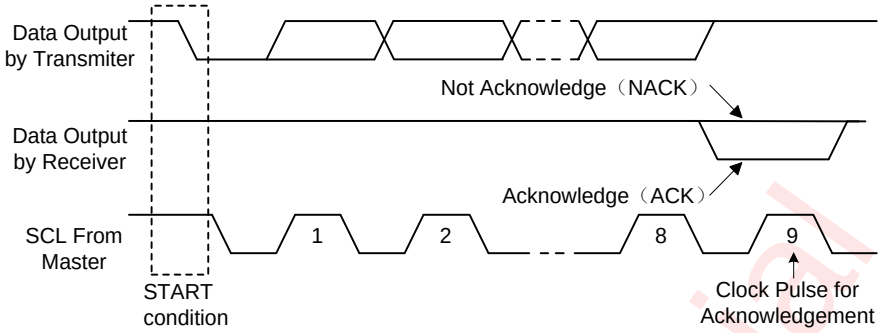


Data Validation Diagram

ACK (ACKNOWLEDGEMENT)

ACK means the successful transfer of I²C bus data. After master sends an 8-bit data, SDA must be released; SDA is pulled to GND by slave device when slave acknowledges.

When master reads, slave device sends 8-bit data, releases the SDA and waits for ACK from master. If ACK is send and I²C stop is not send by master, slave device sends the next data. If ACK is not send by master, slave device stops to send data and waits for I²C stop.



I²C ACK Timing

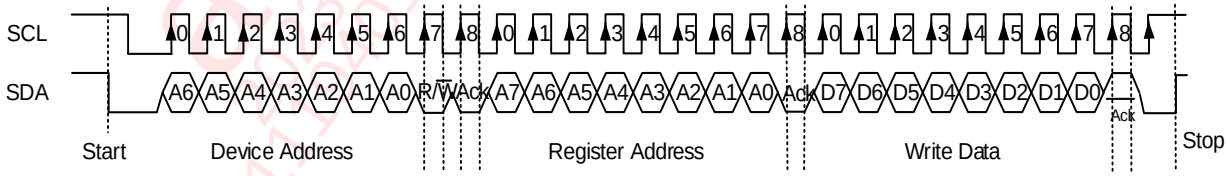
WRITE CYCLE

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol allows a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a start condition, a number of byte transfers (set by the software) and a stop condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow.

In a write process, the following steps should be followed:

a) Master device generates START condition. The "START" signal is generated by lowering the SDA signal while the SCL signal is high.
b) Master device sends slave address (7-bit) and the data direction bit R/W = 0).
c) Slave device sends acknowledge signal if the slave address is correct.
d) Master sends control register address (8-bit)
e) Slave sends acknowledge signal
f) Master sends data byte to be written to the addressed register
g) Slave sends acknowledge signal
h) If master will send further data bytes the control register address will be incremented by one after acknowledge signal (repeat step f and g)
i) Master generates STOP condition to indicate write cycle end

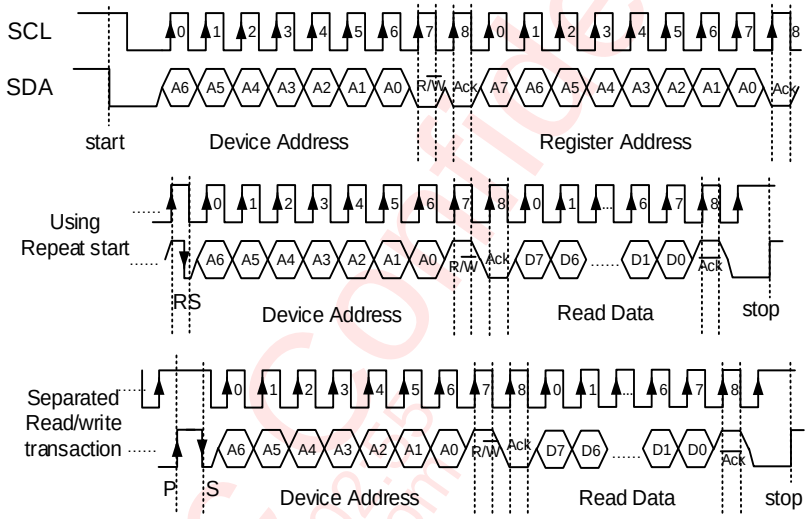


I²C Write Byte Cycle

READ CYCLE

In a read cycle, the following steps should be followed:

a) Master device generates START condition
b) Master device sends slave address (7-bit) and the data direction bit (R/W = 0).
c) Slave device sends acknowledge signal if the slave address is correct.
d) Master sends control register address (8-bit)
e) Slave sends acknowledge signal
f) Master generates STOP condition followed with START condition or REPEAT START condition
g) Master device sends slave address (7-bit) and the data direction bit (R/W = 1).
h) Slave device sends acknowledge signal if the slave address is correct.
i) Slave sends data byte from addressed register.
j) If the master device sends acknowledge signal, the slave device will increase the control register address by one, then send the next data from the new addressed register.
k) If the master device generates STOP condition, the read cycle is ended.



I²C Read Byte Cycle

UNDER VOLTAGE LOCK OUT (UVLO)

When bit UVDIS of the register UVCR (address 79h) is set to “0”, the device monitors the voltage of VDD. If the voltage drops below threshold (2.4V typically), the bit UVST of the register UVCR (address 79h) will be set to “1”. After read-out, the register UVCR will be clear.

If both bit UVDIS and bit UVPD of the register UVCR (address 79h) is set to “0”, UVLO protection function is enabled. Once the event of under voltage occurs, the bit CHIPEN of the register GCR (address 00h) will be cleared to “0”, and then the device will enter into standby mode. If the voltage of VDD rises above the UVLO threshold and then write “1” to bit CHIPEN, the device will enter into active mode again.

By default, control bits UVDIS, UVPD are all “0”. Both UVLO monitor and protection are enabled.

OVER TEMPERATURE PROTECTION (OTP)

When bit OTDIS of the register OTCR (address 77h) is set to “0”, the over-temperature detection is enabled. Once the temperature of this device reaches 150℃, the over-temperature condition is detected, and the bit OTST of the register OTCR (address 77h) will be set to “1”. The OTST will be cleared to “0” after reading the register OTCR.

If both bit OTDIS and bit OTPD of the register OTCR (address 77h) is set to “0”, the Over-Temperature Protection (OTP) function is enabled. Once the event of over-temperature occurs, the bit CHIPEN of the register GCR (address 00h) will be cleared to “0”, and then the device will enter into standby mode. When the temperature returns below 130°C, the device will enter into active mode again after writing “1” to bit CHIPEN.

By default, control bits OTDIS and OTPD are all “0”, both OT monitor and OT protection are enabled.

LED OPEN/SHORT DETECTION

AW21036QPY-Q1 supports LED open/short detection. When bit OSDE[1:0] of the register OSDCR(address 71h) is set to “11” , open detection is enabled, and the detection results can be read out via the registers OSST0~4 (72h~76h). Similarly, when set bit OSDE [1:0] of the register OSDCR (address 71h) to “10”, short detection is enabled, and the results also can be read out via the registers OSST0~4.

We recommend the bit PWMDIS [7:5] of the register SSCR (address 78h) being set to “111” and maintain about 1mA current of each LED when the open/short function is enabled.

CURRENT SETTING

The average output current of LED_n (n=1, 2, …, 36) can be expressed by the following formula,

$$I_{OUT(n)} = K \times \frac{V_{REXT}}{R_{EXT}} \times \frac{GCC}{255} \times \frac{WB}{255} \times \frac{COL_n}{255} \times \frac{BR_n}{256} \qquad n=1, 2, 3, \ldots, 36$$

Where V_{REXT}=0.4V, K=200, R_{EXT} is the value of external resistor, GCC is the 8bit global current configured by the register GCCR (address 6Eh), WB is 8bit white balance parameter configured by the register WBR/WBG/WBB (address 90h/91h/92h), COLn is 8bit individual constant current parameter, and BRn is 8bit individual PWM modulated current parameter.

The maximum output current is decided by the R_{EXT} and the GCC when WB=255, COLn=255, BRn=256. For example: R_{EXT} = 2kΩ, GCC=0xFF, I_{OUT}= I_{MAX}=40mA.

AW21036QPY-Q1 supports white balance calibration function via 3 registers consisting of register WBR, WBG, and WBB. Therein, WBR is used for LED_X (X=1, 4, 7, …, 34), WBG is used for LED_Y (Y=2, 5, 8, …, 35), WBB is used for LED_Z (Z=3, 6, 9, …, 36). The default value of registers WBR/WBG/WBB is 0xff.

Each LED current of AW21036QPY-Q1 features 8bit DC current and 8bit PWM modulated current that are decided by COL source and BR source respectively. The BR and COL sources are as follows.

Mode	General Mode			Breathing Pattern Controller (BPC)			Group Control Mode		
Parameter Source	GEn=0			GEn=1 and PATEN=1			GEn=1 and PATEN=0		
	BR Source		COL Source	BR Source	COL Source		BR Source	COL Source	
LED NO.	RGBMD=0	RGBMD=1			GCOLDIS=0	GCOLDIS=1		GCOLDIS=0	GCOLDIS=1
#1	BR0	BR0	COL0	BPC	GCOLR	COL0	FADEL	GCOLR	COL0
#2	BR1	BR0	COL1		GCOLG	COL1		GCOLG	COL1
#3	BR2	BR0	COL2		GCOLB	COL2		GCOLB	COL2
#4	BR3	BR1	COL3		GCOLR	COL3		GCOLR	COL3
#5	BR4	BR1	COL4		GCOLG	COL4		GCOLG	COL4

#6	BR5	BR1	COL5		GCOLB	COL5		GCOLB	COL5
…	…	…	…		…	…		…	…
#34	BR33	BR11	COL33		GCOLR	COL33		GCOLR	COL33
#35	BR34	BR11	COL34		GCOLG	COL34		GCOLG	COL34
#36	BR35	BR11	COL35		GCOLB	COL35		GCOLB	COL35

Notes:

GEn (n=0~11) refers to BPC/Group-Control-Mode control bit in register GCFG0~1 (address ABh~ACh). PATEN is BPC control bit in register PATCFG (address A0h), GCOLDIS is group color disable bit in register GCFG1(address ACh), GCOLR/GCOLG/GCOLB is for group color control decided by register GCOLR/GCOLG/GCOLB (address A8h~A9h). More details will be introduced later.

PWM MODLULATION

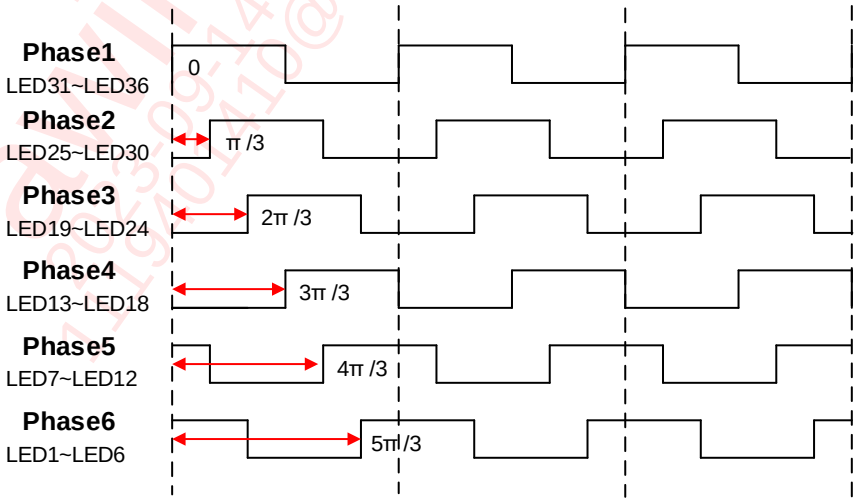
PWM FREQUENCY

The PWM frequency is decided by bits CLKFRQ [2:0] in register GCR (address 00h). Following table shows the relationship of PWM frequency and the CLKFRQ [2:0]. To avoid the MLCC audible noise, it's recommended to use the PWM frequency lower than 500 Hz or higher than 20 kHz.

CLKFRQ[2:0]	000	001	010	011	100	101	110	111
PWM Freq. [Hz]	62k	32k	4k	2k	1k	500	244	122

PWM PHASE CONTROL

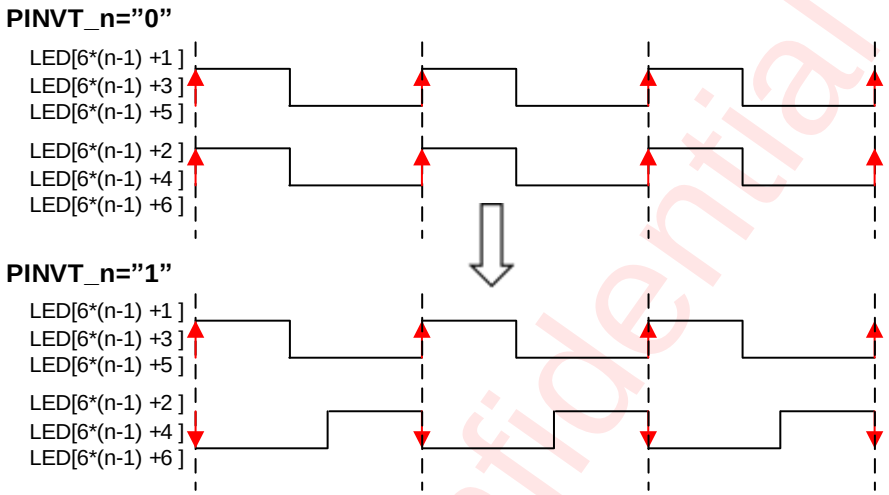
To reduce the peak load current and ceramic-capacitor audible ringing, AW21036QPY-Q1 supports 6 PWM phase shifting (Phase1~Phase6) and phase-inverting scheme. When setting PDE in register PHCR (address 70h) to "1", the phase shifting scheme is enabled, and each adjacent phase differs by 60 degrees，which meaning only 6 of 36 LEDs could switch on in the same time.



Phase shift scheme

When setting PIEn in register PHCR (address 70h, n=1~6) to "1", the PWM phase of the even-numbered

channels is inverted. As shown below, if setting PIEn to “1”, the even-numbered channels (i.e. 6x(n-1)+2, 6x(n-1)+4, 6(n-1)+6) are switched off when the odd-numbered channels (i.e. 6x(n-1)+1, 6x(n-1)+3, 6(n-1)+5) are switched on, which is good for reducing the input-current ripple. For an example, when setting PIE0 to “1”, the channels of LED2, LED4 and LED6 are switched off when the channels of LED1, LED3 and LED5 are switched on.



Phase invert scheme

PWM DISABLE

If the bits PWMDIS [2:0] in register SSCR (address 78h) is set to “111”, the PWM output is disabled, and the duty of each PWM is forced to 100%. In this mode, the BR parameter is not valid, but the COL parameter is still effective. And the PWM outputs of LED1~12, LED13~24 and LED25~36 enabled or not are decided by the bit 0~2 of PWMDIS respectively.

It should be noted that when performing open-short detection, the bits PWMDIS [2:0] need to be set to “111”.

SPREAD SPECTRUM

PWM is a troublesome for some application which is concerned about EMI. AW21036QPY-Q1 has spread spectrum function to optimize the EMI performance. If bit SSE in register SSCR (address 78h) is set to “1”, spread spectrum function is enabled. By setting the bit SSR in register SSCR, four spread spectrum range 5%/15%/25%/35% can be selected. The total electromagnetic emitting energy can spread into a wider range of frequency band that significantly degrades the peak energy of EMI.

RGB CONFIGURE MODE

In RGB applications, every 3 LEDs in RGB share a same BR parameter. To achieve fast register configuration for RGB applications, AW21036QPY-Q1 provides an RGB configuration mode by setting the bit RGBMD in register GCR2 (address 7Ah).

If RGBMD=1, register BR0~BR11 configure brightness parameters for corresponding 12 RGB groups. In other words, in RGB mode, only registers BR1~BR12 need to be configured, and the registers BR13~BR36 not valid any more.

If RGBMD=0, register BR0~BR35 configure brightness parameters for corresponding 36 LEDs independently,

more details as follows.

LED No.	BR parameter source	
	RGBMD=0	RGBMD=1
#1	BR0	BR0
#2	BR1	
#3	BR2	
#4	BR3	BR1
#5	BR4	
#6	BR5	
…	…	…
#34	BR33	BR11
#35	BR34	
#36	BR35	

GROUP CONTROL MODE

AW21036QPY-Q1 supports group control mode, in this mode, all selected LEDs are controlled by the group control registers (GCOLR, GCOLG, GCOLB). The register GCFG0~1 select which LEDs are controlled by group control register. There are total 12 control bit (GEx), each bit set adjacent 3 LED are included in or not. User can configure group control register to setting common brightness and color for all selected LED, so as to simplify lighting effect programming and speed up display refreshing via I²C interface.

If bit COLDIS in register GCFG1 (ACh) is "1", the color parameters of the grouped LED are no longer configured by register GCOLR/G/B but by individual register (COL0~COL35).

The detailed configurations are as follows.

RGB	LED	GE	Brightness		Color	
			GE=0	GE=1	GE=0 or COLDIS=1	GE=1 and COLDIS=0
1	1	GCFG0[0]	BR0	FADEL	COL0	GCOLR
	2		BR1	FADEL	COL1	GCOLG
	3		BR2	FADEL	COL2	GCOLB
2	4	GCFG0[1]	BR3	FADEL	COL3	GCOLR
	5		BR4	FADEL	COL4	GCOLG
	6		BR5	FADEL	COL5	GCOLB
…	…	…	…	…	…	…
8	22	GCFG0[7]	BR21	FADEL	COL21	GCOLR
	23		BR22	FADEL	COL22	GCOLG
	24		BR23	FADEL	COL23	GCOLB
9	25	GCFG1[0]	BR24	FADEL	COL24	GCOLR

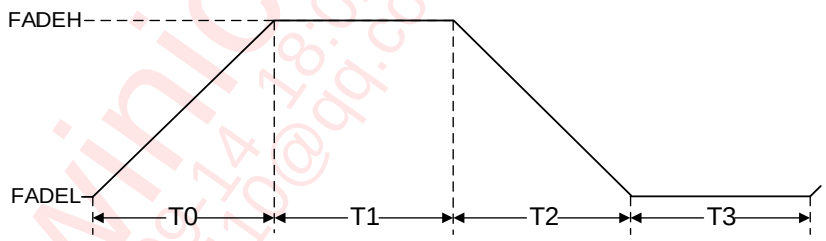
	26		BR25	FADEL	COL25	GCOLG
	27		BR26	FADEL	COL26	GCOLB
…	…	…	…	…	…	…
12	34	GCFG1[3]	BR33	FADEL	COL33	GCOLR
	35		BR34	FADEL	COL34	GCOLG
	36		BR35	FADEL	COL35	GCOLB

PATTERN CONTROLLERS

There is a breathing pattern controller (BPC) in the device. When bit PATEN in register PATCGF (address A0h) is set to “1”, breathing pattern controller is enabled. Pattern controller can be configured as autonomous breathing mode or manual-controlled mode. Each RGB consisting of every three adjacent LEDs can be configured as pattern controlled mode or normal mode by register GCFG0~1. For example, when setting GCFG0 = 0x01, GCFG1 = 0x00, the RGB1 which consists of LED1~LED3 will work in BPC mode and other LED will work in normal mode.

AUTONOMOUS BREATHING MODE

When bit PATMD in register PATCFG is set to “1”, the pattern controller works in autonomous breathing mode. In this mode, the pattern controller will generate a breathing lighting effect, which is configured by the user-defined timing parameter. The waveform of the breathing lighting effect is shown in the following figure. The parameter T0~T3 define 4 key periods in a complete breathing cycle. T0~T3 composite a breathing loop, denoting the rise-time, on-time, fall-time and off- time respectively. Register FADEH (A6h) and FADEL (A7h) control the max and min brightness of the breathing respectively.



LED breath timing in pattern mode

The start point and end point of autonomous breathing loop are configurable. The loop starting point could be selected among T0~T3, which is set by bits LB [1:0] in register PATT2 (address A4h). The end point of the loop can only be selected between the end of T0 and the end of T2, which is determined by bits LE [1:0] in register PATT2. The repeat times is determined by the end point defined. If bits LE [1:0] is not “00”, the end point of breathing loop is the end of T0, and the loop counter increment by 1 at the end of T0. If bit LE [1:0] is “00”, the loop end point is the end of T2, and the loop counter increment by 1 at the end of T2.

The repeat times is decided by bit RPT [11:8] of register PATT2 (address A4h) and RPT [7:0] of register PATT3 (address A5h). When setting RPT [11:0] to “0”, the breathing pattern will run unlimited times.

After the breathing pattern is over, the status bit ENDFLAG in register PATGO (address A2h) will be set to “1”, and ENDFLAG will be cleared to “1” after reading out through I²C bus. Once breathing loop start again or pattern controller switches to manual mode by setting PATMD bit to “0”, the ENDFLAG will also be cleared.

When bit RUN in register PATGO is set to “1”, breathing pattern is started. The full process of the autonomous breathing is as follows:

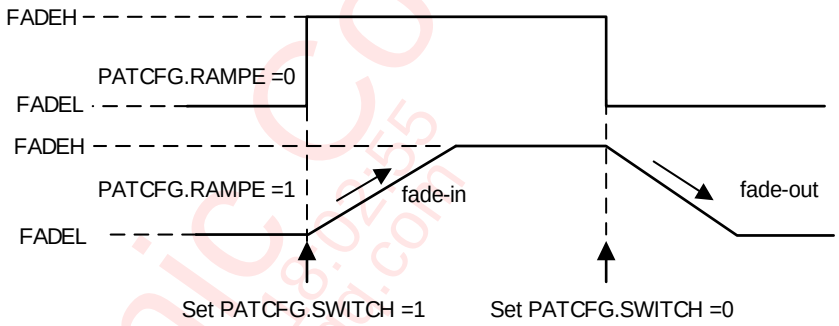
a) Set GCOLR/G/B, FADEH/L parameter.
b) Set GCFG0 and GCFG1 to select the LED in breathing pattern mode or not.
c) Configure PATT0, PATT1, PATT2, and PATT3 for parameters T0~T3, start/stop point, and repeat times.
d) Set PATEN=1 to enable breathing pattern mode.
e) Set PATMD=1 and RAMPE=1 to select auto breathing mode and enable breathing ramp.
f) Set RUN=1 to start the breath pattern.

MANUAL CONTROL MODE

If bit PATMD is set to “0”, manual control mode is selected. In manual control mode, user could program the bit SWITCH of register PATCFG to control the output of pattern controller. When bit SWITCH is “1”, the output of pattern controller is decided by register FADEH. When bit SWITCH is set as “0”, the output is the decided by register FADEL.

If bit RAMPEN in register PATCFG is set to “1”, the smooth ramp up/down will be enabled. At the same time, if SWITCH changes from “0” to “1”, the output will be ramp up to FADEH smoothly. Similarly, if SWITCH changes from “1” to “0”, the output of the pattern controller will ramp down to FADEL smoothly.

However, if the RAMPEN is set to “0”, the output of the pattern controller will change to FADEH or FADEL directly with no ramp as the SWITCH changes.



Manual Control Mode

REGISTER CONFIGURATION

REGISTER LIST

ADDR	NAME	W/R	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
00H	**GCR**	**W/R**	APSE	CLKFRQ			-			CHIPEN	00H
01H ~ 24H	**BR0 ~ BR35**	**W/R**	BR0~BR35								00H
49H	**UPDATE**	**W/R**	UPDATE								00H
4AH ~ 6DH	**COL0 ~ COL35**	**W/R**	COL0~COL35								00H
6EH	**GCCR**	**W/R**	GCC								00H
70H	**PHCR**	**W/R**	PDE	-	PIE						00H
71H	**OSDCR**	**W/R**	-				OTH	STH	OSDE		00H
72H	**OSST0**	**R**	OSST [7:0]								00H
73H	**OSST1**	**R**	OSST [15:8]								00H
74H	**OSST2**	**R**	OSST [23:16]								00H
75H	**OSST3**	**R**	OSST [31:24]								00H
76H	**OSST4**	**R**	-				OSST [35:32]				00H
77H	**OTCR**	**W/R**	TROF		TRST	OTST	OTPD	OTDIS	TRTH		00H
78H	**SSCR**	**W/R**	PWMDIS			SSE	SSR		CLT		00H
79H	**UVCR**	**W/R**	REXT_ST		UVST	PORST	OCPTH	OCPD	UVPD	UVDIS	00H
7AH	**GCR2**	**W/R**	-							RGBMD	00H
7CH	**GCR4**	**-**	-	-	-	-	-	SRR	SRF		00H
7EH	**VER**	**R**	VERSION								A8H
7FH	**RESET**	**W/R**	RESET/ID								18H
90H	**WBR**	**W/R**	*WBR*								FFH
91H	**WBG**	**W/R**	*WBG*								FFH
92H	**WBB**	**W/R**	*WBB*								FFH
A0H	**PATCFG**	**W/R**	-			-	*SWITCH*	*RAMPE*	*PATMD*	*PATEN*	00H
A1H	**PATGO**	**W/R**	-					*ENDF LAG*	PATST	*RUN*	00H
A2H	**PATT0**	**W/R**	*T0*				*T1*				00H
A3H	**PATT1**	**W/R**	*T2*				*T3*				00H
A4H	**PATT2**	**W/R**	*LE*		*LB*		*RPT[11:8]*				00H
A5H	**PATT3**	**W/R**	*RPT[7:0]*								00H
A6H	**FADEH**	**W/R**	*FADEH*								00H
A7H	**FADEL**	**W/R**	*FADEL*								00H
A8H	**GCOLR**	**W/R**	GCOLR								00H
A9H	**GCOLG**	**W/R**	GCOLG								00H
AAH	**GCOLB**	**W/R**	GCOLB								00H

ADDR	NAME	W/R	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
ABH	**GCFG0**	**W/R**	GE7	GE6	GE5	GE4	GE3	GE2	GE1	GE0	00H
ACH	**GCFG1**	**W/R**	-	-	-	GCOL DIS	GE11	GE10	GE9	GE8	00H

REGISTER DETAILED DESCRIPTION

GCR：Global Control Register(Address 00H)

Bit	Symbol	R/W	Description	Default
7	APSE	RW	Auto power-saving mode enable 0: disable 1: enable	0
6:4	CLKFRQ	RW	OSC frequency selection 000: 16MHz 001: 8MHz 010: 1MHz 011: 512kHz 100: 256kHz 101: 125kHz 110: 62.5kHz 111: 31.25kHz	000
3:1	RESERVED	R	Reserved	0
0	CHIPEN	RW	Chip enable 0: disable (default) 1: enable	0

BR：BR Register(Address 01H~24H)

Bit	Symbol	R/W	Description	Default
7:0	BR	RW	Individual 8bit BR parameter for LED1~36 After configuring the BR registers, should write 0x00 to register UPDATE to update the data.	0x00

UPDATE： Update Register(Address 49H)

Bit	Symbol	R/W	Description	Default
7:0	UPDATE	W	Write 0x00 to update BR register.	0x00

COL0~COL35：COL Register(Address 4AH~6DH)

Bit	Symbol	R/W	Description	Default
7:0	COL	RW	Individual 8bit COL parameter for LED1~36.	0x00

GCCR：Global Control Register(Address 6EH)

Bit	Symbol	R/W	Description	Default
7:0	GCC	RW	Global current control.	0x00

PHCR：Phase Control Register(Address 70H)

Bit	Symbol	R/W	Description	Default
7	PDE	RW	PWM phase delay enable 0: disable 1: enable	0
6	RESERVED	R	Reserved	0
5	PIE5	RW	PWM phase invert for LED32, LED34 and LED36 0: Phase invert disabled 1: Phase invert enabled	0
4	PIE4	RW	PWM phase invert for LED26, LED28 and LED30 0: Phase invert disabled 1: Phase invert enabled	0
3	PIE3	RW	PWM phase invert for LED20, LED22 and LED24 0: Phase invert disabled 1: Phase invert enabled	0
2	PIE2	RW	PWM phase invert for LED14, LED16 and LED18 0: Phase invert disabled 1: Phase invert enabled	0
1	PIE1	RW	PWM phase invert for LED8, LED10 and LED12 0: Phase invert disabled 1: Phase invert enabled	0
0	PIE0	RW	PWM phase invert for LED2, LED4 and LED6 0: Phase invert disabled 1: Phase invert enabled	0

OSDCR：Open Short Detect Control Register(Address 71H)

Bit	Symbol	R/W	Description	Default
7:4	RESERVED	R	Reserved	0000
3	OTH	RW	Open threshold 0: 0.1V 1: 0.2V	0
2	STH	RW	Short threshold 0: VDD-1V 1: VDD-0.5V	0
1:0	OSDE	RW	Open short detect enable 0x: detect disable 10: short detect enable 11: open detect enable	00

OSST0~3：Open/Short Status Register (Address 72H~75H)

Bit	Symbol	R/W	Description	Default
7:0	OSST	R	Open/short status of LED1~LED32 0: no open/short event detected 1: open/short event detected	0x00

OSST4：Open/Short Status Register (Address 76H)

Bit	Symbol	R/W	Description	Default
7:4	RESERVED	R	Reserved	0000
3:0	OSST	R	Open/short status of LED33~LED36 0: no open/short detected 1: open/short detected	0000

OTCR：Over Temperature Control Register (Address 77H)

Bit	Symbol	R/W	Description	Default
7:6	TROF	RW	Thermal roll off percentage of I_{OUT} 00: 100% 01: 75% 10: 55% 11: 30%	00
5	TRST	R	Thermal roll off status 0: none roll off	0

			1: roll off	
4	OTST	R	Over-temperature status 0: none over-temperature 1: over-temperature	0
3	OTPD	RW	Over-temperature(OT) protect disable 0: OT protect enable, when OT event occurs, device will clear GCR.CHIPEN to 0. 1: OT protect disable	0
2	OTDIS	RW	Over-temperature detect disable 0: OT detect enable, when OT event occurs, OTCR.OTST will be set. 1: OT detect disable	0
1:0	TRTH	RW	Thermal roll off threshold 00: 140°C 01: 120°C 10: 100°C 11: 90°C	00

SSCR：Spread Spectrum Control Register (Address 78H)

Bit	Symbol	R/W	Description	Default
7	PWMDIS2	RW	0: PWM duty of LED 25~36 determined by BR24~BR35 1: PWM duty of LED 25~36 fixed as 100%	0
6	PWMDIS1	RW	0: PWM duty of LED 13~24 determined by BR12~BR23 1: PWM duty of LED 13~24 fixed as 100%	0
5	PWMDIS0	RW	0: PWM duty of LED 1~12 determined by BR0~BR11 1: PWM duty of LED 1~12 fixed as 100%	0
4	SSE	RW	Spread spectrum enable 0: Disable 1: Enable	0
3:2	SSR	RW	Spread spectrum range 00: ±5% 01: ±15% 10: ±25% 11: ±35%	00
1:0	CLT	RW	Spread spectrum cycle time 00: 1980μs (default) 01: 1200μs 10: 820μs 11: 660μs	00

UVCR：UVLO Control Register (Address 79H)

Bit	Symbol	R/W	Description	Default
7:6	REXT_ST	R	R_{EXT} status 00: Normal 10: R_{EXT} is open 01: R_{EXT} is short or OCP 11: Not defined	00
5	UVST	R	UVLO status 0: No UVLO detected 1: UVLO detected	0
4	PORST	R	Power-on reset status 0: no power-on reset 1: power-on reset (cleared after read out)	0
3	OCPTH	RW	OCP Threshold 0: 85mA 1: 55mA	0
2	OCPD	RW	OCP disable 0: enable OCP 1: disable OCP	0
1	UVPD	RW	UVLO protect disable 0: UVLO protect enable, when under-voltage event occurs, device will clear GCR.CHIPEN to 0. 1: UVLO protect disable	0
0	UVDIS	RW	UVLO detect disable 0: UVLO detect enable, when under-voltage event occurs, UVCR.UVST will be set. 1: UVLO detect disable	0

GCR2：Global Control Register 2(Address 7AH)

Bit	Symbol	R/W	Description	Default
7:1	RESERVED	R	Reserved	0000 000
0	RGBMD	RW	RGB configure mode enable 0: disable 1: enable, every 3 LEDs share a common brightness.	0

GCR4：Global Control Register 4(Address 7CH)

Bit	Symbol	R/W	Description	Default

7:3	RESERVED	R	Reserved	0000 0
2	SRR	RW	Slew rate control for LED output rising time 0: 1ns 1: 6ns	0
1:0	SRF	RW	Slew rate control for LED output falling time 00: 1ns 01: 3ns 10: 6ns 11:10ns	00

VER：Version Register (Address 7Eh)

Bit	Symbol	R/W	Description	Default
7:0	VER	R	Chip version	0xA8

RESET： Software Reset Register (Address 7FH)

Bit	Symbol	R/W	Description	Default
7:0	RESET	RW	Write 00H to the register will reset all registers to their default value. The chip ID 0x18 will be read out from the register.	0x18

WBR： Red Scaling for White Balance(Address 90H)

Bit	Symbol	R/W	Description	Default
7:0	WBR	RW	Red Scaling for White Balance.	0xFF

WBG： Green Scaling for White Balance(Address 91H)

Bit	Symbol	R/W	Description	Default
7:0	WBG	RW	Green Scaling for White Balance.	0xFF

WBB： Blue Scaling for White Balance(Address 92H)

Bit	Symbol	R/W	Description	Default
7:0	WBB	RW	Blue Scaling for White Balance.	0xFF

PATCFG： Pattern Configure Register(Address A0H)

Bit	Symbol	R/W	Description	Default
7:4	RESERVED	R	Reserved	0000
3	SWITCH	RW	Switch on or off at manual mode. 0: LED off 1: LED on	0
2	RAMPE	RW	Ramp enable 0: ramp disable 1: ramp enable	0
1	MODE	RW	Breath pattern control mode selection 0: manual mode (default) 1: auto breath pattern mode	0
0	PATEN	RW	Auto breath pattern controller enable 0: disable 1: enable	0

PATGO： Pattern Configure Register(Address A1H)

Bit	Symbol	R/W	Description	Default
7:3	RESERVED	R	Reserved	0000 0
2	ENDFLG	R	Auto breath pattern loop end flag 0: loop is not over 1: loop is over (will be cleared after reading out)	0
1	STATE	R	Auto breath pattern status 0: pattern is stop 1: pattern is running	0
0	RUN	RW	Auto breath pattern run control Write “1” to run auto breath pattern Note: You shall write “0” and then write “1” to this bit to restart a new auto breath pattern.	0

PATT0： Pattern Timer0(Address A2H)

Bit	Symbol	R/W	Description	Default
7:4	RISE	RW	Ramp rise time	0000

			T0	Time	T0	Time	
			0000	0s	1000	2.1s	
			0001	0.13s	1001	2.6s	
			0010	0.26s	1010	3.1s	
			0011	0.38s	1011	4.2s	
			0100	0.51s	1100	5.2s	
			0101	0.77s	1101	6.2s	
			0110	1.04s	1110	7.3s	
			0111	1.6s	1111	8.3s	
3:0	ON	RW	Hold on time T1	Time	T1	Time	0000
			0000	0.04s	1000	2.1s	
			0001	0.13s	1001	2.6s	
			0010	0.26s	1010	3.1s	
			0011	0.38s	1011	4.2s	
			0100	0.51s	1100	5.2s	
			0101	0.77s	1101	6.2s	
			0110	1.04s	1110	7.3s	
			0111	1.6s	1111	8.3s	

PATT1： Pattern Timer1(Address A3H)

Bit	Symbol	R/W	Description				Default
7:4	FALL	RW	Ramp fall time T2	Time	T2	Time	0000
			0000	0s	1000	2.1s	
			0001	0.13s	1001	2.6s	
			0010	0.26s	1010	3.1s	
			0011	0.38s	1011	4.2s	
			0100	0.51s	1100	5.2s	
			0101	0.77s	1101	6.2s	
			0110	1.04s	1110	7.3s	
			0111	1.6s	1111	8.3s	
3:0	OFF	RW	Hold off time T3	Time	T3	Time	0000
			0000	0.04s	1000	2.1s	
			0001	0.13s	1001	2.6s	
			0010	0.26s	1010	3.1s	
			0011	0.38s	1011	4.2s	

			0100	0.51s	1100	5.2s	
			0101	0.77s	1101	6.2s	
			0110	1.04s	1110	7.3s	
			0111	1.6s	1111	8.3s	

PATT2： Pattern Control Register 1(Address A4H)

Bit	Symbol	R/W	Description	Default
7:6	LE	RW	End point of the auto-breath pattern 00: pattern finally stop at OFF state Other: pattern finally stop at ON state	00
5:4	LB	RW	Start point of the auto-breath loop pattern 00: pattern start from RISE state 01: pattern start from ON state 10: pattern start from FALL state 11: pattern start from OFF state	00
3:0	RPT[11:8]	RW	4 MSB of loop times.	0000

PATT3： Pattern Control Register 2 (Address A5H)

Bit	Symbol	R/W	Description	Default
7:0	RPT[7:0]	RW	8 LSB of auto-breath pattern repeat times Note: when RPT[11:0]=0, the pattern will run forever. In this case, you can switch auto-breath mode to manual mode and then turn the pattern off.	0x00

FADEH： Maximum Brightness for Auto Breath (Address A6H)

Bit	Symbol	R/W	Description	Default
7:0	FADEH	RW	Maximum brightness configure for auto breath.	0x00

FADEL： Minimum Brightness for Auto Breath(Address A7H)

Bit	Symbol	R/W	Description	Default
7:0	FADEL	RW	Minimum brightness configure for auto breath.	0x00

GCOLR： Red Mixing for Group Color (Address A8H)

Bit	Symbol	R/W	Description	Default
7:0	GCOLR	RW	Red mixing for group color.	0x00

GCOLG： Green Mixing for Group Color(Address A9H)

Bit	Symbol	R/W	Description	Default
7:0	GCOLG	RW	Green mixing for group color.	0x00

GCOLB： Blue Mixing for Group Color(Address AAH)

Bit	Symbol	R/W	Description	Default
7:0	GCOLB	RW	Blue mixing for group color.	0x00

GCFG0： Group Configure Register0 (Address ABH)

Bit	Symbol	R/W	Description	Default
7:0	GE[7:0]	RW	Group-Control-Mode/Pattern-Control-Mode enable for LED1~LED24 If bit PATEN in register PATCFG is set to “0”, GE[0]=1: LED1~3 work in group mode GE[1]=1: LED4~6 work in group mode GE[2]=1: LED7~9 work in group mode GE[3]=1: LED10~12 work in group mode GE[4]=1: LED13~15 work in group mode GE[5]=1: LED16~18 work in group mode GE[6]=1: LED19~21 work in group mode GE[7]=1: LED22~24 work in group mode If bit PATEN in register PATCFG is set to “1”, GE[0]=1: LED1~3 work in auto breath pattern mode GE[1]=1: LED4~6 work in auto breath pattern mode GE[2]=1: LED7~9 work in auto breath pattern mode GE[3]=1: LED10~12 work in auto breath pattern mode GE[4]=1: LED13~15 work in auto breath pattern mode GE[5]=1: LED16~18 work in auto breath pattern mode GE[6]=1: LED19~21 work in auto breath pattern mode GE[7]=1: LED22~24 work in auto breath pattern mode	0x00

GCFG1： Group Configure Register1 (Address ACH)

Bit	Symbol	R/W	Description	Default
7:5	RESERVED	R	Reserved	000
4	GCOLDIS	RW	Group/pattern color disable 0: Group/pattern color enable, all LEDs in group/pattern mode share the common COL parameters decided by GCOL_R/G/B. 1: Group/pattern color disable, all LEDs' color parameter in group/pattern mode is configured by their respective register COL.	0
3:0	GE[11:8]	RW	Group-Control-Mode/Pattern-Control-Mode enable for LED25~LED36 If bit PATEN in register PATCFG is set to "0", GE[8]=1: LED25~27 work in group mode GE[9]=1: LED28~30 work in group mode GE[10]=1: LED31~33 work in group mode GE[11]=1: LED34~36 work in group mode If bit PATEN in register PATCFG is set to "1", GE[8]=1: LED25~27 work in auto breath pattern mode GE[9]=1: LED28~30 work in auto breath pattern mode GE[10]=1: LED31~33 work in auto breath pattern mode GE[11]=1: LED34~36 work in auto breath pattern mode	0000

APPLICATION INFORMATION

R_{EXT}

The selection of R_{EXT} determined the maximum LED1~LED36 current I_{max} as described in below formula (1).

$$I_{max} = K \times \frac{V_{REXT}}{R_{EXT}} \quad (1)$$

Where V_{REXT} = 0.4V, K = 200, the recommended minimum value of R_{EXT} is 1KΩ.

When R_{EXT} = 2KΩ, I_{max} = 40mA

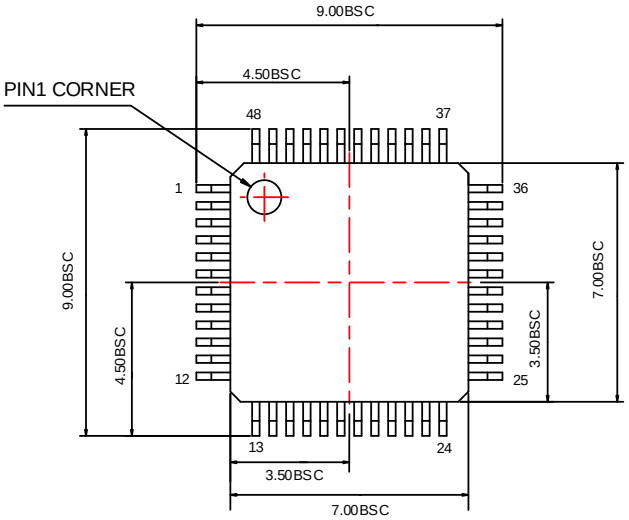
When R_{EXT} = 4KΩ, I_{max} = 20mA.

PCB LAYOUT CONSIDERATION

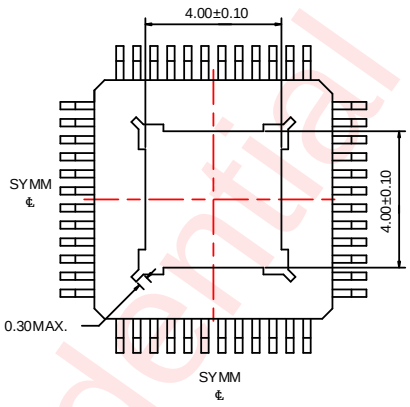
AW21036QPY-Q1 is a 36-channel LEDs driver programmed via I²C compatible interface. When all LEDs are operating, the device power dissipation is large. To obtain the good thermal performance and avoid thermal shutdown, PCB layout should be considered carefully. Here are some guidelines:

1. The C_1、C_2、C_{LED} should be placed as close to the chip as possible.
2. The R_{EXT} should be placed as close to the chip as possible.
3. The Thermal PAD must be well connecting to the GND of the PCB, and add as many thermal vias as possible beneath the thermal PAD on the PCB for the heat conductivity of the device and PCB.

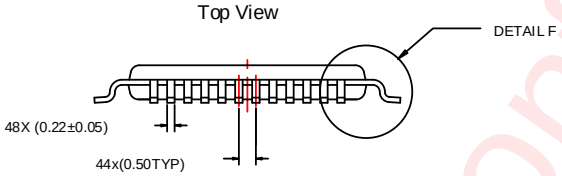
PACKAGE DESCRIPTION



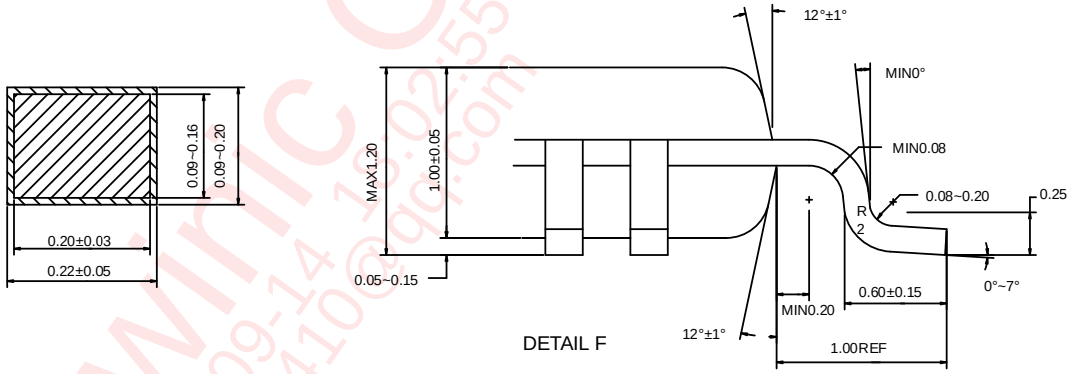
Top View



Bottom View



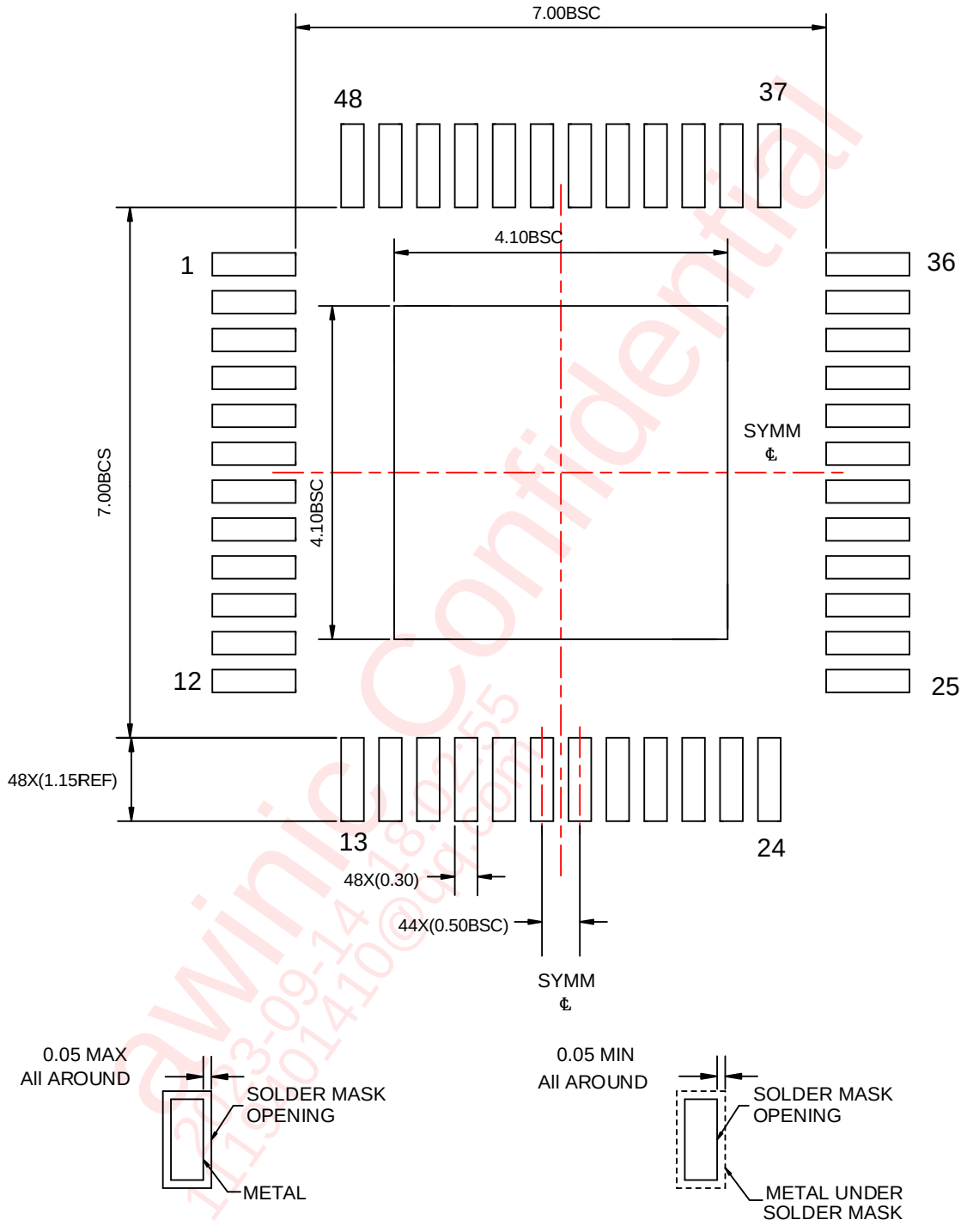
Side View



DETAIL F

UNIT:mm

LAND PATTERN DATA



NON SOLDER MASK DEFINED

SOLDER MASK DEFINED

Unit: mm

REVISION HISTORY

Version	Date	Change Record
V0.9	Apr. 2022	Officially released
V1.0	Oct. 2022	AEC-Q100 Qualified; EC Table Modified;

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