
Bluetooth 5.2 Dual Mode and Proprietary 2.4 GHz Wireless System on Chip

Specification

Beken Corporation

Building 41, Capital of Tech Leaders, 1387 Zhangdong Road,
Zhangjiang High-Tech Park, Pudong New District, Shanghai, China

Tel : (86)21 51086811

Fax : (86)21 60871089

*This document contains information that may be proprietary to, and/or secrets of, Beken Corporation.
The contents of this document should not be disclosed outside the companies without specific written
permission.*

*Disclaimer: Descriptions of specific implementations are for illustrative purpose only, actual hardware
implementation may differ.*

Table of Contents

1	General Description.....	3
1.1	Overview.....	3
1.2	Features	4
2	PIN information.....	6
2.1	QFN32.....	6
2.2	QFN40.....	8
2.3	QFN48.....	10
3	Functional Description.....	12
3.1	GPIO.....	12
3.2	Timers.....	13
3.2.1	PWM Timers.....	13
3.2.2	Watch dog timer and RTC timer.....	14
3.2.3	Sub-micro Second Event Timer.....	15
3.3	ADC.....	15
3.4	UART, I2C and SPI.....	15
3.5	USB.....	16
3.6	True random number generator	16
3.7	I2S Digital Audio	16
3.8	Code Encryption and System Security.....	17
3.9	Angle of Arrival and Angle of Departure	17
4	Electrical Specifications	18
5	Package Information.....	21
5.1	QFN 4x4 32-Pin	21
5.2	QFN 5x5 40-Pin	22
5.3	QFN 6x6 48-Pin	23
6	Solder Reflow Profile.....	24
7	Order Information.....	25

1 General Description

1.1 Overview

The BK3633 chip is a highly integrated wireless system on chip, which supports Bluetooth 5.2 Dual Mode and proprietary 2.4 GHz protocols. It integrates a high-performance RF transceiver, baseband, low power processor, rich feature peripheral units, programmable protocol and profile to support a wide range of applications. The Flash program memory makes it suitable for customized applications.

The BK3633 is designed with advanced technology process and integrated with switch DCDC regulator, that it has ultra-low power consumption and ultra-low leakage power. The embedded high order interference suppression filter and fast automatic gain control logic make it work well in high interference environment.

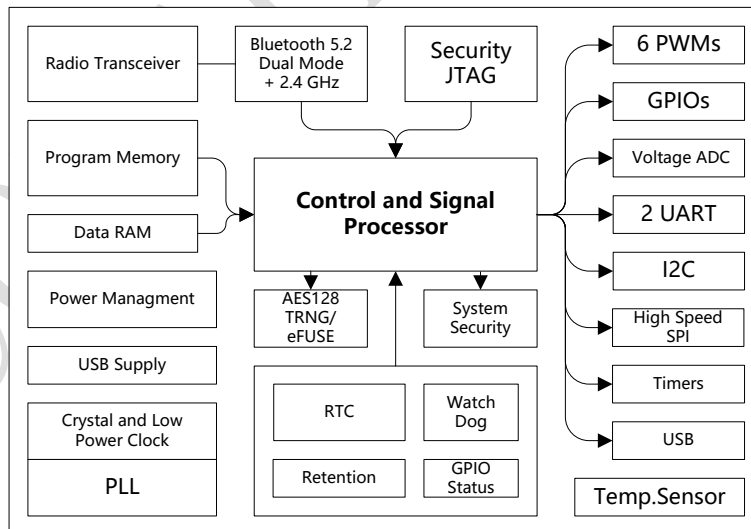


Figure 1 BK3633 Block Diagram

1.2 Features

- Bluetooth 5.2 Dual Mode and proprietary 2.4 GHz protocol
- Around 5 mA full operation current
- Less than 1 uA deep sleep current with low power running timer
- Bluetooth 5.1 standard Angle of Arrival and Angle of Departure
- Maximum sixteen antenna array for precise in-door positioning
- Bluetooth Low Energy 125 kbps, 500kbps, 1Mbps and 2Mbps
- Classic Bluetooth 1 Mbps
- Proprietary 2.4 GHz 1Mbps and 2 Mbps
- High output power up to 12 dBm and Bluetooth LE Power Control
- 32-bit RISC Core with 80 KB data memory and up to 80 MHz speed
- 500 KB programmable Flash
- Operation voltage from 0.9 ~1.5V(boost) ,2.0~3.6V(buck)
- Clock
 - 16 MHz crystal reference clock with internal tuning load capacitance
 - 80 MHz digital PLL clock
 - 32 kHz ring oscillator
 - External 32KHz crystal oscillator
 - MCU can run with any clock source with internal frequency divider
 - Dedicate audio PLL clock for I2S main clock
- Interface and peripheral units
 - Quad IO FLASH programming
 - I2C, SPI interface up to 96 MHz
 - Two UART interface and UART download

- Multi-channels high resolution 32 bit PWM with capture mode
- USB Host and Device interface, with USB audio capability
- IrDA receiver and transmitter amplify
- On-chip high accurate temperature sensor
- On-chip 10 bit general ADC
- GPIO with multiplexed interface functions
- True random number generator
- I2S/PCM digital audio interface with master and slave mode
- High quality high speed and low power clock output
- Code encryption and online decryption
- Secure JTAG and system protection
- Typical Package Type
 - 32-pin QFN 4x4, 40-pin QFN5x5 and 48-pin QFN6x6

2 PIN information

2.1 QFN32

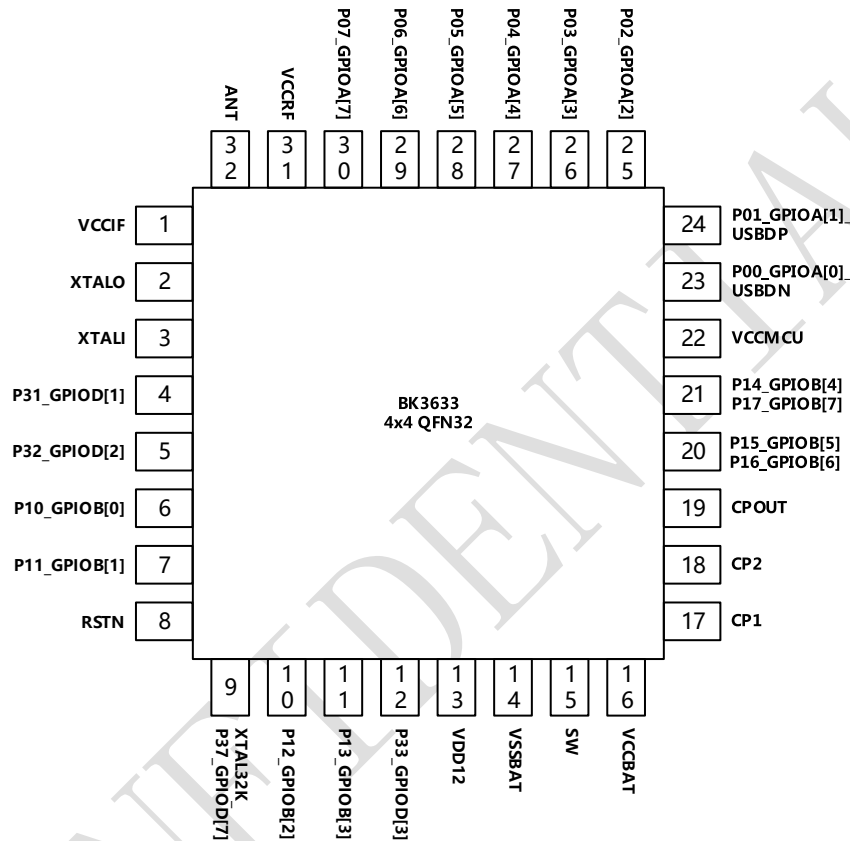


Figure 2 BK3633 QFN32 pin assignment

Table 1 BK3633 QFN32 Pin Description

PIN	Name	Pin Function	Description
1	VCCIF	Power	IF power, 1.5 V
2	XTALO	Analog	16 MHz crystal output
3	XTALI	Analog	16 MHz crystal input
4	P31	Digital I/O	General purpose IO
5	P32	Digital I/O	General purpose IO

6	P10	Digital I/O	General purpose IO
7	P11	Digital I/O	General purpose IO
8	RSTN	Analog	Reset PIN of system, `0` is active.
9	XTAL32K _P37	Analog	32 kHz Crystal input, and GPIO P37
10	P12	Digital I/O	General purpose IO
11	P13	Digital I/O	General purpose IO
12	P33	Digital I/O	General purpose IO
13	VDD12	Analog	LDO output, 1.2 V
14	VSSBAT	Ground	Ground
15	SW	Analog	Switch regulator pin for two battery mode
16	VCCBAT	Power	Power, 3 V
17	CP1	Analog	Charge pump component for FLASH
18	CP2	Analog	Charge pump component for FLASH
19	CPOUT	Power	Charge pump output voltage for FLASH
20	P15_P16	Digital I/O	General purpose IO
21	P14_P17	Digital I/O	General purpose IO
22	VCCMCU	Power	Power, 1.5 V
23	P00_USBDN	Digital I/O	General purpose IO, USBDN
24	P01_USBDP	Digital I/O	General purpose IO, USBDP
25	P02	Digital I/O	General purpose IO
26	P03	Digital I/O	General purpose IO
27	P04	Digital I/O	General purpose IO
28	P05	Digital I/O	General purpose IO
29	P06	Digital I/O	General purpose IO
30	P07	Digital I/O	General purpose IO
31	VCCRF	Power	RF power, 1.5 V
32	ANT	RF	RF signal port

2.2 QFN40

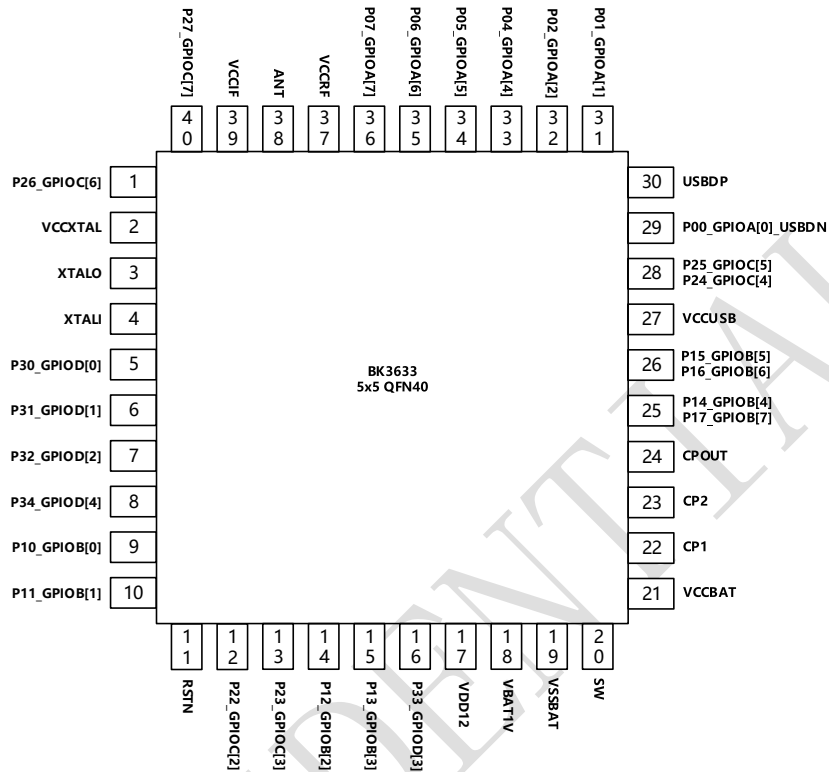


Figure 3 BK3633 QFN40 pin assignment

Table 2 BK3633 QFN40 Pin Description

PIN	Name	Pin Function	Description
1	P26	Digital I/O	General purpose IO
2	VCCXTAL	Power	XTAL power
3	XTALO	Analog	16 MHz crystal output
4	XTALI	Analog	16 MHz crystal input
5	P30	Digital I/O	General purpose IO
6	P31	Digital I/O	General purpose IO
7	P32	Digital I/O	General purpose IO
8	P34	Digital I/O	General purpose IO
9	P10	Digital I/O	General purpose IO
10	P11	Digital I/O	General purpose IO

11	VCC	Analog	Reset PIN of system, `0` is active.
12	P22	Digital I/O	General purpose IO
13	P23	Digital I/O	General purpose IO
14	P12	Digital I/O	General purpose IO
15	P13	Digital I/O	General purpose IO
16	P33	Digital I/O	General purpose IO
17	VDD12	Analog	LDO output
18	VBAT1V	Analog	One battery mode (battery input) or two battery mode (Ground)
19	VSSBAT	Ground	Ground
20	SW	Analog	Switch regulator pin for two battery mode
21	VCCBAT	Power	Power
22	CP1	Analog	Charge pump component for FLASH
23	CP2	Analog	Charge pump component for FLASH
24	CPOUT	Power	Charge pump output voltage for FLASH
25	P14_P17	Digital I/O	General purpose IO
26	P15_P16	Digital I/O	General purpose IO
27	VCCUSB	Power	Leave NC without USB
28	P25_P24	Digital I/O	General purpose IO
29	P00_USBDN	Digital I/O	General purpose IO, USBDN
30	USBDP	I/O	USBDP
31	P01	Digital I/O	General purpose IO
32	P02	Digital I/O	General purpose IO
33	P04	Digital I/O	General purpose IO
34	P05	Digital I/O	General purpose IO
35	P06	Digital I/O	General purpose IO
36	P07	Digital I/O	General purpose IO
37	VCCRF	Power	RF power
38	ANT	RF	RF signal port
39	VCCIF	Power	IF power
40	P27	Digital I/O	General purpose IO

2.3 QFN48

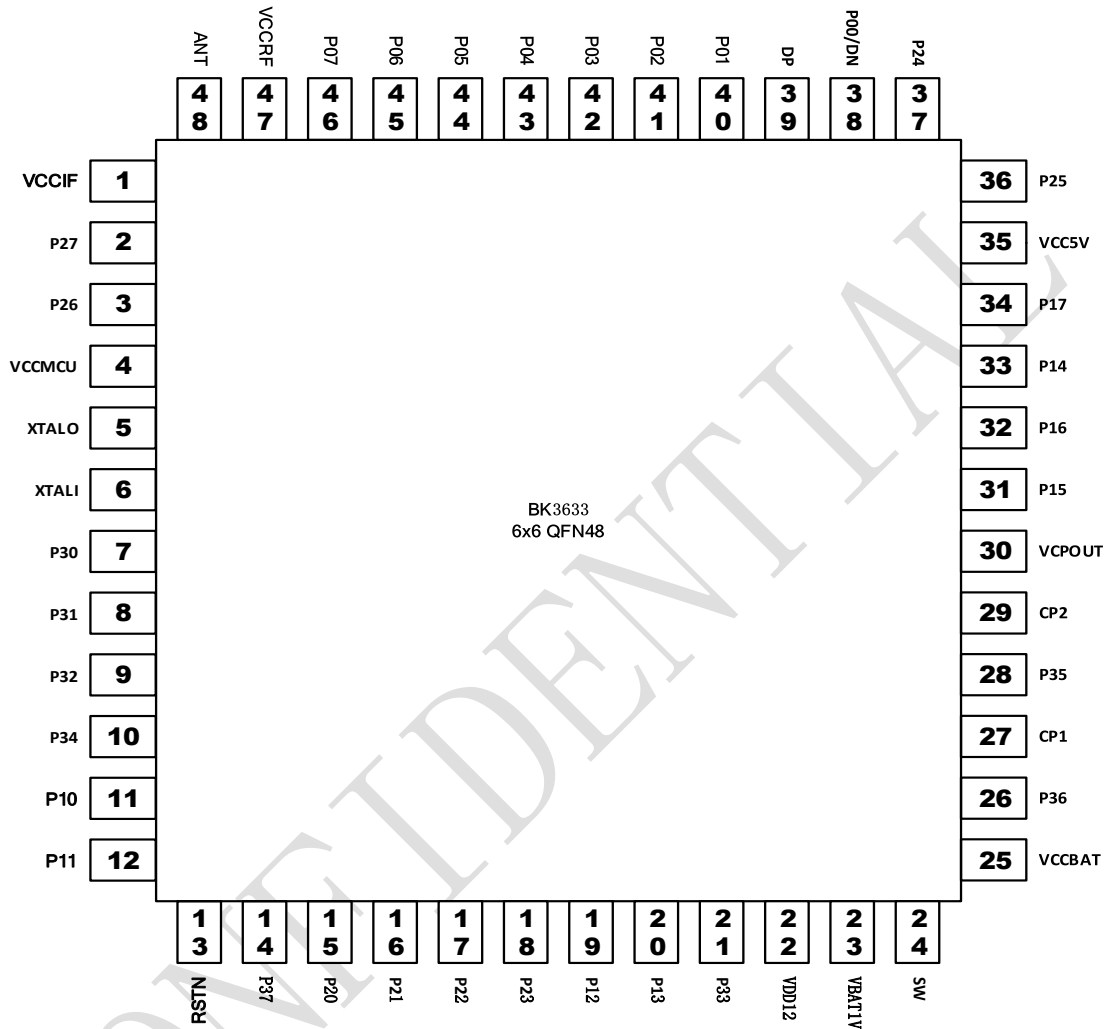


Figure 4 BK3633 QFN48 pin assignment

Table 3 BK3633 QFN48 Pin Description

PIN	Name	Pin Function	Description
1	VCCIF	Power	IF power, 1.5 V
2	P27	Digital I/O	General purpose IO
3	P26	Digital I/O	General purpose IO
4	VCCMCU	Power	Power, 1.5 V
5	XTALO	Analog	16 MHz crystal output
6	XTALI	Analog	16 MHz crystal input

7	P30	Digital I/O	General purpose IO
8	P31	Digital I/O	General purpose IO
9	P32	Digital I/O	General purpose IO
10	P34	Digital I/O	General purpose IO
11	P10	Digital I/O	General purpose IO
12	P11	Digital I/O	General purpose IO
13	RSTN	Analog	Reset PIN of system
14	P37	Digital I/O	General purpose IO
15	P20	Digital I/O	General purpose IO
16	P21	Digital I/O	General purpose IO
17	P22	Digital I/O	General purpose IO
18	P23	Digital I/O	General purpose IO
19	P12	Digital I/O	General purpose IO
20	P13	Digital I/O	General purpose IO
21	P33	Digital I/O	General purpose IO
22	VBAT1V	Power	The battery of 1V
23	VDD12	Analog	LDO output of GADC
24	SW	Analog	Switch regulator pin for two battery mode
25	VCCBAT	Power	The battery of 3V
26	P36	Digital I/O	General purpose IO
27	CP1	Analog	Charge pump component for FLASH
28	P35	Digital I/O	General purpose IO
29	CP2	Analog	Charge pump component for FLASH
30	VCPOUT	Power	Charge pump output voltage for FLASH
31	P15	Digital I/O	General purpose IO
32	P16	Digital I/O	General purpose IO
33	P14	Digital I/O	General purpose IO
34	P17	Digital I/O	General purpose IO
35	VCC5V	Power	5V power
36	P25	Digital I/O	General purpose IO
37	P24	Digital I/O	General purpose IO
38	P00/DN	Digital I/O/USB DN	General purpose IO/analog/USB DN
39	DP	Digital	USB DP

		I/O/USB DP	
40	P01	Digital I/O	General purpose IO
41	P02	Digital I/O	General purpose IO
42	P03	Digital I/O	General purpose IO
43	P04	Digital I/O	General purpose IO
44	P05	Digital I/O	General purpose IO
45	P06	Digital I/O	General purpose IO
46	P07	Digital I/O	General purpose IO
47	VCCRF	Power	RF power
48	ANT	RF	RF signal port

3 Functional Description

3.1 GPIO

The BK3633 has 32 GPIO pins, which can be configured as either input or output. There are secondary functions available for GPIO pins and configurable by firmware.

At the beginning of the chip starts up, the chip will enter programming mode, JTAG mode or normal according received command from Mode Selecting Pin.

Table 4 BK3633 GPIO function mapping

	Description		PROGRAM Mode	JATG mode
GPIOA[0]	UART	UART_TX/SCL/USBDN	DL_UART_TX	
GPIOA[1]		UART_RX/SDA/USBDP	DL_UART_RX	
GPIOA[2]	I2C	SCL		
GPIOA[3]		SDA		JTAG_NTRST

GPIOA[4]	SPI	SPI_SCK	SPI_MOSI	JTAG_TDI
GPIOA[5]		SPI_MOSI	SPI_MISO	JTAG_TDO
GPIOA[6]		SPI_MISO/PWM[5]	SPI_SCK	JTAG_TCK
GPIOA[7]		SPI_NSS/PWM[4]	SPI_CS	JTAG_TMS
GPIOB[0]	PWM	PWM[0]		
GPIOB[1]		PWM[1]		
GPIOB[2]		PWM[2]		
GPIOB[3]		PWM[3]		
GPIOB[4]		PWM[4]		
GPIOB[5]		PWM[5]		
GPIOB[6]	N/A	UART2_TX		
GPIOB[7]	N/A	UART2_RX		
GPIOC[0]				
GPIOC[1]				
GPIOC[2]				
GPIOC[3]				
GPIOC[4]				
GPIOC[5]	PCM/I2S	PCM_BCLK		
GPIOC[6]		PCM_SCLK		
GPIOC[7]		PCM_DOUT		
GIOD[0]		PCM_DIN		
GIOD[1]	ADC and Clock Output	Ch1		
GIOD[2]		Ch2		
GIOD[3]		Ch3/CLKOUT		
GIOD[4]		Ch4		
GIOD[5]		CLKOUT2/Ch5		
GIOD[6]		Ch6		
GIOD[7]				

Each GPIO pin can be the source to wake up MCU from shut down state. In the shutdown state, any voltage level change on the pre-configured GPIO pin will trigger the wake-up procedure.

3.2 Timers

3.2.1 PWM Timers

There are six 32 bits PWM timers. The clock of PWM timers can be selected as 32 KHz clock or 16 MHz clock by register.

There are four modes of PWM timers.

First mode is the timer mode. The timer mode can generate interrupt to MCU.

Second mode is the PWM mode, which can generate PWM waveform and output to GPIO pins to drive external device such as LED. Six GPIO pins can be used to output PWM waveform separately.

Third mode is the capture mode, which can count the clock cycle between either combination of falling edge or rising edge of the signal in the special pin.

Fourth mode is the pulse mode, which can count the number of either active high or active low pulse.

3.2.2 Watch dog timer and RTC timer

The watch dog timer and RTC timer run on the always on power domain, whose clock source is 32 kHz clock.

The 16 bits watch dog timer runs with 4 kHz frequency that its period can be up to 16 second. After watch dog timer is expired, it will reset the whole chip.

The 32 bits RTC timer in always on power domain run with ROOSC frequency that its period can be up to one day. After RTC timer is expired,

it will wake up the MCU.

3.2.3 Sub-micro Second Event Timer

There is a sub-micro second resolution timer recording the timing of special event such as the moment of the Bluetooth transmitter first bit of the packet or receiver synchronization word gets matched. Also it can get a shot of the timing of the edge of special GPIO.

3.3 ADC

A 10-bit generic ADC is integrated in BK3633. Total six external channels and two internal channels can be selected for ADC transfer. It supports both single and continuous mode.

ADC Channel Number	ADC Source
Channel 1	GPIO31
Channel 2	GPIO32
Channel 3	GPIO33
Channel 4	GPIO34
Channel 5	GPIO35
Channel 6	VBAT1V-pin
Channel 7	VCCBAT-pin
Channel 0 - Internal Channel	Temperature Sensor

3.4 UART, I2C and SPI

There are two set UARTs, one set I2C and one set SPI interface, which support both master and slave mode.

The UART baud rate can be up to 3.2 MHz, and the SPI clock speed can be up to 96 MHz.

3.5 USB

It integrates USB host and device transceiver and base band.

The USB interface supports EP0 to EP8. For EP0 there is 64 Bytes FIFO each direction. For every channel of EP1 to EP4, there is 256 Bytes FIFO each direction. For every channel of EP5 to EP8 there is 64 Bytes FIFO in single direction.

3.6 True random number generator

By using device noise variation characteristic, it provides one bit true random number generator.

3.7 I2S Digital Audio

The I2S audio interface is mapped to GPIO[25,26,27,30], which support arbitrate sample rate from 8 kHz to 96 kHz. When working as master, the main clock can be output from GPIO33.

The I2S interface supports both PCM mono channel mode and I2S stereo channel mode. The data width can be 16, 24 and 32 bit.

3.8 Code Encryption and System Security

There is one times NVM for code encryption and system security. Each unit can have different password for code encryption, where hardware will do the decryption automatically.

The download and debug interface could be closed permanently by user to keep system security.

User could also use the NVM for other purpose such as unique ID or MAC address. The NVM used for code encryption could be closed for read and write operation, and other space could be closed for write operation. Once the access right is changed, no roll back is possible to provide permanent security of the system.

3.9 Angle of Arrival and Angle of Departure

It supports up to sixteen antenna array for angle estimation. Any GPIO could be configured as antenna switch control pin.

4 Electrical Specifications

Table 6 BK3633 DC Characteristics

Name	Parameter (Condition)	Min	Typical	Max	Unit
VCCBAT	Battery Supply	0.9	3.0	3.6	V
TEMP	Temperature	-40	+20	+125	°C
VIH	High level	VCC-0.3		VCC+0.3	V
VIL	Low level	VSS		VSS+0.3	V
VOH	High level (IOH=-0.25mA)	VCC- 0.3		VCC	V
VOL	Low level(IOL=0.25mA)	VSS		VSS+0.3	V
IVDD	Deep sleep (1 kHz Timer)		0.9		uA
IVDD	Shut down		100		nA
IVDD	Sleep current (RF OFF, 32 kHz clock, DIG Retention)		2		uA
IVDD	Active RX (3.3 V)		5.5		mA
IVDD	Active TX @ 0 dBm (3.3 V)		6.1		mA

Table 7 BK3633 RF Characteristics

FOP	Operating frequency	2402		2480	MHz
FXTAL	Crystal frequency		16		MHz
RFSK	Air data rate	0.125	1	2	Mbps
PRF	Output power	-20	9.5	+12	dBm
PRF	High output power PA	-20	9.5	+20	dBm
BLE 1 Mbps data rate performance					
PBW	Modulation 20 dB bandwidth			1	MHz
PRF1	Out of band emission 2 MHz		-35		dB
PRF2	Out of band emission 3 MHz		-45		dB
Carrier Drift	Maximum carrier drift	-50	5	50	kHz
Drift Rate	Maximum drift rate		2.5	20	kHz/50us
Δf_{1avg}	Maximum modulation	225	255	275	kHz
Δf_{2min}	Minimum modulation	185	213		kHz
$\Delta f_{2avg}/\Delta f_{1avg}$		0.8	0.92		

Max Input	30.8% PER		0		dBm
RXSNS	30.8% PER sensitivity		-96		dBm
Intermodulation	Pin=-64 dBm; Punwant=-50 dBm; f0=2f1-f2, f2-f1=3 MHz or 4 MHz or 5 MHz		-27	-22	dBm
C/ICO	Co-channel C/I		9		dB
C/I1ST	ACS C/I 1MHz		-3		dB
C/I2ND	ACS C/I 2MHz		-39		dB
C/I3RD	ACS C/I 3MHz		-49		dB
C/I1STI	ACS C/I Image channel		-32		dB
C/I2NDI	ACS C/I Image +1 MHz		-43		dB
Blocking	@ 30 MHz ~2GHz		5		dBm
Blocking	@ 2GHz ~2.399 GHz		-3		dBm
Blocking	@ 2.484GHz~3GHz		-2		dBm
Blocking	@ 3 GHz ~ 12.75GHz		5		dBm
Leakage	Leakage @ < 1GHz		-71		dBm
Leakage	Leakage @ >1GHz		-56		dBm
RSSI	Dynamic range	-97		-62	dBm
RSSI	Resolution		1		dB

Table 8 BK3633 ADC Characteristics

Name	Condition	Min	Typical	Max	Unit
Conversion Clock(Fs)				16	MHz
Conversion Time			16		Cycle
VREF	Internal		0.5		V
	External			0.6	V
Resolution			10		bits
No Missing Code			9		bits
Input Voltage Range		0		ADC_VREF*2	V
Input Impedance			16/(Fs*Cs)		kOhm
Input Capacitance(Cs)			8		pF
Offset		-90		90	mV
DNL			1		bits
INL			2		bits
Offset Temperature Drift				0.2	LSB/°C
Gain Temperature				0.01	%/°C

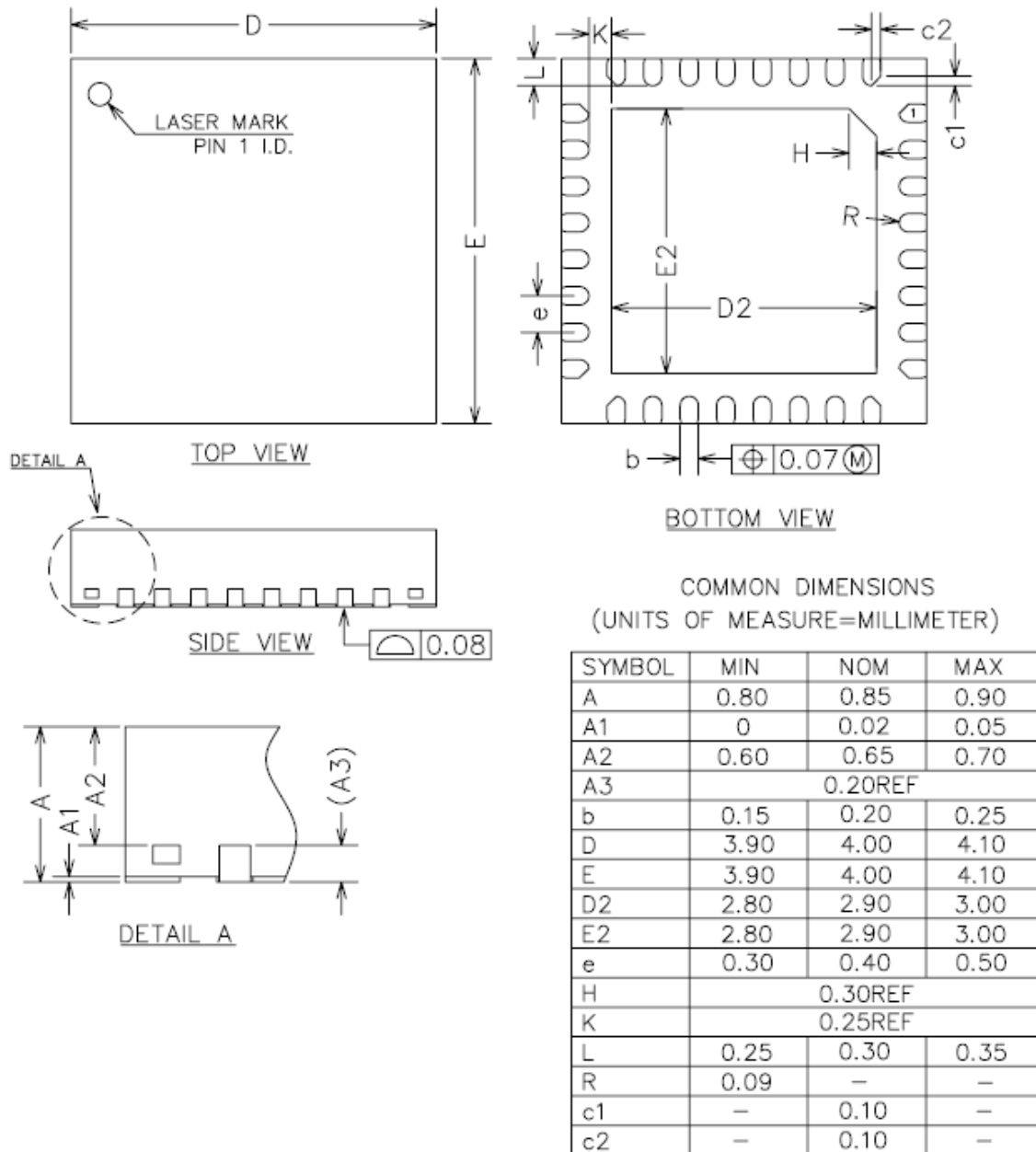
Drift					
SNDR			60		dB
Dynamic Range			64		dB
Tstartup				1	us
Current Consumption			750		uA

CONFIDENTIAL

5 Package Information

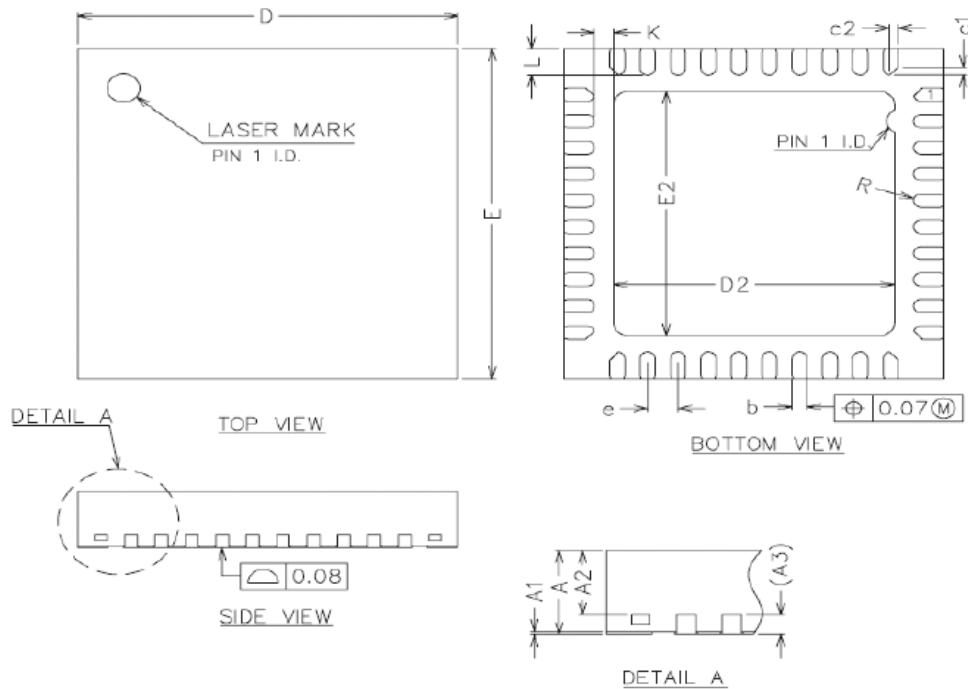
5.1 QFN 4x4 32-Pin

The BK3633 32-Pin uses the 4mmx4mm QFN package.



5.2 QFN 5x5 40-Pin

The BK3633 40-Pin uses the 5mmx5mm QFN package.

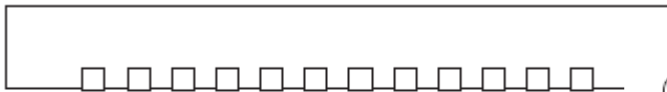
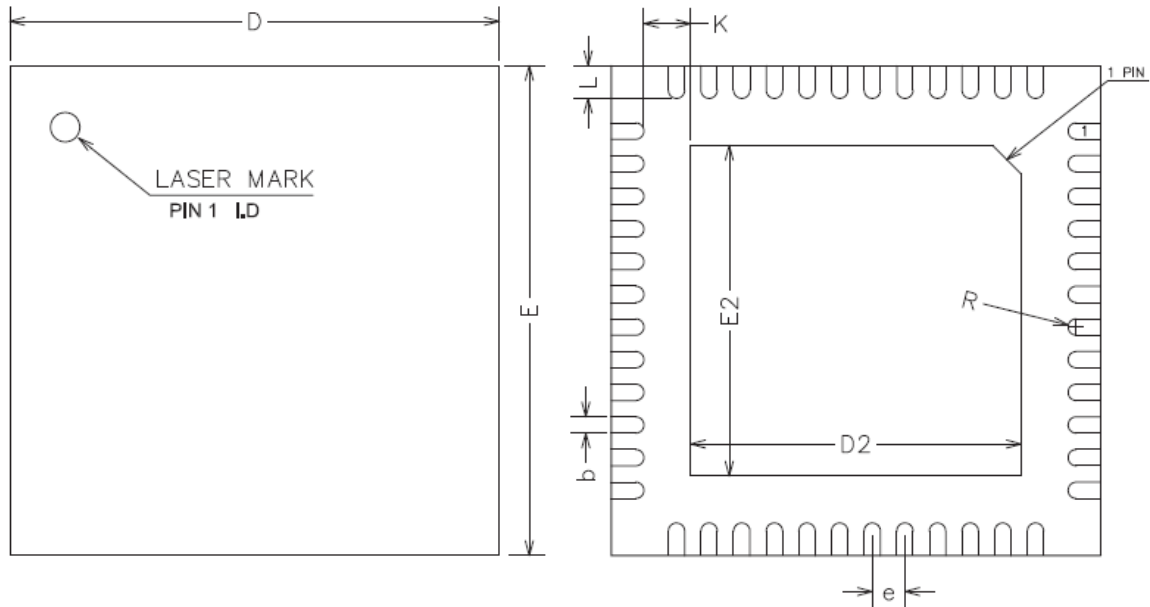


COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0	0.02	0.05
A2	0.50	0.65	0.60
A3	0.20REF		
b	0.15	0.20	0.25
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.60	3.70	3.80
E2	3.60	3.70	3.80
e	0.35	0.40	0.45
K	0.20	-	-
L	0.35	0.40	0.45
R	0.075	-	-
C1	-	0.12	-
C2	-	0.12	-

5.3 QFN 6x6 48-Pin

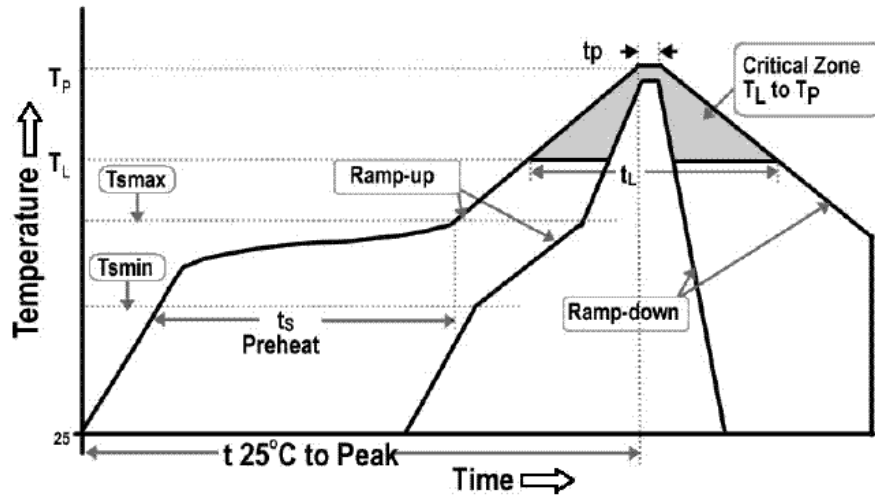
The BK3633 48-Pin uses the 6mmx6mm QFN package.



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3	0.20REF		
b	0.15	0.20	0.25
D	5.90	6.00	6.10
E	5.90	6.00	6.10
D2	3.95	4.05	4.15
E2	3.95	4.05	4.15
e	0.35	0.40	0.45
K	0.20	-	-
L	0.35	0.40	0.45
R	0.09	-	-

6 Solder Reflow Profile



Profile Feature		Specification
Average Ramp-Up Rate (tsmax to tp)		3 °C/second max.
Pre_heat	Temperature Min (T _{smin})	150 °C
	Temperature Max (T _{smax})	200 °C
	Time (ts)	60-180 seconds
Time Maintained above	Temperature (T _L)	217 °C
	Time (t _L)	60-150 seconds
Peak/Classification Temperature (T _p)		260 °C
Time within 5 °C of Actual Peak Temperature (tp)		20-40 seconds
Ramp-Down Rate 6		6 °C/second max.
Time 25 °C to Peak Temperature 8		8 minutes max.

RoHS Compliant

The product does not contain lead, mercury, cadmium, hexavalent chromium, PBB&PBDE content in accordance with directive 2002/95/EC(RoHS).

ESD Sensitivity

Integrated circuits are ESD sensitive and can be damaged by static electricity. Proper ESD techniques should be used when handling these devices.

7 Order Information

Part number	Package	Packing	Minimum Order Quantity
BK3633QN32	QFN 4mmx4mm 32-Pin	Tape Reel	3K
BK3633QN40	QFN 5mmx5mm 40-Pin	Tape Reel	3K
BK3633QN48	QFN 6mmx6mm 48-Pin	Tape Reel	3K

Revision History

Version	Date	Author(s)	Description
0.1	20/02/2020	WF	Initial draft
0.2	07/04/2020	MS	Updated some information of package
0.3	19/05/2020	MS	Updated some information of PIN
0.4	30/06/2020	MS	Updated flash information
0.5	09/09/2020	Qxu	Updated Electrical Specifications, PIN information, Add Solder Reflow Profile
0.6	19/10/20	MS	Updated the GADC information and QFN package of QFN 6X6 48PIN
0.7	27/10/20	MS	Updated the description of RSTN PIN
0.8	16/12/20	MS	Updated the information of QFN48 package
0.9	13/04/21	MS	Updated the forms of QFN48 and QFN40 because of USB problems

单击下面可查看定价，库存，交付和生命周期等信息

[>>Beken\(博通集成电路\)](#)