BL9162

300mA High PSRR, Ultra-low Noise, Ultra-Fast CMOS LDO Regulator

FEATURES

- Ultra-low Noise
- Ultra-Fast Transient Response
- High PSRR: -87dB @ 217Hz
  -83dB @ 1KHz
  -54dB @ 1MHz
- 0.1μA Standby Current When Shutdown
- Low Dropout: 140mV@300mA (V_{OUT}=2.8V)
- Wide Operating Voltage Ranges: 1.6V to 5.5V
- Current Limiting and Short Circuit Current Protection
- Thermal Shutdown Protection
- Only 1μF Output Capacitor Required for Stability
- Fast output discharge
- Available in SOT23-5, SC70-5 and DFN1X1-4L Packages

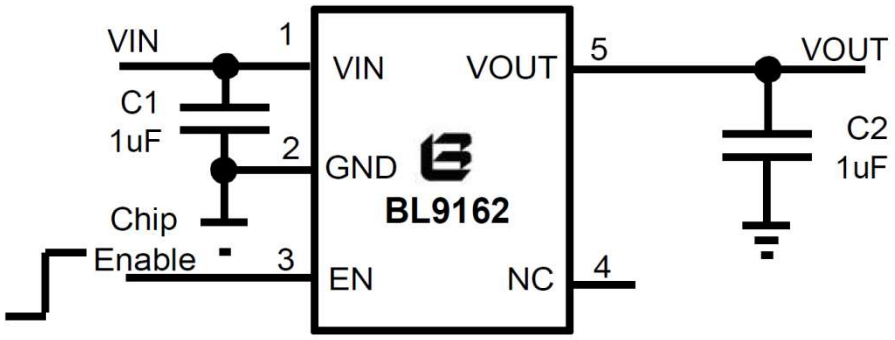
APPLICATIONS

- Cellular and Smart Phones
- Cordless Telephones
- Camera and Machine Vision Modules
- Battery-Powered Equipment
- Laptop, Palmtops, Notebook Computers
- Hand-Held Instruments
- PCMCIA Cards
- Portable Information Appliances

DESCRIPTION

The BL9162 is designed for portable applications with demanding performance and space requirements. The BL9162 performance is optimized for battery-powered systems to deliver ultra-low noise and low quiescent current. Regulator ground current increases only slightly in dropout, further prolonging the battery life. The BL9162 also works with low-ESR ceramic capacitors, reducing the amount of board space necessary for power applications, critical in hand-held wireless devices. The BL9162 consumes only 0.1μA current in shutdown mode and has fast turn-on time (Typical 100μs). The other features include ultra- low dropout voltage, high output accuracy, current limiting protection, and high ripple rejection ratio.

TYPICAL APPLICATION



ORDERING INFORMATION

BL9162 - XXX X X XXX

Package:
RN: SOT23-5
URN: SC70-5
DRN: DFN1x1-4L

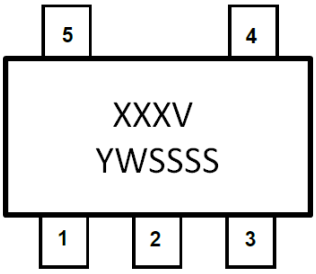
Enable Option:
A: active high with internal pull down

Output Voltage Accuracy:
B:±2%

Output Voltage:
100:1.0V 105:1.05V 110:1.1V 115:1.15V
120:1.2V 150:1.5V 180:1.8V 250:2.5V
260:2.6V 280:2.8V 300:3.0V 330:3.3V
360:3.6V 400:4.0V

Package Marking

SOT23-5 &SC70-5



DFN1×1-4L

V: Output voltage
Y: Data code—Year
W: Data code—Week

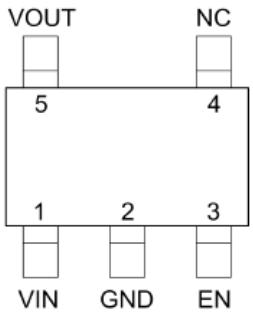
Output Voltage	V		Output Voltage	V	
	SOT23-5	SC70-5 & DFN1X1-4L		SOT23-5	SC70-5 & DFN1X1-4L
1.0V	B	A	2.5V	E	P
1.05V	- B	- A	2.6V	T	Q
1.1V	F	B	2.8V	G	S
1.15V	- F	- B	3.0V	I	U
1.2V	A	C	3.3V	K	X
1.5V	C	F	3.6V	Y	Y
1.8V	D	I	4.0V	Z	Z

Y	4	5	6	…	0	1	…
Year	2014	2015	2016	…	2020	2021	…

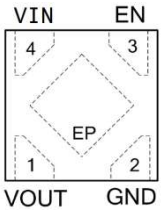
W	A	…	Y	Z	a	…	y	z
Week	1	…	25	26	27	…	51	52

PIN CONFIGURATIONS

SOT23-5 & SC70-5 (TOP VIEW)



DFN1X1-4L (TOP VIEW)



Thermal Resistance (Note3)

Package	Θ_{JA}	Θ_{JC}
SOT23-5	250℃/W	130℃/W
SC70-5	333℃/W	170℃/W

Pin Description

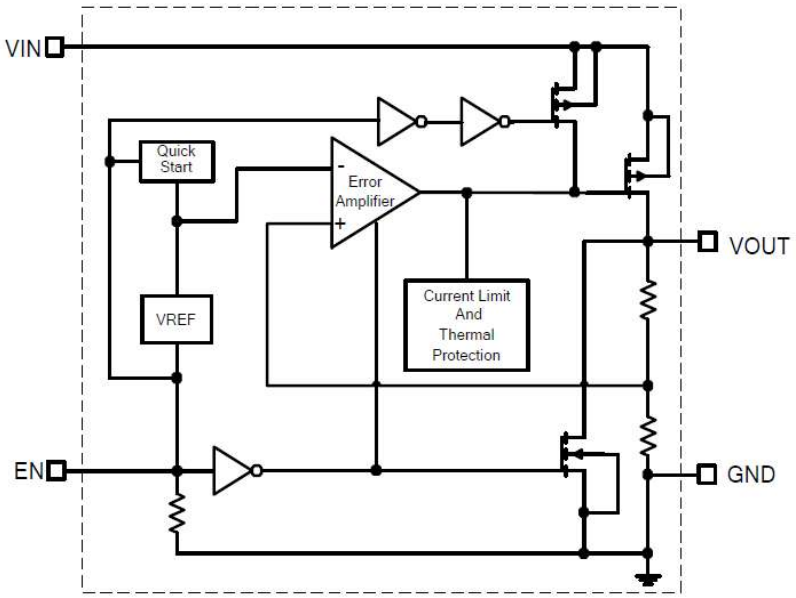
SOT23-5 & SC70-5

PIN	NAME	FUNCTION
1	VIN	Power Input Voltage.
2	GND	Ground.
3	EN	Chip Enable Pin, This pin has an internal pull-down resistor
4	NC	No Connection.
5	VOUT	Output Voltage.

DFN1X1-4L

PIN	NAME	FUNCTION
1	VOUT	Output Voltage.
2	GND	Ground.
3	EN	Chip Enable Pin, This pin has an internal pull-down resistor
4	VIN	Power Input Voltage.
Exposed Pad		The exposed pad should be connected to a large ground plane to maximize thermal performance.

Block Diagram



Absolute Maximum Rating (Note 1)

Input Supply Voltage (VIN)	-0.3V to +6V	Maximum Junction Temperature	150°C
EN Pin Input Voltage	-0.3V to VIN	Operating Temperature Range (Note2)	-40°C to 85°C
Output Voltages	-0.3V to VIN+0.3V	Storage Temperature Range	-65°C to 125°C
Output Current	300mA	Lead Temperature (Soldering, 10s)	300°C

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The BL9162 is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: Thermal Resistance is specified with approximately 1 square of 1 ozcopper.

Electrical Characteristics (Note 4)

(V_{IN}=Vout +1V, EN=V_{IN}, C_{IN}=C_{OUT}=1μF, T_A=25℃, unless otherwise noted.)

Parameter		Symbol	Conditions	MIN	TYP	MAX	unit
Input Voltage		V_{IN}		1.6		5.5	V
Output Voltage Accuracy		ΔV_{OUT}	V_{IN}=Vout+1V, I_{OUT}=1mA	-2		+2	%
Current Limit		I_{LIM}	R_{LOAD}=1Ω	350			mA
Short Circuit Current		I_{SHORT}	V_{OUT}=0V		180		mA
Quiescent Current		I_Q	V_{EN}>1.2V, I_{OUT}=0mA		45	70	μA
Dropout Voltage		V_{DROP}	I_{OUT}=300mA, V_{OUT}=3.3V		130	200	mV
			I_{OUT}=300mA, V_{OUT}=2.8V		140	210	
			I_{OUT}=300mA, V_{OUT}=1.8V		210	300	
			I_{OUT}=300mA, V_{OUT}=1.0V		450	650	
Line Regulation (Note 5)		ΔV_{LINE}	V_{IN}=Vout+1V to 5.5V I_{OUT}=1mA		0.03	0.17	%/V
Load Regulation (Note 6)		ΔV_{LOAD}	1mA<I_{OUT}<300mA V_{IN}=Vout+1V		0.002		%mA
Output Voltage Temperature Coefficient (Note 7)		TC_{VOUT}	I_{OUT}=1mA		±60		ppm/℃
Standby Current		I_{STBY}	V_{EN}=GND, Shutdown		0.1	1	μA
EN Input Bias Current		I_{IBSD}	V_{EN}=GND or V_{IN}		0.1	1	μA
EN Input Threshold	Logic Low	V_{IL}	V_{IN}=3V to 5.5V, Shutdown			0.4	V
	Logic High	V_{IH}	V_{IN}=3V to 5.5V, Start up	1.2			V
Output Noise Voltage		e_{NO}	10 to100kHz; C_{OUT}=1uF I_{OUT}=100mA; V_{OUT}=2.8V		50		μV_{RMS}
			10 to100kHz; C_{OUT}=1uF I_{OUT}=100mA; V_{OUT}=1.8V		38		
Power Supply Rejection Ratio	f=217Hz	PSRR	I_{OUT}=10mA V_{OUT}=1.8V V_{IN}=2.8V		-87		dB
	f=1KHz				-83		
	f=10KHz				-72		
	f=1MHz				-54		
Thermal Shutdown Temperature		T_{SD}	Shutdown, Temp increasing		170		℃
Thermal Shutdown Hysteresis		T_{SDHY}			25		℃

Note 4: Production test at +25°C. Specifications over the temperature range are guaranteed by design and characterization.

Note 5: Line regulation is calculated by $\Delta V_{LINE} = \left| \left(\frac{V_{OUT1} - V_{OUT2}}{\Delta V_{IN} \times V_{OUT(normal)}} \right) \right| \times 100$

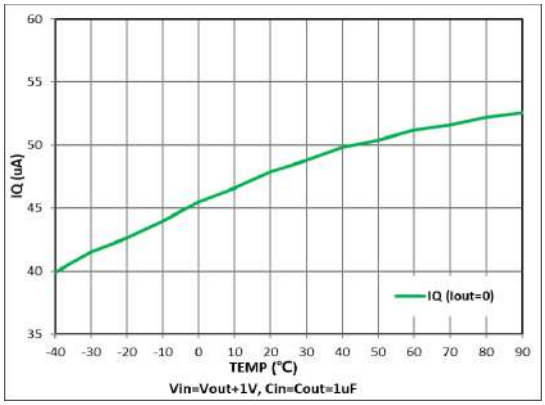
Where V_{OUT1} is the output voltage when V_{IN}=5.5V, and V_{OUT2} is the output voltage when V_{IN}=4.3V, ΔV_{IN}=1.2V. V_{OUT} (normal) =3.3V.

Note 6: Load regulation is calculated by $\Delta V_{LOAD} = \left| \left(\frac{V_{OUT1} - V_{OUT2}}{\Delta I_{OUT} \times V_{OUT(normal)}} \right) \right| \times 100$

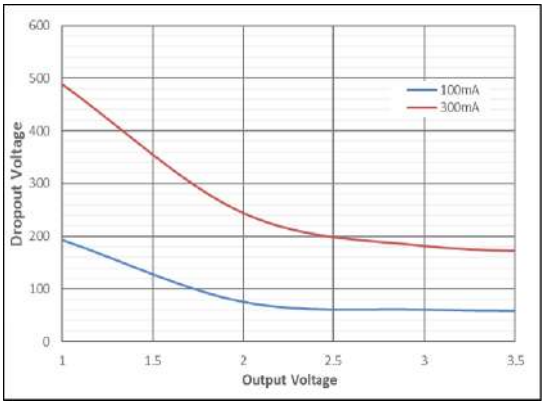
Where V_{OUT1} is the output voltage when I_{OUT}=1mA, and V_{OUT2} is the output voltage when I_{OUT}=300mA. ΔI_{OUT}=299mA, V_{OUT}(normal)=2.8V.

Note 7: The temperature coefficient is calculated by $TC_{V_{OUT}} = \frac{\Delta V_{OUT}}{\Delta T \times V_{OUT}}$

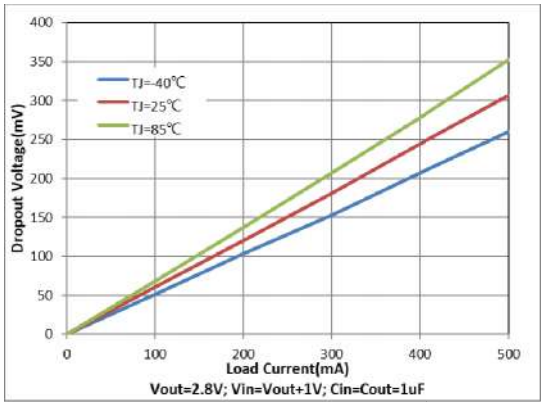
Typical Performance Characteristics



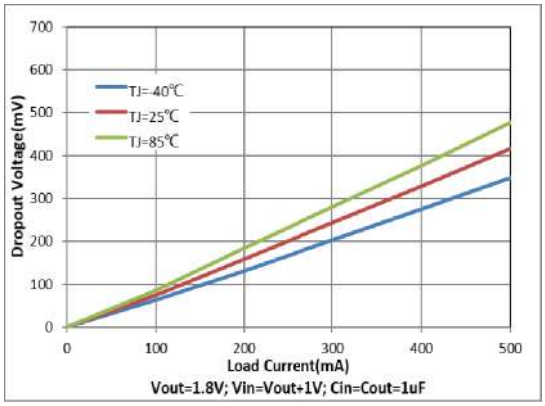
Quiescent Current vs Temperature



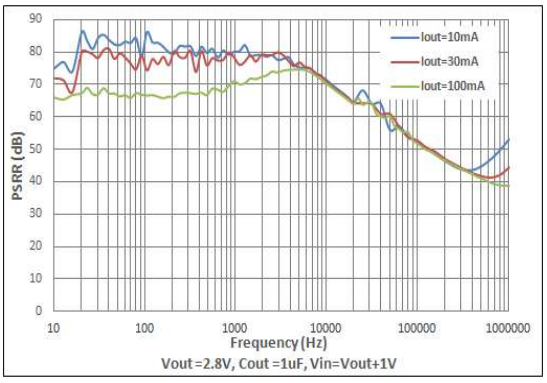
Dropout Voltage vs Output



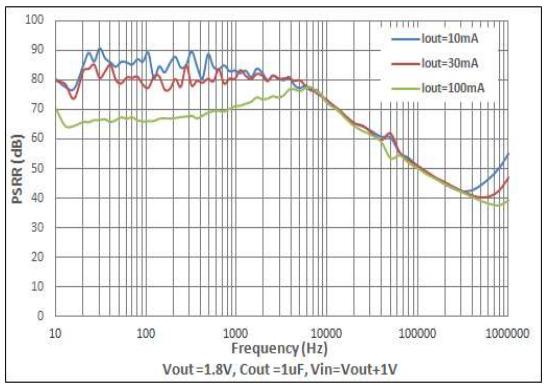
Output Dropout Voltage vs Load Current (Vout=2.8V)



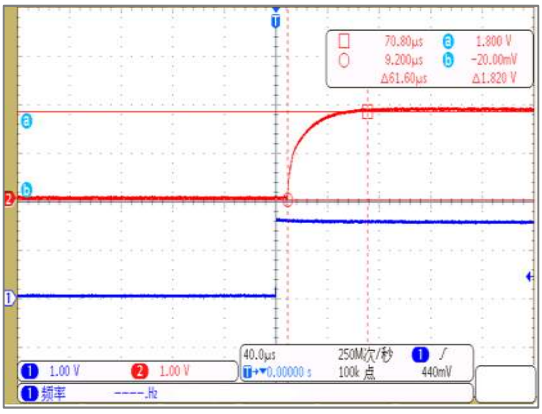
Dropout Voltage vs Load Current (Vout=1.8V)



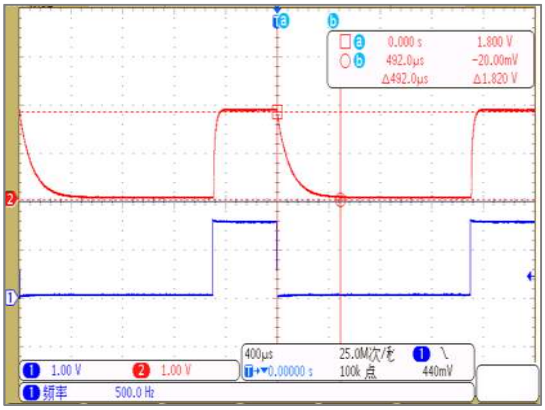
Power-Supply Ripple Rejection vs Frequency (Vout=2.8V)



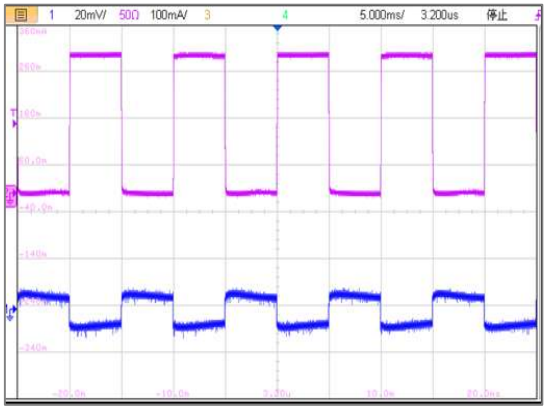
Power-Supply Ripple Rejection vs Frequency(Vout=1.8V)



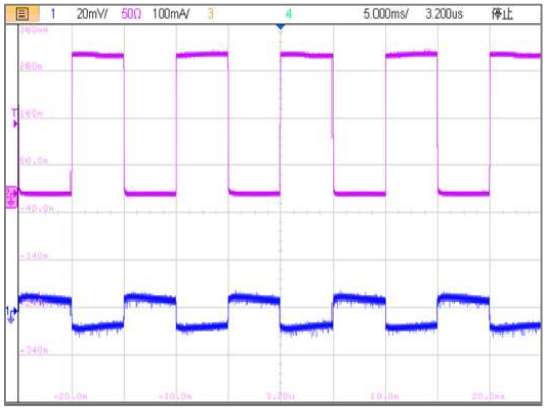
EN Start (Vout=1.8V)



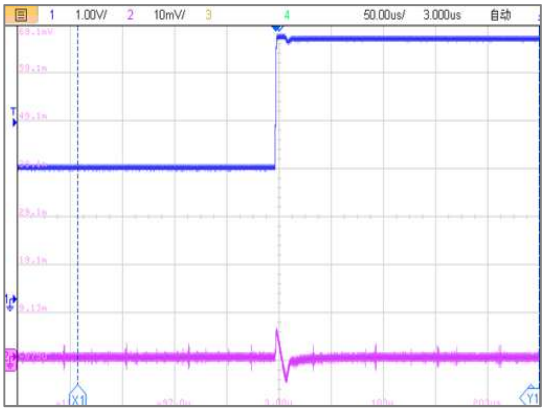
EN Shutdown (Vout=1.8V)



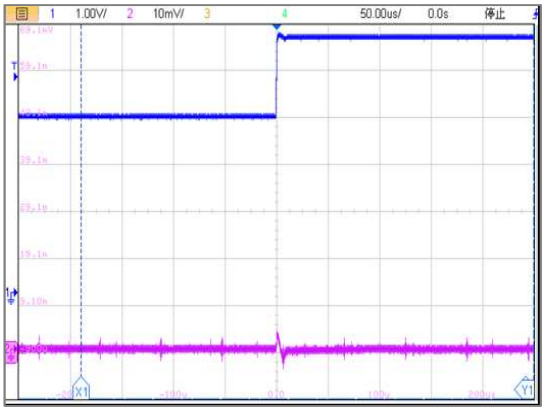
Load Trans 1mA – 300mA (Vout= 1.8V)



Load Trans 1mA – 300mA (Vout= 2.8V)



Line Trans 2.8V~5.5V (Vout=1.8V,Iout=1mA)



Line Trans 3.8V~5.5V (Vout=2.8V,Iout=1mA)

Applications Information

Like any low-dropout regulator, the external capacitors used with the BL9162 must be carefully selected for regulator stability and performance. Using a capacitor whose value is > 1μF on the BL9162 input and the amount of capacitance can be increased without limit. The input capacitor must be located a distance of not more than 0.5 inch from the input pin of the IC and returned to a clean analog ground. Any good quality ceramic or tantalum can be used for this capacitor. The capacitor with larger value and lower ESR (equivalent series resistance) provides better PSRR and line-transient response. The output capacitor must meet both requirements for minimum amount of capacitance and ESR in all LDOs application. Generally, 1.0-μF X7R-type ceramic capacitors are recommended because these capacitors have minimal variation in value and equivalent series resistance (ESR) over temperature. Output capacitor of larger capacitance can reduce noise and improve load transient response, stability, and PSRR. The output capacitor should be located not more than 0.5 inch from the VOUT pin of the BL9162 and returned to a clean analog ground.

Enable Function

The BL9162 features an LDO regulator enable/disable function. To assure the LDO regulator will switch on; the EN turn on control level must be greater than 1.2 volts. The LDO regulator will go into the shutdown mode when the voltage on the EN pin falls below 0.4 volts. For to protect the system, the BL9162 have a quick discharge function. If the enable function is not needed in a specific application, it may be tied to VIN to keep the LDO regulator in a continuously on state.

Thermal Considerations

Thermal protection limits power dissipation in BL9162. When the operation junction temperature exceeds 170°C, the OTP circuit starts the thermal shutdown function turn the pass element off. The pass element turns on again after the junction temperature cools by 25°C.

For continue operation, do not exceed absolute maximum operation junction temperature 125°C. The power dissipation definition in device is:

$$PD(MAX) = (TJ(MAX) - TA) / \theta JA$$

Where TJ(MAX) is the maximum operation junction temperature 125°C, TA is the ambient temperature and the θJA is the junction to ambient thermal resistance. For recommended operating conditions specification of BL9162, where TJ(MAX) is the maximum junction temperature of the die (125°C) and TA is the maximum ambient temperature. The junction to ambient thermal resistance (θJA is layout dependent) for SOT-23-5 package is 250°C/W, on standard JEDEC 51-3 thermal test board. The maximum power dissipation at TA= 25°C can be calculated by following formula:

PD(MAX) = (125°C−25°C)/250 = 400mW (SOT-23-5)

The maximum power dissipation depends on operating ambient temperature for fixed TJ(MAX) and

thermal resistance θJA. It is also useful to calculate the junction of temperature of the BL9162 under a set of specific conditions. In this example let the Input voltage VIN=3.3V, the output current Io=300mA and the case temperature TA=40°C measured by a thermal couple during operation. The power dissipation for the VOUT=2.8V version of the BL9162 can be calculated as:

PD = (3.3V−2.8V) ×300mA+3.6V×100uA=150mW

And the junction temperature, TJ, can be calculated as follows:

TJ=TA+PD×θJA=40°C+0.15W×250°C/W=40°C+37.5°C=77.5°C<TJ(MAX) =125°C

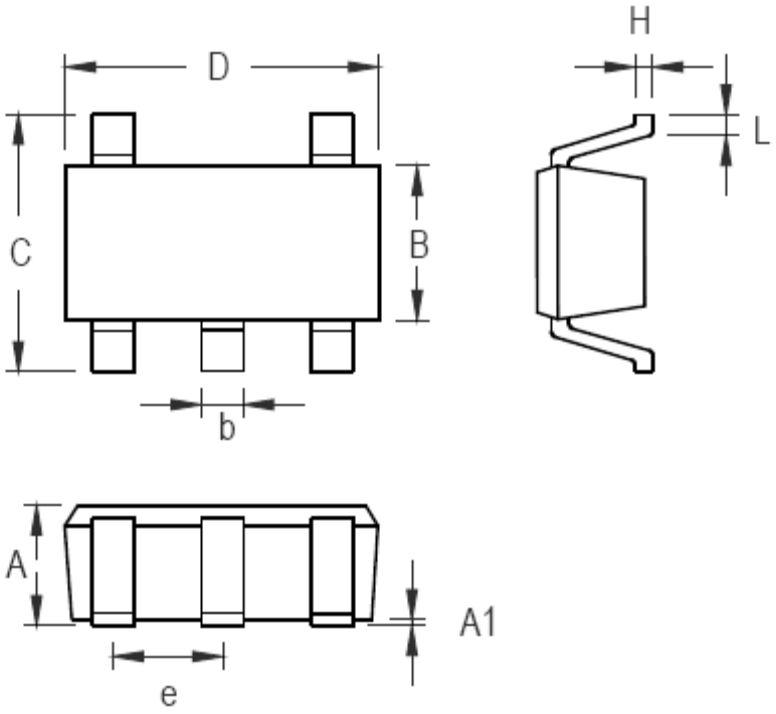
For this operating condition, TJ is lower than the absolute maximum operating junction temperature,125°C, so it is safe to use the BL9162 in this configuration.

Layout considerations

To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the PCB be designed with separate ground planes for VIN and VOUT, with each ground plane connected only at the GND pin of the device.

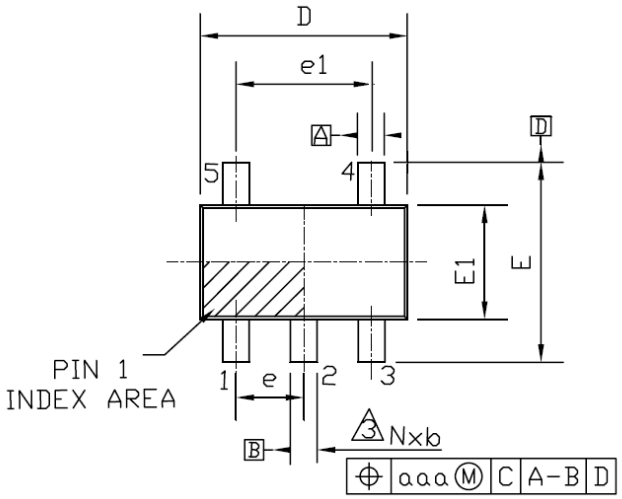
Package Description

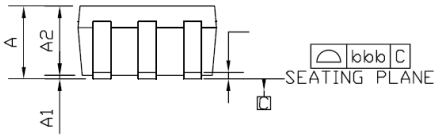
SOT23-5

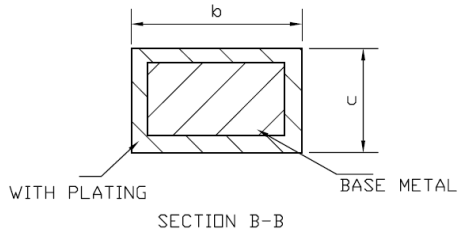


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.889	1.295	0.035	0.051
A1	0.000	0.152	0.000	0.006
B	1.397	1.803	0.055	0.071
b	0.356	0.559	0.014	0.022
C	2.591	2.997	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

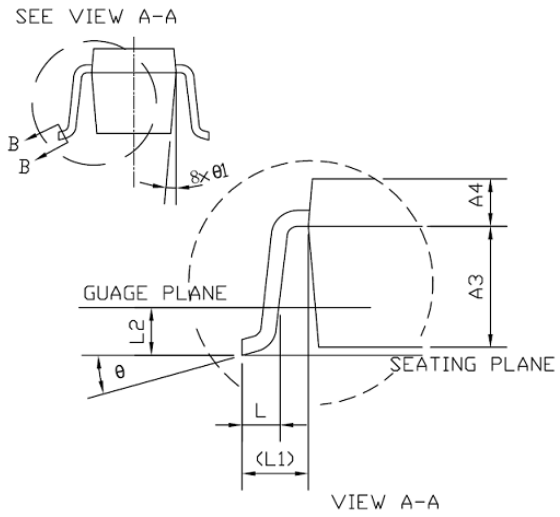
SC70-5







COMMON DIMENSION			
SYMBOL	IN MILLIMETERS		
	MIN	NOMAL	MAX
A	0.80	–	1.10
A1	0	–	0.10
A2	0.80	0.90	1.00
A3	0.47	0.52	0.57
A4	0.33	0.38	0.43
b	0.15	–	0.30
c	0.10	–	0.25
D	1.85	2.00	2.20
e	0.65 BSC		
e1	1.30 BSC		
E	1.80	2.10	2.40
E1	1.15	1.25	1.35
L	0.10	–	0.45
L1	0.42 REF.		
L2	0.20 BSC		
θ	0°	4°	30°
θ1	4°	–	12°
aaa	0.10		
bbb	0.10		



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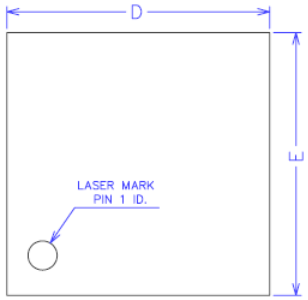
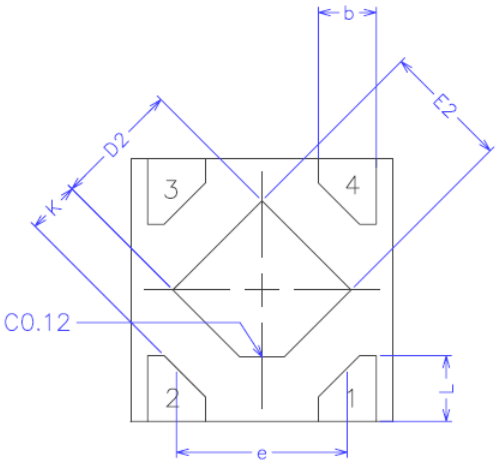
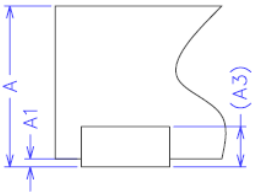
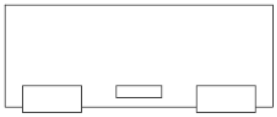


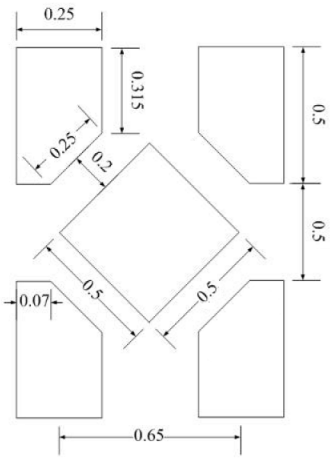


COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.34	0.37	0.40
A1	0.00	0.02	0.05
A3		0.100REF	
b	0.17	0.22	0.27
D	0.95	1.00	1.05
E	0.95	1.00	1.05
D2	0.43	0.48	0.53
E2	0.43	0.48	0.53
L	0.20	0.25	0.30
e	–	0.65	–
K	0.15	–	–







RECOMMENDED LAND PATTERN (Unit: mm)

单击下面可查看定价，库存，交付和生命周期等信息

>>BELLING(上海贝岭)