



TISP4015L1AJ, TISP4030L1AJ, TISP4040L1AJ
TISP4015L1BJ, TISP4030L1BJ, TISP4040L1BJ

**VERY LOW VOLTAGE
BIDIRECTIONAL THYRISTOR OVERVOLTAGE PROTECTORS**

TISP40xxL1AJ/BJ VLV Overvoltage Protectors

Low Capacitance

'4015.....	28 pF
'4030.....	27 pF
'4040.....	23 pF

Digital Line Signal Level Protection

- ISDN
- xDSL

Safety Extra Low Voltage, SELV, values

Device	V _{DRM} V	V _(BO) V
'4015	± 8	± 15
'4030	± 15	± 30
'4040	± 25	± 40

30 A "L" Series specified for:

- ITU-T recommendations K.20, K.45, K.21
- FCC Part 68 and GR-1089-CORE

Wave Shape	Standard	I _{TSP} A
2/10 μs	GR-1089-CORE	150
8/20 μs	IEC 61000-4-5	120
10/160 μs	FCC Part 68	65
10/700 μs	ITU-T K.20/45/21 FCC Part 68	45
10/560 μs	FCC Part 68	35
10/1000 μs	GR-1089-CORE	30

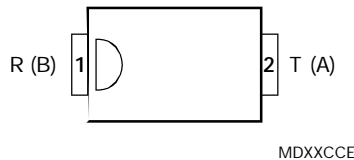
Available in SMA and SMB Packages
SMA Saves 25 % Placement Area Over SMB

How to Order

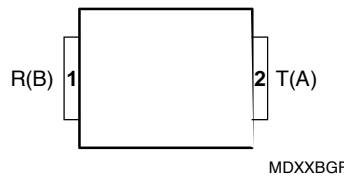
Device	Package	Carrier	Order As
TISP40xxL1	SMA/DO-214AC J-Bend (AJ)	Embossed Tape Reeled (R)	TISP40xxL1AJR-S
	SMB/DO-214AA J-Bend (BJ)		TISP40xxL1BJR-S

Insert xx value corresponding to protection voltages of 15 V, 30 V and 40 V.

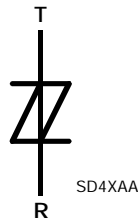
SMA Package (Top View)



SMB Package (Top View)



Device Symbol



Terminals T and R correspond to the alternative line designators of A and B

Additional Information

Click these links for more information:



[PRODUCT SELECTOR](#) [TECHNICAL LIBRARY](#) [INVENTORY](#) [SAMPLES](#) [CONTACT](#)

Agency Recognition

Description	
UL	File Number: E215609

..... **UL Recognized Component**

Description

These devices are designed to limit overvoltages on digital telecommunication lines. Overvoltages are normally caused by a.c. power system or lightning flash disturbances which are induced or conducted on to the telephone line. A single device provides 2-point protection and is typically used for the protection of transformer windings and low voltage electronics.

The protector consists of a symmetrical voltage-triggered bidirectional thyristor. Overvoltages are initially clipped by breakdown clamping until the voltage rises to the breakover level, which causes the device to crowbar into a low-voltage on-state condition. This low-voltage on state causes the current resulting from the overvoltage to be safely diverted through the device. The device switches off when the diverted current falls below the holding current value.



Asia-Pacific: Tel: +886-2 2562-4117 • Email: asiacus@bourns.com

EMEA: Tel: +36 88 885 877 • Email: eurocus@bourns.com

The Americas: Tel: +1-951 781-5500 • Email: americus@bourns.com

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*RoHS Directive 2015/863, Mar 31, 2015 and Annex.

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WARNING Cancer and Reproductive Harm
www.P65Warnings.ca.gov

TISP40xxL1AJ/BJ VLV Overvoltage Protectors

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Absolute Maximum Ratings, $T_A = 25\text{ }^\circ\text{C}$ (Unless Otherwise Noted)

Rating	Symbol	Value	Unit
Repetitive peak off-state voltage	V_{DRM}	'4015 ± 8 '4030 ± 15 '4040 ± 25	V
Non-repetitive peak on-state pulse current (see Notes 1 and 2) 2/10 μs (Telcordia GR-1089-CORE, 2/10 μs voltage wave shape) 8/20 μs (IEC 61000-4-5, combination wave generator, 1.2/50 voltage, 8/20 current) 10/160 μs (FCC Part 68, 10/160 μs voltage wave shape) 5/310 μs (ITU-T K.20/45/21, 10/700 μs voltage wave shape) 5/320 μs (FCC Part 68, 9/720 μs voltage wave shape) 10/560 μs (FCC Part 68, 10/560 μs voltage wave shape) 10/1000 μs (Telcordia GR-1089-CORE, 10/1000 μs voltage wave shape)	I_{TSP}	± 150 ± 120 ± 65 ± 45 ± 45 ± 35 ± 30	A
Non-repetitive peak on-state current (see Notes 1 and 2) 20 ms (50 Hz) full sine wave 16.7 ms (60 Hz) full sine wave 0.2 s 50 Hz/60 Hz a.c. 2 s 50 Hz/60 Hz a.c. 1000 s 50 Hz/60 Hz a.c.	I_{TSM}	20 22 13 5 1.8	A
Initial rate of rise of current (2/10 waveshape)	di/dt	130	A/ μs
Maximum junction temperature	T_{JM}	150	$^\circ\text{C}$
Storage temperature range	T_{stg}	-65 to +150	$^\circ\text{C}$

NOTES: 1. Initially, the device must be in thermal equilibrium with $T_J = 25\text{ }^\circ\text{C}$.
 2. The surge may be repeated after the device returns to its initial conditions.

Electrical Characteristics, $T_A = 25\text{ }^\circ\text{C}$ (Unless Otherwise Noted)

Parameter	Test Conditions	Min	Typ	Max	Unit
I_{DRM} Repetitive peak off-state current	$V_D = V_{\text{DRM}}$			± 5	μA
$V_{(\text{BO})}$ Breakover voltage	$di/dt = \pm 0.8\text{ A/ms}$	'4015 '4030 '4040		± 15 ± 30 ± 40	V
$V_{(\text{BO})}$ Impulse breakover voltage	$dv/dt = \pm 1000\text{ V}/\mu\text{s}$, Linear voltage ramp, Maximum ramp value = $\pm 500\text{ V}$ $di/dt = \pm 5\text{ A}/\mu\text{s}$, Linear current ramp, Maximum ramp value = $\pm 10\text{ A}$	'4015 '4030 '4040		± 34 ± 50 ± 63	V
$I_{(\text{BO})}$ Breakover current	$di/dt = \pm 0.8\text{ A/ms}$			± 0.8	A
I_D Off-state current	$V_D = \pm 6\text{ V}$ $V_D = \pm 13\text{ V}$ $V_D = \pm 22\text{ V}$	'4015 '4030 '4040		± 2	μA
I_H Holding current	$I_T = \pm 5\text{ A}$, $di/dt = \pm 30\text{ mA/ms}$	± 50			mA

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TISP40xxL1AJ/BJ VLV Overvoltage Protectors

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Electrical Characteristics, $T_A = 25\text{ }^\circ\text{C}$ (Unless Otherwise Noted)

Parameter	Test Conditions	Min	Typ	Max	Unit
C_{off} Off-state capacitance	$f = 1\text{ MHz}, V_d = 1\text{ V rms}, V_D = 0$	'4015	28	36	pF
		'4030	27	35	
		'4040	23	29	
	$f = 1\text{ MHz}, V_d = 1\text{ V rms}, V_D = 1\text{ V}$	'4015	25	33	
		'4030	24	31	
		'4040	20	26	
	$f = 1\text{ MHz}, V_d = 1\text{ V rms}, V_D = 2\text{ V}$	'4015	23	30	
		'4030	22	29	
		'4040	18	24	

Thermal Characteristics

Parameter	Test Conditions	Min	Typ	Max	Unit
$R_{\theta JA}$ Junction to free air thermal resistance	EIA/JESD51-3 PCB, $I_T = I_{TSM(1000)}$, SMA			125	$^\circ\text{C/W}$
	$T_A = 25\text{ }^\circ\text{C}$, (see Note 3) SMB			120	
	265 mm x 210 mm populated line card, SMA		60		
	4-layer PCB, $I_T = I_{TSM(1000)}$, $T_A = 25\text{ }^\circ\text{C}$ SMB		55		

NOTE 3: EIA/JESD51-2 environment and PCB has standard footprint dimensions connected with 5 A rated printed wiring track widths.

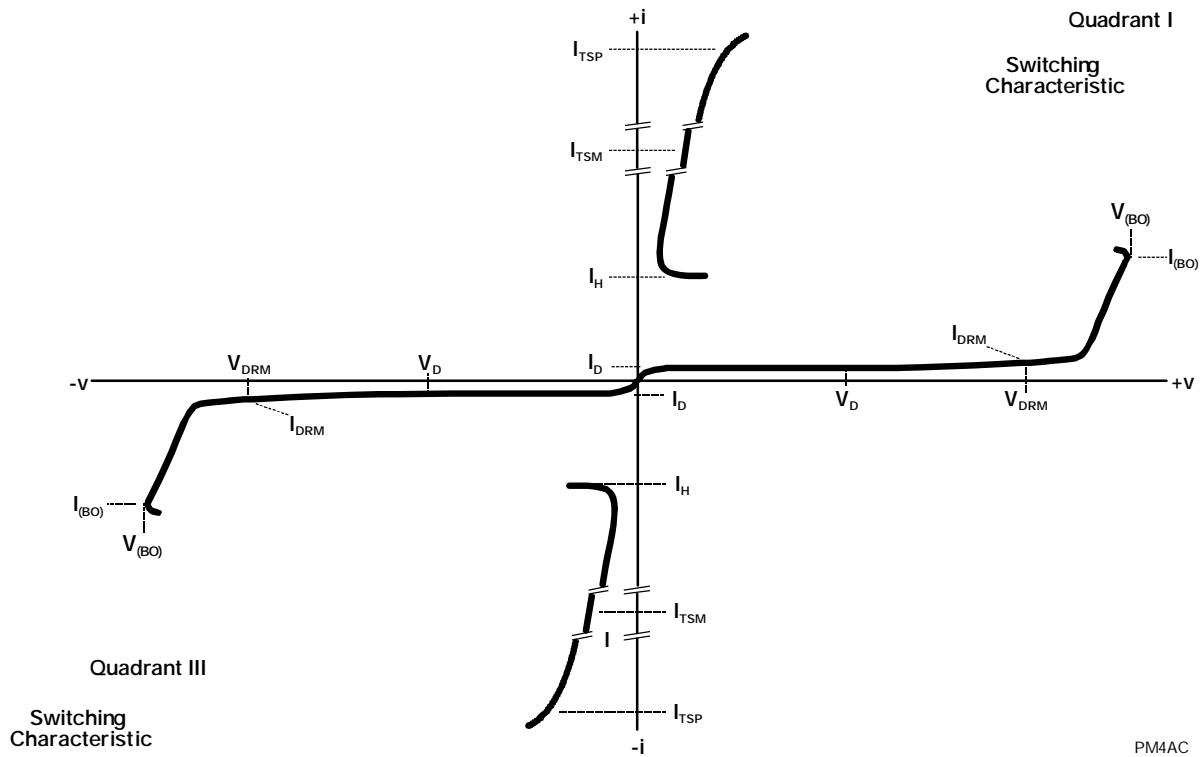
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Parameter Measurement Information



PM4AC

Figure 1. Voltage-Current Characteristic for T and R Terminals
All Measurements are Referenced to the R Terminal

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Typical Characteristics

**OFF-STATE CURRENT
vs
JUNCTION TEMPERATURE**

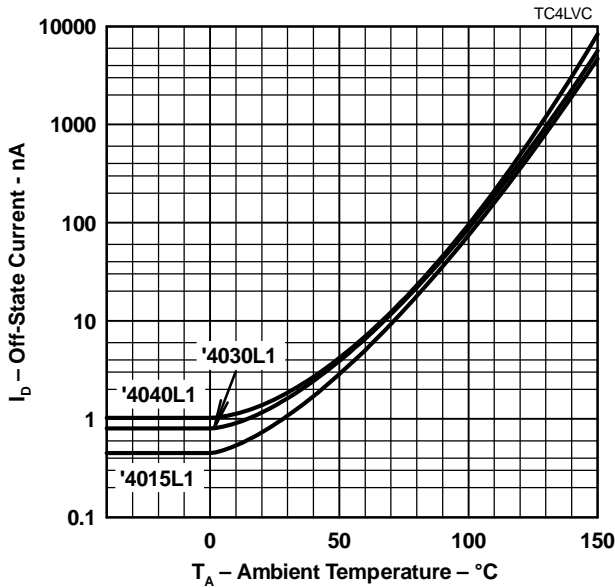


Figure 2.

**NORMALIZED BREAKOVER VOLTAGE
vs
JUNCTION TEMPERATURE**

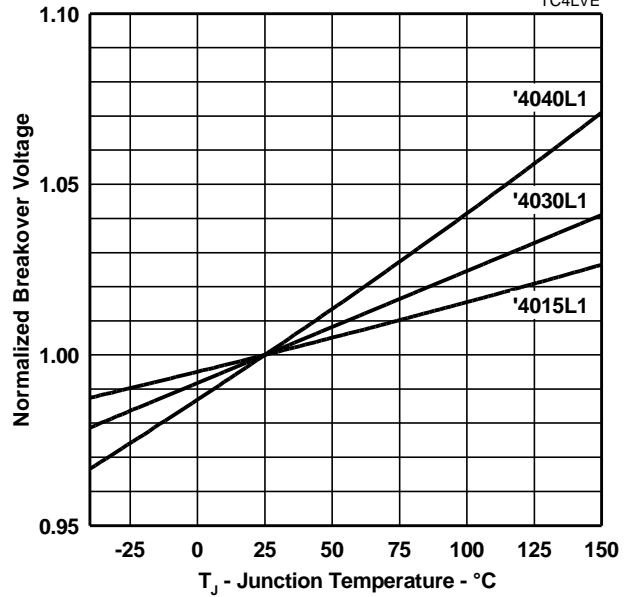


Figure 3.

**ON-STATE CURRENT
vs
ON-STATE VOLTAGE**

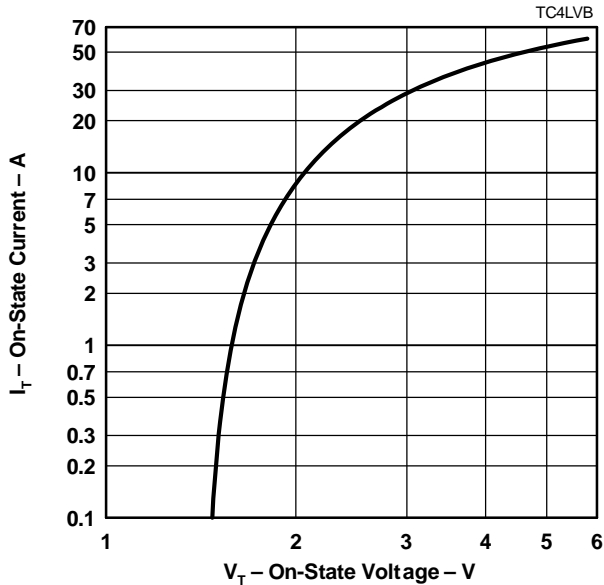


Figure 4.

**NORMALIZED HOLDING CURRENT
vs
JUNCTION TEMPERATURE**

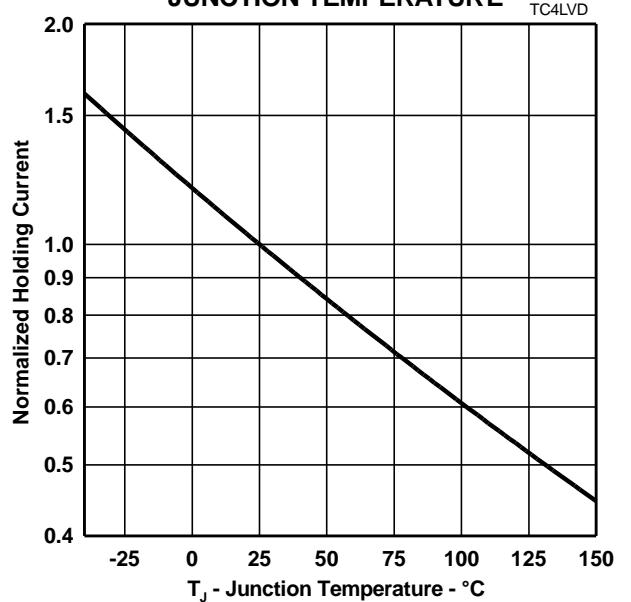


Figure 5.

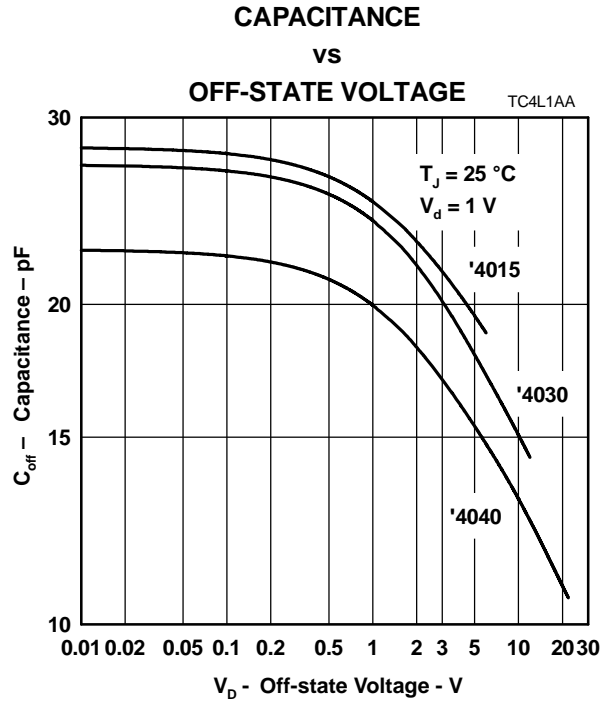
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Typical Characteristics



Rating and Thermal Information

NON-REPETITIVE PEAK ON-STATE CURRENT
VS
CURRENT DURATION

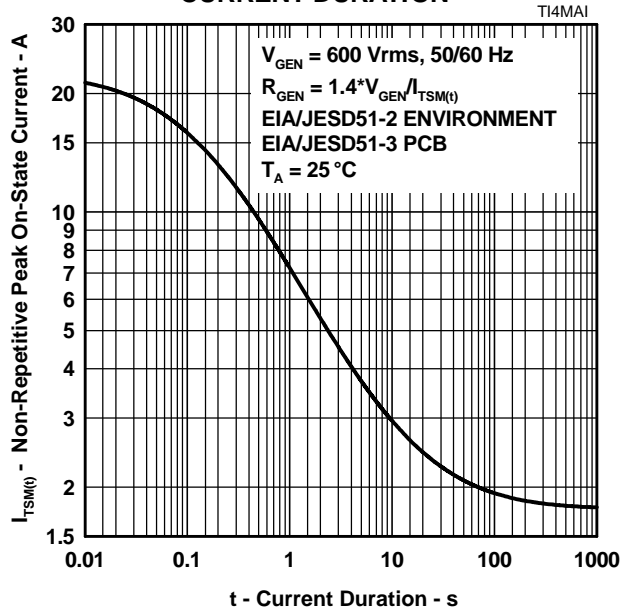


Figure 7.

V_{DRM} DERATING FACTOR

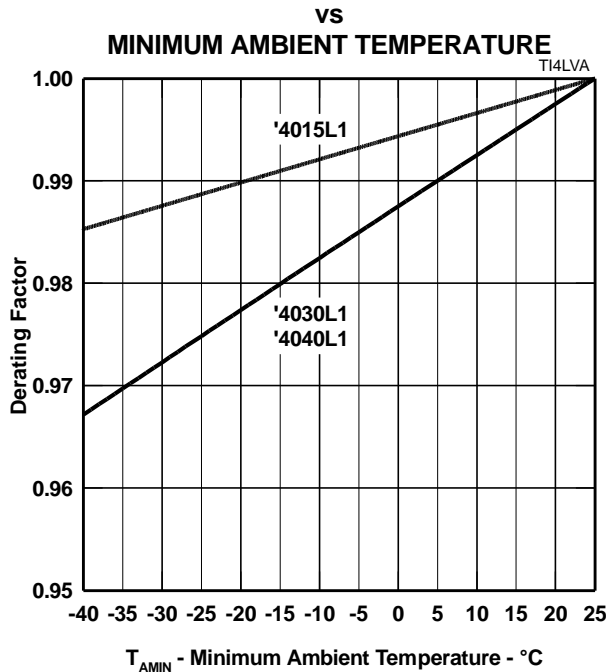


Figure 8.

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APPLICATIONS INFORMATION

Transformer Protection

The inductance of a transformer winding reduces considerably when the magnetic core material saturates. Saturation occurs when the magnetizing current through the winding inductance exceeds a certain value. It should be noted that this is a different current to the transformed current component from primary to secondary. The standard inductance-current relationship is:

$$E = -\left(L \frac{di}{dt}\right)$$

where:

L = unsaturated inductance value in H

di = current change in A

dt = time period in s for current change di

E = winding voltage in V

Rearranging this equation and working large Δ changes to saturation gives the useful circuit relationship of:

$$E \times \Delta t = L \times \Delta i$$

A transformer winding volt-second value for saturation gives the designer an idea of circuit operation under overvoltage conditions. The volt-second value is not normally quoted, but most manufacturers should provide it on request. A $50 \text{ V}\mu\text{s}$ winding will support rectangular voltage pulses of 50 V for 1 μs , 25 V for 2 μs , 1 V for 50 μs and so on. Once the transformer saturates, primary to secondary coupling will be lost and the winding resistance, RW, shunts the overvoltage protector, Th1 - see Figure 9. This saturated condition is a concern for long duration impulses and a.c. fault conditions because the current capability of the winding wire may be exceeded. For example, if the on-state voltage of the protector is 1 V and the winding resistance is 0.2Ω , the winding would bypass a current of $1/0.2 = 5 \text{ A}$, even though the protector was in the low voltage condition.

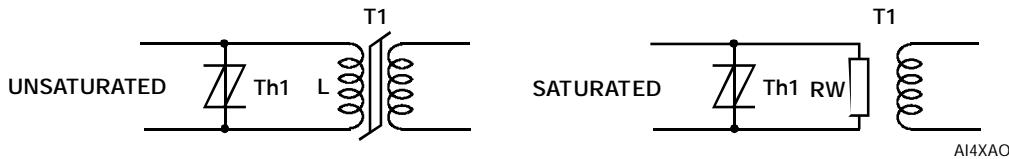


Figure 9. Transformer Saturation

Figure 10 shows a generic protection arrangement. Resistors R1 and R2, together with the overcurrent protection, prevent excessive winding current flow under a.c. conditions. Normally these resistors would only be needed for special cases, e.g. some T1/E1 designs. Alternatively, a split winding could be used with a single resistor connecting the windings. This resistor could be by-passed by a small capacitor to reduce signal attenuation.

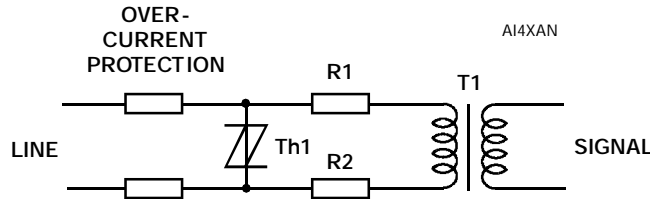


Figure 10. Transformer Winding Protection

Overcurrent protection upstream from the overvoltage protector can be fuse, PTC or thick film resistor based. For very high frequency circuits, fuse inductance due to spiral wound elements may need to be evaluated.

TISP® Device Voltage Selection

Normally, the working voltage value of the protector, V_{DRM} , would be chosen to be just greater than the peak signal amplitude over the equipment temperature range. This would give the lowest possible protection voltage, $V_{\text{(BO)}}$. This would minimize the peak voltage applied to the transformer winding and increase the time to core saturation.

In high frequency circuits, there are two further considerations. Low voltage protectors have a higher capacitance than high voltage protectors.

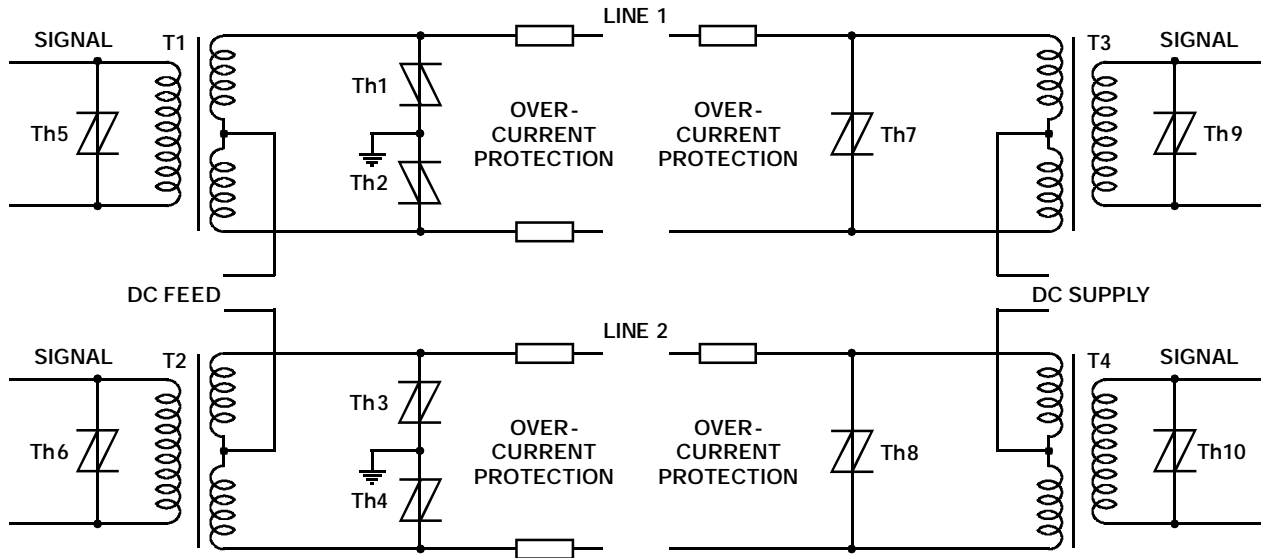
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4-Wire Digital Systems (Continued)



TRANSFORMER COUPLED FOUR-WIRE INTERFACE

Figure 12. 4-Wire System

For an HDSL d.c. feed voltage of 180 V or less and operation down to an ambient of -25 °C, the following Th1, Th2, Th3 and Th4 protectors are suitable: TISP4250M3 or TISP4250H3, TISP3250H3 (combines Th1 and Th2 or Th3 and Th4) and TISP7250H3 (combines Th1, Th2 and Th7 or Th3, Th4 and Th8). Possible overcurrent protection components are covered in the 2-wire digital systems clause.

For ISDN interfaces powered with ± 40 V (ETSI, ETS 300 012 1992) the following Th1, Th2, Th3 and Th4 protectors are suitable: TISP4070M3 or TISP4070H3 or TISP4070L3, TISP3070F3 or TISP3070H3 (combines Th1 and Th2 or Th3 and Th4) and TISP7070F3 or TISP7070H3 (combines Th1, Th2 and Th7 or Th3, Th4 and Th8). At the terminating adaptor, the Th7 and Th8 protectors do not "see" the d.c. feed voltage and should be selected to not clip the maximum signal level. Generally, the TISP40xxL1 series will be suitable.

Internal ISDN lines are not exposed to high stress levels and the chances of a.c. power intrusion are low (ETSI EN 300 386-2 1997). Accordingly, the equipment port protection needs are at a lower level than ports connected to outside lines.

Home Phone Networking

Using the existing house telephone wiring, home phone networking systems place the local network traffic in a high band above the POTS and ADSL (Asymmetrical Digital Subscriber Line) spectrum. Local network rates are 1 Mbps or more. To reject noise and harmonics, an in-line protection and 5 MHz to 10 MHz bandpass filter module is used for the equipment. These modules are available from magnetic component manufacturers (e.g. Bel Fuse Inc.) A typical circuit for the telephone line magnetics module is shown in Figure 13. Transformer T1 isolates the equipment from the house wiring. The isolated winding output is voltage limited by a very low-voltage protector, Th1. With a differential voltage of about 12 V peak to peak, the TISP4015L1 could be used for Th1. After filtering, connection is made to the differential transceiver of the processing IC.

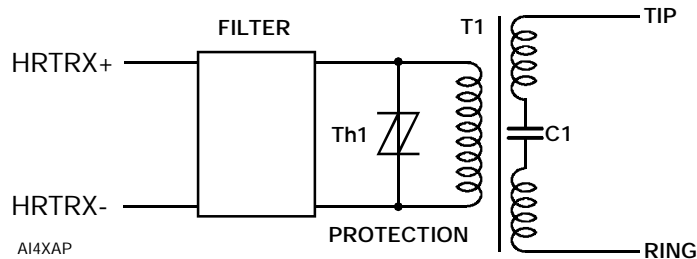


Figure 13. Home Phone Networking Isolation/filter/protection Circuit

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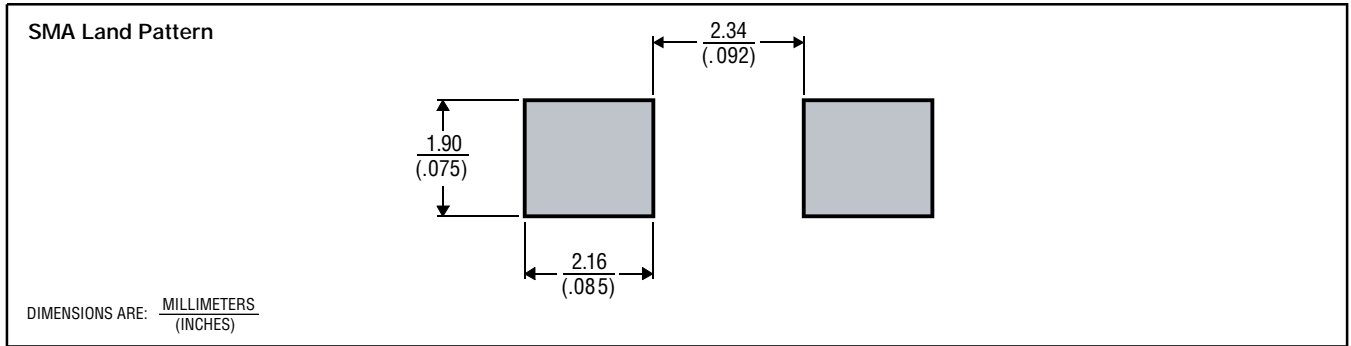
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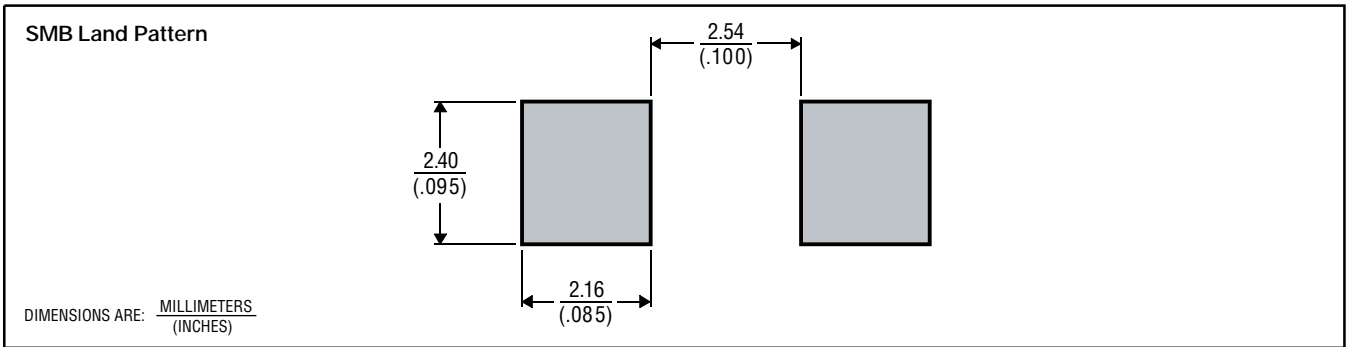
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MECHANICAL DATA

Recommended Printed Wiring Land Pattern Dimensions



MDXXBIC



MDXXBIB

Device Symbolization Code

Devices will be coded as below. As the device parameters are symmetrical, terminal 1 is not identified.

Device	Symbolization Code	Device	Symbolization Code
TISP4015L1AJ	4015L	TISP4015L1BJ	4015L1
TISP4030L1AJ	4030L	TISP4030L1BJ	4030L1
TISP4040L1AJ	4040L	TISP4040L1BJ	4040L1

Carrier Information

For production quantities, the carrier will be embossed tape reel pack. Evaluation quantities may be shipped in bulk pack or embossed tape.

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