TISP4070M3BJ THRU TISP4115M3BJ, TISP4125M3BJ THRU TISP4220M3BJ, TISP4240M3BJ THRU TISP4400M3BJ

BIDIRECTIONAL THYRISTOR OVERVOLTAGE PROTECTORS

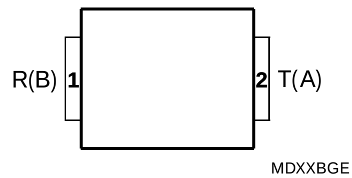
TISP4xxxM3BJ Overvoltage Protector Series

ITU-T K.20/21/44/45 rating
.... 4 kV 10/700, 100 A 5/310

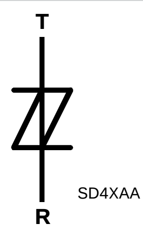
Ion-Implanted Breakdown Region
Precise and Stable Voltage
Low Voltage Overshoot under Surge

Device	V_{DRM} V	$V_{(BO)}$ V
‘4070	58	70
‘4080	65	80
‘4095	75	95
‘4115	90	115
‘4125	100	125
‘4145	120	145
‘4165	135	165
‘4180	145	180
‘4200	155	200
‘4220	160	220
‘4240	180	240
‘4250	190	250
‘4265	200	265
‘4290	220	290
‘4300	230	300
‘4350	275	350
‘4360	290	360
‘4395	320	395
‘4400	300	400

SMBJ Package (Top View)



Device Symbol



Terminals T and R correspond to the alternative line designators of A and B

Wave Shape	Standard	I_{TSP} A
2/10 μs	GR-1089-CORE	300
8/20 μs	IEC 61000-4-5	220
10/160 μs	FCC Part 68	120
10/700 μs	ITU-T K.20/21/45	100
10/560 μs	FCC Part 68	75
10/1000 μs	GR-1089-CORE	50

Additional Information

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Agency Recognition

	Description
UL	File Number: E215609

Low Differential Capacitance.. 39 pF max.

............UL Recognized Component

Description

These devices are designed to limit overvoltages on the telephone line. Overvoltages are normally caused by a.c. power system or lightning flash disturbances which are induced or conducted on to the telephone line. A single device provides 2-point protection and is typically used for the protection of 2-wire telecommunication equipment (e.g. between the Ring and Tip wires for telephones and modems). Combinations of devices can be used for multi-point protection (e.g. 3-point protection between Ring, Tip and Ground).

The protector consists of a symmetrical voltage-triggered bidirectional thyristor. Overvoltages are initially clipped by breakdown clamping until the voltage rises to the breakover level, which causes the device to crowbar into a low-voltage on state. This low-voltage on state causes the current resulting from the overvoltage to be safely diverted through the device. The high crowbar holding current helps prevent d.c. latchup as the diverted current subsides.

The TISP4xxxM3BJ range consists of nineteen voltage variants to meet various maximum system voltage levels (58 V to 320 V). They are guaranteed to voltage limit and withstand the listed international lightning surges in both polarities. These medium (M) current protection devices are in a plastic package SMBJ (JEDEC DO-214AA with J-bend leads) and supplied in embossed tape reel pack. For alternative voltage and holding current values, consult the factory. For higher rated impulse currents in the SMB package, the 100 A 10/1000 TISP4xxxH3BJ series is available.

How to Order

Device	Package	Carrier	Order As
TISP4xxxM3BJ	BJ (J-Bend DO-214AA/SMB)	Embossed Tape Reeled	TISP4xxxM3BJR-S

Insert xxx value corresponding to protection voltages of 070, 080, 095, 115, etc.

WARNING Cancer and Reproductive Harm
www.P65Warnings.ca.gov

NOVEMBER 1997 – REVISED JULY 2019
*RoHS Directive 2015/863, Mar 31, 2015 and Annex.
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Absolute Maximum Ratings, T_A = 25 °C (Unless Otherwise Noted)

Rating	Symbol	Value	Unit
Repetitive peak off-state voltage, (see Note 1)	V_{DRM}		V
‘4070		±58	
‘4080		±65	
‘4095		±75	
‘4115		±90	
‘4125		±100	
‘4145		±120	
‘4165		±135	
‘4180		±145	
‘4200		±155	
‘4220		±160	
‘4240		±180	
‘4250		±190	
‘4265		±200	
‘4290		±220	
‘4300		±230	
‘4350		±275	
‘4360		±290	
‘4395		±320	
‘4400		±300	
Non-repetitive peak on-state pulse current (see Notes 2, 3 and 4)	I_{TSP}		A
2/10 µs (GR-1089-CORE, 2/10 µs voltage wave shape)		300	
8/20 µs (IEC 61000-4-5,combination wave generator, 1.2/50 voltage, 8/20 current)		220	
10/160 µs (FCC Part 68, 10/160 µs voltage wave shape)		120	
5/200 µs (VDE 0433, 10/700 µs voltage wave shape)		110	
0.2/310 µs (I3124, 0.5/700 µs voltage wave shape)		100	
5/310 µ (ITU-T K.20/21/45, K.44 10/700 µs voltage wave shape)		100	
5/310 µs (FTZ R12, 10/700 µs voltage wave shape)		100	
10/560 µs (FCC Part 68, 10/560 µs voltage wave shape)		75	
10/1000 µs (GR-1089-CORE, 10/1000 µs voltage wave shape)		50	
Non-repetitive peak on-state current (see Notes 2, 3 and 5)	I_{TSM}		A
20 ms (50 Hz) full sine wave		30	
16.7 ms (60 Hz) full sine wave		32	
1000 s 50 Hz/60 Hz a.c.		2.1	
Initial rate of rise of on-state current, Exponential current ramp, Maximum ramp value < 100 A	di_T/dt	300	A/µs
Junction temperature	T_J	-40 to +150	°C
Storage temperature range	T_{stg}	-65 to +150	°C

NOTES: 1. See Applications Information and Figure 11 for voltage values at lower temperatures.
2. Initially, the TISP4xxxM3BJ must be in thermal equilibrium with T_J = 25 °C.
3. The surge may be repeated after the TISP4xxxM3BJ returns to its initial conditions.
4. See Applications Information and Figure 12 for current ratings at other temperatures.
5. EIA/JESD51-2 environment and EIA/JESD51-3 PCB with standard footprint dimensions connected with 5 A rated printed wiring track widths. See Figure 9 for the current ratings at other durations. Derate current values at -0.61 %/°C for ambient temperatures above 25 °C.

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Electrical Characteristics, T_A = 25 °C (Unless Otherwise Noted)

Parameter		Test Conditions		Min	Typ	Max	Unit
I_{DRM}	Repetitive peak off-state current	$V_D = V_{DRM}$	T_A = 25 °C T_A = 85 °C			±5 ±10	μA
$V_{(BO)}$	Breakover voltage	dv/dt = ±250 V/ms, R_{SOURCE} = 300 Ω	'4070 '4080 '4095 '4115 '4125 '4145 '4165 '4180 '4200 '4220 '4240 '4250 '4265 '4290 '4300 '4350 '4360 '4395 '4400			±70 ±80 ±95 ±115 ±125 ±145 ±165 ±180 ±200 ±220 ±240 ±250 ±265 ±290 ±300 ±350 ±360 ±395 ±400	V
$V_{(BO)}$	Impulse breakover voltage	dv/dt ≤ ±1000 V/μs, Linear voltage ramp, Maximum ramp value = ±500 V di/dt = ±20 A/μs, Linear current ramp, Maximum ramp value = ±10 A	'4070 '4080 '4095 '4115 '4125 '4145 '4165 '4180 '4200 '4220 '4240 '4250 '4265 '4290 '4300 '4350 '4360 '4395 '4400			±78 ±88 ±102 ±122 ±132 ±151 ±171 ±186 ±207 ±227 ±247 ±257 ±272 ±298 ±308 ±359 ±370 ±405 ±410	V
$I_{(BO)}$	Breakover current	dv/dt = ±250 V/ms, R_{SOURCE} = 300 Ω		±0.15		±0.6	A
V_T	On-state voltage	I_T = ±5 A, t_W = 100 μs				±3	V
I_H	Holding current	I_T = ±5 A, di/dt = +/-30 mA/ms		±0.15		±0.35	A
dv/dt	Critical rate of rise of off-state voltage	Linear voltage ramp, Maximum ramp value < 0.85V_{DRM}		±5			kV/μs
I_D	Off-state current	V_D = ±50 V	T_A = 85 °C			±10	μA

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Electrical Characteristics, T_A = 25 °C (Unless Otherwise Noted)

Parameter		Test Conditions		Min	Typ	Max	Unit
C_{off}	Off-state capacitance	f = 1 MHz, V_d = 1 V rms, V_D = 0	4070 thru ‘4115		83	100	pF
			‘4125 thru ‘4220		62	74	
			‘4240 thru ‘4400		50	60	
		f = 1 MHz, V_d = 1 V rms, V_D = -1 V	‘4070 thru ‘4115		78	94	
			‘4125 thru ‘4220		56	67	
			‘4240 thru ‘4400		45	54	
		f = 1 MHz, V_d = 1 V rms, V_D = -2 V	‘4070 thru ‘4115		72	87	
			‘4125 thru ‘4220		52	62	
			‘4240 thru ‘4400		42	50	
		f = 1 MHz, V_d = 1 V rms, V_D = -50 V	‘4070 thru ‘4115		36	44	
			‘4125 thru ‘4220		26	31	
			‘4240 thru ‘4400		19	22	
		f = 1 MHz, V_d = 1 V rms, V_D = -100 V	‘4125 thru ‘4220		21	25	
		(see Note 6)	‘4240 thru ‘4400		15	18	

NOTE 6: To avoid possible voltage clipping, the ‘4125 is tested with V_D = -98 V.

Thermal Characteristics

Parameter		Test Conditions	Min	Typ	Max	Unit
$R_{\theta JA}$	Junction to free air thermal resistance	EIA/JESD51-3 PCB, $I_T = I_{TSM(1000)}$, T_A = 25 °C, (see Note 7)			115	°C/W
		265 mm x 210 mm populated line card, 4-layer PCB, $I_T = I_{TSM(1000)}$, T_A = 25 °C		52		

NOTE 7: EIA/JESD51-2 environment and PCB has standard footprint dimensions connected with 5 A rated printed wiring track widths.

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Parameter Measurement Information

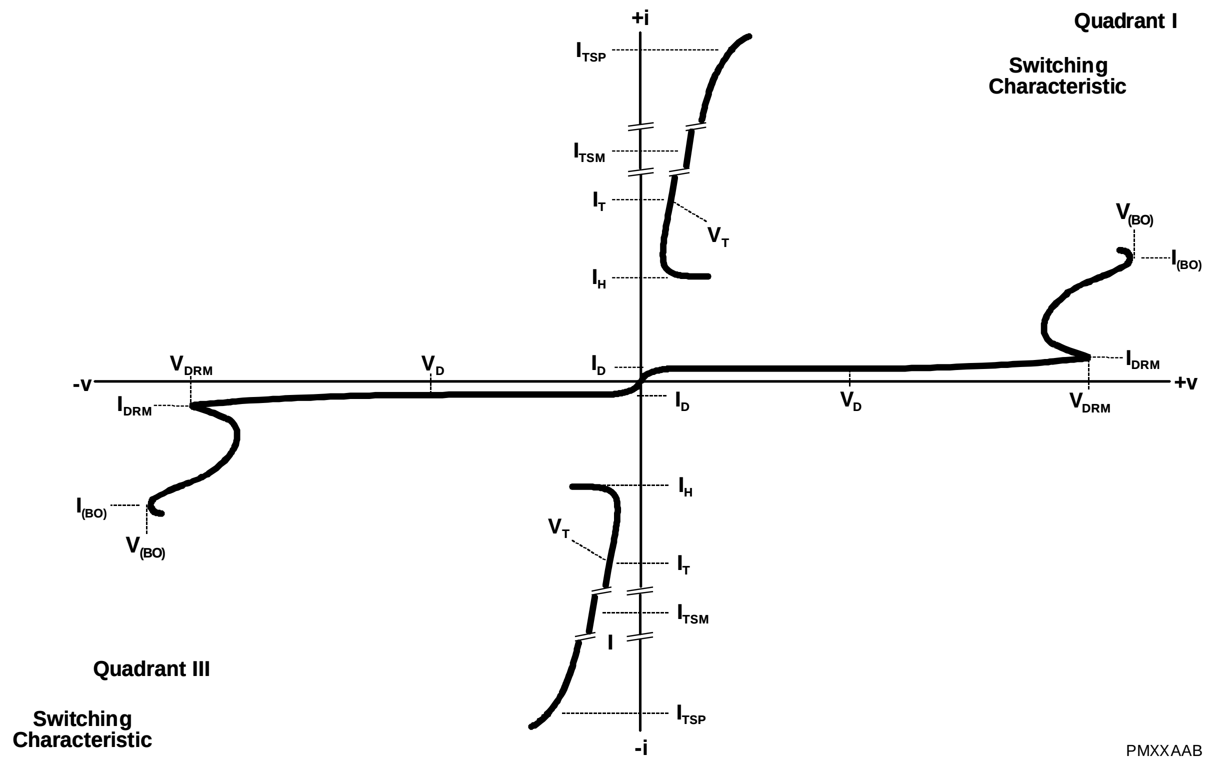

Figure 1. Voltage-Current Characteristic for T and R Terminals
All Measurements are Referenced to the R Terminal

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Typical Characteristics

OFF-STATE CURRENT vs JUNCTION TEMPERATURE

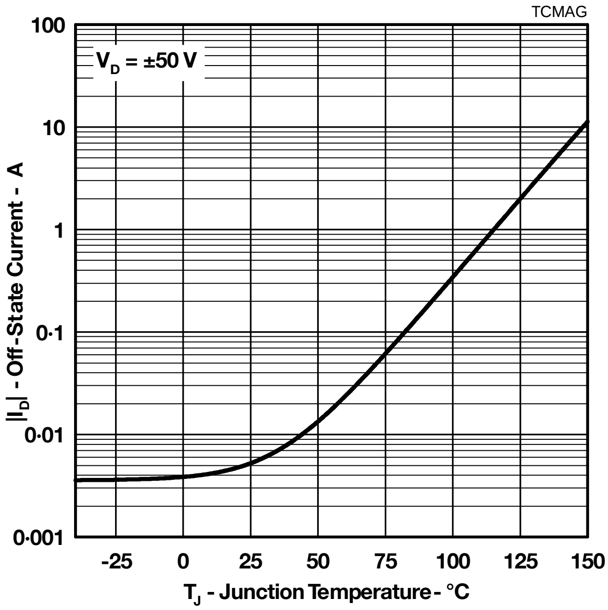

Figure 2.

NORMALIZED BREAKOVER VOLTAGE vs JUNCTION TEMPERATURE

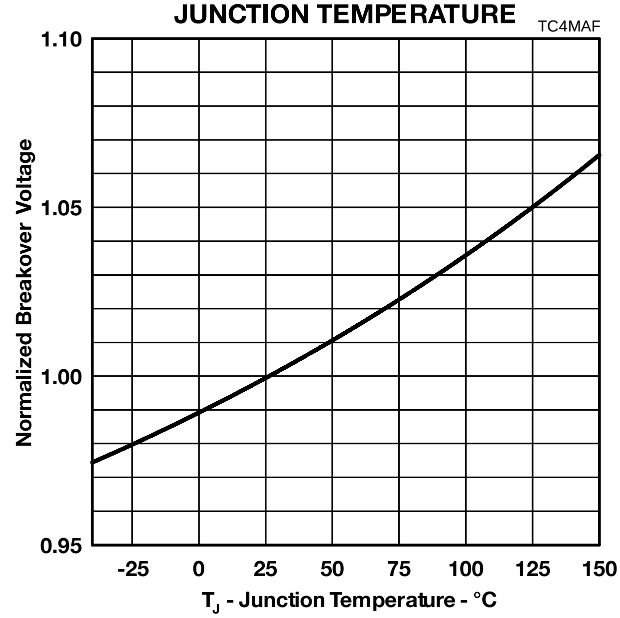

Figure 3.

ON-STATE CURRENT vs ON-STATE VOLTAGE

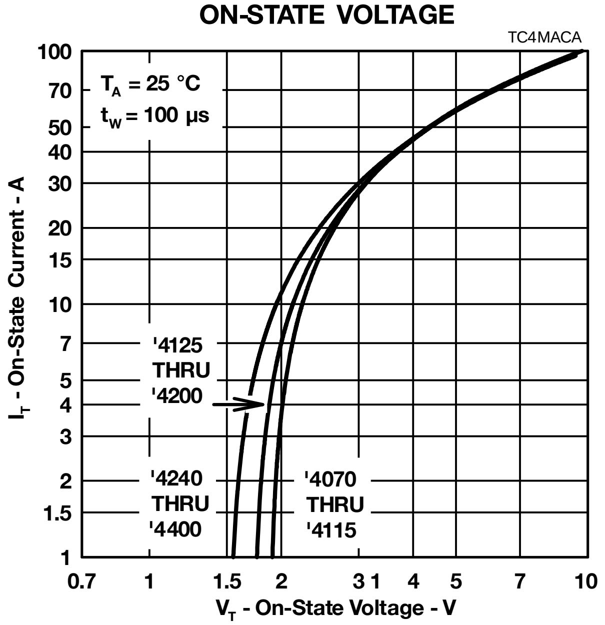

Figure 4.

NORMALIZED HOLDING CURRENT vs JUNCTION TEMPERATURE

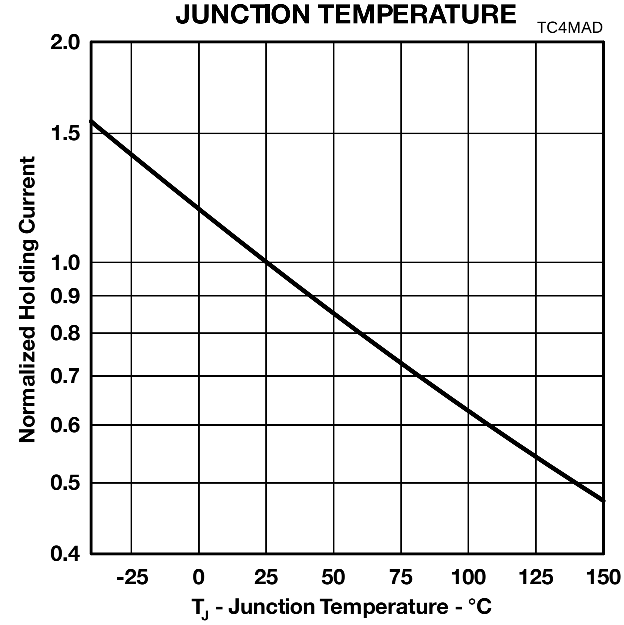

Figure 5.

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Typical Characteristics

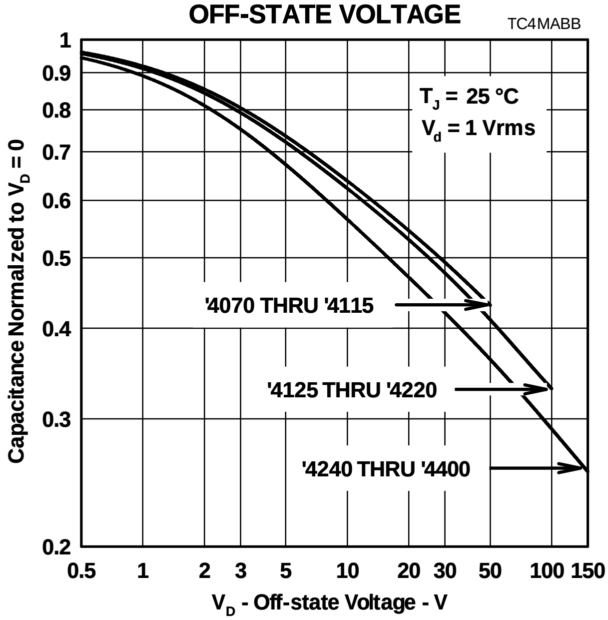

Figure 6.

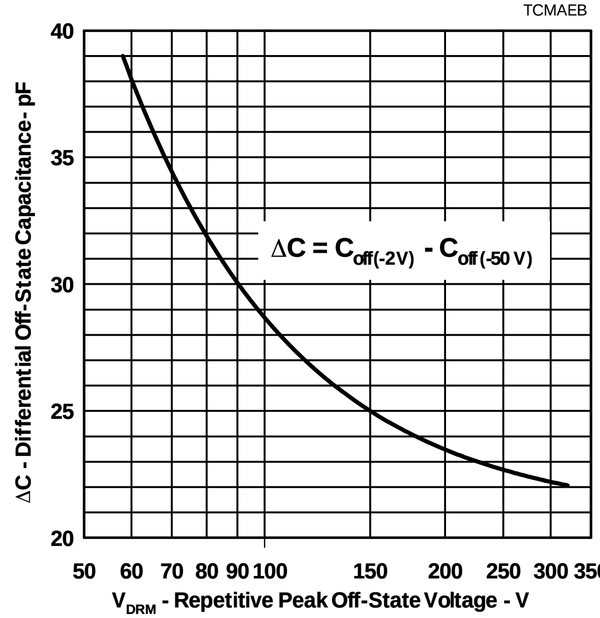

Figure 7.

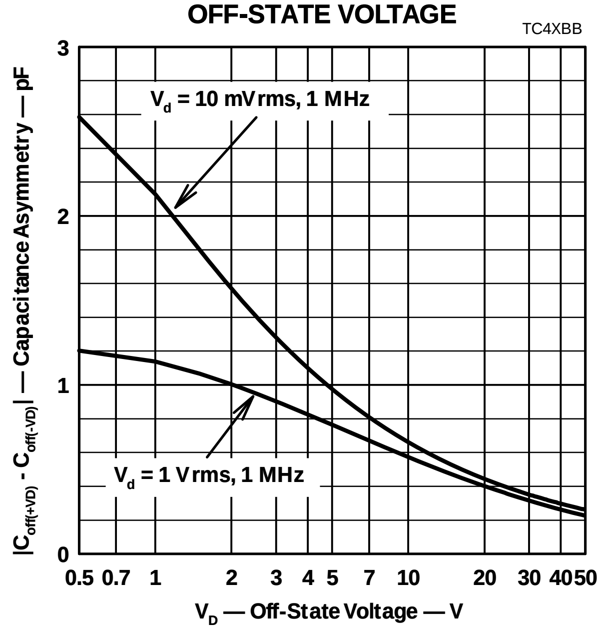

Figure 8.

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Rating and Thermal Information

NON-REPETITIVE PEAK ON-STATE CURRENT vs CURRENT DURATION

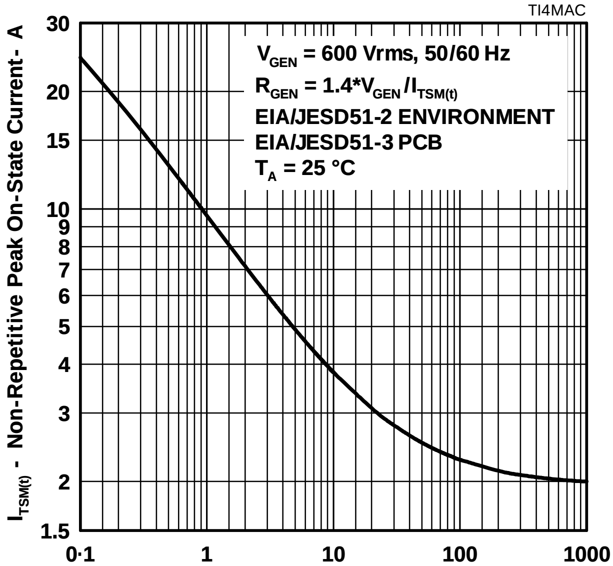

Figure 9.

THERMAL IMPEDANCE vs POWER DURATION

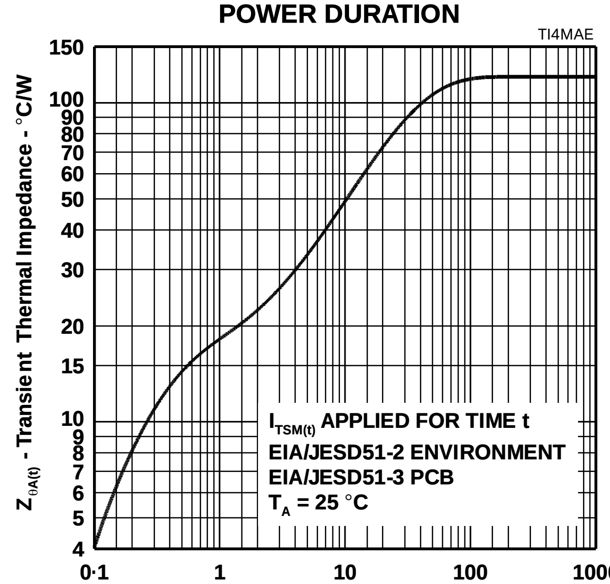

Figure 10.

V_{DRM} DERATING FACTOR vs MINIMUM AMBIENT TEMPERATURE

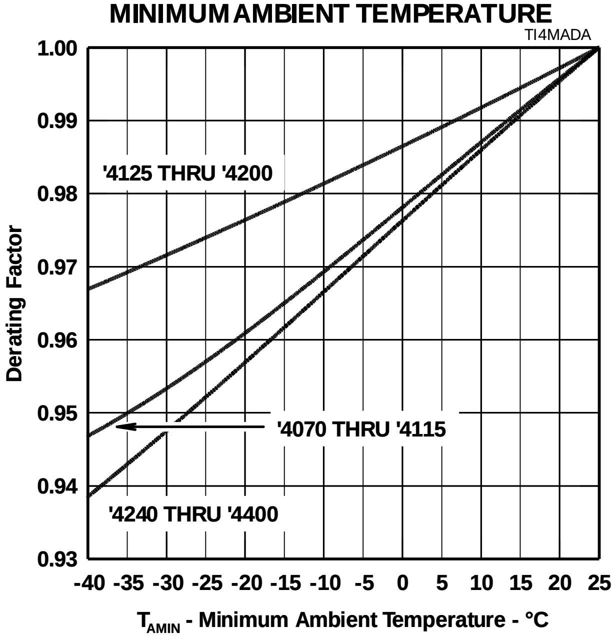

Figure 11.

IMPULSE RATING vs AMBIENT TEMPERATURE

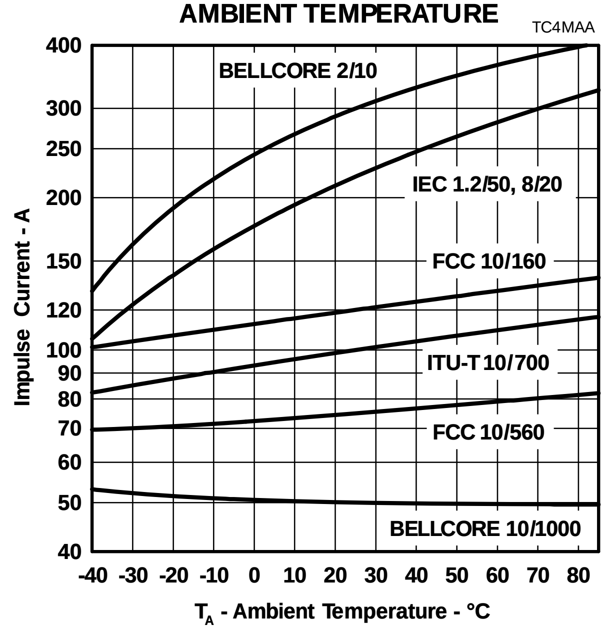

Figure 12.

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APPLICATIONS INFORMATION

Deployment

These devices are two terminal overvoltage protectors. They may be used either singly to limit the voltage between two conductors (Figure 13) or in multiples to limit the voltage at several points in a circuit (Figure 14).

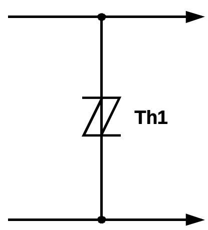

Figure 13. Two Point Protection

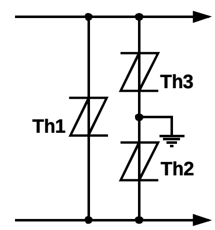

Figure 14. Multi-Point Protection

In Figure 13, protector Th1 limits the maximum voltage between the two conductors to ±V(BO). This configuration is normally used to protect circuits without a ground reference, such as modems. In Figure 14, protectors Th2 and Th3 limit the maximum voltage between each conductor and ground to the ±V(BO) of the individual protector. Protector Th1 limits the maximum voltage between the two conductors to its ±V(BO) value. If the equipment being protected has all its vulnerable components connected between the conductors and ground, then protector Th1 is not required.

Impulse Testing

To verify the withstand capability and safety of the equipment, standards require that the equipment is tested with various impulse wave forms. The table below shows some common values.

Standard	Peak Voltage Setting V	Voltage Wave Shape µs	Peak Current Value A	Current Wave Shape µs	TISP4XXXM3 25 °C Rating A	Series Resistance Ω
GR-1089-CORE	2500	2/10	500	2/10	300	11
	1000	10/1000	100	10/1000	50	
FCC Part 68 (March 1998)	1500	10/160	200	10/160	120	2x5.6
	800	10/560	100	10/560	75	3
	1500	9/720 †	37.5	5/320 †	100	0
	1000	9/720 †	25	5/320 †	100	0
I3124	1500	0.5/700	37.5	0.2/310	100	0
ITU-T K.20/K.21	1500 4000	10/700	37.5 100	5/310	100	0

† FCC Part 68 terminology for the waveforms produced by the ITU-T recommendation K.21 10/700 impulse generator

If the impulse generator current exceeds the protector's current rating, then a series resistance can be used to reduce the current to the protector's rated value to prevent possible failure. The required value of series resistance for a given waveform is given by the following calculations. First, the minimum total circuit impedance is found by dividing the impulse generator's peak voltage by the protector's rated current. The impulse generator's fictive impedance (generator's peak voltage divided by peak short circuit current) is then subtracted from the minimum total circuit impedance to give the required value of series resistance.

For the FCC Part 68 10/560 waveform, the following values result. The minimum total circuit impedance is 800/75 = 10.7 Ω and the generator's fictive impedance is 800/100 = 8 Ω. This gives a minimum series resistance value of 10.7 - 8 = 2.7 Ω. After allowing for tolerance, a 3 Ω ±10% resistor would be suitable. The 10/160 waveform needs a standard resistor value of 5.6 Ω per conductor. These would be R1a and R1b in Figure 16 and Figure 17. FCC Part 68 allows the equipment to be non-operational after the 10/160 (conductor to ground) and 10/560 (inter-conductor) impulses. The series resistor value may be reduced to zero to pass FCC Part 68 in a non-operational mode, e.g. Figure 15. For this type of design, the series fuse must open before the TISP4xxxM3 fails. For Figure 15, the maximum fuse i^2t is 2.3 A^2s. In some cases, the equipment will require verification over a temperature range. By using the rated waveform values from Figure 12, the appropriate series resistor value can be calculated for ambient temperatures in the range of -40 °C to 85 °C.

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AC Power Testing

The protector can withstand currents applied for times not exceeding those shown in Figure 9. Currents that exceed these times must be terminated or reduced to avoid protector failure. Fuses, PTC (Positive Temperature Coefficient) thermistors and fusible resistors are overcurrent protection devices which can be used to reduce the current flow. Protective fuses may range from a few hundred milliamperes to one ampere. In some cases, it may be necessary to add some extra series resistance to prevent the fuse opening during impulse testing. The current versus time characteristic of the overcurrent protector must be below the line shown in Figure 9. In some cases, there may be a further time limit imposed by the test standard (e.g. UL 1459 wiring simulator failure).

Capacitance

The protector characteristic off-state capacitance values are given for d.c. bias voltage, VD, values of 0, -1 V, -2 V and -50 V. Where possible values are also given for -100 V. Values for other voltages may be calculated by multiplying the VD = 0 capacitance value by the factor given in Figure 6. Up to 10 MHz, the capacitance is essentially independent of frequency. Above 10 MHz, the effective capacitance is strongly dependent on connection inductance. In many applications, such as Figure 16 and Figure 18, the typical conductor bias voltages will be about -2 V and -50 V. Figure 7 shows the differential (line unbalance) capacitance caused by biasing one protector at -2 V and the other at -50 V.

Figure 8 shows the typical capacitance asymmetry; the difference between the capacitance measured with a positive value of VD and the capacitance value when the polarity of VD is reversed. Capacitance asymmetry is an important parameter in ADSL systems where the protector often has no d.c. bias and the signal level is in the region of ±10 V.

Normal System Voltage Levels

The protector should not clip or limit the voltages that occur in normal system operation. For unusual conditions, such as ringing without the line connected, some degree of clipping is permissible. Under this condition, about 10 V of clipping is normally possible without activating the ring trip circuit.

Figure 11 allows the calculation of the protector VDRM value at temperatures below 25 °C. The calculated value should not be less than the maximum normal system voltages. The TISP4265M3BJ, with a VDRM of 200 V, can be used for the protection of ring generators producing 100 V rms of ring on a battery voltage of -58 V (Th2 and Th3 in Figure 18). The peak ring voltage will be 58 + 1.414*100 = 199.4 V. However, this is the open circuit voltage and the connection of the line and its equipment will reduce the peak voltage. In the extreme case of an unconnected line, clipping the peak voltage to 190 V should not activate the ring trip. This level of clipping would occur at the temperature when the VDRM has reduced to 190/200 = 0.95 of its 25 °C value. Figure 11 shows that this condition will occur at an ambient temperature of -28 °C. In this example, the TISP4265M3BJ will allow normal equipment operation provided that the minimum expected ambient temperature does not fall below -28 °C.

JESD51 Thermal Measurement Method

To standardize thermal measurements, the EIA (Electronic Industries Alliance) has created the JESD51 standard. Part 2 of the standard (JESD51-2, 1995) describes the test environment. This is a 0.0283 m^3 (1 ft^3) cube which contains the test PCB (Printed Circuit Board) horizontally mounted at the center. Part 3 of the standard (JESD51-3, 1996) defines two test PCBs for surface mount components; one for packages smaller than 27 mm on a side and the other for packages up to 48 mm. The SMBJ measurements used the smaller 76.2 mm x 114.3 mm (3.0 “ x 4.5 “) PCB. The JESD51-3 PCBs are designed to have low effective thermal conductivity (high thermal resistance) and represent a worst case condition. The PCBs used in the majority of applications will achieve lower values of thermal resistance, and can dissipate higher power levels than indicated by the JESD51 values.

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Typical Circuits

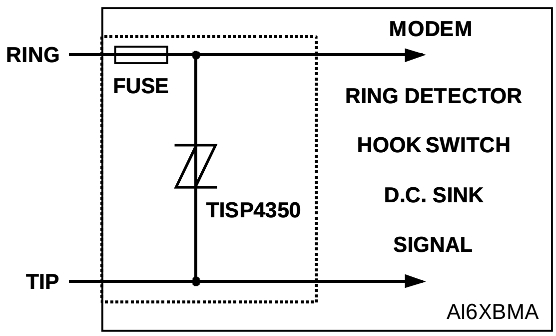

Figure 15. Modem Inter-Wire Protection

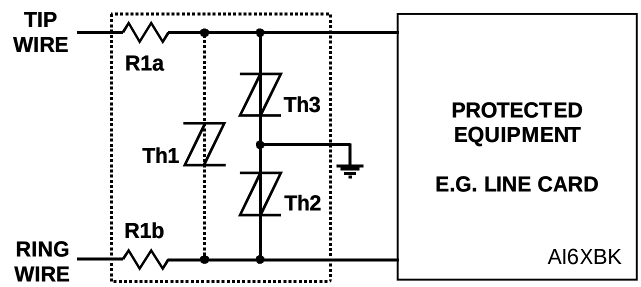

Figure 16. PROTECTION MODULE

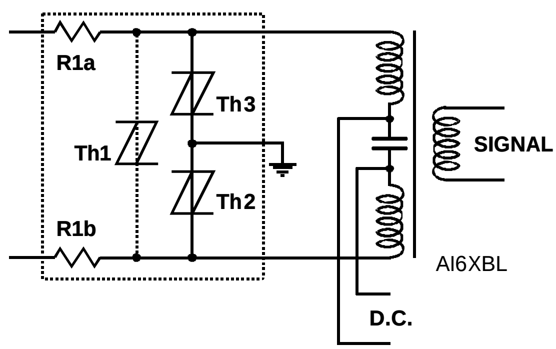

Figure 17. ISDN Protection

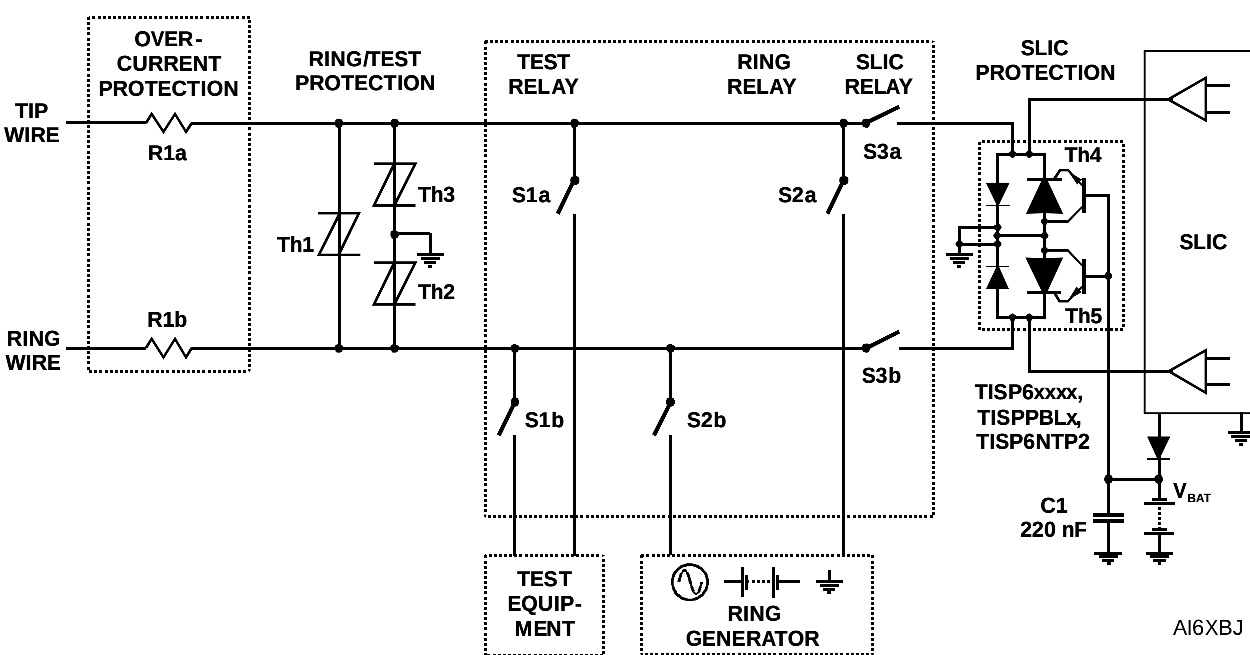

Figure 18. Line Card Ring/Test Protection

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Device Symbolization Code

Devices will be coded as below. As the device parameters are symmetrical, terminal 1 is not identified.

Device	Symbolization Code
TISP4070M3BJ	4070M3
TISP4080M3BJ	4080M3
TISP4095M3BJ	4095M3
TISP4115M3BJ	4115M3
TISP4125M3BJ	4125M3
TISP4145M3BJ	4145M3
TISP4165M3BJ	4165M3
TISP4180M3BJ	4180M3
TISP4200M3BJ	4200M3
TISP4220M3BJ	4220M3
TISP4240M3BJ	4240M3
TISP4250M3BJ	4250M3
TISP4265M3BJ	4265M3
TISP4290M3BJ	4290M3
TISP4300M3BJ	4300M3
TISP4350M3BJ	4350M3
TISP4360M3BJ	4360M3
TISP4395M3BJ	4395M3
TISP4400M3BJ	4400M3

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Asia-Pacific: Tel: +886-2 2562-4117 • Email: asiacus@bourns.com
EMEA: Tel: +36 88 885 877 • Email: eurocus@bourns.com
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www.bourns.com

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