DUAL-GATE UNIDIRECTIONAL OVERVOLTAGE PROTECTOR

BOURNS®

TISP83121D Unidirectional P & N-Gate Protector

Overvoltage Protection for Dual-Voltage Ringing SLICs
– Programmable Protection Configurations up to ±100 V
– Typically 5 Lines Protected by:
Two TISP83121D + Diode Steering Networks

High Surge Current
– 150 A, 10/1000 µs
– 250 A, 10/700 µs
– 500 A, 8/20 µs

Pin Compatible with the LCP3121
– 50 % more surge current
– Functional Replacement in Diode Steering Applications

Small Outline Surface Mount Package

Description

The TISP83121D is a dual-gate reverse-blocking unidirectional thyristor designed for the protection of dual-voltage ringing SLICs (Subscriber Line Interface Circuits) against overvoltages on the telephone line caused by lightning, a.c. power contact and induction.

The device chip is a four-layer NPNP silicon thyristor structure which has an electrode connection to every layer. For negative overvoltage protection the TISP83121D is used in a common anode configuration with the voltage to be limited applied to the cathode (K) terminal and the negative reference potential applied to the gate 1 (G1) terminal. For positive overvoltage protection the TISP83121D is used in a common cathode configuration with the voltage to be limited applied to the anode (A) terminal and the positive reference potential applied to the gate 2 (G2) terminal.

The TISP83121D is a unidirectional protector and to prevent reverse bias, requires the use of a series diode between the protected line conductor and the protector. Further, the gate reference supply voltage requires an appropriately poled series diode to prevent the supply from being shorted when the TISP83121D crowbars.

Under low level power cross conditions the TISP83121D gate current will charge the gate reference supply. If the reference supply cannot absorb the charging current its potential will increase, possibly to damaging levels. To avoid excessive voltage levels a clamp (zener or avalanche breakdown diode) may be added in shunt with the supply. Alternatively, a grounded collector emitter-follower may be used to reduce the charging current by the transistor's H_{FE} value.

This monolithic protection device is made with an ion-implanted epitaxial-planar technology to give a consistent protection performance and be virtually transparent to the system in normal operation.

Additional Information

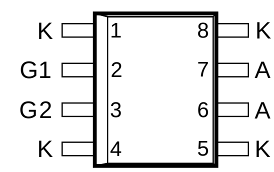
Click these links for more information:

PRODUCT SELECTOR | TECHNICAL LIBRARY | INVENTORY | SAMPLES | CONTACT

Agency Recognition

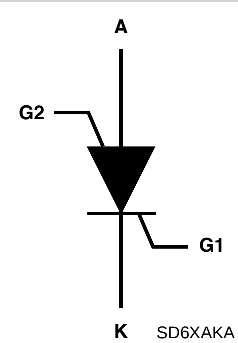
	Description
UL	File Number: E215609

8-SOIC Package (Top View)



For operation at the rated current values connect pins 1, 4, 5 and 8 together.

Device Symbol



.... **UL Recognized Component**

WARNING Cancer and Reproductive Harm
www.P65Warnings.ca.gov

FEBRUARY 1999 – REVISED JULY 2019
*RoHS Directive 2015/863, Mar 31, 2015 and Annex.
Specifications are subject to change without notice.
Users should verify actual device performance in their specific applications.
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How To Order

Device	Package	Carrier	Order As
TISP83121	D (8-pin Small-Outline)	R (Embossed Tape Reeled)	TISP83121DR-S

Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Repetitive peak off-state voltage, 0 °C to 70 °C	V_{DRM}	100	V
Non-repetitive peak on-state pulse current (see Notes 1 and 2)	I_{TSP}		A
10/1000 µs (GR-1089-CORE, open-circuit voltage wave shape 10/1000 µs)		150	
5/310 µs (CCITT K20/21, open-circuit voltage wave shape 7 kV, 10/700 µs)		250	
8/20 µs (ANSI C62.41, open-circuit voltage wave shape 1.2/50 µs)		500	
Non-repetitive peak on-state current, 50 Hz, halfwave rectified sinewave, (see Notes 1 and 2)	I_{TSM}		A
100 ms		22	
1 s		8	
900 s		3	
Junction temperature	T_J	-40 to +150	°C
Storage temperature range	T_{stg}	-65 to +150	°C

NOTES: 1. Initially the protector must be in thermal equilibrium with 0 °C < T_J < 70 °C. The surge may be repeated after the device returns to its initial conditions. For operation at the rated current value, pins 1, 4, 5 and 8 must be connected together.
2. Above 70 °C, derate linearly to zero at 150 °C lead temperature.

Electrical Characteristics, T_J = 25 °C (Unless Otherwise Noted)

Parameter		Test Conditions	Min	Typ	Max	Unit
I_D	Off-state current	V_d = 70 V, I_G = 0			1	µA
I_{DRM}	Repetitive peak off-state current	V_d = V_{DRM} = 100 V, I_G = 0, 0 °C to 70 °C			10	µA
I_H	Holding current	I_T = 1 A, di/dt = -1A/ms, T_J = 0 to 70 °C			300	mA
		T_J = 25 °C	90			mA
		T_J = 70 °C	60			mA
I_R	Reverse current	V_R = 0.3 V			1	mA
I_{G1T}	Gate G1 trigger current	I_T = +1 A, $t_{p(g)}$ = 20 µs			+200	mA
I_{G2T}	Gate G2 trigger current	I_T = +1 A, $t_{p(g)}$ = 20 µs			-180	mA
V_{G1T}	G1-K trigger voltage	I_T = +1 A, $t_{p(g)}$ = 20 µs			+1.8	V
V_{G2T}	G2-A trigger voltage	I_T = +1 A, $t_{p(g)}$ = 20 µs			-1.8	V
C_{AK}	Anode-cathode off-state capacitance	f = 1 MHz, V_d = 1 V rms, V_D = 5 V, I_G = 0 (see Note 3)			100	pF

NOTE 3: These capacitance measurements employ a three terminal capacitance bridge incorporating a guard circuit. The unmeasured device terminals are a.c. connected to the guard terminal of the bridge.

Thermal Characteristics

Parameter		Test Conditions	Min	Typ	Max	Unit
$R_{\theta JA}$	Junction to free air thermal resistance	T_A = 25 °C, EIA/JESD51-3 PCB, EIA/JESD51-2 environment, $I_T = I_{TSM(900)}$			105	°C/W

Parameter Measurement Information

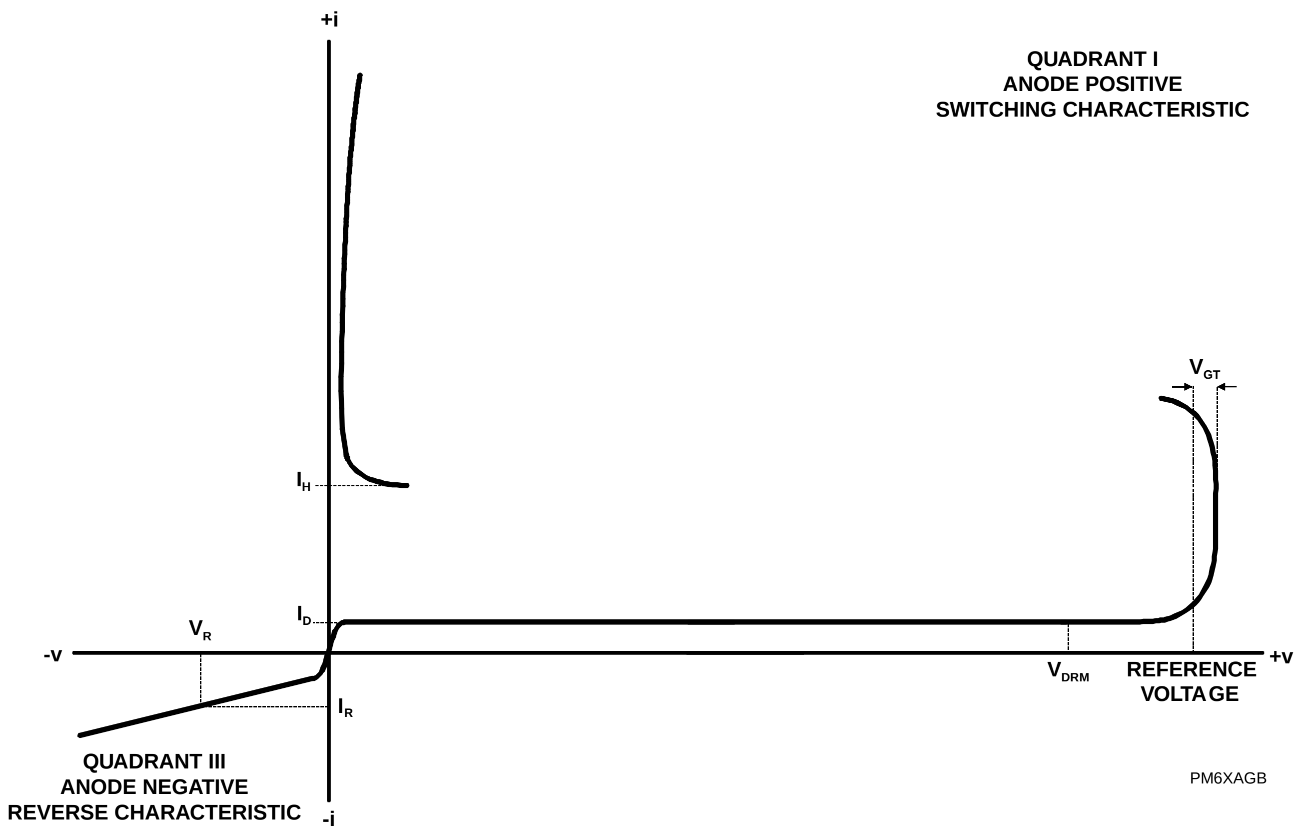

Figure 1. Voltage-Current Characteristic

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