BCT4157
Low-Voltage, 2.8Ω SPDT Analog Switch

GENERAL DESCRIPTION

The BCT4157 is a high-bandwidth, fast single-pole double-throw (SPDT) CMOS switch. It can be used as an analog switch or as a low-delay bus switch. Specified over a wide operating power supply voltage range, 1.65V to 5.5V, the BCT4157 has a maximum ON resistance of 5.1-ohms at 1.65V, 3.9-ohms at 2.3V & 2.85-ohms at 4.5V.

Break-before-make switching prevents both switches being enabled simultaneously. This eliminates signal disruption during switching.

The control input, S, tolerates input drive signals up to 5.5V, independent of supply voltage.

FEATURES

- CMOS Technology for Bus and Analog Applications
- Low ON Resistance: 2.8ohms @ 2.7V
- Wide VCC Range: 1.65V to 5.5V
- Rail-to-Rail Signal Range
- Control Input Overvoltage Tolerance: 5.5V min.
- High Off Isolation: 57dB at 10MHz
- 54dB (10MHz) Crosstalk Rejection Reduces Signal Distortion
- Break-Before-Make Switching
- High Bandwidth: 300 MHz
- Extended Industrial Temperature Range: –40°C to 85°C
- Improved Direct Replacement for NC7SB4157
- Packaging (Pb-free & Green available):

APPLICATIONS

Cell Phones
PDAs
Portable Instrumentation
Battery Powered Communications
Computer Peripherals

ORDERING INFORMATION

Ordering Code	Package Description	Temp Range	Top Marking	QTY/Reel
BCT4157EXT-TR	SC70-6L	–40°C to +85°C	ABG	3000
BCT4157ELT-TR	DFN 1.1x0.9-6L	–40°C to +85°C	ABG	3000

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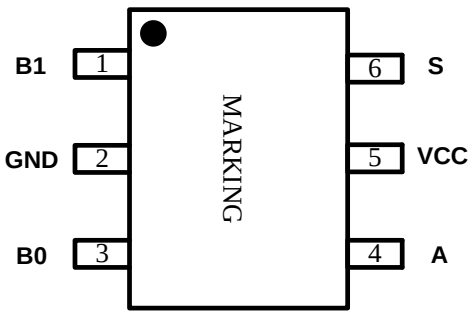
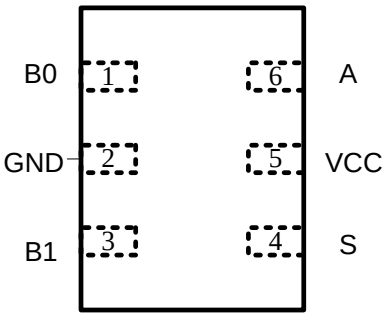
PIN CONFIGURATION (Top View)



BCT4157
SC70-6L



BCT4157
DFN1.1x0.9-6L

PIN DESCRIPTION

Pin		Name	Description
BCT4157 SC70	BCT4157 DFN1.1x0.9		
6	4	S	Logic Control
5	5	Vcc	Positive Power Supply
4	6	A	Common Output/Data Port
3	1	B0	Data Port (Normally Closed)
2	2	GND	Ground
1	3	B1	Data Port

Logic Function Table

Logic Input (S)	Function
0	B0 Connected to A
1	B1 Connected to A

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ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage V_{CC}.....–0.5V to +7V

DC Switch Voltage (V_S) (2).....–0.5V to V_{CC} +0.5V

DC Input Voltage (V_{IN}) (2).....–0.5V to +7.0V

DC V_{CC} or Ground Current (I_{CC}/I_{GND}).....±100mA
DC Output Current (V_{OUT}) 128mA
Storage Temperature Range (T_{STG})..... –65°C to +150°C
Junction Temperature under Bias (T_J) ..... 150°C
Junction Lead Temperature (T_L) (Soldering, 10 seconds) ..... 260°C
Power Dissipation (P_D) @ +85°C 180mW

RECOMMENDED OPERATING CONDITIONS(3)

Supply Voltage Operating (V_{CC}).....1.65V to 5.5V
Control Input Voltage (V_{IN}).....0V to V_{CC}
Switch Input Voltage (V_{IN}).....0V to V_{CC}
Output Voltage (V_{OUT}).....0V to V_{CC}
Operating Temperature (T_A).....–40°C to +85°C
Thermal Resistance (θJA).....350°C/W

Note 1:Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied.

Note 2:The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Note 3:Control input must be held HIGH or LOW; it must not float.

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DC ELECTRICAL CHARACTERISTICS (TA = - 40°C to +85°C)

Parameter	Description	Test Conditions	Supply Voltage	Temp (ºC)	Min.	Typ	Max.	Units
V_{IAR}	Analog Input Signal Range		V_{CC}	T_A = 25°C & –40°C to 85°C	0		V_{CC}	V
R_{ON}	ON Resistance(4)	I_{out} = 100mA, B_0 or B_1=1.5V	2.7V	T_A = 25°C		2.8	7.0	Ω
R_{ON}	ON Resistance(4)	I_{out} = 100mA, B_0 or B_1=1.5V	4.5V	T_A = 25°C		2.0	4.5	
ΔR_{ON}	ON Resistance Match Between Channels(4,5,6)	I_{out} = 100mA, B_0=B_1=1.5V	2.7V	T_A = 25°C			0.75	Ω
R_{ONF}	ON Resistance(4,5,7) Flatness	I(A) = -100mA; B0 or B1= 0V, 1.5V, 2.3V	2.7V	T_A = 25°C		1.5		Ω
R_{ONF}	ON Resistance(4,5,7) Flatness	I(A) = -100mA; B0 or B1= 0V, 1.5V, 3.0V,	4.5V	T_A = 25°C		0.5		Ω
V_{IH}	Input High Voltage	Logic High Level	V_{CC} = 1.65V to 1.95V	T_A = 25°C & –40°C to 85°C	1.5			V
			V_{CC} = 2.3V to 5.5V		1.7			
V_{IL}	Input Low Voltage	Logic Low Level	V_{CC} = 1.65V to 1.95V				0.5	V
			V_{CC} = 2.3V to 5.5V				0.8	

DC ELECTRICAL CHARACTERISTICS (TA = - 40°C to +85°C)

Parameter	Description	Test Conditions	Supply Voltage	Temp (ºC)	Min.	Typ	Max.	Units
I_{IN}	Input Leakage Current	0 ≤V_{IN} ≤5.5V	V_{CC} = 0V to 5.5V	T_A = 25°C			±0.1	µA
				T_A = –40°C to 85°C			±1.0	
I_{OFF}	OFF State Leakage Current	A=1V,4.5V, B0 or B1=4.5V, 1V	V_{CC} = 5.5V	T_A = 25°C	-2.0		2.0	
I_{CC}	Quiescent Supply Current	All channels ON or OFF, V_{IN} = V_{CC} or GND, I_{OUT} = 0	V_{CC} = 5.5V	T_A = 25°C			1	
				T_A = –40°C to 85°C			10	

Note 4: Measured by voltage drop between A and B pins at the indicated current through the device. ON resistance is determined by the lower of the voltages on two ports (A or B)
Note 5: Parameter is characterized but not tested in production.
Note 6: ΔR_{ON} = R_{ON} max – R_{ON} min. measured at identical V_{CC}, temperature and voltage levels.
Note 7: Flatness is defined as difference between maximum and minimum value of ON resistance over the specified range of conditions..
Note 8: Guaranteed by design.

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CAPACITANCE[12]

Parameter	Description	Test Conditions	Supply Voltage	Temp (ºC)	Min.	Typ	Max.	Units
C_{IN}	Control Input		V_{CC} = 5.0V	T_A = 25°C		2.3		pF
C_{IO-B}	For B Port, Switch OFF	f= 1 MHz[12]				6.5		
C_{IOA-ON}	For A Port, Switch ON					18.5		

SWITCH AND AC CHARACTERISTICS

Parameter	Description	Test Conditions	Supply Voltage	Temp (ºC)	Min.	Typ	Max.	Units
t_{PLH} t_{PHL}	Propagation Delay: A to Bn	See test circuit diagrams 1 and 2. V_I Open [10]	V_{CC}= 2.3V to 2.7V	T_A = 25°C & –40 to 85°C		1.2		ns
			V_{CC} = 3.0V to 3.6V			0.8		
			V_{CC}= 4.5V to 5.5V			0.3		
t_{PZL} t_{PZH}	Output Enable Turn ON Time: A to Bn	diagrams 1 & 2. See test circuit V_I = 2V_{CC} for T_{PZL}, V_I = 0V for t_{PZH}	V_{CC}= 1.65V to 1.95V	T_A = 25°C	7		23	
			V_{CC}= 2.3V to 2.7V		3.5		13	
			V_{CC}= 3.0V to 3.6V		2.5		6.9	
			V_{CC}= 4.5V to 5.5V		1.7		5.2	
t_{PZL} t_{PZH}	Output Enable Turn ON Time: A TO Bn	See test circuit diagrams 1 and 2. V_I = 2V_{CC} for T_{PZL}, V_I = 0V for t_{PZH}	V_{CC} = 2.5V	T_A = 25°C & –40 to 85°C			24	
			V_{CC} = 3.3V				14	
			V_{CC} = 3.0V to 3.6V				7.6	
			V_{CC} = 4.5V to 5.5V				5.7	

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Parameter	Description	Test Conditions	Supply Voltage	Temp (ºC)	Min.	Typ	Max.	Units
t_{PLZ} t_{PHZ}	Output Disable Turn OFF Time: A to Bn	See test circuit diagrams 1 and 2. V_I = 2V_{CC} for T_{PZL}, V_I = 0V for t_{PZH}	V_{CC} = 1.65V to 1.95V	T_A = 25°C	3		12.5	ns
			V_{CC} = 2.3V to 2.7V		2		7	
			V_{CC} = 3.0V to 3.6V		1.5		5	
			V_{CC} = 4.5V to 5.5V		0.8		3.5	
t_{PLZ} t_{PHZ}	Output Disable Turn OFF Time: A to Bn	See test circuit diagrams 1 and 2. V_I = 2V_{CC} for T_{PZL}, V_I = 0V for t_{PZH}	V_{CC} = 2.5V	T_A = –40 to 85°C			13	
			V_{CC} = 3.3V				7.5	
			V_{CC} = 3.0V to 3.6V				5.3	
			V_{CC} = 4.5V to 5.5V				3.8	
t_{BM}	Break Before Make Time	See test circuit diagram 9.(9)	V_{CC} = 2.5V	T_A = 25°C & –40 to 85°C	0.5			
			V_{CC} = 3.3V		0.5			
			V_{CC} = 3.0V to 3.6V		0.5			
			VCC = 4.5V to 5.5V		0.5			
Q	Charge Injection	C_L = 0.1nF, V_{GEN} = 0V, R_{GEN} = 0Ω. See test circuit 4.	V_{CC} = 5.0V	T_A = 25°C		7		pC
			VCC = 3.3V			3		
OIRR	Off Isolation	R_L = 50Ω, V_{GEN} = 0V, R_{GEN} = 0Ω. See test circuit 5. (11)	V_{CC} = 1.65V to 5.5V	T_A = 25°C		–57		dB
X_{TALK}	Crosstalk Isolation	See test circuit 6.	V_{CC} = 1.65V to 5.5V	T_A = 25°C		–54		
f_{3dB}	–3dB Bandwidth	See test circuit 9	V_{CC} = 1.65V to 5.5V	T_A = 25°C		300		MHz

Note 9: Guaranteed by design
Note 10: Guaranteed by design but not production tested. The device contributes no other propagation delay other than the RC delay of the switch ON resistance and the 50pF load capacitance, whne driven by an ideal voltage source with zero output impedance.
Note 11: Off Isolation = 20 Log10 [V_A / V_{Bn}] and is measured in dB.
Note 12: TA = 25°C, f = 1MHz. Capacitance is characterized but not tested in production.

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TEST CIRCUITS AND TIMING DIAGRAMS

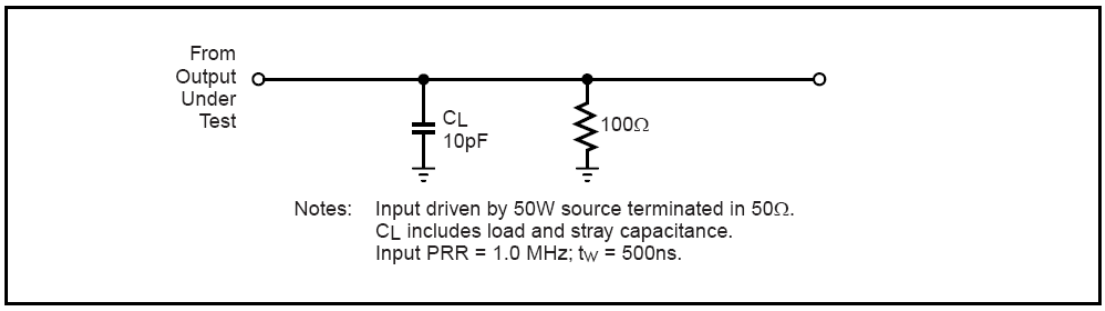

Figure 1. AC Test Circuit

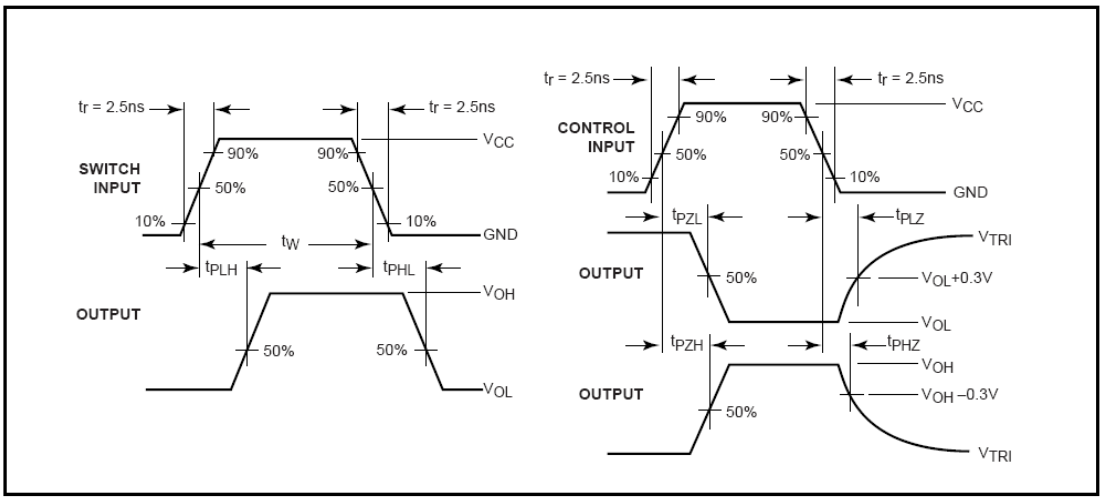

Figure 2. AC Waveforms

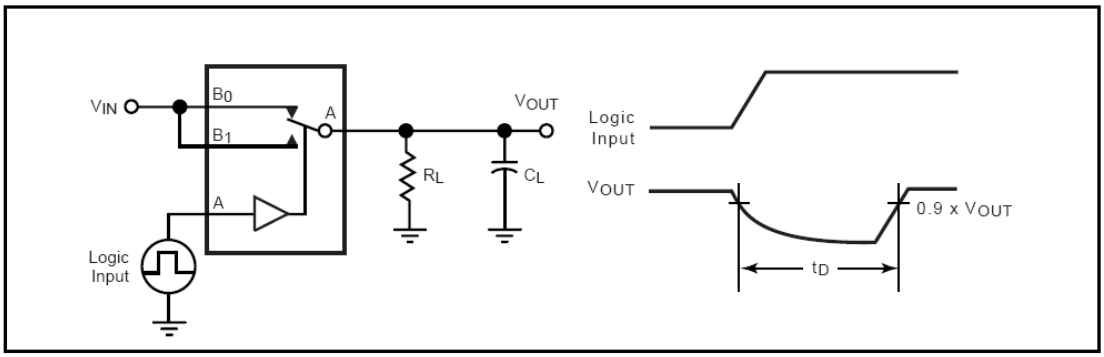

Figure 3. Break Before Make Interval Timing

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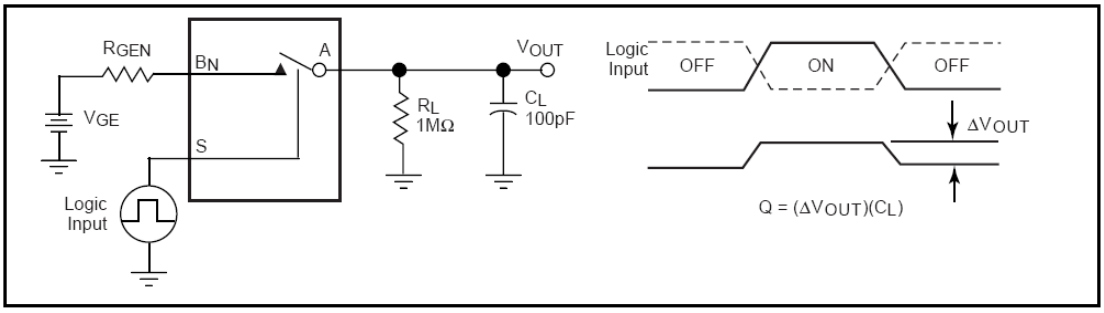

Figure 4. Charge Injection Test

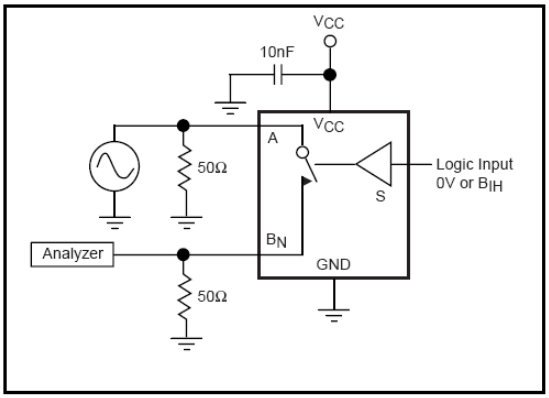

Figure 5. Off Isolation

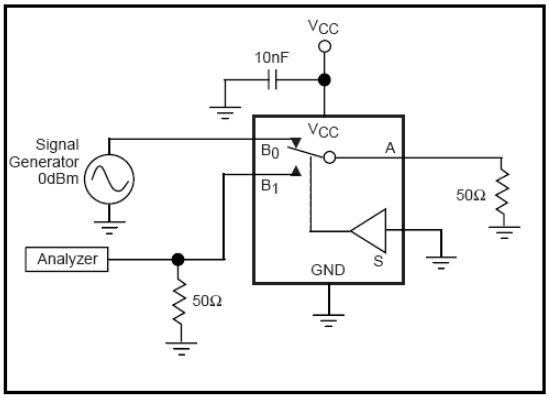

Figure 6. Crosstalk

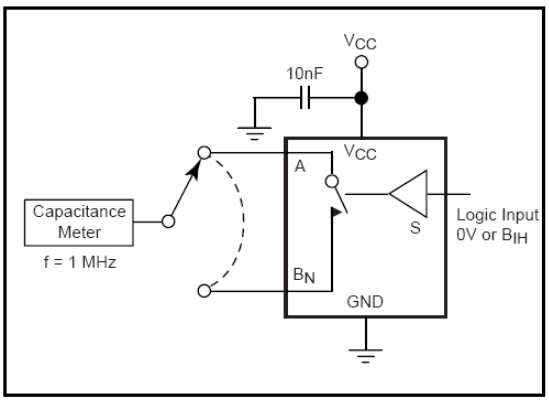

Figure 7. Channel Off Capacitance

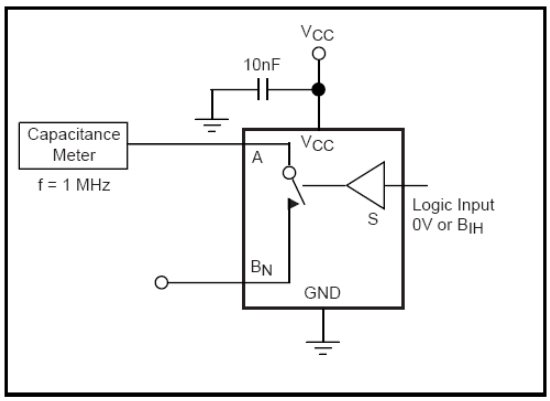

Figure 8. Channel On Capacitance

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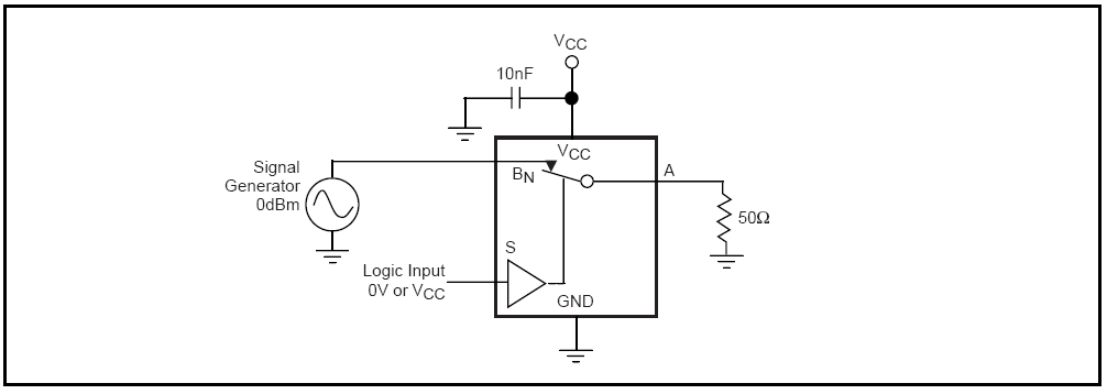

Figure 9. Bandwidth

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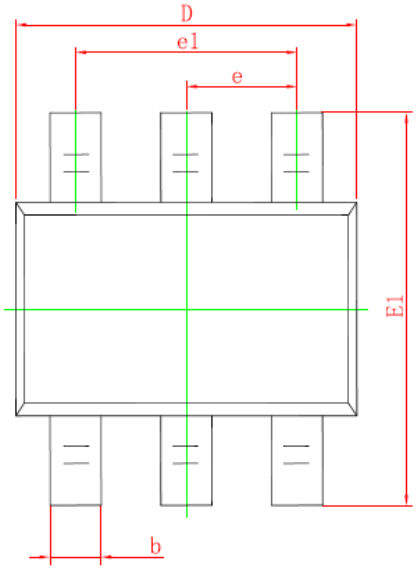

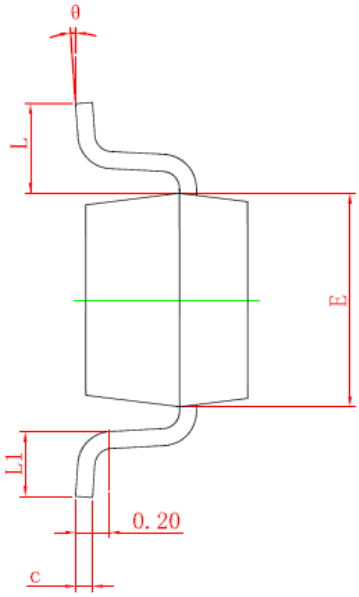

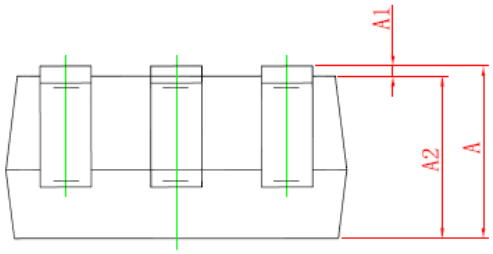

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.150	0.350	0.006	0.014
c	0.110	0.175	0.004	0.007
D	2.000	2.200	0.079	0.087
E	1.150	1.350	0.045	0.053
E1	2.150	2.450	0.085	0.096
e	0.650 TYP.		0.026 TYP.	
e1	1.200	1.400	0.047	0.055
L	0.525 REF.		0.021 REF.	
L1	0.260	0.460	0.010	0.018
θ	0°	8°	0°	8°

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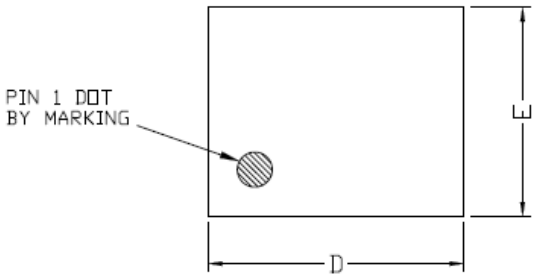
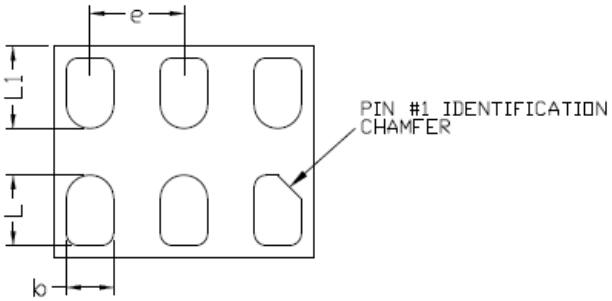
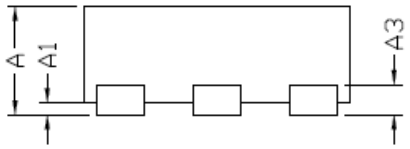


TOP VIEW



BOTTOM VIEW



SIDE VIEW

COMMON DIMENSIONS(MM)			
PKG.	X1:EXTREME THIN		
REF.	MIN.	NOM.	MAX
A	0.40	–	0.50
A1	0.00	–	0.05
A3	0.125 REF.		
D	1.05	1.10	1.15
E	0.85	0.90	0.95
b	0.15	0.20	0.25
L	0.25	0.30	0.35
L1	0.30	0.35	0.40
e	0.40 BSC		

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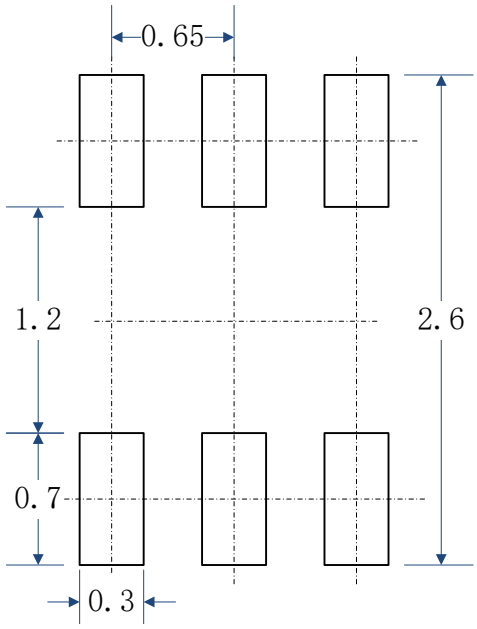
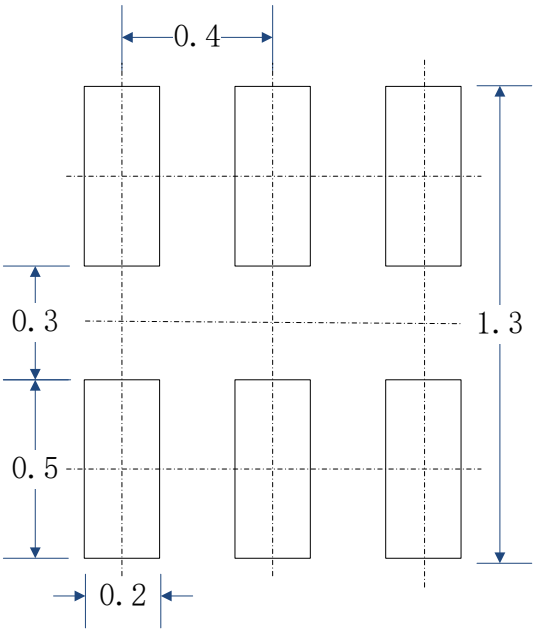
PCB Layout Pattern: DFN1.1x0.9-6L



SC70-6L RECOMMENDED PCB LAYOUT PATTERN (Unit: mm)



DFN1.1x0.9-6L RECOMMENDED PCB LAYOUT PATTERN (Unit: mm)

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