

## DATASHEET

# HY SERIES SUPERCAPACITOR

Revision 3.1, May 2021

The HY series of supercapacitors are high temperature (85°C) cylindrical cells offering excellent value. They are available as single cells, or dual cell modules with a choice of cell balancing options.

## Features:

- High power output to support peak current loads
- On-board energy storage to handle power surges (high capacitance and energy density)
- Long cycle life
- Wide temperature range (-40°C to +85°C)

## Applications:

- Energy Harvesting for wireless sensors
- Peak power support for GSM/GPRS transmission
- Last gasp power for remote meter status transmission
- Peak power support for locks & actuators
- Peak power support for portable drug delivery systems
- Short term bridging power for battery hot swap



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## Electrical Specifications

## Single cells

## Part numbering code

H	Y	N	vvv	dd	lll	S	ccc	R
Model	Cylindrical	# of cells	Voltage	Diameter (mm)	Length (mm)	Tolerance	Capacitance ( $\mu\text{F}$ )	Lead format
High temp		1	2R7 = 2.7V	6C = 6.3 08 = 8.0 10 = 10 1B = 12.5 16 = 16 18 = 18	012 = 12 068 = 68 120 = 120	M $\pm$ 20% S +50% /-20% V +30% /-10%	Two digits + number of zeros. 155 = 1500000 $\mu\text{F}$ = 1.5F	R = radial S = 2 solder pins W = 4 Cu tabs

Rated Voltage: 2.7V

Temperature Range: -40°C to +85°C

Parameters measured at 25°C

CAP-XX Part no.	Cap (F)	ESR Max @ 1KHz (m $\Omega$ )	Diameter (mm)	Length (mm)	IL max @ 72 Hrs ( $\mu\text{A}$ )
HY12R708012V105R	1	260	8	12	10
HY12R708012V205R	2	120	8	12	12
HY12R708014V205R	2	130	8	14	12
HY12R708016V205R	2	80	8	16	10
HY12R708020V335R	3.3	65	8	20	11
HY12R710020V505R	5	70	10	20	18
HY12R710020V705R	7	60	10	20	18
HY12R710025V705R	7	55	10	25	25
HY12R710025V106R	10	55	10	25	30
HY12R710030V106R	10	40	10	30	40
HY12R71B020V106R	10	50	12.5	20	30
HY12R716025V256R	25	25	16	25	80
HY12R718040V506R	50	15	18	40	150

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## Dual Cell Modules

## Part numbering code

H	Y	N	vvv	tt	ll	S	ccc	R	B
Model	Cylindrical	# of cells	Voltage	Module thickness (mm)	Length (mm)	Tolerance	Cap. (µF)	Lead & package format	Balancing
High Temp		2	5R5 = 5.5V	8E = 8.5 11 = 11	14 = 14 27 = 27	M ± 20% S +50% /-20% V +30% /-10%	Two digits + number of zeros.	R = shrink wrap – see dwg	R = Resistor* A = Active*

\*R pair of balancing resistors, 0402 resistors, nominal value stated in table below

\*A = CAP-XX active balancing circuit which draws < 1µA.

Rated Voltage: 5.5V

Temperature Range: -40°C to +85°C

Parameters measured at 25°C

## Shrink Wrap

CAP-XX Part no.	Cap (F)	ESR Max @ 1KHz (mΩ)	Thick x Width (mm)	Length (mm)	IL max @ 72 Hrs (µA) with active balance x=A	IL max @ 72 Hrs (µA) with resistor balance x=R	Nominal balancing resistor value (kΩ) x=R
HY25R58E14V504Rx	0.5	520	8.5 x 17	14	11	68	47
HY25R58E14V105Rx	1	240	8.5 x 17	14	15	72	47
HY25R58E16V105Rx	1	260	8.5 x 17	16	13	70	47
HY25R58E18V105Rx	1	160	8.5 x 17	18	11	68	47
HY25R58E22V155Rx	1.5	160	8.5 x 17	22	16	73	47
HY25R51122V255Rx	2.5	140	11 x 22	22	21	143	22
HY25R51122V355Rx	3.5	120	11 x 22	22	26	148	22
HY25R51127V355Rx	3.5	110	11 x 22	27	26	148	22
HY25R51127V505Rx	5	110	11 x 22	27	31	153	22
HY25R51132V505Rx	5	80	11 x 22	32	41	163	22

## Notes:

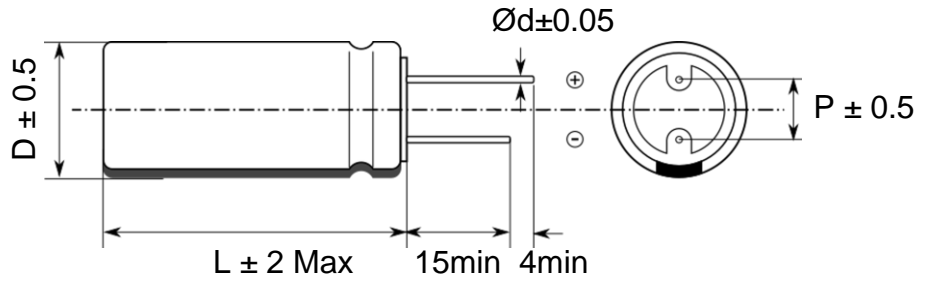
1. x = R (for passive balancing with 2 resistors) or A for active balancing using an op amp.
2. Lists the default value of balancing resistor for this module. Contact CAP-XX if a different value is desired.
3. For a possible module consisting of 2 single cells listed on page 2, but not shown in table above, please contact CAP-XX.

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**Dimensions** (all units in mm)

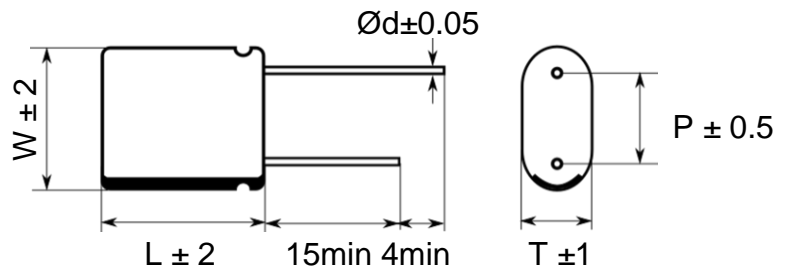
**HY1 Series Shrink Wrap Radial Lead 1F – 50F**

ΦD	P	Φd
6.3	2.3	0.6
8	3.5	0.6
10	5.5	0.6
12.5	5.5	0.6
16	8	0.8
18	8	0.8



**HY2 Series Shrink Wrap, 0.5F – 5F; L = R**

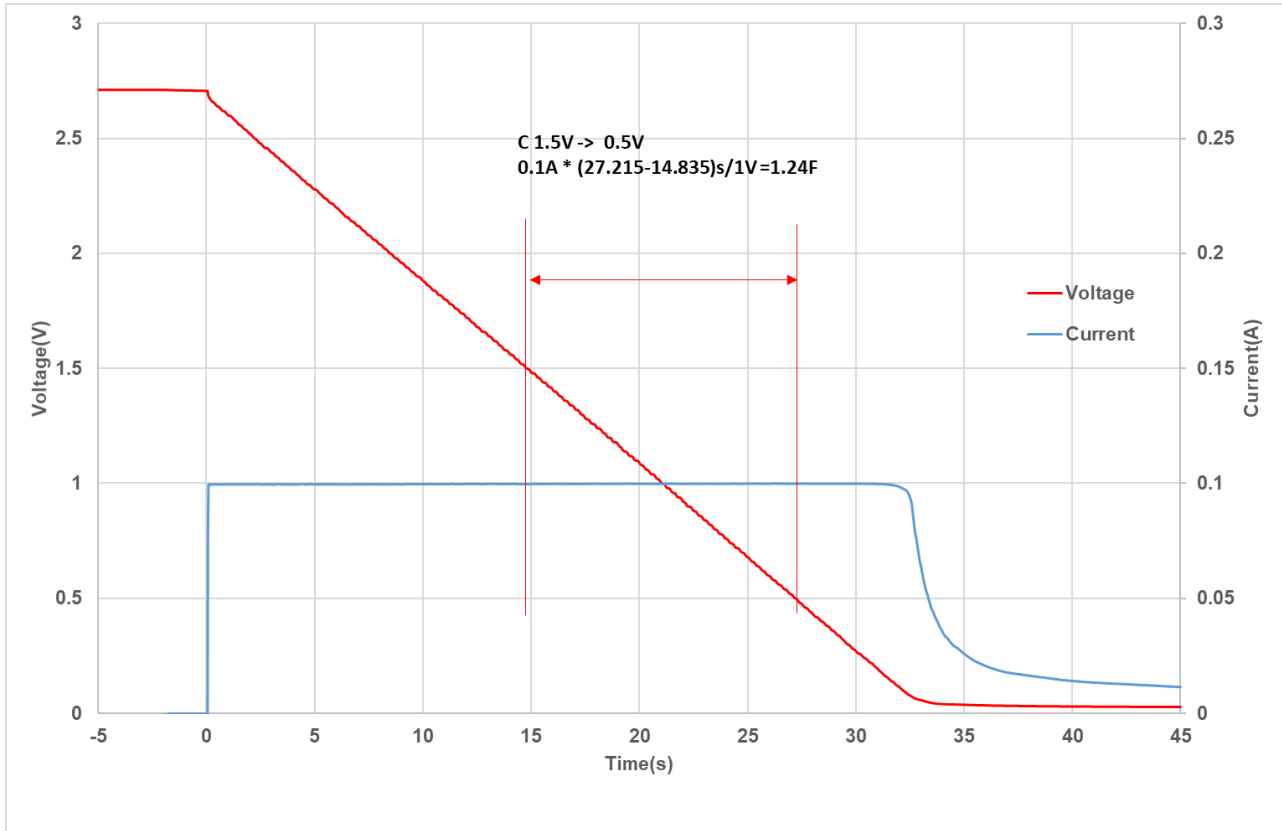
Cell dia.	T	W	P	Φd
8	8.5	17	11.5	0.6
10	11	22	15.5	0.6



## Measurement of capacitance

Capacitance is measured at 25°C using the method specified by IEC62391 shown in Fig 1. This measures DC capacitance. The capacitor is charged to rated voltage,  $V_R$ , at constant current, held at rated voltage for at least 30 minutes and then discharged at constant current. The time taken to discharge from  $0.8 \times V_R$  to  $0.4 \times V_R$  is measured to calculate capacitance as:

$$C = I \times (T_1 - T_2) / (V_1 - V_2)$$



**Fig 1: HY12R708012V105R Capacitance measurement**

In this case,  $C = 0.1A \times 12.38s / 1V = 1.24F$ , which is well within the  $1F +30\% / - 10\%$  tolerance for a HY12R708012V105R cell.

## Measurement of ESR

Equivalent Series Resistance (ESR) is measured at 25°C by applying a step load current to the supercapacitor and measuring the resulting voltage drop. CAP-XX waits for a delay of 200µs after the step current is applied to ensure the voltage and current have settled. In this case, for a HY12R708012V105R the ESR is measured as  $140\text{mV}/1\text{A} = 140\text{m}\Omega$ .

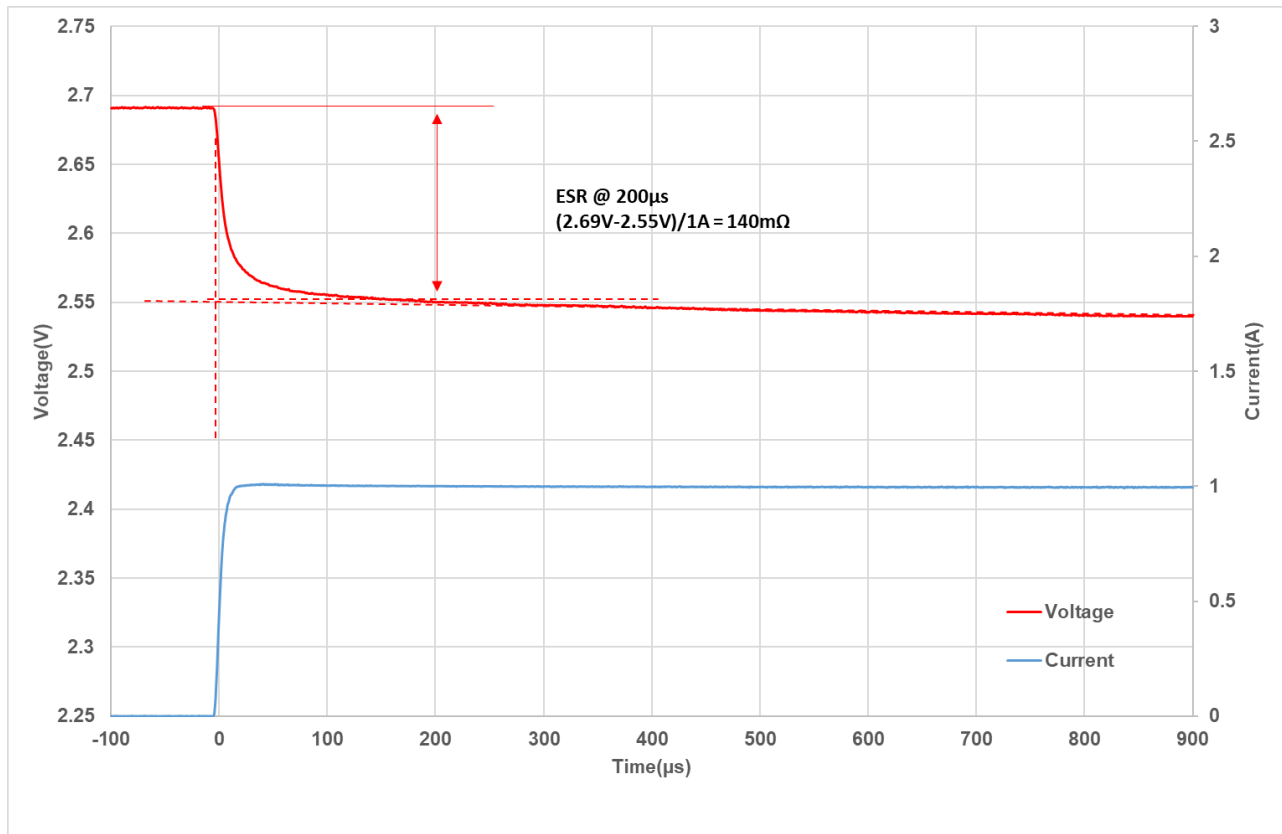


Fig 2: HY12R708012V105R ESR Measurement

## Measurement of Leakage Current

Leakage current is measured by holding the supercapacitor at rated voltage at 25°C and measuring the current drawn through a high value resistor, typically 1KΩ or 2.2KΩ. The leakage current decays over time as shown in Fig 3 which shows the average leakage current for HY series supercapacitors. Fig3 shows that the long-term equilibrium leakage current is typically 1.5μA/F but the datasheet quotes the maximum values after 72hrs at rated voltage.

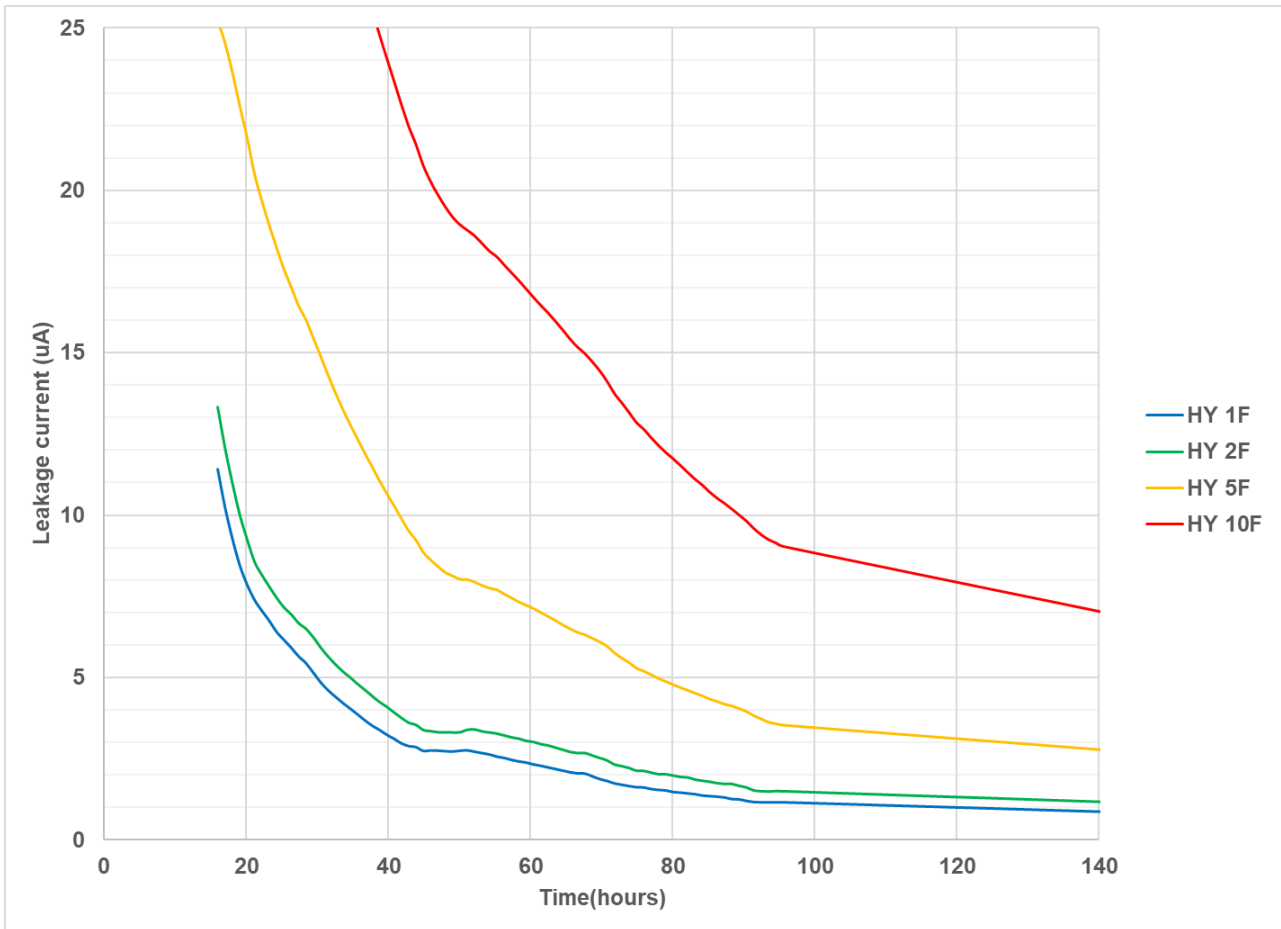


Fig 3: Leakage current measurement

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### Variation in DC Capacitance and ESR with temperature

Figure 4 shows that DC capacitance does not vary with significantly over the operating temperature range of -40°C to +85°C.

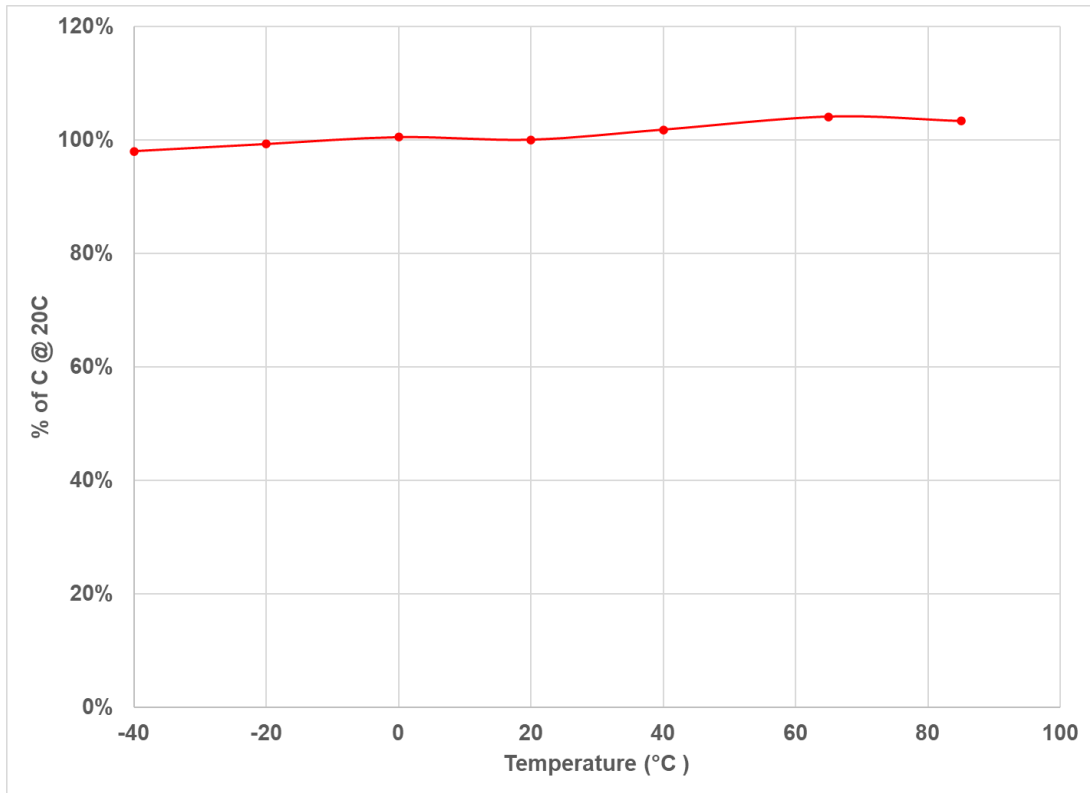


Fig 4: Variation in DC Capacitance over the operating temperature range

Figure 5 shows variation in DC ESR over the operating temperature range.

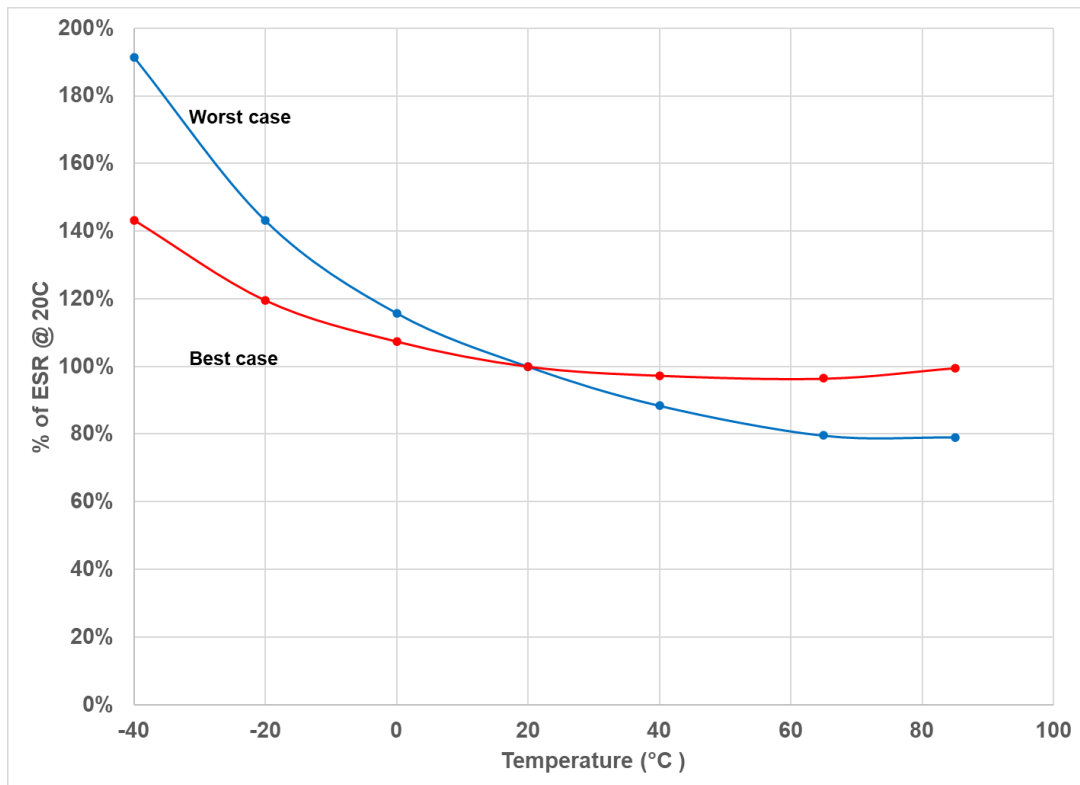


Fig 5: Variation in DC ESR over the operating temperature range



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From Figure 5,  $ESR_{DC}$  at  $-40^{\circ}\text{C}$  varies from  $\sim 1.4$  to  $1.9 \times ESR_{DC}$  at room temperature.  $ESR_{DC}$  at  $85^{\circ}\text{C}$  is 80% to 100% of  $ESR_{DC}$  at room temperature. The variation in ESR with temperature is due to the change in the mobility of ions in solution in the electrolyte.

## Peak Current

Peak current is limited by  $V_{rated}/(ESR + R_L)$  where  $R_L$  is the load resistance including parasitic resistance such as PCB traces. The current then decays and is given by:

$$[V_{rated}/(ESR + R_L)] \cdot e^{-t/[(ESR+R_L) \cdot C]}$$

where  $t$  = time in seconds. At high peak current, the supercapacitor discharges rapidly so that self heating due to the high current is negligible. Table 1 Shows short circuit current for a range of supercapacitors initially charged to 2.7V at the instant the short circuit is applied and after 100ms. It also shows the temperature increase recorded due to the short circuit.

**Table 1:**

Capacitance (F)	Instantaneous peak current (A)	Current after 100ms (A)	Temperature rise ( $^{\circ}\text{C}$ )
10	92	49	3
5	80	38	2.1
2	36	14	1.3
1	28	9	1

In all cases the temperature rise is not significant. A one-time peak current pulse is only limited by the  $ESR_{DC} + \text{Load resistance}$ , not by any thermal limitations.

The voltage drop when a constant current pulse of duration  $\tau$  is applied =

$$V_{INIT} - V_{FINAL} = I \cdot ESR_{DC} + I \cdot \tau / C$$

Where:

$I$  = constant current

$\tau$  = duration of constant current

$V_{INIT}$  = the initial voltage when the current pulse is first applied

$V_{FINAL}$  = the supercapacitor voltage at the end of the pulse

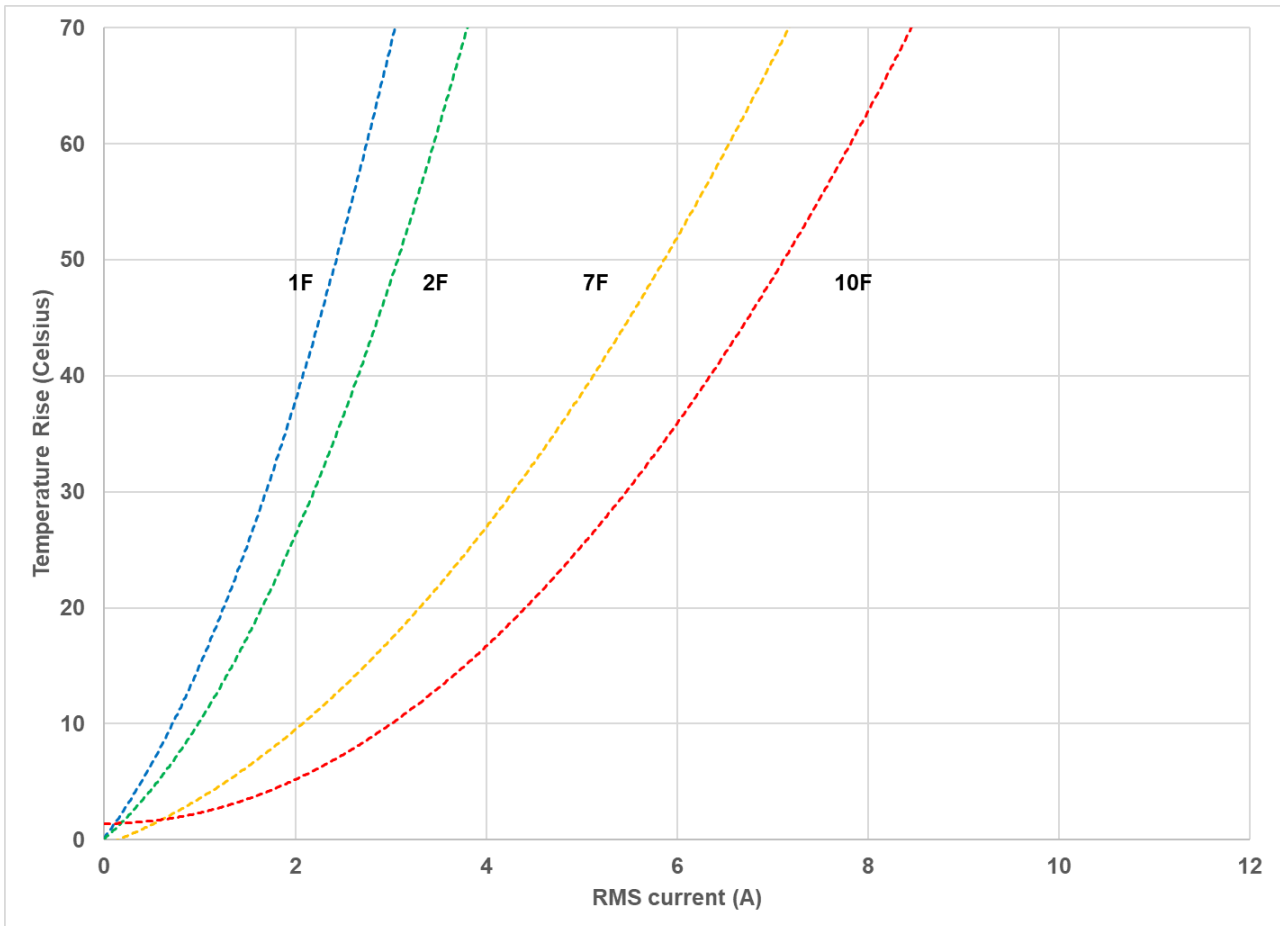
Re-arranging terms, the maximum current that can be sustained for a time  $\tau$ , when the supercapacitor is initially charged to rated voltage,  $V_R$ , and discharged to  $V_{MIN}$ , the minimum voltage that supports the given application =

$$I_{MAX} = \frac{V_R - V_{MIN}}{ESR_{DC} + \frac{\tau}{C}}$$

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## Maximum Continuous Current

Continuous current flow into/out of the supercapacitor will cause self-heating, which limits the maximum continuous current the supercapacitor can handle. This is measured by a current square wave with 50% duty cycle, charging the supercapacitor to rated voltage at a constant current, and then discharging the supercapacitor to half rated voltage at the same constant current value. For a square wave with 50% duty cycle, the RMS current is the same as the current amplitude. Fig 6 shows the increase in temperature above ambient temperature as a function of RMS current for various supercapacitors.



**Fig 6: Self heating with RMS current for HY series supercapacitors**

From Fig 6, the maximum RMS current in an application can be calculated. For example, if the ambient temperature is 40°C, and the maximum operating temperature for the supercapacitor is 85°C, then the maximum RMS current for a 10F supercapacitor should be limited to 6.8A, which causes a 45°C temperature increase.

## Effective capacitance (Ceff)

Effective capacitance is the capacitance seen for short pulse widths. Due to the supercapacitor's frequency response, for shorter pulse widths there will be less capacitance available than the DC capacitance. In Fig 7, consider the voltage drop due to capacitance after 10ms = 2.662V – 2.654V = 8mV. Therefore  $C_{eff}(10ms) = \text{Discharge\_Current} \times 10ms / \text{Voltage drop}(10ms) = 1.05A \times 0.01s / 0.008V = 1.3F$ . The voltage drop due to capacitance after 100ms = 2.662V – 2.636V = 26mV, hence  $C_{eff}(100ms) = 1.05A \times 0.1s / 0.026V = 4.0F$ . Fig 8 shows  $C_{eff}$  as a % of DC capacitance for the GY series of supercapacitors.

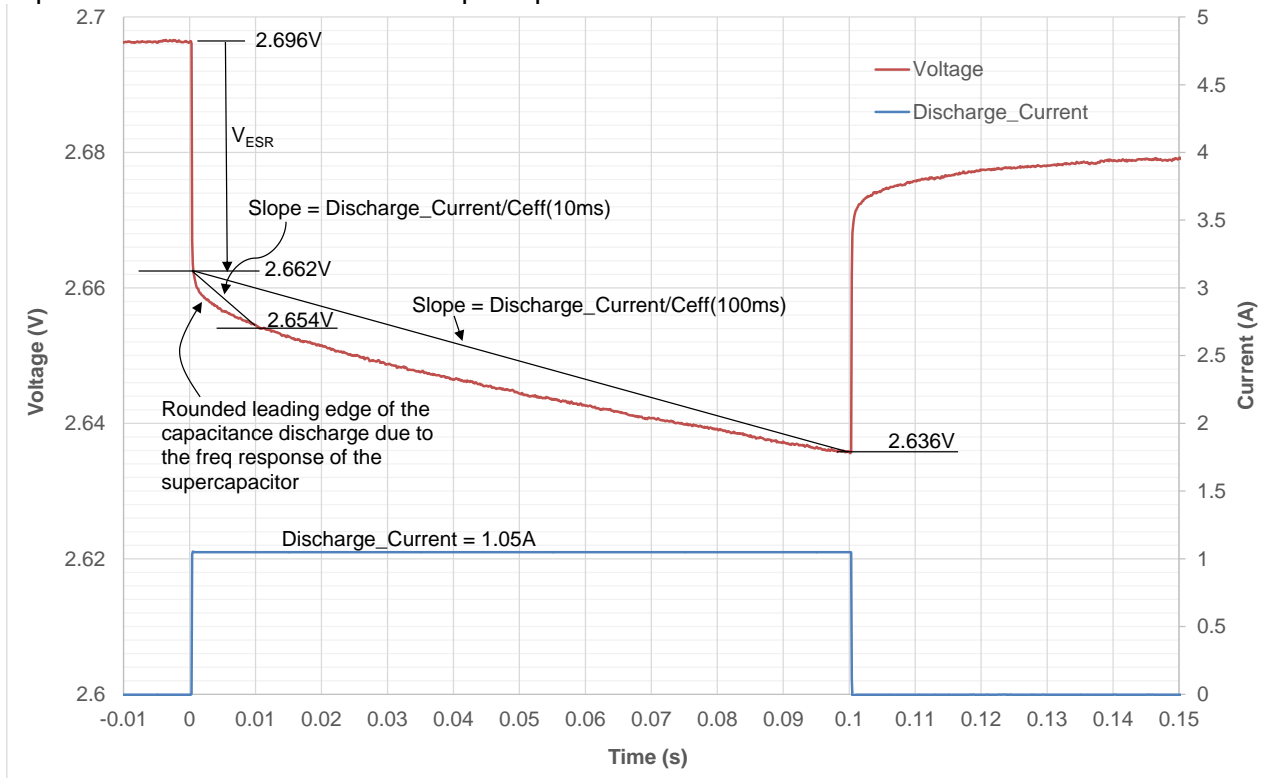
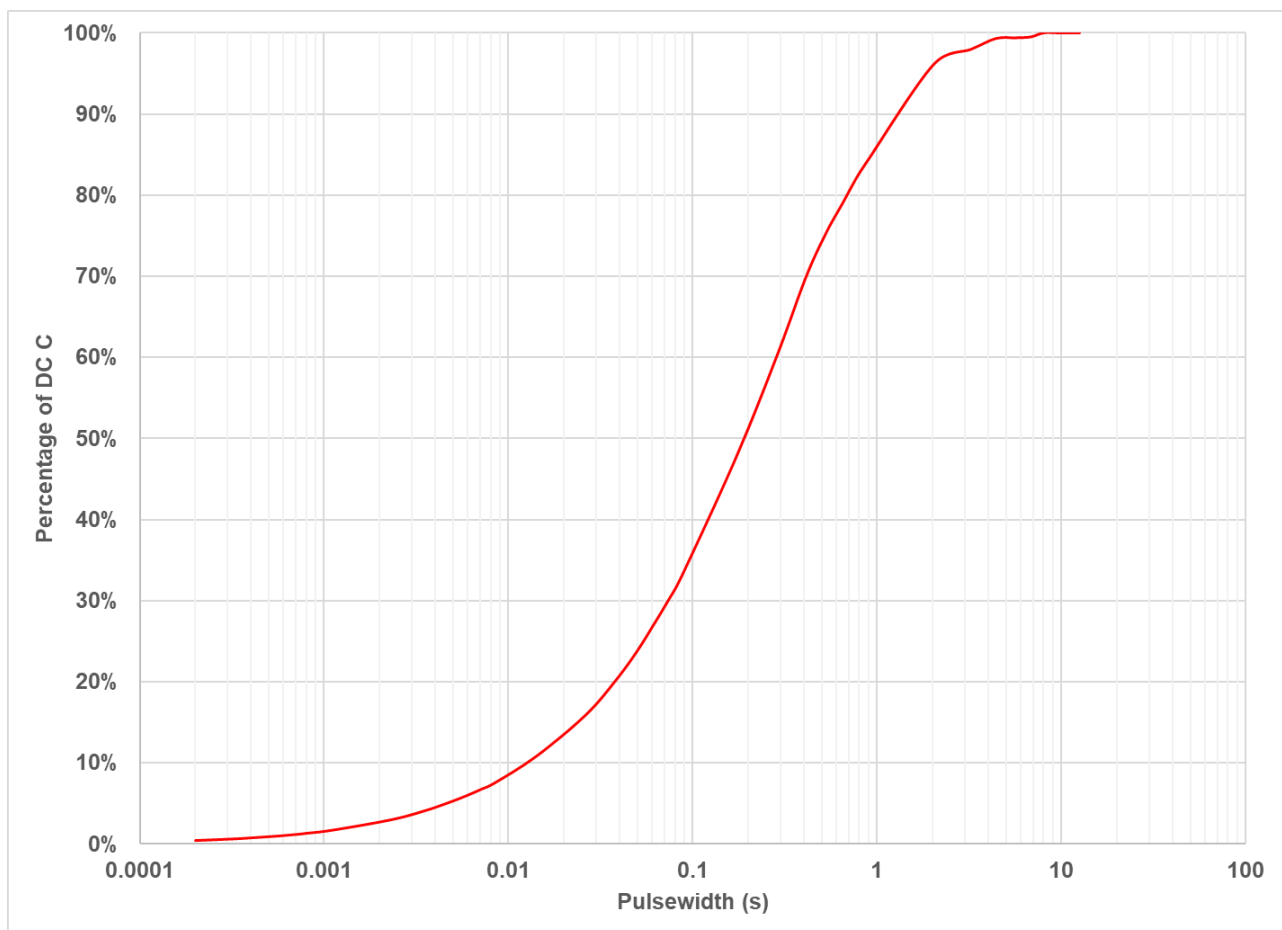


Fig 7: Discharge pulse illustrating the concept of Ceff



**Fig 8: Typical effective capacitance for HY 2.7V series supercapacitors**

For any given pulse width,  $T$ , with a constant discharge current  $I_{DISCH}$ , the voltage drop is given by:

$$V_{drop} = I_{DISCH} \times ESR + I_{DISCH} \times T / C_{eff}(T)$$

Where  $C_{eff}(T)$  = DC capacitance x % at time  $T$  read from Fig 8.

Shorter pulses need less capacitance to support them, so the supercapacitors can support short pulses despite their frequency response.

## Balancing options

In many applications a voltage  $> 2.7V$  but  $\leq 5.5V$  is required. For these applications 2 supercapacitor cells are connected in series in dual cell modules such as the CAP-XX HY2 series which is rated to 5.5V. These cells should have a balancing circuit to ensure that the cell voltages remain approximately equal or the cell with the lower  $C$  will have a higher voltage across it, causing it to age faster than its companion cell, hence losing even more  $C$  until it goes over voltage. This is a reason why a balancing circuit should aim to maintain the voltage across each cell equal, rather than just prevent over-voltage. As an example, if the dual cell module was at 5.0V and there were over-voltage protection circuits that prevented each cell from exceeding 2.7V, then module could have one cell at 2.7V and the other at 2.3V. The cell at 2.7V will age faster than the cell at 2.3V and will age faster than if both cells were held at 2.5V shortening module life.

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In the HY2 series modules there is a PCB connecting the 2 cells. This PCB can have one of two balancing options:

1. Option “R” as the last character in the HY2 series part number.  
A pair of balancing resistors are fitted, one resistor across each cell. The balancing resistors increase leakage current drawn by the module. Leakage current increases with capacitance, so modules made with larger cells need lower value balancing resistors that draw greater balancing current to ensure good voltage balancing between the cells. The dual cell module tables on page 3 specify the default value of balancing resistor supplied.
2. Option “A” as the last character in the HY2 series part number.  
An op amp maintains the midpoint voltage =  $\frac{1}{2}$  the supercapacitor module terminal voltage. This solution maintains the midpoint voltage very accurately, responds more quickly as the supercapacitor charges and discharges and only adds  $\sim 1\mu\text{A}$  to leakage current.

If the application uses a supercapacitor charging IC that has an integrated supercapacitor midpoint balancing circuit, or there is a balancing circuit on the PCB, then order 2 x HY1 cells and place them in series. This makes the midpoint available to your balancing circuit. The dimensions of 2 HY1 cells placed next to each other are the same as a shrink wrapped HY2 series cell, refer to Dimensions on page 4 of this datasheet. Refer to the Application Whitepaper on Supercapacitor Cell Balancing under the DESIGN AIDS section of the CAP-XX website, [www.cap-xx.com](http://www.cap-xx.com) for more information on cell balancing.

## Storage

CAP-XX recommends storing supercapacitors in their original packaging in an air conditioned room, preferably at  $< 30^{\circ}\text{C}$  and  $< 50\%$  relative humidity. CAP-XX supercapacitors can be stored at any temperature not exceeding their maximum operating temperature but storage at continuous high temperature and humidity is not recommended and will cause premature ageing.

Do not store supercapacitors in the following environments:

- High temperature / high humidity
- Direct sunlight
- In direct contact with water, salt, oil or other chemicals
- In direct contact with corrosive materials, acids, alkalis or toxic gases
- Dusty environment
- In environments subjected to shock and vibration

## Soldering

When soldering it is important to not over-heat the supercapacitor to not adversely affect its performance. CAP-XX recommends that only the leads come in contact with solder and not the supercapacitor body.

### Hand Soldering

Heat transfers from the leads into to the supercapacitor body, so the soldering iron temperature should be  $< 350^{\circ}\text{C}$  soldering time should be kept to the minimum possible and be less than 4 seconds.

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**Wave Soldering**

The PCB should be pre-heated only from the bottom and for < 60 secs with temperature  $\leq 100^{\circ}\text{C}$  on the top side of the board for PCBs  $\geq 0.8\text{mm}$  thick. The table below lists suggested solder temperatures.

Solder temperature $^{\circ}\text{C}$	Suggested solder time (s)
220	7
240	7
250	5
260	3

**Reflow Soldering**

Infrared or conveyor oven soldering techniques can be used providing the supercapacitor body is not subject to temperatures  $> 85^{\circ}\text{C}$ . Do not use a standard reflow oven.

**Transportation**

All the supercapacitor cells in this datasheet store  $< 0.3\text{Wh}$  energy. The energy in watt-hours is calculated as:  $\frac{1}{2} \times \text{Capacitance} \times V_{\text{rated}}^2 / 3600$ . The largest cell in this range is 50F, so stored energy =  $\frac{1}{2} \times 50 \times 2.7^2 / 3600 = 0.0506\text{Wh}$ . Under regulation UN3499 there is no restriction on shipping these supercapacitors. Their shipping description is "Electrical Capacitors" with harmonized shipping code 8532.29.0040.

单击下面可查看定价，库存，交付和生命周期等信息

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