CW2017

Lithium-ion Fuel Gauge IC with ID Measurement Function

Features

- System-Side or Pack-Side Fuel Gauging
- ±3% Maximum SOC Measurement Error
- 14-bit Sigma-Delta ADC for Cell Voltage, Temperature and ID Resistor Measurement
- Configurable Interrupt for Battery SOC Change, High or Low Battery Temperature
- No Offset Accumulation During Life Time
- No Full-to-Empty Battery Learning Cycle
- No Sense Resistor Required
- Patented “FastCali” Fuel Gauging Algorithm
- External Thermistor Supported
- ID Resistor Measurement Supported
- Ultra-low Power Consumption
  - Normal Mode 17μA
  - Sleep Mode <1μA
- General I^2C Interface
- Tiny, Lead(Pb)-Free, TDFN 2mmx2mm-8L Package

Applications

- Smartphone
- Tablet PCs
- Handheld and Portable Devices
- Lithium-ion or Lithium Polymer Battery Packs

General Description

The CW2017 is an ultra-compact, system-side or pack-side, sensing resistor free, fuel gauging IC for Lithium-ion(Li+) based batteries in handheld and portable devices.

The CW2017 tracks the Li+ battery’s operation conditions and performs state-of-the-art algorithm to calculate the relative State-of-Charge (SOC) of very different battery chemistry systems (LiCoOx, polymer Li-ion, LiMnOx etc.).

The CW2017 includes a 14-bit Sigma-Delta ADC, a precision voltage reference and build-in NTC bias circuits. The IC allows users to eliminate the expensive current sensing resistor which usually occupies very large PCB area. The IC sends out the alarm signal if the battery SOC level or the temperature measured reaches the pre-programmed threshold.

The CW2017 integrates the ID resistor sensing feature. It can also be used as an alternative sensing port.

The CW2017 uses a 2-wire I^2C compatible serial interface that operates in standard (100kHz) mode or fast (400kHz) mode.

Application Circuits

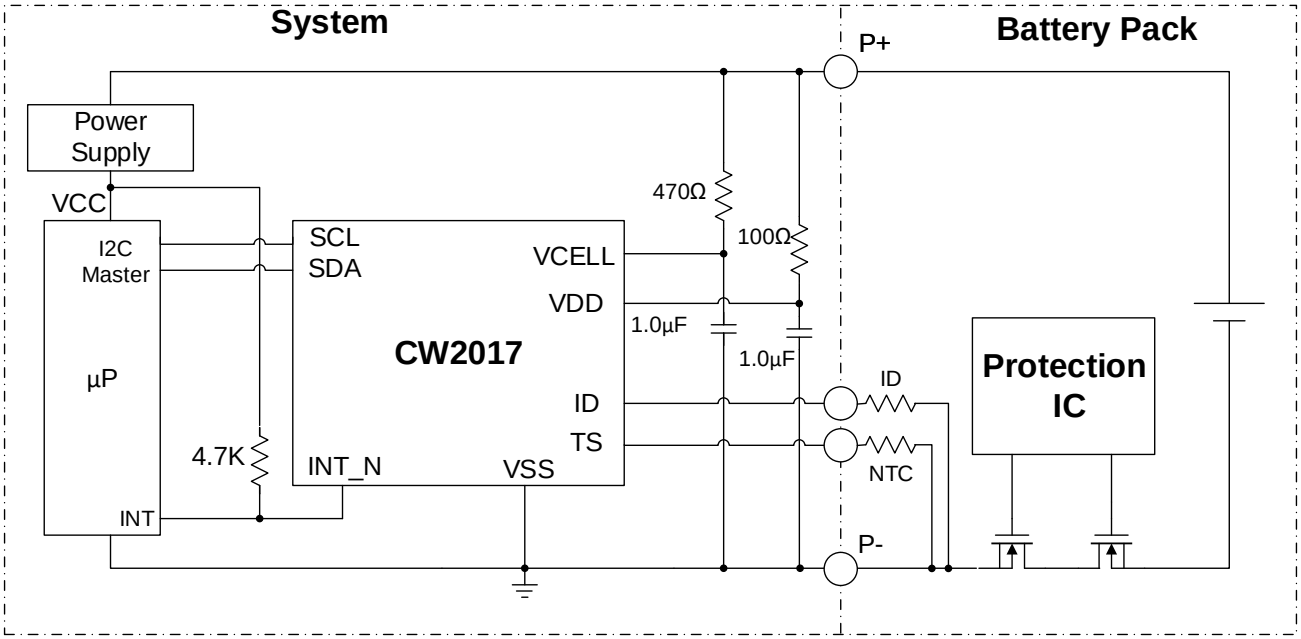


Figure 1. Typical Application Diagram (System Side)

Figure1 is a typical application diagram of CW2017 used in system side, recommended external components are marked on the figure.

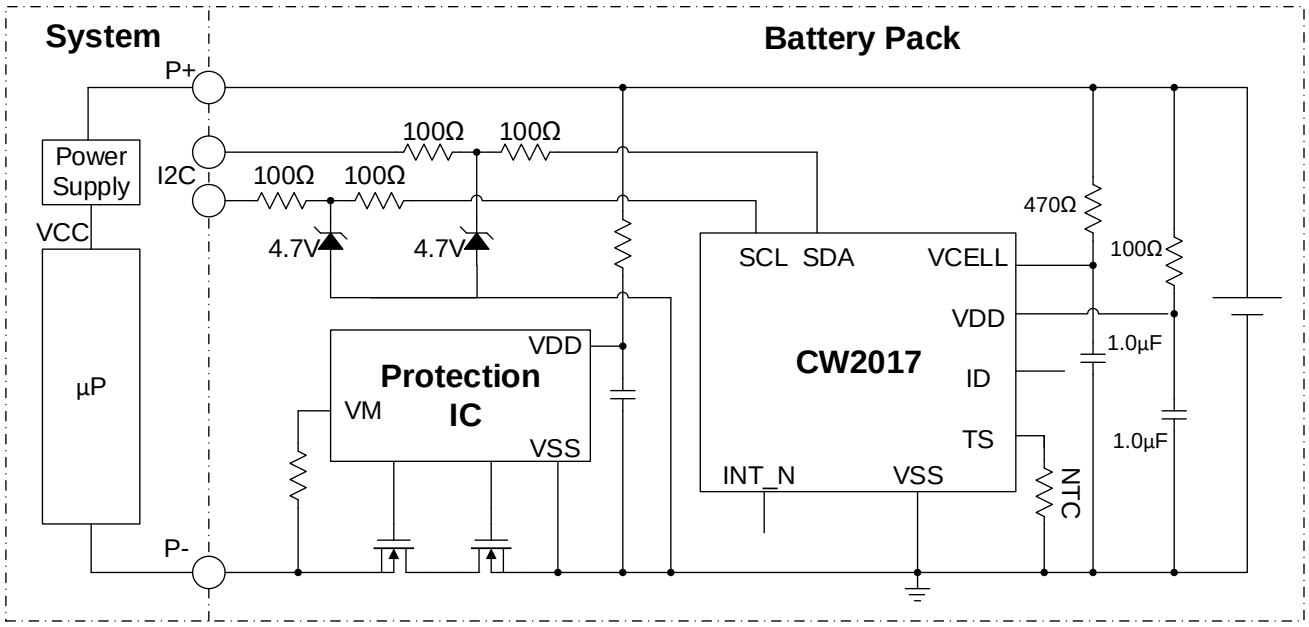


Figure 2. Typical Application Diagram (Pack Side)

Figure 2 is a typical application diagram of CW2017 used in pack side, recommended external components are marked on the figure.

The CW2017 can be used in application with multi-battery connected in series or in parallel. Please refers to the application note for more information or contacts support@cellwise-semi.com for more support.

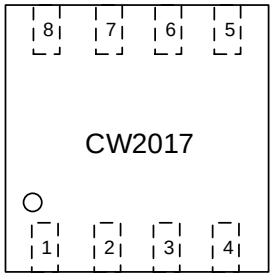
Ordering Information

PART	OPERATING TEMPERATURE	PACKAGE	TOP MARK
CW2017AAAD	-40ºC to 85ºC	TDFN8	2017XXXX

Note: XXXX stands for the manufacture info.

Pin Configuration

TDFN Package Top view
2mm*2mm – 8pin
(Pad Side Down)



Pin Descriptions

PIN	NAME	DESCRIPTION
1	ID	ID measuring I/O. It can be left floating if unused.
2	VCELL	Battery voltage monitor I/O.
3	VDD	System power supply.
4	VSS	General purpose ground connection.
5	INT_N	Alarm signal for MCU interrupt controller. It can be left floating if unused.
6	TS	Thermistor measuring I/O.
7	SCL	Serial clock input.
8	SDA	Serial data input/output.

Type Number

CW2017XXXX

Package type	D: TDFN 2mm*2mm-8L;
Parameter generation	A: Standard firmware and parameter, A version
Standard Li+ battery application	A: CellWise Li-Polymer profile
Function and revision	A: A generation product

Absolute Maximum Ratings

		VALUE		UNITS
		MIN	MAX	
Voltage respect to VSS	ID, CELL, VDD, INT_N, TS, SCL, SDA	-0.3	6	V
Output Current	INT_N, SDA		10	mA
Operation Temperature	T_A	-40	85	°C
Junction Temperature	T_J	-40	150	°C
Storage Temperature	T_{STG}	-50	150	°C
ESD	All pins. HBM model.		±2000	V
Moisture Sensitivity Level	MSL	Level 3		

Caution:

Stresses beyond "Absolute Maximum Ratings" condition may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended DC Operating Conditions

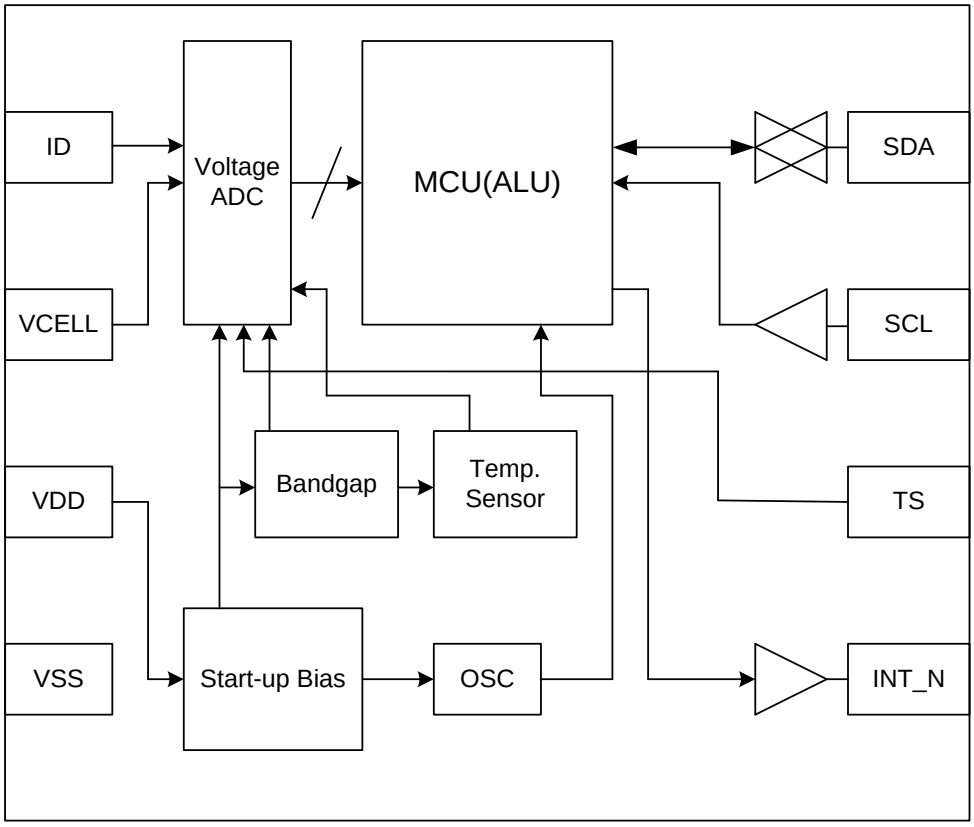
PARAMETER	DESCRIPTION	MIN	MAX	UNITS
Input Voltage Range	ID, VCELL, VDD, INT_N, TS, SCL, SDA	-0.3	5.5	V
I^2C Clock Frequency			400	kHz
Operation Temperature		-40	85	℃

Electrical Characteristics

$2.5 \leq V_{DD} \leq 4.7$, T_A= -40 to 85ºC, unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY CONTROL						
VDD power on threshold	V_{ON_VDD}	I2C communication enable		2.4		V
VDD power off threshold	V_{OFF_VDD}	I2C communication stop		2.2		V
QUIESCENT CURRENT						
Sleep mode current	I_{SLEEP}				2	μA
Normal mode current	I_{NOR}			17		μA
CELL VOLTAGE MEASUREMENT ADC CHARACTERISTICS						
Cell pin measurement range	V_{CELL_R}		2.5		4.7	V
Conversion time	t_{CELL_CONV}			5		ms
Effective bits				14		bits
Measurement resolution	V_{LSB_CELL}			312.5		μV
Measurement error	V_{ERR_CELL}	T_A= 25ºC and cell voltage is 4V	-8		8	mV
		T_A= -40 to 85ºC and cell voltage is 4V	12		12	mV
TS PIN TEMPERATURE ADC CHARACTERISTICS						
Measurement range	V_{TS_R}		0		2.2	V
Conversion time	t_{TS_CONV}			5		ms
Effective bits				14		bits
Measurement resolution	V_{LSB_TS}			312.5		μV
Measurement error	V_{ERR_TS}	T_A= 25ºC and cell voltage is 4V	-8		8	mV
		T_A= -40 to 85ºC and cell voltage is 4V	12		12	mV
ID PIN VOLTAGE MEASUREMENT ADC CHARACTERISTICS						
Measurement range	V_{ID_R}		0		2.2	V
Conversion time	t_{ID_CONV}			5		ms
Effective bits				14		bits
Measurement resolution	V_{LSB_ID}			312.5		μV
Measurement error	V_{ERR_ID}	T_A= 25ºC and cell voltage is 4V	-8		8	mV
		T_A= -40 to 85ºC and cell voltage is 4V	12		12	mV
DIGITAL IO CHARACTERISTICS						
Input voltage, high	V_{IH}		1.4			V
Input voltage, low	V_{IL}				0.5	V
Output voltage, low	V_{OL}	with 4mA current sink			0.4	V

Functional Block Diagram



Notes: Some buffer blocks are omitted

Detailed Description

Power State

By default, after power up, the CW2017 stays in sleep mode to minimize power consumption. The device needs two steps to enter normal operation mode: step one, clear sleep register by writing 0x30 to REG 0x08; step two, clear restart register by writing 0x00 to REG 0x08.

In normal operation, master controller can also restart the CW2017 operation by writing 0x30 to REG 0x08 and then 0x00 to REG 0x08. After restart operation, the CW2017 will reboot the firmware and restart the normal operation procedure.

FastCali Algorithm

From battery OCV (open circuits voltage), the CW2017 could deduce the SOC (state of charge) of this battery. There are two ways to obtain OCV: idle battery voltage that has been relaxed at least for half an hour; battery voltage adds the internal resistor voltage drop when charging or discharging.

Combined the creative “equipment current track” technology, which precisely calculates the present voltage drop on the battery internal resistor, with the “FastCali” algorithm, the CW2017 can promptly infer the OCV value no matter the battery is in charging, relaxing or discharging state.

First SOC Estimation after Power Up

The CW2017 considers the battery as a free one that has been relaxed more than 0.5 hours when power up. It treats the battery voltage measured by the 14bits ADC as an OCV voltage. According to this voltage,

the CW2017 deduces the first SOC value. The algorithm heals the initial error of the first SOC during the normal use afterwards.

Temperature Sensing & ID usage

The TS pin is an external battery temperature sensing pin. A driving circuit is integrated, please use a 10kΩ NTC thermistor (β value = 3435K±1% at 25/85℃) to connect between the TS and VSS pins directly. The ID pin is a general purpose ADC input. A typical application is ID resistor identification. USB ID, USB connector temperature can be measured either.

Interrupt

The CW2017 have 3 interrupt options: SOC change, Max. Temperature and Min. Temperature. If any INT event occur, the relevant register will be set, and INT_N pin will generate a low pulse with about 1ms duration to inform master controller.

Battery Profile

The battery profile of the CW2017 is programmable to match batteries with max. charging voltages of 4.20V, 4.35V, 4.40V or other voltages. User's battery needs to have battery characterization to get its exclusive profile for more accurate SOC. Please contact Cellwise for details.

Register Map

Below table shows the I²C register map for the CW2017.

REGISTER NAME	ADDRESS	DESCRIPTION	READ/ WRITE	DEFAULT VALUE
VERSION	0x00	IC Version	R	0xA0
VCELL_H	0x02	CELL pin voltage conversion result, VCELL[13:8]	R	0x00
VCELL_L	0x03	CELL pin voltage conversion result, VCELL[7:0]	R	0x00
SOC_H	0x04	SOC result, SOC[15:8]	R	0x00
SOC_L	0x05	SOC result, SOC[7:0]	R	0x00
TEMP	0x06	Battery temperature	R	0x00
CONFIG	0x08	IC configuration	R/W	0xF0
INT_CONF	0x0A	Interrupt configuration	R/W	0x40
SOC_ALERT	0x0B	SOC interrupt threshold	R/W	0x14
TEMP_MAX	0x0C	Maximum temperature threshold	R/W	0xAA
TEMP_MIN	0x0D	Minimum temperature threshold	R/W	0x50
VOLT_ID_H	0x0E	ID pin voltage conversion result, VID[13:8]	R	0x00
VOLT_ID_L	0x0F	ID pin voltage conversion result, VID[7:0]	R	0x00

VCELL Register (0x02~0x03)

The VCELL register is an **UNSIGNED** 14bit read-only register that updates continuously the battery terminal voltage. Battery voltage is measured between the VCELL pin to VSS pin as a ground reference. A 14bit sigma-delta A/D converter is used and the voltage resolution is 312.5uV for CW2017. This A/D converter updates the cell voltage for a period of <10ms after IC POR and then four times a second afterwards.

$$\mathbf{V}(uV) = \boldsymbol{Value}_{(0x02\ \ 0x03\ \ DEC)} * \mathbf{312.5}$$

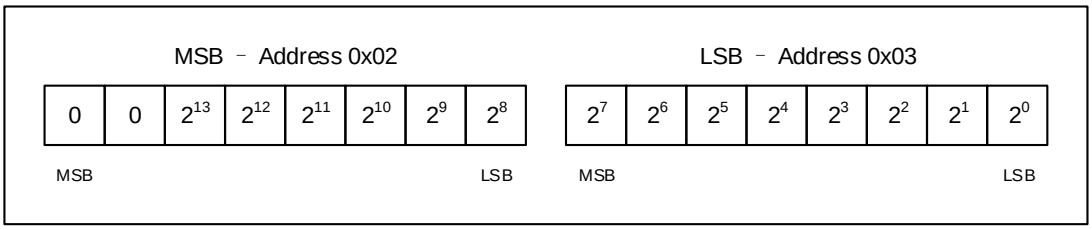


Figure 3. VCELL Register Format

SOC Register (0x04~0x05)

The SOC register is an **UNSIGNED** 16bit read-only register that indicates the State-of-Charge of the battery cell. SOC value is a relative concept which display as a percentage of the cell's total capacity. This register intrinsically adjusts itself to the change of battery cell's parameter due to aging, poor cell parameter distribution control or rapid change in total capacity.

In this register, the high 8bit part contains the SOC information in 1% units which can be directly used by end user if this accuracy is already good enough for application. The low 8bit part provides more accurate part of the SOC information and the LSB is 1/256%.

$$\mathbf{SOC}(\%) = \boldsymbol{Value}_{(0x04\ \ DEC)} + \frac{\boldsymbol{Value}_{(0x05\ \ DEC)}}{\mathbf{256}}$$

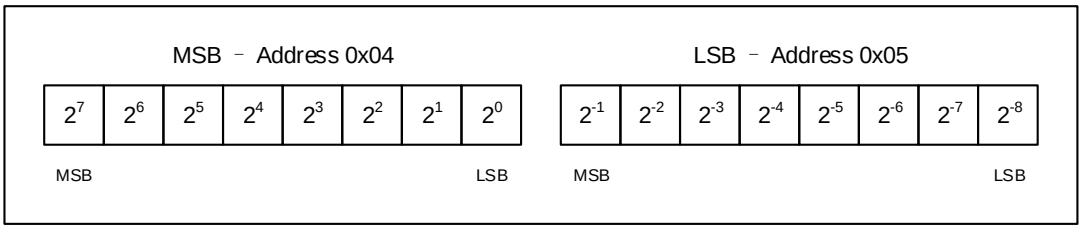


Figure 4. SOC Register Format

TEMP Register (0x06)

The TEMP register is an **UNSIGNED** 8bit read-only register. Temp Register reports real-time battery temperature. The scope is from -40 to 87.5 degrees Celsius, LSB is 0.5 degree Celsius.

$$\mathbf{TEMP}(\mathcal{C}) = -\mathbf{40} + \frac{\boldsymbol{Value}_{(0x06\ \ DEC)}}{\mathbf{2}}$$

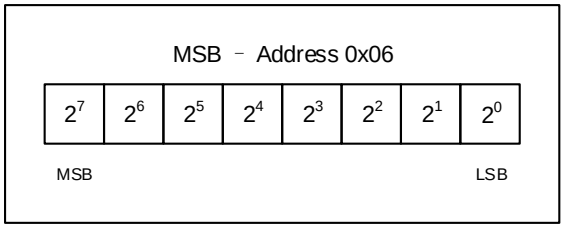


Figure 5. TEMP Register Format

CONFIG Register (0x08)

CONFIG register is used for Master to control the IC.

The default value is 0xF0. SLEEP and RESTART bit are set 1.

To power up CW2017, master controller need to write 0x30 to clear sleep mode, then write 0x00 to restart chip to enter normal mode. To reset chip, master controller needs to write 0x30 to enter reset mode, then write 0x00 to trigger restart. The CW2017 will reload battery profile and restart calculation. CONFIG [3:0] is reserved. Don't do any operation with it.

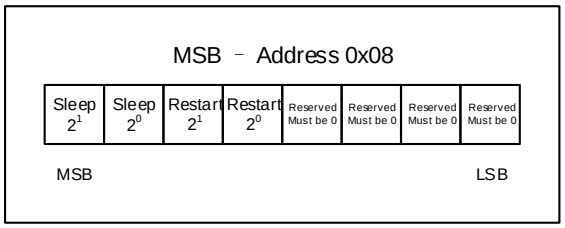


Figure 6. CONFIG Register Format

INT_CONF Register (0x0A)

INT_CONF [7:4] are used to enable interrupt, and INT_CONF [3:0] are used to indicate relative interrupt incident. There are three interrupt sources.

SOC_INT indicates SOC change.

TMX_INT is the maximum temperature flag. It will be set when temperature is higher than TEMP_MAX value.

TMN_INT is the minimum temperature flag. It will be set when temperature is lower than TEMP_MIN value.

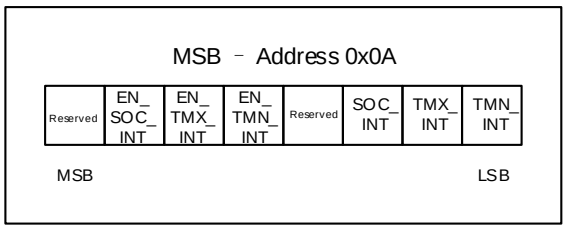


Figure 7. INT_CONF Register Format

SOC_ALERT Register (0x0B)

UPDATE_FLAG bit can be marked after battery profile update successfully by master controller to check whether chip has been reset. Default value is 0.

SOC_ALERT [6:0] configures specified SOC alert threshold to remind master controller.
Set SOC_ALERT [6:0] to 0x7F to generate interrupt as long as the integer part of SOC changes.

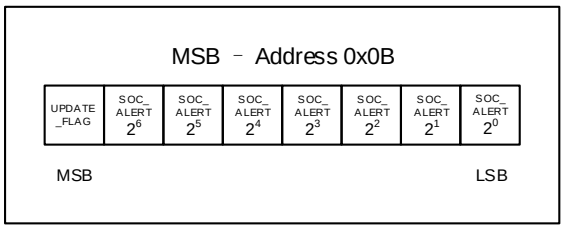


Figure 8. SOC_ALERT Register Format

TEMP_MAX Register (0x0C)

TEMP_MAX is the maximum temperature warning threshold.
When temperature reach this value, TMX_INT(0x0A) bit is set, and a low pulse is sent by INT_N pin.

$$\mathbf{TEMP_{MAX}}(℃) = -40 + \frac{Value_{(0x0C\ \ DEC)}}{2}$$

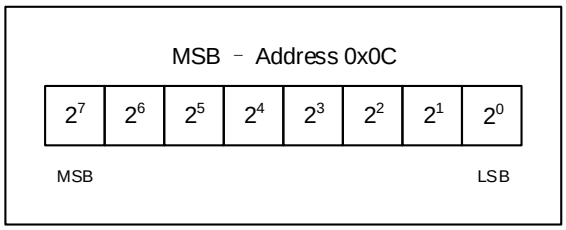


Figure 9. TEMP_MAX Register Format

TEMP_MIN Register (0x0D)

TEMP_MIN is the minimum temperature warning threshold.
When temperature reach this value, TMN_INT(0x0A) bit is set, and a low pulse is sent by INT_N pin.

$$\mathbf{TEMP_{MIN}}(℃) = -40 + \frac{Value_{(0x0D\ \ DEC)}}{2}$$

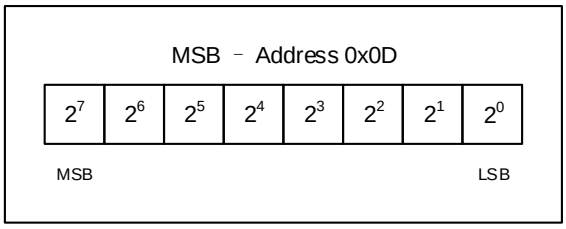


Figure 10. TEMP_MIN Register Format

VOLT_ID Register (0x0E~0x0F)

VOLT_ID is a **SIGNED** 14bit register that returns ADC results by ID pin.

$$\mathbf{V}(uV) = Value_{(0x0E\ \ 0x0F\ \ DEC)} * 312.5$$

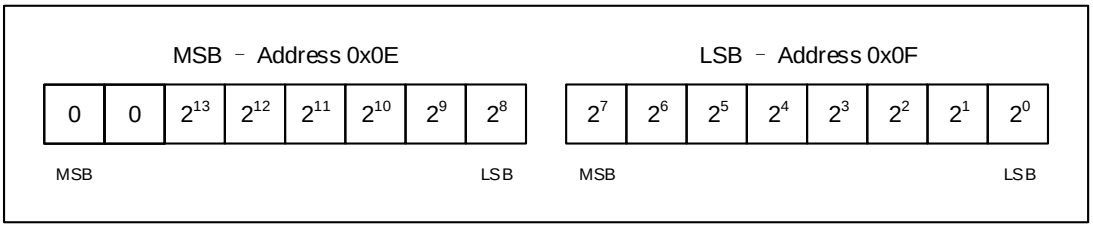


Figure 11. VOLT_ID Register Format

I²C Characteristics

The CW2017 includes an I²C bus which provides access to internal registers to program charging parameters and report device status. To adjust these parameters, data transmission from the host to the CW2017 and vice versa must take place through the two wires. The two wires of the bus consist of the SDA line, over which all data is sent and the SCL line which is a clock signal used to synchronize sending/receiving of the data. Data on the I²C bus can be transferred up to 100kbps in the standard-mode or up to 400kbps in the fast-mode. When the bus is free, both lines are HIGH. The device operates as a slave device. The slave address is 0xC6/C7h. The I²C interface of the CW2017 works after the voltage on the VDD rises above POR threshold.

Data Validity

The data on the SDA line must be stable during the HIGH period of the SCL, unless generating a START or STOP condition. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred.

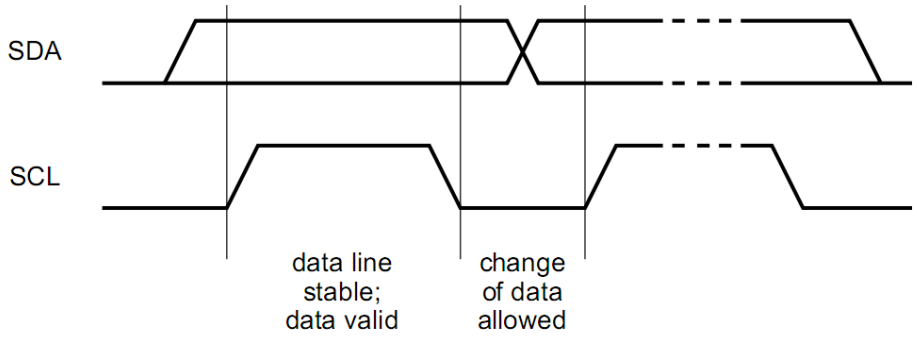


Figure 12. Bit Transfer on the I2C Bus

START and STOP Conditions

All transactions begin with a START (S) and are terminated by a STOP (P). A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition. START and STOP conditions are always generated by the master. The bus is considered to be busy after the START condition and free after the STOP condition.

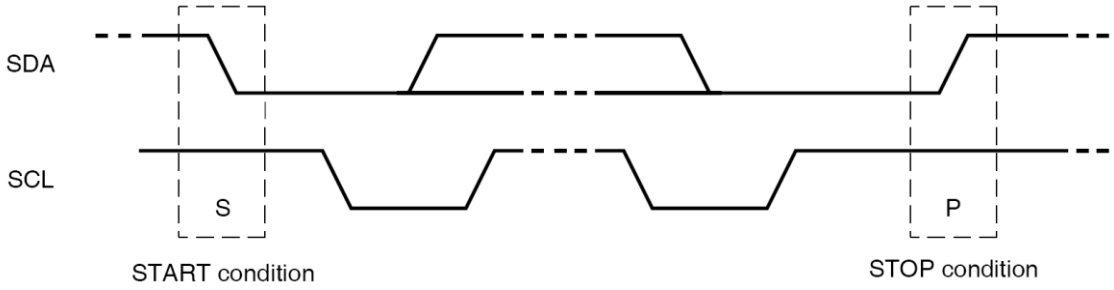


Figure 13. START and STOP Conditions

Byte Format

Every byte put on the SDA line must be eight bits long, the number of bytes that can be transmitted per transfer is unrestricted. Each byte must be followed by an Acknowledge bit. Data is transferred with the MOST Significant Bit (MSB) first. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, for example servicing an internal interrupt, it can hold the clock line SCL LOW to force the master into a wait state. Data transfer then continues when the slave is ready for another byte of data and releases clock line SCL.

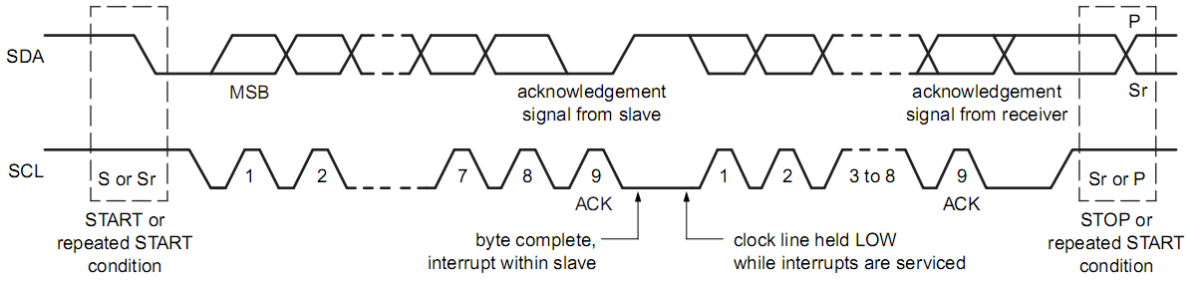


Figure 14. Data Transfer on the I2C Bus

Acknowledge (ACK) and Not Acknowledge (NACK)

The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. The master generates all clock pulses, including the acknowledge ninth clock pulse. The Acknowledge signal is defined as follows: The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line LOW and it remains stable LOW during the HIGH period of this clock pulse. When SDA remains HIGH during this ninth clock pulse, this is defined as the Not Acknowledge signal. The master can then generate either a STOP condition to abort the transfer, or a repeated a START condition to start a new transfer.

The Salve Address and R/W Bit

After the START condition (S), a slave address is sent. This address is seven bits long followed by an eighth bit which is data direction bit (R/W), a ‘zero’ indicates a transmission (WRITE), an ‘one’ indicates a request for data (READ). A data transfer is always terminated by a STOP condition (P) generated by the master.

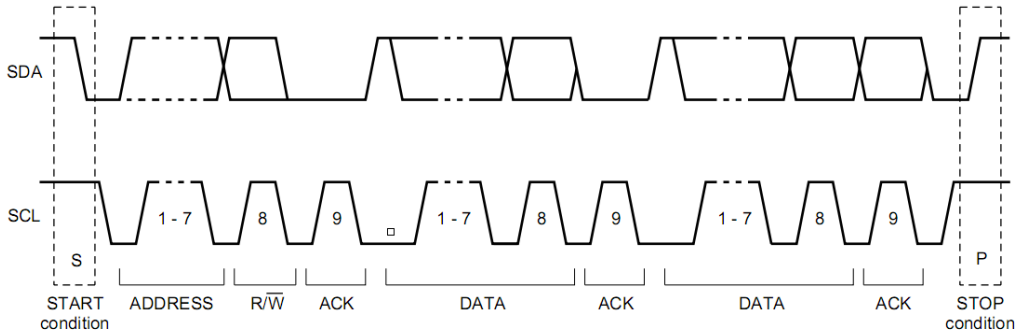


Figure 15. Complete Data Transfer

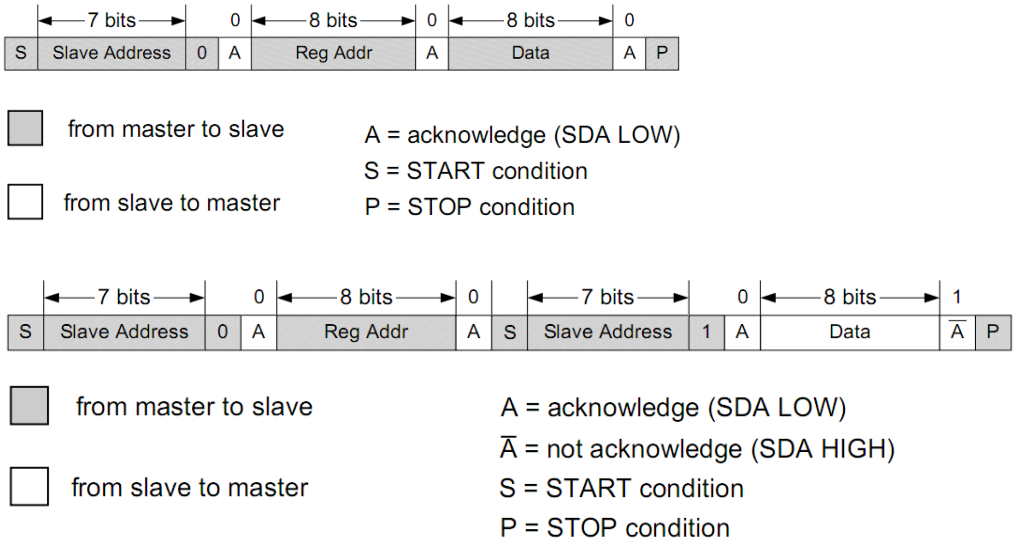


Figure 16. Write and Read Transaction

Device Address

I²C device address is consisted of 7bits slave address and 1 read/write control bit.

ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0	R/W

Figure 17. I2C address structure

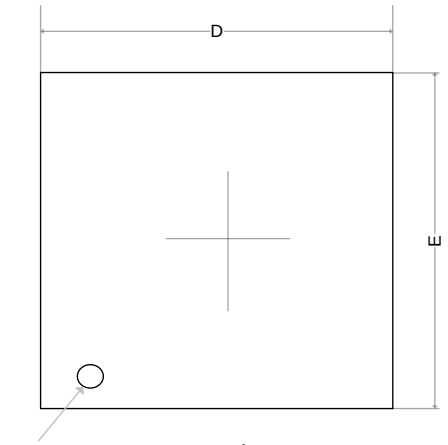
Address of CW2017 is fixed on 0b1100011. Combine with the R/W bit:

Read command of the CW2017 is 0xC7;

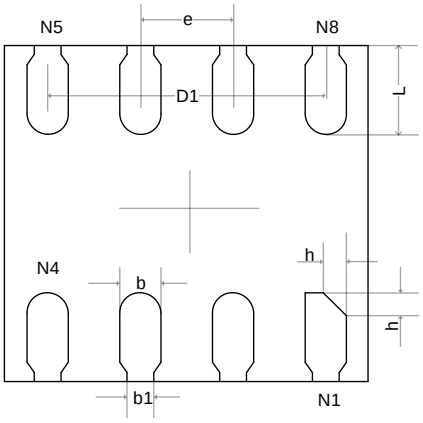
Write command of the CW2017 is 0xC6.

Package Information

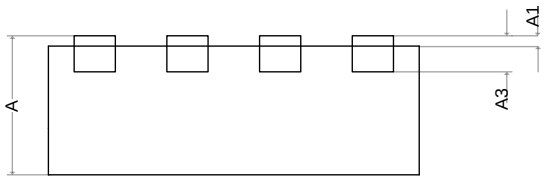
TDFN 2x2-8L(P0.50T0.45/0.55) PACKAGE OUTLINE DIMENSIONS



Top View



Bottom View

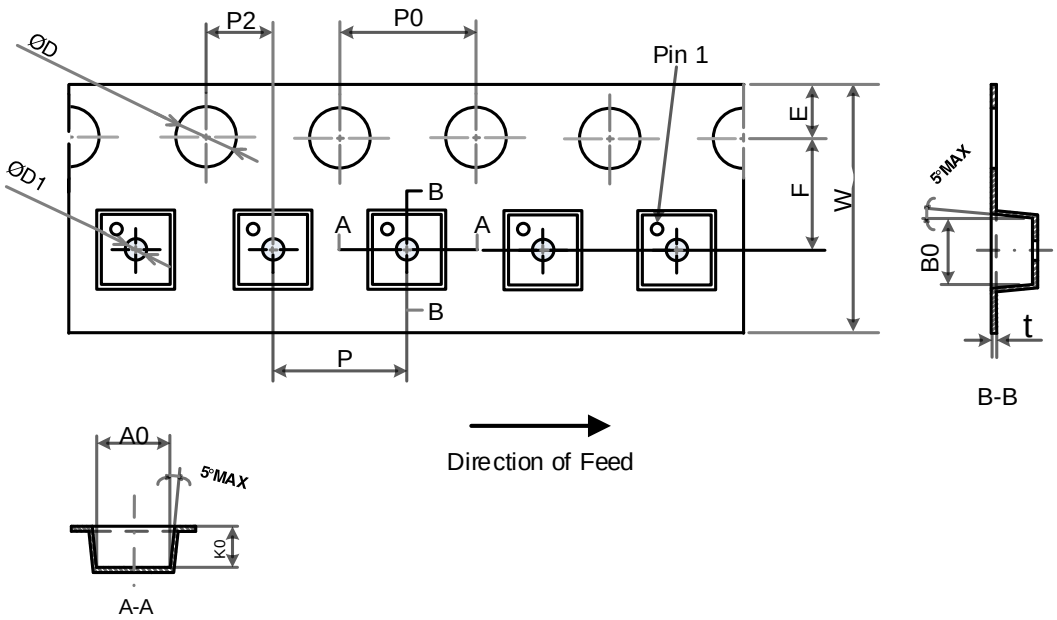


Side View

SYMBOL	DIMENSIONS IN MILLIMETERS		DIMENSIONS IN INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.7	0.8	0.027	0.031
A1	--	0.05	--	0.002
A3	0.18	0.25	0.007	0.010
D	1.90	2.10	0.075	0.121
E	1.90	2.10	0.075	0.121
D1	1.50BSC		0.059BSC	
h	0.10	0.20	0.004	0.008
b	0.18REF		0.007REF	
b1	0.18	0.30	0.007	0.012
e	0.50BSC		0.020TYP.	
L	0.45	0.55	0.017	0.021

Tape and Reel Information

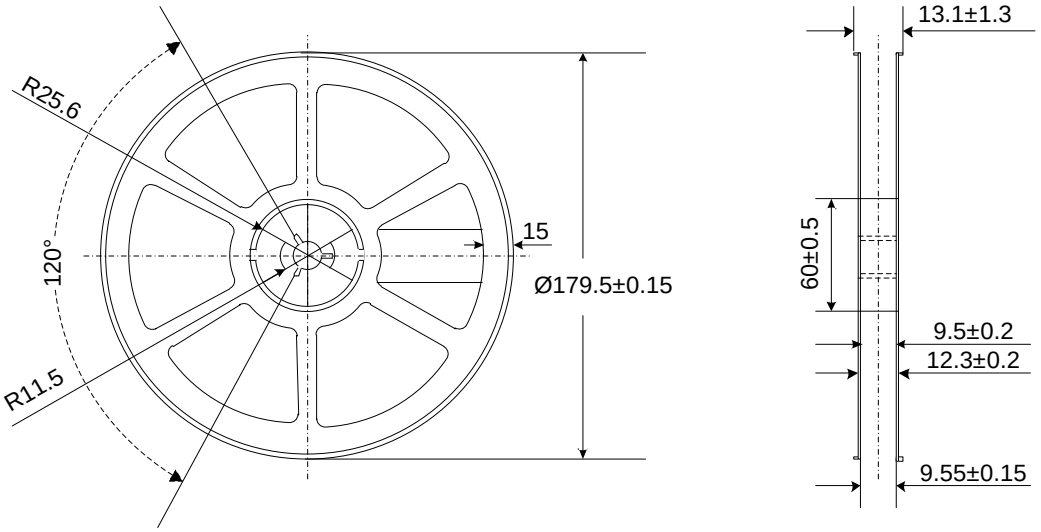
TDFN 2mm*2mm-8L Package Tape Information



Dimensions	Unit: mm	Dimensions	Unit: mm
E	1.75±0.10	W	$8.00^{+0.30}/_{-0.10}$
F	3.50±0.05	P	4.00±0.10
P2	2.00±0.05	A0	2.25±0.05
D	1.50±0.10	B0	2.25±0.05
D1	0.60±0.05	K0	0.80±0.05
P0	4.00±0.10	t	0.25±0.02
10P0	40.0±0.20	N/A	N/A

Carrier Tape Color: Black
Cover Tape Width: 5.30±0.10
Cover Tape Color: Transparent
All DIM in mm
All the package materials are Pb free and Halogen free.

TDFN 2mm*2mm-8L Package Reel Information



Color: Blue

All DIM in mm

Revision History

DATE	VERSION	CHANGED ITEM	WRITTEN BY	APPROVED BY
2018.08.12	0.1	First version	Richard	Jun
2019.01.10	1.0	Update descriptions and application diagram on page 1,2	Richard	Jun

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As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.

2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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